EVALUATION KIT AVAILABLE

MAX9632

36V, Precision, Low-Noise, Wide-Band Amplifier

General Description

The MAX9632 is a low-noise, precision, wide-band operational amplifier that can operate in a very wide +4.5V to +36V supply voltage range. The IC operates in dual (±18V) mode.

The exceptionally fast settling time and low distortion make the IC an excellent solution for precision acquisition systems. The rail-to-rail output swing maximizes the dynamic range when driving high-resolution 24-bit ΣΔ ADCs even with low supply voltages.

The IC achieves 55MHz of gain-bandwidth product and ultra-low 0.94nV/√Hz input voltage noise with only 3.9mA of quiescent current.

The IC is offered in 8-pin SO, µMAX®, and TDFN packages and is rated for operation over the -40°C to +125°C temperature range.

Applications

High-Resolution ADC Drivers
High-Resolution DAC Buffers
Medical Imaging
Low-Noise Signal Processing
Test and Measurement Systems
ATE

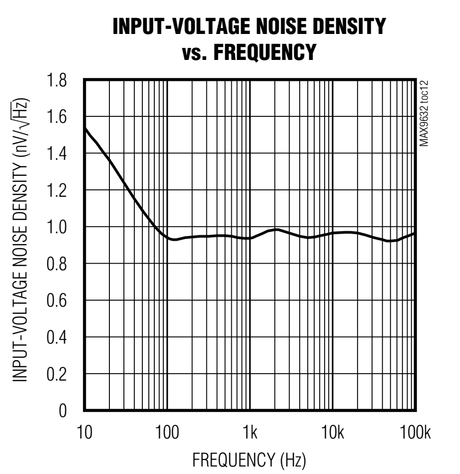
Benefits and Features

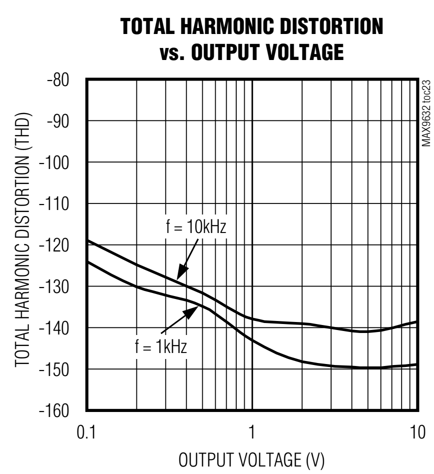
- **DC and AC Performance Ideal for High-Resolution ADC Driver Applications**
  - **55MHz Gain-Bandwidth**
  - **600ns Settling Time to 16-Bit Accuracy**
  - **THD of -128dB at 10kHz**
  - **Low Input Offset Voltage 125µV (max)**
  - **0.94nV/√Hz Ultra-Low Input Voltage Noise**
  - **Low Input Offset Temperature Drift 0.5µV/°C (max)**
  - **Unity-Gain Stable**
- **Wide Supply for High-Voltage Front-Ends**
  - **+4.5V to +36V Supply Range**
- **Improved Reliability with ESD Protection**
  - **±8kV HBM and ±1kV CDM ESD**
- **Low Pin Count Packages Save Board Space**
  - **8-Pin SO, µMAX, TDFN Packages**

Ordering Information

PART	TEMP RANGE	PIN-PACKAGE	TOP MARK
MAX9632ASA+	-40°C to +125°C	8 SO	—
MAX9632ATA+	-40°C to +125°C	8 TDFN-EP*	BML
MAX9632AUA+	-40°C to +125°C	8 µMAX	—

+Denotes a lead(Pb)-free/RoHS-compliant package.
**EP = Exposed pad.*





ABSOLUTE MAXIMUM RATINGS

V_{CC} to V_{EE} ....-0.3V to +40V
All Other Pins..................................(V_{EE} - 0.3V) to (V_{CC} + 0.3V)
Short-Circuit (GND) Duration, OUT....................................... 10s
Continuous Input Current (any pin)................................ ±20mA
Continuous Power Dissipation (T_A = +70°C) (Note 1)
Multilayer SO (derate 7.4mW/°C above +70°C) 588mW
Multilayer TDFN (derate 23.8mW/°C above +70°C)...1905mW
Multilayer µMAX (derate 4.8mW/°C above +70°C)..387.8mW

ESD Protection
HBM 8kV
CDM... 1kV
Operating Temperature Range........................ -40°C to +125°C
Junction Temperature ....+150°C
Lead Temperature (soldering, 10s) ....+300°C
Soldering Temperature (reflow) ....+260°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

PACKAGE THERMAL CHARACTERISTICS (Note 1)

8 TDFN
Junction-to-Ambient Thermal Resistance (θ_{JA}) ....42°C/W
Junction-to-Case Thermal Resistance (θ_{JC}) ....8°C/W

8 SO
Junction-to-Ambient Thermal Resistance (θ_{JA}) ....136°C/W
Junction-to-Case Thermal Resistance (θ_{JC}) ....38°C/W

8 µMAX
Junction-to-Ambient Thermal Resistance (θ_{JA}) .....206.3°C/W
Junction-to-Case Thermal Resistance (θ_{JC}) ....42°C/W

Note 1: Package thermal resistances were obtained using the method described in JEDEC specification JESD51-7, using a four-layer board. For detailed information on package thermal considerations, refer to www.maximintegrated.com/thermal-tutorial.

ELECTRICAL CHARACTERISTICS

(V_{CC} = 15V, V_{EE} = -15V, R_L = 10kΩ to V_{GND}, V_{IN+} = V_{IN-} = V_{GND} = 0V, V_{SHDN} = V_{GND}, T_A = -40°C to +125°C. Typical values are at T_A = +25°C, unless otherwise noted.) (Note 2)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
POWER SUPPLY						
Supply Voltage Range	V_{CC}	Guaranteed by PSRR	4.5		36	V
Supply Current	I_{CC}			3.9	6.5	mA
Power-Supply Rejection Ratio	PSRR	T_A = +25°C	125	140		dB
		-40°C ≤ T_A ≤ +125°C	120			
SHUTDOWN						
Shutdown Input Voltage	V_{SHDN}	Device disabled	V_{CC} - 0.35		V_{CC}	V
		Device enabled	V_{EE}		V_{CC} - 3.0	
Shutdown Current	I_{SHDN}	V_{SHDN} = V_{CC}		1	15	µA
DC SPECIFICATIONS						
Input Offset Voltage	V_{OS}	T_A = +25°C		30	125	µV
		-40°C ≤ T_A ≤ +125°C			165	
Input Offset Voltage Drift	±ΔV_{OS}	(Note 3)		0.15	0.5	µV/°C
Input Bias Current	I_B			30	180	nA
Input Offset Current	I_{OS}			15	100	nA
Input Common-Mode Range	V_{CM}	Guaranteed by CMRR	V_{EE} + 1.8		V_{CC} - 1.4	V

ELECTRICAL CHARACTERISTICS (continued)

(V_{CC} = 15V, V_{EE} = -15V, R_L = 10kΩ to V_{GND}, V_{IN+} = V_{IN-} = V_{GND} = 0V, V_{SHDN} = V_{GND}, T_A = -40°C to +125°C. Typical values are at T_A = +25°C, unless otherwise noted.) (Note 2)

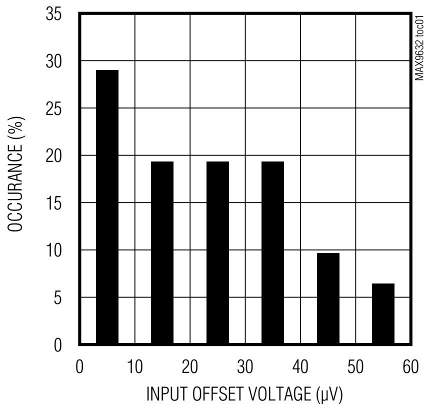
PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Common-Mode Rejection Ratio	CMRR	V_{EE} + 1.8V ≤ V_{CM} ≤ V_{CC} - 1.4V, T_A = +25°C		120	135		dB
		V_{EE} + 1.8V ≤ V_{CM} ≤ V_{CC} - 1.4V, -40°C ≤ T_A ≤ +125°C		110			
Large-Signal Gain	A_{VOL}	V_{EE} + 0.2V ≤ V_{OUT} ≤ V_{CC} - 0.2V, R_L = 10kΩ		125	140		dB
		V_{EE} + 0.6V ≤ V_{OUT} ≤ V_{CC} - 0.6V, R_L = 600Ω		120	135		
Output Voltage Swing	V_{OH}	V_{CC} - V_{OUT}	R_L = 10kΩ		50	150	mV
			R_L = 600Ω		150	400	
	V_{OL}	V_{OUT} - V_{EE}	R_L = 10kΩ		50	150	
			R_L = 600Ω		150	400	
Short-Circuit Current	I_{SC}	T_A = +25°C			56		mA
AC SPECIFICATIONS							
Gain-Bandwidth Product	GBWP				55		MHz
Slew Rate	SR	0 ≤ V_{OUT} ≤ 5V			30		V/µs
Settling Time	t_S	To 0.0015%, V_{OUT} = 10V_{P-P}, C_L = 100pF, AV = 1V/V			600		ns
Total Harmonic Distortion	THD	f = 1kHz, V_{OUT} = 3V_{RMS}, R_L = 600Ω, AV = 1V/V			-136		dB
		f = 10kHz, V_{OUT} = 3V_{RMS}, R_L = 600Ω, AV = 1V/V			-128		
Input-Voltage Noise Density	e_N	f = 1kHz			0.94		nV/√Hz
Input Voltage Noise		0.1Hz ≤ f ≤ 10Hz			65		nV_{P-P}
Input-Current Noise Density	i_N	f = 1kHz			3.75		pA/√Hz
Capacitive Loading	C_L	No sustained oscillation, AV = 1V/V			350		pF

Note 2: All devices are 100% production tested at T_A = +25°C. Temperature limits are guaranteed by design.
Note 3: Guaranteed by design.

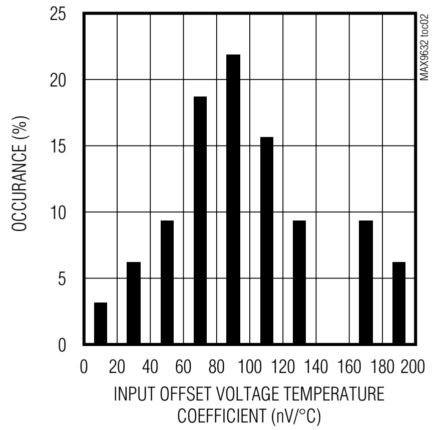
Typical Operating Characteristics

(V_{CC} = 15V, V_{EE} = -15V, R_L = 10kΩ to V_{GND}, V_{IN+} = V_{IN-} = V_{GND} = 0V, V_{SHDN} = V_{GND}, T_A = -40°C to +125°C. Typical values are at T_A = +25°C, unless otherwise noted.)

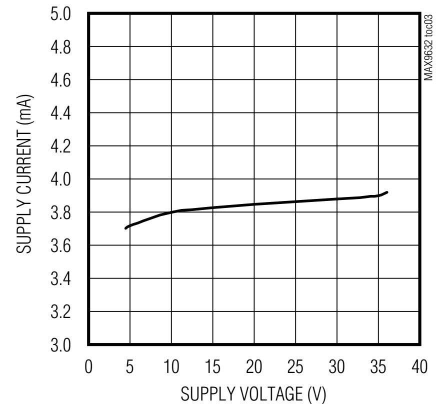
INPUT OFFSET VOLTAGE HISTOGRAM



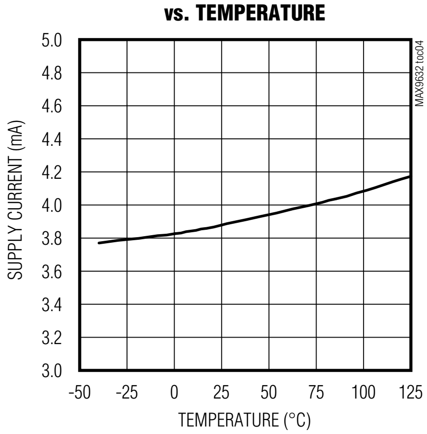
INPUT OFFSET VOLTAGE TEMPERATURE COEFFICIENT HISTOGRAM



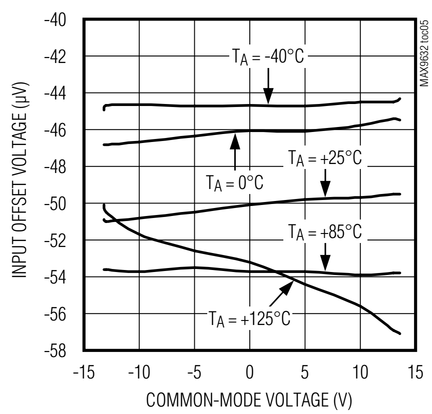
SUPPLY CURRENT vs. SUPPLY VOLTAGE



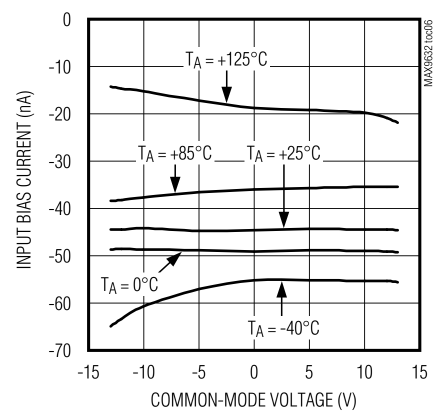
SUPPLY CURRENT vs. TEMPERATURE



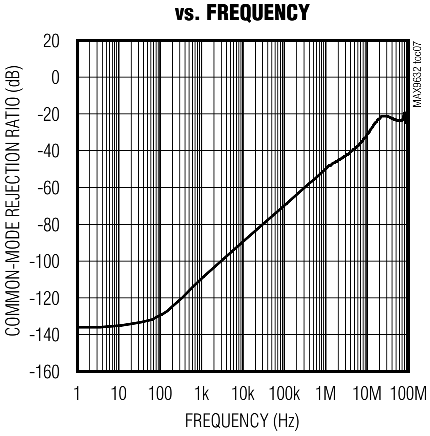
INPUT OFFSET VOLTAGE vs. COMMON-MODE VOLTAGE



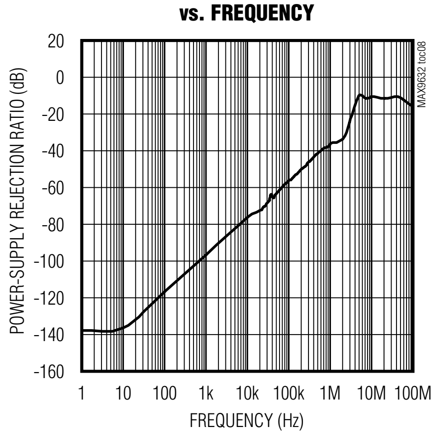
INPUT BIAS CURRENT vs. INPUT COMMON-MODE VOLTAGE



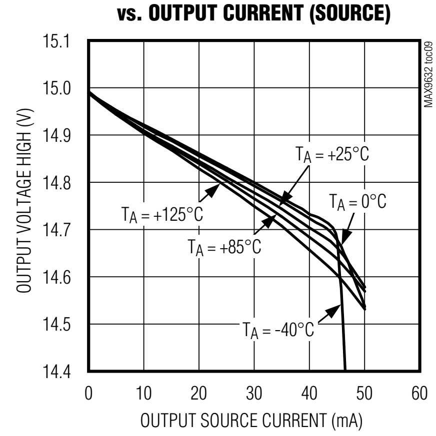
COMMON-MODE REJECTION RATIO vs. FREQUENCY



POWER-SUPPLY REJECTION RATIO vs. FREQUENCY



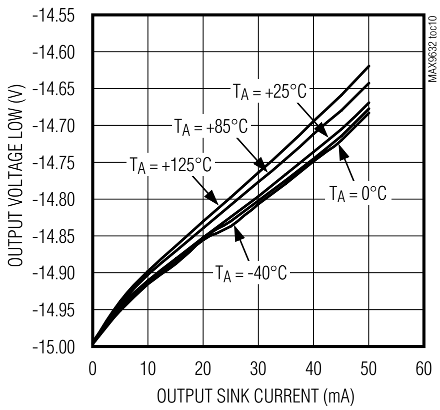
OUTPUT VOLTAGE HIGH vs. OUTPUT CURRENT (SOURCE)



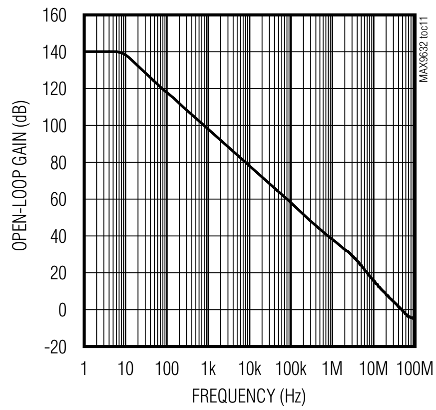
Typical Operating Characteristics (continued)

(V_{CC} = 15V, V_{EE} = -15V, R_L = 10kΩ to V_{GND}, V_{IN+} = V_{IN-} = V_{GND} = 0V, V_{SHDN} = V_{GND}, T_A = -40°C to +125°C. Typical values are at T_A = +25°C, unless otherwise noted.)

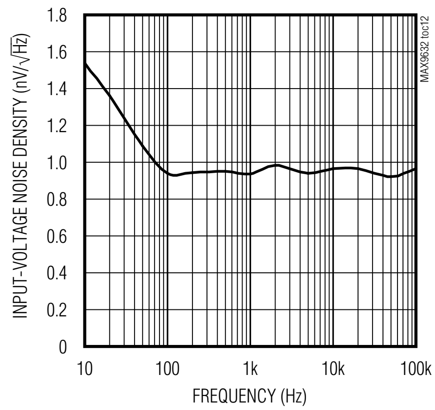
OUTPUT VOLTAGE LOW vs. OUTPUT CURRENT (SINK)



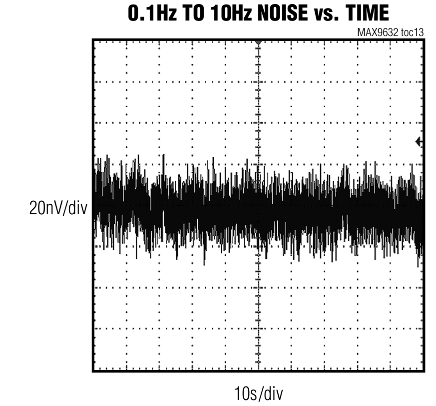
OPEN-LOOP GAIN vs. FREQUENCY



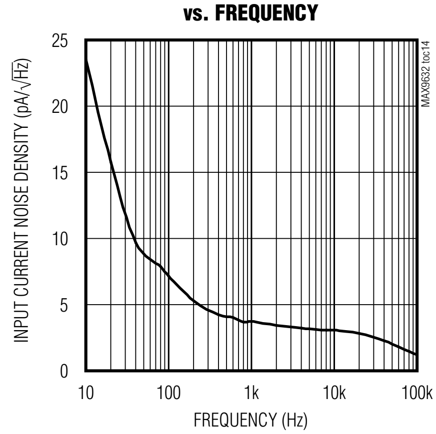
INPUT-VOLTAGE NOISE DENSITY vs. FREQUENCY



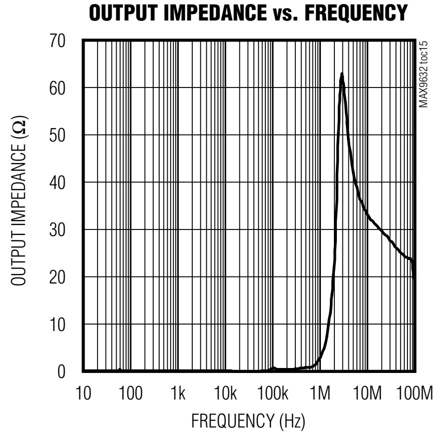
0.1Hz TO 10Hz NOISE vs. TIME



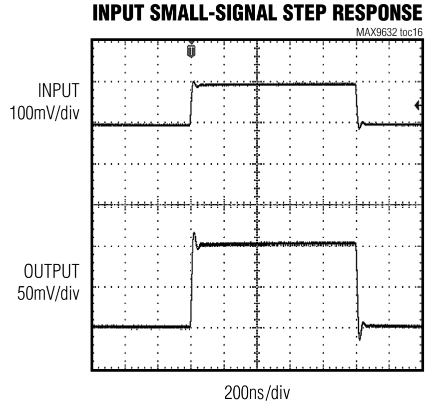
INPUT-CURRENT NOISE DENSITY vs. FREQUENCY



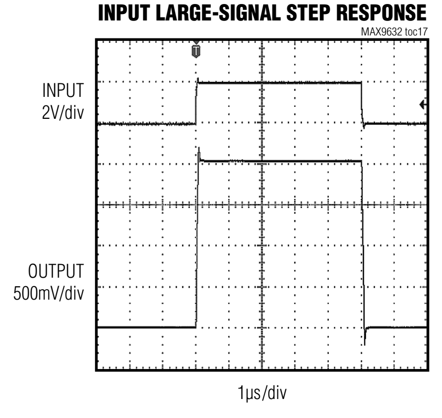
OUTPUT IMPEDANCE vs. FREQUENCY



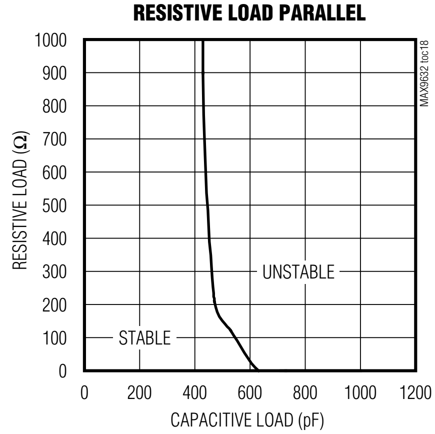
INPUT SMALL-SIGNAL STEP RESPONSE



INPUT LARGE-SIGNAL STEP RESPONSE

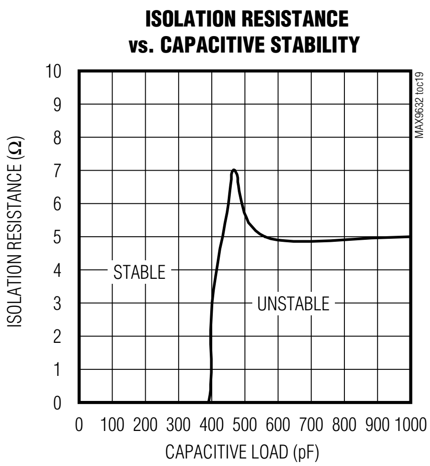


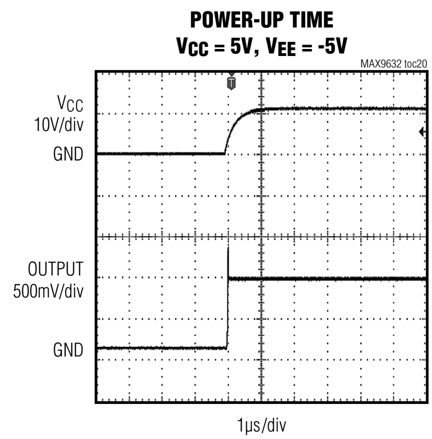
STABILITY vs. CAPACITIVE AND RESISTIVE LOAD PARALLEL

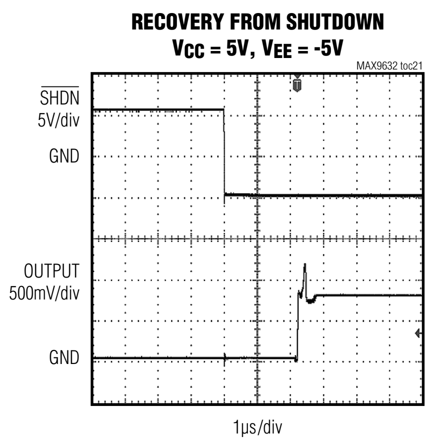


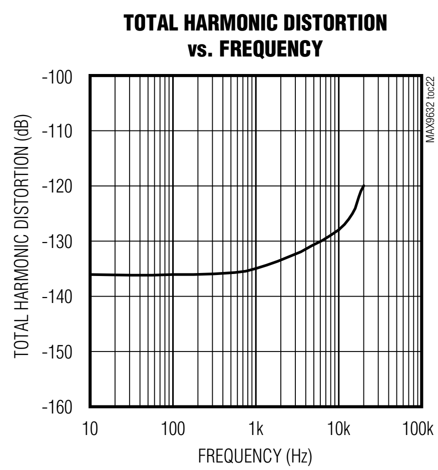
Typical Operating Characteristics (continued)

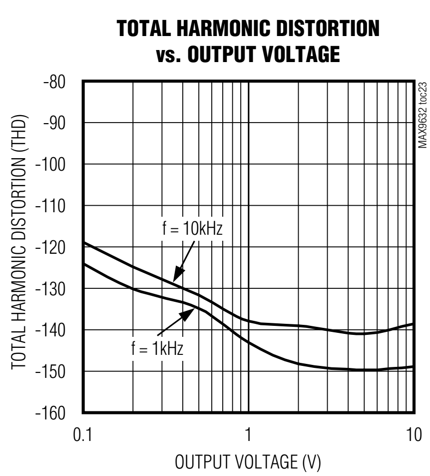
(V_{CC} = 15V, V_{EE} = -15V, R_L = 10kΩ to V_{GND}, V_{IN+} = V_{IN-} = V_{GND} = 0V, V_{SHDN} = V_{GND}, T_A = -40°C to +125°C. Typical values are at T_A = +25°C, unless otherwise noted.)



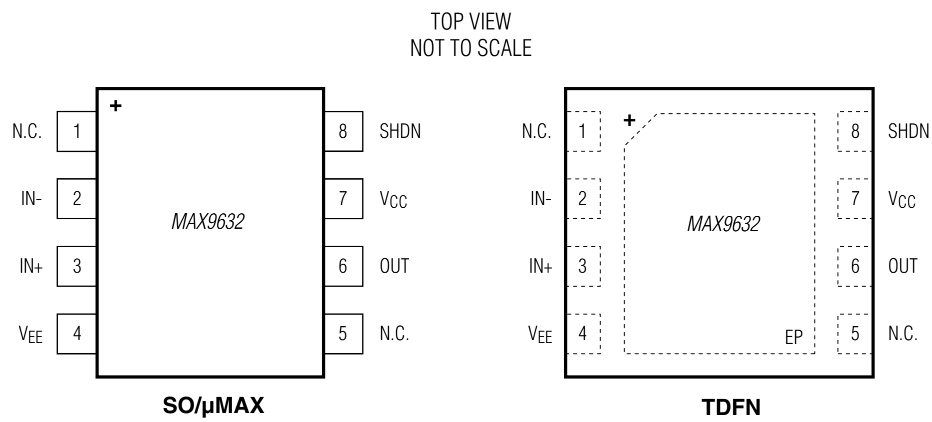








Pin Configuration



Pin Description

PIN	NAME	FUNCTION
1, 5	N.C.	Not Connected
2	IN-	Negative Input
3	IN+	Positive Input
4	V_{EE}	Negative Supply Voltage
6	OUT	Output
7	V_{CC}	Positive Supply Voltage
8	SHDN	Active-High Shutdown
—	EP	Exposed Pad (TDFN Only). Connect to a large V_{EE} plane to maximize thermal performance. Not intended as an electrical connection point.

Detailed Description

The MAX9632 is designed in a new 36V, high-speed complementary BiCMOS process that is optimized for excellent AC dynamic performance combined with high-voltage operation.

The IC offers precision, high-bandwidth, ultra-low noise and exceptional distortion performance.

The IC is unity-gain stable and operates either with single-supply voltage up to 36V or with dual supplies up to ±18V.

Applications Information

Operating Supply Voltage

The IC can operate with dual supplies from ±2.25V to ±18V or with a single supply from +4.5V to +36V with respect to ground. Even though the IC supports high-voltage operation with excellent performance, the device can also operate in very popular applications at 5V.

Low Noise and Low Distortion

The IC is designed for extremely low-noise applications such as professional audio equipment, very high performance instrumentations, automated test equipment, and medical imaging. The low noise, combined with fast settling time, makes it ideal to drive high-resolution sigma-delta or SARs analog-to-digital converters.

The IC is also designed for ultra-low-distortion performance. THD specifications in the *Electrical Characteristics* table and *Typical Operating Characteristics* are calculated up to the fifth harmonic. Even when driving high-voltage swing up to $10V_{P-P}$, the IC maintains excellent low distortion operation over and above 100kHz of bandwidth.

Rail-to-Rail Output Stage

The output stage swings to within 50mV (typ) of either power-supply rail with a 10kΩ load and provides a 55MHz GBW with a 30V/s slew rate. The device is unity-gain stable and can drive a 100pF capacitive load without compromising stability. Stability with higher capacitive loads can be improved by adding an isolation resistor in series with the op-amp output. This resistor improves the circuit's phase margin by isolating the load capacitor from the amplifier's output. The *Typical Operating Characteristics* show a profile of the isolation resistor and capacitive load values that maintain the device into the stable region.

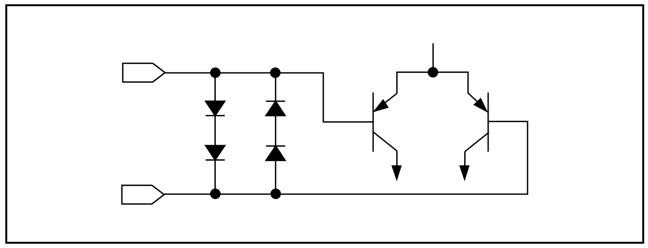


Figure 1. Input Protection Circuit

Input Differential Voltage Protection

During normal op-amp operation, the inverting and noninverting inputs of the IC are at essentially the same voltage. However, either due to fast input voltage transients or other fault conditions, these inputs can be forced to be at two different voltages.

Internal back-to-back diodes protect the inputs from an excessive differential voltage (Figure 1). Therefore, IN+ and IN- can be any voltage within the range shown in the *Absolute Maximum Ratings* section. Note the protection time is still dependent on the package thermal limits.

If the input signal is fast enough to create the internal diodes' forward bias condition, the input signal current must be limited to 20mA or less. If the input signal current is not inherently limited, an input series resistor can be used to limit the signal input current. Care should be taken in choosing the input series resistor value, since it degrades the low-noise performance of the device.

Shutdown

The shutdown is referenced to the positive supply. See the *Electrical Characteristics* table for the proper levels of functionality. A high level (above V_{CC} - 0.35V) disables the op amp and puts the output into a high-impedance state. A low level (below V_{CC} - 3V) enables the device. As an example, if the op amp is powered with dual supplies of ±15V, the device is enabled when shutdown is at or below 12V. The device is disabled when shutdown is at or above 14.65V. If the op amp is powered with a single supply of 36V, the device is enabled when shutdown is at or below 33V. The device is disabled when shutdown is at or above 35.65V. This input must be connected to a valid high or low voltage and should not be left disconnected.

Power Supplies and Layout

The MAX9632 can operate with dual supplies from ±2.25V to ±18V or with a single supply from +4.5V to +36V with respect to ground. When used with dual supplies, bypass both V_{CC} and V_{EE} with their own 0.1µF capacitor to ground. When used with a single supply, bypass V_{CC} with a 0.1µF capacitor to ground.

Careful layout technique helps optimize performance by decreasing the amount of stray capacitance at the op amp's inputs and outputs. To decrease stray capacitance, minimize trace lengths by placing external components close to the op amp's pins.

For high-frequency designs, ground vias are critical to provide a ground return path for high-frequency signals and should be placed near the decoupling capacitors. Signal routing should be short and direct to avoid parasitic effects. Avoid using right angle connectors since they may introduce a capacitive discontinuity and ultimately limit the frequency response.

Electrostatic Discharge (ESD)

The IC has built-in circuits to protect it from ESD events. An ESD event produces a short, high-voltage pulse that is transformed into a short current pulse once it discharges through the device. The built-in protection circuit provides a current path around the op amp that prevents it from being damaged. The energy absorbed by the protection circuit is dissipated as heat.

ESD protection is guaranteed up to ±8kV with the Human Body Model (HBM). The Human Body Model simulates the ESD phenomenon wherein a charged body directly transfers its accumulated electrostatic charge to the ESD-sensitive device. A common example of this phenomenon is when a person accumulates static charge by walking across a carpet and then transfers all of the charge to an ESD-sensitive device by touching it.

Not all ESD events involve the transfer of charge into the device. ESD from a charged device to another body is also a common form of ESD.

If a charged device comes into contact with another conductive body that is at a lower potential, it discharges into that body. Such an ESD event is known as Charged Device Model (CDM) ESD, which can be even more destructive than HBM ESD (despite its shorter pulse duration) because of its high current. The IC guarantees CDM ESD protection up to ±1kV.

Driving High-Resolution Sigma-Delta ADCs

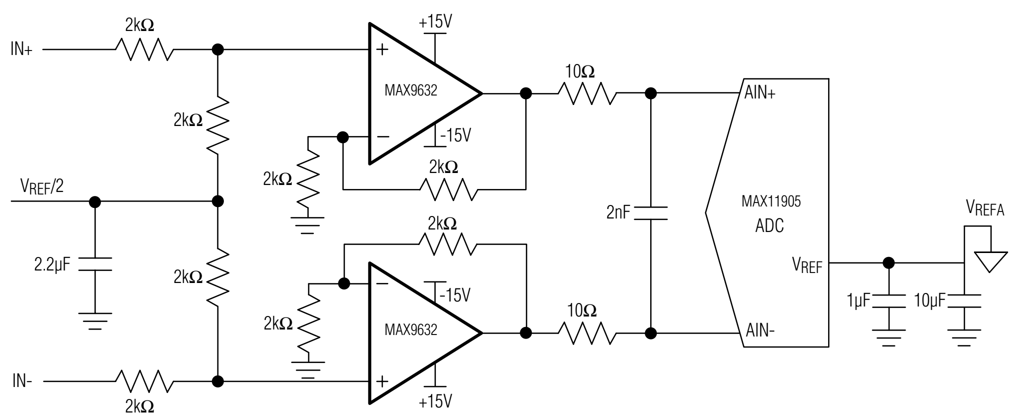
The MAX9632's excellent AC specifications and 55MHz bandwidth are a good fit for driving high-speed, high-precision SAR ADCs. These ADCs require an ultra-low noise op amp to achieve high signal-to-noise ratio (SNR). The MAX11905 is a 20-bit, 1.6Msps fully differential ADC with 98.3dB SNR at f_{IN} = 10kHz. The MAX11905 measures analog inputs up to $\pm V_{REF}$. Sampling up to 1.6Msps, the MAX11905 achieves better than -123dB THD and 125 SFDR at f_{IN} = 10kHz.

The *Typical Application Circuit* shows an example of the MAX9632 driving the MAX11905.

Chip Information

PROCESS: BiCMOS

Typical Application Circuit



Package Information

For the latest package outline information and land patterns (footprints), go to **www.maximintegrated.com/packages**. Note that a "+", "#", or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

PACKAGE TYPE	PACKAGE CODE	OUTLINE NO.	LAND PATTERN NO.
8 SO	S8+2	21-0041	90-0096
8 TDFN-EP	T833+3	21-0137	90-0060
8 µMAX	U8+3	21-0036	90-0092

Revision History

REVISION NUMBER	REVISION DATE	DESCRIPTION	PAGES CHANGED
0	10/10	Initial release	—
1	4/11	Updated short-circuit current spec	3
2	8/11	Updated TDFN land pattern number	11
3	10/11	Added μMAX package	1, 2, 7
4	6/14	Revised the *Features* and *Driving High-Resolution Sigma-Delta ADCs* sections and updated *Typical Application Circuit* and *Package Information* section	1, 9, 10
5	12/14	Revised *Benefits and Features* section	1