MAX9277/MAX9281

3.12Gbps GMSL Serializers for Coax or STP Output Drive and LVDS Input

General Description

The MAX9277/MAX9281 are 3.12Gbps Gigabit Multimedia Serial Link (GMSL) serializers with 3- or 4-data lane LVDS input (oLDI) and a CML serial output programmable for 50Ω coax or 100Ω shielded twisted pair (STP) cable drive. The MAX9281 has HDCP content protection but otherwise is the same as the MAX9277. The serializers pair with any GMSL deserializer capable of coax input. When programmed for STP output they are backward compatible with any GMSL deserializer. The output amplitude is programmable 100mV to 500mV single-ended (coax) or 100mV to 400mV differential (STP).

The audio channel supports L-PCM I²S stereo and up to 8 channels of L-PCM in TDM mode. Sample rates of 32kHz to 192kHz are supported with sample depth up to 32 bits.

The embedded control channel operates at 9.6kbps to 1Mbps in UART-UART and UART-I²C modes, and up to 1Mbps in I²C-I²C mode. Using the control channel, a µC can program serializer, deserializer and peripheral device registers at any time, independent of video timing, and manage HDCP operation (MAX9281). A GPO output supports touch-screen controller interrupt requests from the remote end of the link.

For use with longer cables, the serializers have programmable pre/deemphasis. Programmable spread spectrum is available on the serial output. The serial output meets ISO 10605 and IEC61000-4-2 ESD standards. The core supply is 1.7 to 1.9V and the I/O supply is 1.7 to 3.6V. The package is a lead-free, 48-pin, 7mm x 7mm TQFN with exposed pad, optional wettable flanks, and 0.5mm lead pitch.

Applications

- High-Resolution Automotive Navigation
- Rear-Seat Infotainment
- Megapixel Camera Systems

***Ordering Information* appears at end of data sheet.**

Features and Benefits

- Ideal for High-Definition Video Applications
  - Drives Low-Cost 50Ω Coax Cable and FAKRA Connectors or 100Ω STP
  - 104MHz High-Bandwidth Mode Supports 1920x720p/60Hz Display With 24-Bit Color
  - Serializer Pre/Deemphasis Allows 15m Cable at Full Speed
  - Up to 192kHz Sample Rate and 32-Bit Sample Depth For 7.1 Channel HD Audio
- Multiple Data Rates for System Flexibility
  - Up to 3.12Gbps Serial-Bit Rate
  - 6.25MHz to 104MHz Pixel Clock
  - 9.6kbps to 1Mbps Control Channel in UART, mixed UART/I²C, or I²C Mode with Clock Stretch Capability
- Reduces EMI and Shielding Requirements
  - Serial Output Programmable for 100mV to 500mV Single-Ended or 100mV to 400mV Differential
  - Programmable Spread Spectrum Reduces EMI
  - Bypassable Input PLL for Pixel Clock Jitter Attenuation
  - Tracks Spread Spectrum on Input
  - High-Immunity Mode for Maximum Control-Channel Noise Rejection
- Peripheral Features for System Power-Up and Verification
  - Built-In PRBS Generator for BER Testing of the Serial Link
  - Programmable Choice of Nine Default Device Addresses
  - Dedicated “Up/Down” GPO for Touch-Screen Interrupt and Other Uses
  - Remote/Local Wake-Up from Sleep Mode
- Meets Rigorous Automotive and Industrial Requirements
  - -40ºC to +105ºC Operating Temperature
  - 8kV Contact and 15kV Air ISO 10605 and IEC 61000-4-2 ESD Protection

19-6764; Rev 4; 8/19

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Absolute Maximum Ratings

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IOVDD to AGND.....-0.5V to +3.9V
LVDSVDD to AGND .....-0.5V to +3.9V
GND to AGND .....-0.5V to +0.5V
LMN_ to AGND (15mA current limit).....-0.5V to +3.9V
OUT+, OUT- to AGND.....-0.5V to +1.9V
All Other Pins to AGND.....-0.5V to (V_{IOVDD} + 0.5V)

OUT+, OUT- Short Circuit to Ground or Supply.....Continuous
Continuous Power Dissipation (T_A = +70ºC)
TQFN (derate 40mW/ºC above +70ºC) 3200mW
Junction Temperature.....+150ºC
Storage Temperature.....-65ºC to +150ºC
Lead Temperature (soldering, 10s) .....+300ºC
Soldering Temperature (reflow).....+260ºC

Note 1: AGND, GND connected to PCB ground.

Package Thermal Characteristics (Note 2)

TQFN
Junction-to-Case Thermal Resistance (θ_{JC})..... 1°C/W
Junction-to-Ambient Thermal Resistance (θ_{JA}) ..... 25°C/W

Note 2: Package thermal resistances were obtained using the method described in JEDEC specification JESD51-7, using a four-layer board. For detailed information on package thermal considerations, refer to **www.maximintegrated.com/thermal-tutorial**.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC Electrical Characteristics

(V_{AVDD} = V_{DVDD} = 1.7V to 1.9V, V_{IOVDD} = 1.7V to 3.6V, $V_{LVDSVDD}$ = 3.0V to 3.6V, R_L = 100Ω ±1% (differential), T_A = -40°C to +105°C, unless otherwise noted. Differential input voltage $|V_{ID}|$ = 0.1V to 1.2V, input common-mode voltage V_{CM} = $|V_{ID}/2|$ to 2.4V - $|V_{ID}/2|$. Typical values are at V_{AVDD} = V_{DVDD} = V_{IOVDD} = 1.8V, $V_{LVDSVDD}$ = 3.3V, T_A = +25°C.) (Note 3)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
SINGLE-ENDED INPUTS (CX/TP, $\overline{PWDN}$, MS/CNTL0, CDS/CNTL3, SD, SCK, WS, $\overline{AUTOS}$, CNTL1, CNTL2, HIM)							
High-Level Input Voltage	V_{IH1}	(CX/TP, $\overline{PWDN}$, MS/CNTL0, CDS/CNTL3, $\overline{AUTOS}$, HIM)		0.65 x V_{IOVDD}			V
		SD, SCK, WS, CNTL1, CNTL2		0.7 x V_{IOVDD}			
Low-Level Input Voltage	V_{IL1}					0.35 x V_{IOVDD}	V
Input Current	I_{IN1}	V_{IN} = 0V to V_{IOVDD}		-10		+20	µA
THREE-LEVEL LOGIC INPUTS (CONF0, CONF1, ADD0, ADD1, BWS)							
High-Level Input Voltage	V_{IH}			0.7 x V_{IOVDD}			V
Low-Level Input Voltage	V_{IL}					0.3 x V_{IOVDD}	V
Mid-Level Input Current	I_{INM}	(Note 4)		-10		+10	µA
Input Current	I_{IN}			-150		+150	µA
SINGLE-ENDED OUTPUT (GPO)							
High Level Output Voltage	V_{OH1}	I_{OUT} = -2mA		V_{IOVDD} - 0.2			V
Low Level Output Voltage	V_{OL1}	I_{OUT} = 2mA				0.2	V
OUTPUT Short-Circuit Current	I_{OS}	V_{OUT} = 0V	V_{IOVDD} = 3.0V to 3.6V	16	35	64	mA
			V_{IOVDD} = 1.7V to 1.9V	3	12	21	

DC Electrical Characteristics (continued)

(V_{AVDD} = V_{DVDD} = 1.7V to 1.9V, V_{IOVDD} = 1.7V to 3.6V, $V_{LVDSVDD}$ = 3.0V to 3.6V, R_L = 100Ω ±1% (differential), T_A = -40°C to +105°C, unless otherwise noted. Differential input voltage $|V_{ID}|$ = 0.1V to 1.2V, input common-mode voltage V_{CM} = $|V_{ID}/2|$ to 2.4V - $|V_{ID}/2|$. Typical values are at V_{AVDD} = V_{DVDD} = V_{IOVDD} = 1.8V, $V_{LVDSVDD}$ = 3.3V, T_A = +25°C.) (Note 3)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
OPEN-DRAIN INPUT/OUTPUT (RX/SDA, TX/SCL, $\overline{LFLT}$)							
High-Level Input Voltage	V_{IH2}			0.7 x V_{IOVDD}			V
Low-Level Input Voltage	V_{IL2}					0.3 x V_{IOVDD}	V
Input Current	I_{IN2}	(Note 5)	RX/SDA, TX/SCL	-110		+5	µA
			LFLT	-80		+5	
Low-Level Output Voltage	V_{OL2}	I_{OUT} = 3mA	V_{IOVDD} = 1.7V to 1.9V			0.4	V
			V_{IOVDD} = 3.0V to 3.6V			0.3	
Input Capacitance	C_{IN}	Each pin (Note 9)				10	pF
DIFFERENTIAL SERIAL OUTPUT (OUT+, OUT-)							
Differential Output Voltage	V_{OD}	Pre-emphasis off (Figure 1)		300	400	500	mV
		3.3dB preemphasis setting (Figure 2)		350		610	
		3.3dB deemphasis setting (Figure 2)		240		425	
Change in V_{OD} Between Complementary Output States	ΔV_{OD}	Preemphasis off, deemphasis only				15	mV
Output Offset Voltage (V_{OUT+} + V_{OUT-})/2 = V_{OS}	V_{OS}	Preemphasis off		1.1	1.4	1.56	V
Change in V_{OS} between Complementary Output States	ΔV_{OS}					15	mV
Output Short-Circuit Current	I_{OS}	V_{OUT+} or V_{OUT-} = 0V		-62			mA
		V_{OUT+} or V_{OUT-} = 1.9V				25	
Magnitude of Differential Output Short-Circuit Current	I_{OSD}	V_{OD} = 0V				25	mA
Output Termination Resistance (Internal)	R_{OUT}	From OUT+, OUT- to V_{AVDD}		45	54	63	Ω
SINGLE-ENDED SERIAL OUTPUT (OUT+, OUT-)							
Single-Ended Output Voltage	V_{OUT}	Pre-emphasis off, high drive (Figure 3)		375	500	625	mV
		3.3dB preemphasis setting, high drive (Figure 2)		435		765	
		3.3dB deemphasis setting, high drive (Figure 2)		300		535	
Output Short-Circuit Current	I_{OS}	V_{OUT+} or V_{OUT-} = 0V		-69			mA
		V_{OUT+} or V_{OUT-} = 1.9V				32	
Output Termination Resistance (Internal)	RO	From OUT+ or OUT- to V_{AVDD}		45	54	63	Ω

DC Electrical Characteristics (continued)

(V_{AVDD} = V_{DVDD} = 1.7V to 1.9V, V_{IOVDD} = 1.7V to 3.6V, $V_{LVDSVDD}$ = 3.0V to 3.6V, R_L = 100Ω ±1% (differential), T_A = -40°C to +105°C, unless otherwise noted. Differential input voltage $|V_{ID}|$ = 0.1V to 1.2V, input common-mode voltage V_{CM} = $|V_{ID}/2|$ to 2.4V - $|V_{ID}/2|$. Typical values are at V_{AVDD} = V_{DVDD} = V_{IOVDD} = 1.8V, $V_{LVDSVDD}$ = 3.3V, T_A = +25°C.) (Note 3)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
REVERSE CONTROL-CHANNEL RECEIVER (OUT+, OUT-)							
High Switching Threshold	V_{CHR}	Normal-immunity mode				27	mV
		High-immunity mode				40	
Low Switching Threshold	V_{CLR}	Normal-immunity mode		-27			mV
		High-immunity mode		-40			
LINE FAULT DETECTION INPUT (LMN_)							
Short-to-GND Threshold	V_{TG}	(Figure 4)				0.3	V
Normal Threshold	V_{TN}	(Figure 4)		0.57		1.07	V
Open Threshold	V_{TO}	(Figure 4)		1.45		V_{IO} + 0.06	V
Open Input Voltage	V_{IO}	(Figure 4)		1.47		1.75	V
Short-to-Battery Threshold	V_{TE}	(Figure 4)		2.47			V
LVDS INPUTS (RXIN_, RXCLKIN_)							
Differential Input High Threshold	V_{TH}	V_{CM} = 1.2V				50	mV
Differential Input Low Threshold	V_{TL}	V_{CM} = 1.2V		-50			mV
Input Differential Termination Resistance	R_{TERM}			85	110	135	Ω
Input Current	I_{IN+}, I_{IN-}	$\overline{PWDN}$ = high or low, IN+ and IN- are shorted		-25		+25	µA
Power-Off Input Current	I_{IN0+}, I_{IN0-}	V_{AVDD} = V_{DVDD} = V_{IOVDD} = 0V		-40		+40	µA
POWER SUPPLY							
Total Supply Current (AVDD + DVDD + IOVDD) (Note 6) (Worst-Case Pattern) (Figure 5)	I_{WCS}	BWS = low	$f_{PCLKIN\_}$ = 16.6MHz		100	125	mA
			$f_{PCLKIN\_}$ = 33.3MHz		106	140	
			$f_{PCLKIN\_}$ = 66.6MHz		123	155	
			$f_{PCLKIN\_}$ = 104MHz		146	190	
		BWS = mid	$f_{PCLKIN\_}$ = 36.6MHz		108	145	
			$f_{PCLKIN\_}$ = 104MHz		152	195	
LVDSVDD Worst-Case Supply Current (Figure 5, Note 6)	I_{WCS}	BWS = low	$f_{PCLKIN\_}$ = 16.6MHz		24	30	mA
			$f_{PCLKIN\_}$ = 33.3MHz		24	30	
			$f_{PCLKIN\_}$ = 66.6MHz		24	30	
			$f_{PCLKIN\_}$ = 104MHz		24	30	
		BWS = mid	$f_{PCLKIN\_}$ = 36.6MHz		29	35	
			$f_{PCLKIN\_}$ = 104MHz		29	35	

DC Electrical Characteristics (continued)

(V_{AVDD} = V_{DVDD} = 1.7V to 1.9V, V_{IOVDD} = 1.7V to 3.6V, $V_{LVDSVDD}$ = 3.0V to 3.6V, R_L = 100Ω ±1% (differential), T_A = -40°C to +105°C, unless otherwise noted. Differential input voltage $|V_{ID}|$ = 0.1V to 1.2V, input common-mode voltage V_{CM} = $|V_{ID}/2|$ to 2.4V - $|V_{ID}/2|$. Typical values are at V_{AVDD} = V_{DVDD} = V_{IOVDD} = 1.8V, $V_{LVDSVDD}$ = 3.3V, T_A = +25°C.) (Note 3)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Sleep Mode Supply Current	I_{CCS}	Single wake-up receiver enabled, LVDS inputs not driven			42	170	µA
Power-Down Supply Current	I_{CCZ}	$\overline{PWDN}$ = GND			6	120	µA
ESD PROTECTION							
OUT+, OUT- (Note 6)	V_{ESD}	Human body model, R_D = 1.5kΩ, C_S = 100pF			±8		kV
		IEC 61000-4-2, R_D = 330Ω, C_S = 150pF	Contact discharge		±10		
			Air discharge		±12		
		ISO 10605, R_D = 2kΩ, C_S = 330pF	Contact discharge		±10		
			Air discharge		±25		
RXIN_, RXCLKIN_ (Note 7)	V_{ESD}	Human body model, R_D = 1.5kΩ, C_S = 100pF			±8		kV
		IEC 61000-4-2, R_D = 330Ω, C_S = 150pF	Contact discharge		±6		
			Air discharge		±20		
		ISO 10605, R_D = 2kΩ, C_S = 330pF	Contact discharge		±8		
			Air discharge		±30		
All Other Pins (Note 8)	V_{ESD}	Human body model, R_D = 1.5kΩ, C_S = 100pF			±4		kV

AC Electrical Characteristics

(V_{AVDD} = V_{DVDD} = 1.7V to 1.9V, V_{IOVDD} = 1.7V to 3.6V, $V_{LVDSVDD}$ = 3.0V to 3.6V, R_L = 100Ω ±1% (differential), T_A = -40°C to +105°C, unless otherwise noted. Differential input voltage $|V_{ID}|$ = 0.1V to 1.2V, input common-mode voltage V_{CM} = $|V_{ID}/2|$ to 2.4V - $|V_{ID}/2|$. Typical values are at V_{AVDD} = V_{DVDD} = V_{IOVDD} = 1.8V, $V_{LVDSVDD}$ = 3.3V, T_A = +25°C.) (Note 3)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
CLOCK INPUT (RXCLKIN)						
Clock Frequency	$f_{RXCLKIN\_}$	BWS = low, DRS = ‘1’	8.33		16.66	MHz
		BWS = low, DRS = ‘0’	16.66		104	
		BWS = mid, DRS = ‘1’	18.33		36.66	
		BWS = mid, DRS = ‘0’	36.66		104	
		BWS = high, DRS = ‘1’	6.25		12.5	
		BWS = high, DRS = ‘0’	12.5		78	
I²C/UART PORT TIMING						
I²C/UART Bit Rate			9.6		1000	kbps
Output Rise Time	t_R	30% to 70%, C_L = 10pF to 100pF, 1kΩ pullup to IOVDD	20		150	ns

AC Electrical Characteristics (continued)

(V_{AVDD} = V_{DVDD} = 1.7V to 1.9V, V_{IOVDD} = 1.7V to 3.6V, $V_{LVDSVDD}$ = 3.0V to 3.6V, R_L = 100Ω ±1% (differential), T_A = -40°C to +105°C, unless otherwise noted. Differential input voltage $|V_{ID}|$ = 0.1V to 1.2V, input common-mode voltage V_{CM} = $|V_{ID}/2|$ to 2.4V - $|V_{ID}/2|$. Typical values are at V_{AVDD} = V_{DVDD} = V_{IOVDD} = 1.8V, $V_{LVDSVDD}$ = 3.3V, T_A = +25°C.) (Note 3)

PARAMETER	SYMBOL	CONDITIONS			MIN	TYP	MAX	UNITS
Output Fall Time	t_F	70% to 30%, C_L = 10pF to 100pF, 1kΩ pullup to IOVDD			20		150	ns
I²C TIMING (Figure 6)								
SCL Clock Frequency	f_{SCL}	Low f_{SCL} range: (I2CMSTBT = 010, I2CSLVSH = 10)			9.6		100	kHz
		Mid f_{SCL} range: (I2CMSTBT 101, I2CSLVSH = 01)			> 100		400	kHz
		High f_{SCL} range: (I2CMSTBT = 111, I2CSLVSH = 00)			> 400		1000	kHz
START Condition Hold Time	$t_{HD:STA}$	f_{SCL} range	Low		4.0			µs
			Mid		0.6			
			High		0.26			
Low Period of SCL Clock	t_{LOW}	f_{SCL} range	Low		4.7			µs
			Mid		1.3			
			High	V_{IOVDD} = 1.7V to < 3V (Note 9)	0.6			
				V_{IOVDD} = 3.0V to 3.6V	0.5			
High Period of SCL Clock	t_{HIGH}	f_{SCL} range	Low		4.0			µs
			Mid		0.6			
			High		0.26			
Repeated START Condition Setup Time	$t_{SU:STA}$	f_{SCL} range	Low		4.7			µs
			Mid		0.6			
			High		0.26			
Data Hold Time	$t_{HD:DAT}$	f_{SCL} range	Low		0			µs
			Mid		0			
			High		0			
Data Setup Time	$t_{SU:DAT}$	f_{SCL} range	Low		250			ns
			Mid		100			
			High		50			
Setup Time for STOP Condition	$t_{SU:STO}$	f_{SCL} range	Low		4.0			µs
			Mid		0.6			
			High		0.26			
Bus Free Time	t_{BUF}	f_{SCL} range	Low		4.7			µs
			Mid		1.3			
			High		0.5			

AC Electrical Characteristics (continued)

(V_{AVDD} = V_{DVDD} = 1.7V to 1.9V, V_{IOVDD} = 1.7V to 3.6V, $V_{LVDSVDD}$ = 3.0V to 3.6V, R_L = 100Ω ±1% (differential), T_A = -40°C to +105°C, unless otherwise noted. Differential input voltage $|V_{ID}|$ = 0.1V to 1.2V, input common-mode voltage V_{CM} = $|V_{ID}/2|$ to 2.4V - $|V_{ID}/2|$. Typical values are at V_{AVDD} = V_{DVDD} = V_{IOVDD} = 1.8V, $V_{LVDSVDD}$ = 3.3V, T_A = +25°C.) (Note 3)

PARAMETER	SYMBOL	CONDITIONS			MIN	TYP	MAX	UNITS
Data Valid Time Note 14	$t_{VD:DAT}$	f_{SCL} range	Low				3.45	µs
			Mid				0.9	
			High	V_{IOVDD} = 1.7V to < 3V (Note 10)			0.55	
				V_{IOVDD} = 3.0V to 3.6V			0.45	
Data Valid Acknowledge Time Note 14	$t_{VD:ACK}$	f_{SCL} range	Low				3.45	µs
			Mid				0.9	
			High	V_{IOVDD} = 1.7V to < 3V (Note 11)			0.55	
				V_{IOVDD} = 3.0V to 3.6V			0.45	
Pulse Width of Spikes Suppressed	t_{SP}	f_{SCL} range	Low				50	ns
			Mid				50	
			High				50	
Capacitive Load Each Bus Line	C_B	Note 12					100	pF
SWITCHING CHARACTERISTICS (Note 12)								
Differential Output Rise/Fall Time	t_R, t_F	20% to 80%, V_{OD} ≥ 400mV, R_L = 100Ω, serial bit rate = 3.12Gbps				90	150	ps
Total Serial Output Jitter (Differential Output)	t_{TSOJ1}	3.12Gbps PRBS signal, measured at V_{OD} = 0V differential, preemphasis disabled (Figure 7)				0.21		UI
Deterministic Serial Output Jitter (Differential Output)	t_{DSOJ2}	3.12Gbps PRBS signal, measured at V_{OD} = 0V differential, preemphasis disabled (Figure 7)				0.09		UI
Total Serial Output Jitter (Single-Ended Output)	t_{TSOJ1}	3.12Gbps PRBS signal, measured at V_O/2, preemphasis disabled (Figure 3)				0.19		UI
Deterministic Serial Output Jitter (Single-Ended Output)	t_{DSOJ2}	3.12Gbps PRBS signal, measured at V_O/2, preemphasis disabled (Figure 3)				0.1		UI
CNTL_ Input Setup Time	t_{SET}	(Figure 8)			3			ns
CNTL_ Input Hold Time	t_{HOLD}	(Figure 8)			1.5			ns
RXIN_ Skew Margin	t_{RSKM}	No RXCLKIN spread (Figure 9)			0.3			UI

AC Electrical Characteristics (continued)

(V_{AVDD} = V_{DVDD} = 1.7V to 1.9V, V_{IOVDD} = 1.7V to 3.6V, $V_{LVDSVDD}$ = 3.0V to 3.6V, R_L = 100Ω ±1% (differential), T_A = -40°C to +105°C, unless otherwise noted. Differential input voltage $|V_{ID}|$ = 0.1V to 1.2V, input common-mode voltage V_{CM} = $|V_{ID}/2|$ to 2.4V - $|V_{ID}/2|$. Typical values are at V_{AVDD} = V_{DVDD} = V_{IOVDD} = 1.8V, $V_{LVDSVDD}$ = 3.3V, T_A = +25°C.) (Note 3)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
GPI to GPO Delay	t_{GPIO}	Deserializer GPI to serializer GPO (Figure 10)				350	µs
Serializer Delay (Note 13)	t_{SD}	(Figure 11)	Spread-spectrum enabled			5440	Bits
			Spread-spectrum disabled			1920	
Link Start Time	t_{LOCK}	(Figure 12)				3.5	ms
Power-Up Time	t_{PU}	(Figure 13)				8	ms
I²S/TDM INPUT TIMING							
WS Frequency	f_{WS}	(See Table 5)		8		192	kHz
Sample Word Length	n_{WS}	(See Table 5)		8		32	Bits
SCK Frequency	f_{SCK}	f_{SCK} = f_{WS} x n_{WS} x (2 or 8)		(8 x 2) x 2		(192 x 32) x 8	kHz
SCK Clock High Time	t_{HC}	$V_{SCK} \geq V_{IH}$, t_{SCK} = $1/f_{SCK}$ (Note 13)		0.35 x t_{SCK}			ns
SCK Clock Low Time	t_{LC}	$V_{SCK} \leq V_{IL}$, t_{SCK} = $1/f_{SCK}$ (Note 13)		0.35 x t_{SCK}			ns
SD, WS Setup Time	t_{SET}	(Figure 14, Note 13)		2			ns
SD, WS Hold Time	t_{HOLD}	(Figure 14, Note 13)		2			ns

Note 3: Limits are 100% production tested at T_A = +105°C. Limits over the operating temperature range are guaranteed by design and characterization, unless otherwise noted.

Note 4: To provide a midlevel, leave the input open, or, if driven, put driver in high impedance. High-impedance leakage current must be less than ±10µA.

Note 5: I_{IN} MIN due to voltage drop across the internal pullup resistor.

Note 6: HDCP not enabled (MAX9281 only). See Table 22 for additional supply current when HDCP is enabled.

Note 7: Specified pin to ground.

Note 8: Specified pin to all supply/ground.

Note 9: The I²C bus standard t_{LOW} min = 0.5µs.

Note 10: The I²C bus standard $t_{VD:DAT}$ max = 0.45µs.

Note 11: The I²C bus standard $t_{VD:ACK}$ max = 0.45µs.

Note 12: Not production tested. Guaranteed by design.

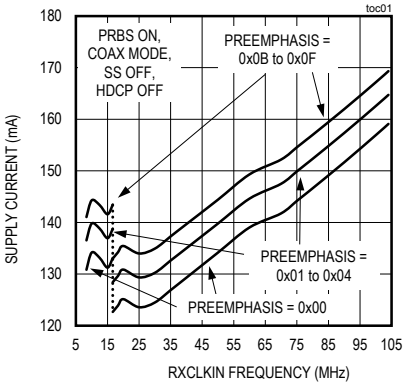
Note 13: Measured in serial link bit times. Bit time = 1/(30 x f_{PCLKIN}) for BWS = '0' or open. Bit time = 1/(40 x f_{PCLKIN}) for BWS = '1'.

Note 14: I²C valid times apply only when the device is operating as a local side device.

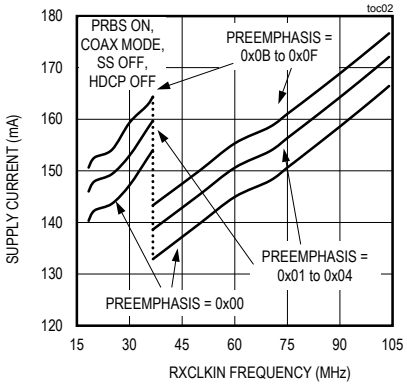
Typical Operating Characteristics

(V_{AVDD} = V_{DVDD} = V_{IOVDD} = 1.8V, $V_{LVDSVDD}$ = 3.3V, T_A = +25°C, unless otherwise noted.)

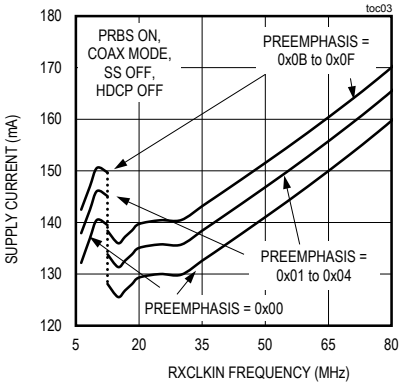
SUPPLY CURRENT vs. RXCLKIN FREQUENCY (BWS = LOW)



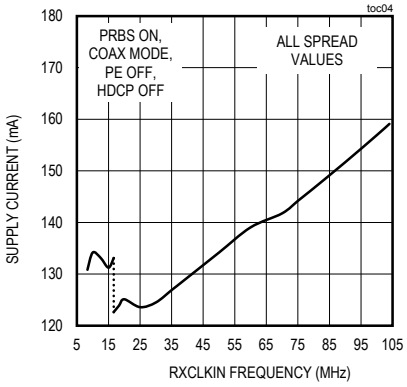
SUPPLY CURRENT vs. RXCLKIN FREQUENCY (BWS = OPEN)



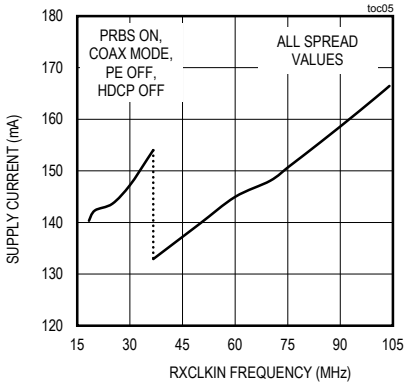
SUPPLY CURRENT vs. RXCLKIN FREQUENCY (BWS = HIGH)



SUPPLY CURRENT vs. RXCLKIN FREQUENCY (BWS = LOW)



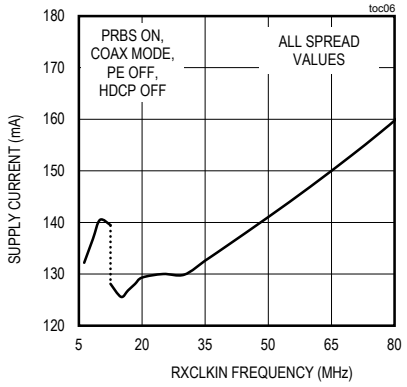
SUPPLY CURRENT vs. RXCLKIN FREQUENCY (BWS = OPEN)



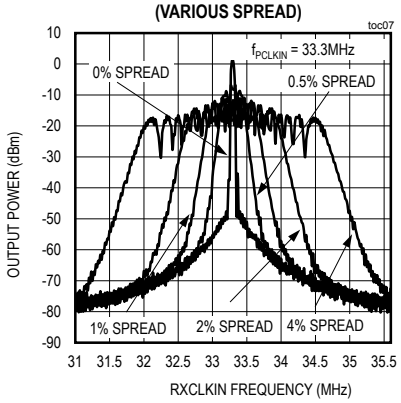
Typical Operating Characteristics (continued)

(V_{AVDD} = V_{DVDD} = V_{IOVDD} = 1.8V, $V_{LVDSVDD}$ = 3.3V, T_A = +25°C, unless otherwise noted.)

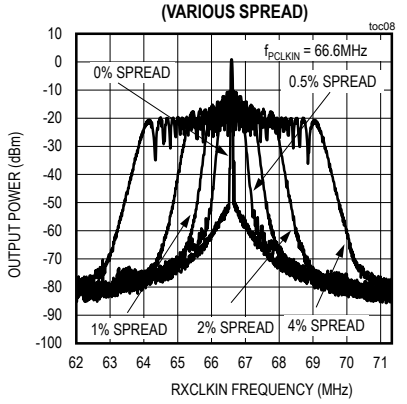
SUPPLY CURRENT vs. RXCLKIN FREQUENCY (BWS = HIGH)



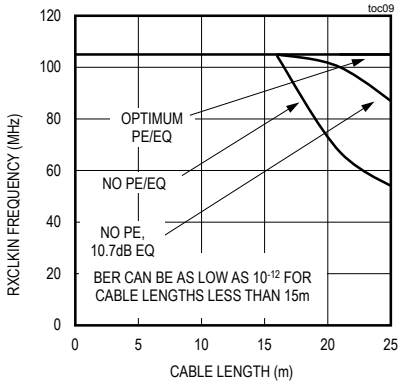
OUTPUT SPECTURM vs. RXCLKIN FREQUENCY (VARIOUS SPREAD)



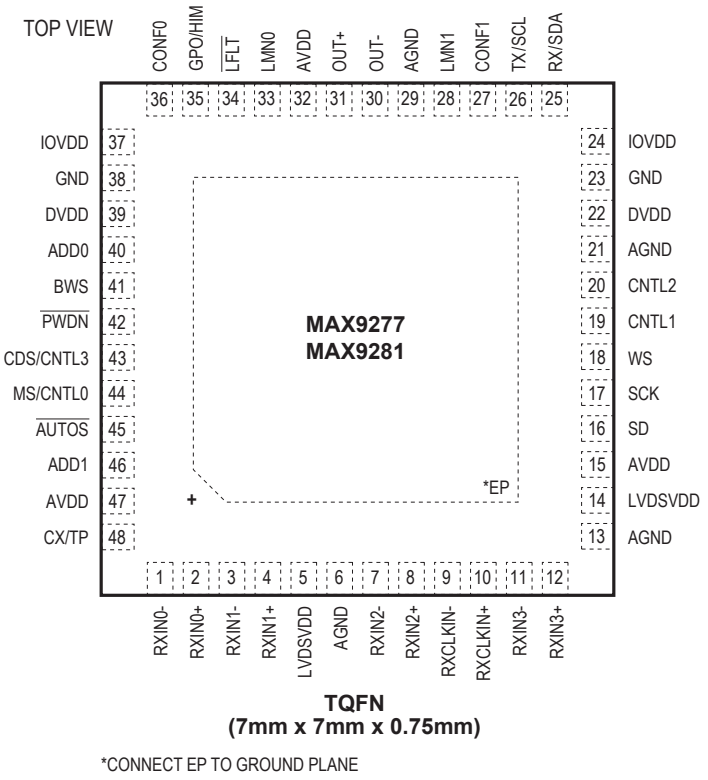
OUTPUT SPECTURM vs. RXCLKIN FREQUENCY (VARIOUS SPREAD)



MAXIMUM RXCLKIN FREQUENCY vs. COAX CABLE LENGTH (BER ≤ 10^{-10})



Pin Configuration



TQFN
(7mm x 7mm x 0.75mm)

*CONNECT EP TO GROUND PLANE

Pin Description

PIN	NAME	FUNCTION
1–4, 7, 8, 11, 12	RXIN_-, RXIN_+	LVDS Data Inputs. Set BWS = low to use RXIN0_ to RXIN2_ (3-channel mode). Set BWS = high or open to use RXIN0_ to RXIN3_ (4-channel or high-bandwidth mode). Certain data bits encrypted when HDCP is enabled (MAX9281 only, Table 2)
5, 14	LVDSVDD	3.3V LVDS Power Supply. Bypass LVDSVDD to AGND with 0.1µF and 0.001µF capacitors as close as possible to the device with the smallest value capacitor closest to LVDSVDD.
6, 13, 21, 29	AGND	Analog and LVDS Ground
9, 10	RXCLKIN-, RXCLKIN+	LVDS Clock Input. Provides the PLL reference clock.
15, 32, 47	AVDD	1.8V Analog Power Supply. Bypass AVDD to EP with 0.1µF and 0.001µF capacitors as close as possible to the device with the smaller capacitor closest to AVDD.
16	SD	I2S/TDM Serial-Data Input with Internal Pulldown to GND. Disable I2S/TDM encoding to use SD as an additional control/data input latched on the selected edge of PCLKIN. Encrypted when HDCP is enabled.
17	SCK	I2S/TDM Serial-Clock Input with Internal Pulldown to GND

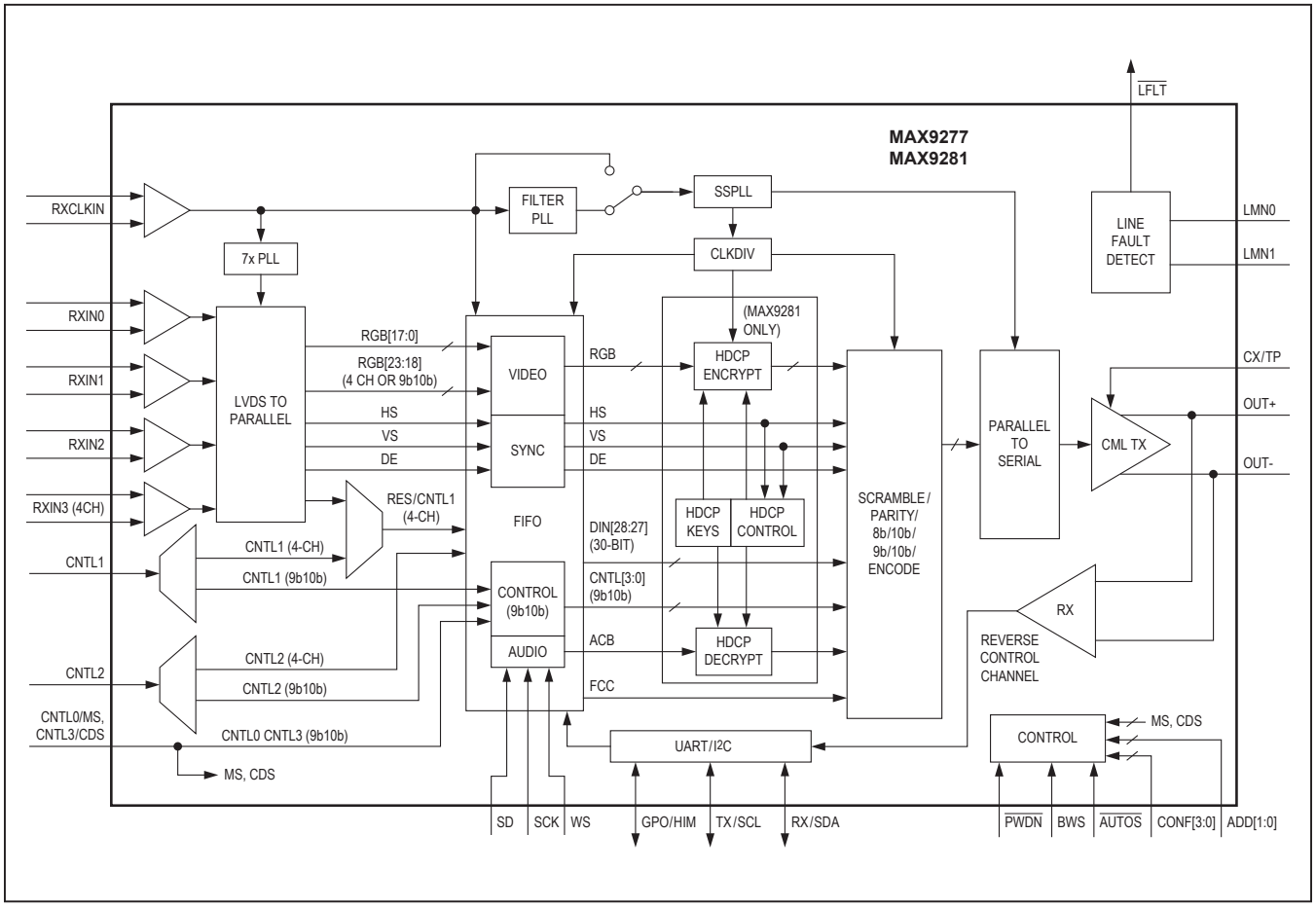
Pin Description (continued)

PIN	NAME	FUNCTION
18	WS	I2S/TDM Word-Select Input with Internal Pulldown to GND
19	CNTL1	Control Input With Internal Pulldown to GND. Input data is latched every RXCLKIN_ cycle (Figure 15). CNTL1 is not available in 3-channel mode (BWS = low). Set BWS = high or open (4-channel or high-bandwidth mode) to use this input. CNTL1 not encrypted when HDCP is on (MAX9281 only) CNTL1 or RES ("Reserved" from VESA Standard Panel Specification) is mapped to internal bit DIN27. See the *Reserved Bit (RES)/CNTL1* section.
20	CNTL2	Control Input With Internal Pulldown to GND. Input data is latched every RXCLKIN_ cycle (Figure 15). CNTL2 is not available in 3-channel mode (BWS = low). Set BWS = high or open (4-channel or high-bandwidth mode) to use this input. CNTL2 not encrypted when HDCP is on (MAX9281 only). CNTL2 is mapped to internal bit DIN28.
22, 39	DVDD	1.8V Digital Power Supply. Bypass DVDD to GND with 0.1µF and 0.001µF capacitors as close as possible to the device with the smaller value capacitor closest to DVDD.
23, 38	GND	Digital and I/O Ground
24, 37	IOVDD	I/O Supply Voltage. 1.8V to 3.3V logic I/O Power Supply. Bypass IOVDD to GND with 0.1µF and 0.001µF capacitors as close as possible to the device with the smallest value capacitor closest to IOVDD. IOVDD sets the voltage levels for all pins except for the LVDS inputs and OUT+/-.
25	RX/SDA	UART Receive/I2C Serial Data Input/Output with Internal 30kΩ Pullup to IOVDD. Function is determined by the state of CONF[1:0] at power-up (Table 10). RX/SDA has an open-drain driver and requires a pullup resistor. RX: Input of the serializer's UART. SDA: Data input/output of the serializer's I2C Master/Slave.
26	TX/SCL	UART Transmit/I2C Serial Clock Input/Output with Internal 30kΩ Pullup to IOVDD. Function is determined by the state of CONF[1:0] at power-up (Table 10). TX/SCL has an open-drain driver and requires a pullup resistor. TX: Output of the serializer's UART. SCL: Clock input/output of the serializer's I2C Master/Slave.
27	CONF1	Three-Level Configuration Input. The state of CONF1 latches at power-up or when resuming from power-down mode ($\overline{PWDN}$ = low). Use 6kΩ (max) for pullup to IOVDD/pulldown to GND. See Table 10 for details.
28	LMN1	Line-Fault Monitor Input 1 (see Figure 4 for details)
30	OUT-	Inverting CML Coax/Twisted-Pair Serial Output
31	OUT+	Noninverting CML Coax/Twisted-Pair Serial Output
33	LMN0	Line-Fault Monitor Input 0 (see Figure 4 for details)
34	$\overline{LFLT}$	Active-Low Open-Drain Line-Fault Output. $\overline{LFLT}$ has a 60kΩ internal pullup to IOVDD. $\overline{LFLT}$ = low indicates a line fault. $\overline{LFLT}$ is output high when $\overline{PWDN}$ = low.
35	GPO/HIM	General-Purpose Output/High Immunity Mode Input. Functions as HIM input with internal pulldown to GND at power-up or when resuming from power-down mode ($\overline{PWDN}$ = low), and switches to GPO output automatically after power-up. HIM: Default HIGHIMM bit value is latched at power-up or when resuming from power-down mode ($\overline{PWDN}$ = low) and is active-high. Connect HIM to IOVDD with a 30kΩ or less pullup resistor to set high or leave open to set low. HIGHIMM can be programmed to a different value after power-up. HIGHIMM in the deserializer must be set to the same value. GPO: Output follows the state of the GPI (or INT) input on the deserializer. GPO is low after power-up or when $\overline{PWDN}$ is low.

Pin Description (continued)

PIN	NAME	FUNCTION
36	CONF0	Three-Level Configuration Input. The state of CONF0 latches at power-up or when resuming from power-down mode ($\overline{PWDN}$ = low). Use 6kΩ (max) for pullup to IOVDD/pulldown to GND. See Table 10 for details.
40	ADD0	Three-Level Address Selection Input. The state of ADD0 latches at power-up or when resuming from power-down mode ($\overline{PWDN}$ = low). Use 6kΩ (max) for pullup to IOVDD/pulldown to GND. See Table 1 for details.
41	BWS	Three-Level Bus Width Select Input. Set BWS to the same level on both sides of the serial link. Set BWS = low with 6kΩ (max) pulldown for 3-channel mode. Set BWS = high with 6kΩ (max) pullup to IOVDD for 4-channel mode. Set BWS = open for high-bandwidth mode.
42	$\overline{PWDN}$	Active-Low, Power-Down Input with Internal Pulldown to EP. Set $\overline{PWDN}$ low to enter power-down mode to reduce power consumption.
43	CDS/CNTL3	Control Direction Selection/Auxiliary Control Signal Input with Internal Pulldown to GND. Function is determined by the CDSCNTL3 register bit and defaults to CDS on power-up. CDS (CDSCNTL3 = 0): Control link direction selection input with internal pulldown to GND. Set CDS = low when the control channel master µC is connected at the serializer. Set CDS = high when the control channel master µC is connected at the deserializer. CNTL3 (CDSCNTL3 = 1): Used only in high-bandwidth mode (BWS = open). CNTL3 not encrypted when HDCP is enabled (MAX9281 only).
44	MS/CNTL0	Mode Select/Auxiliary Control Signal Input with Internal Pulldown to GND. Function is determined by the MSCNTL0 register bit and defaults to MS on power-up. MS (MSCNTL0 = 0): Set MS = low, to select base mode. Set MS = high to select the bypass mode. CNTL0 (MSCNTL0 = 1): Used only in high-bandwidth mode (BWS = open). CNTL0 not encrypted when HDCP is enabled (MAX9281 only).
45	$\overline{AUTOS}$	Active-Low Auto-Start Input With Internal Pulldown to GND. Set $\overline{AUTOS}$ = high, to disable serialization at power-up or when resuming from power-down mode ($\overline{PWDN}$ = low). Set $\overline{AUTOS}$ = low, to enable serialization and automatic PLL range selection power-up or when resuming from power-down mode.
46	ADD1	Three-Level Address Selection Input. The state of ADD1 latches at power-up or when resuming from power-down mode ($\overline{PWDN}$ = low). Use 6kΩ (max) for pullup to IOVDD/pulldown to GND. See Table 1 for details.
48	CX/TP	Coax/Twisted Pair Input With Internal Pulldown to GND. Set CX/TP low for twisted-pair cable drive (differential output). Set CX/TP high for coax cable drive (single-ended output).
—	EP	Exposed Pad. EP is internally connected to AGND. MUST connect EP to the PCB ground plane through an array of vias for proper thermal and electrical performance.

Functional Diagram



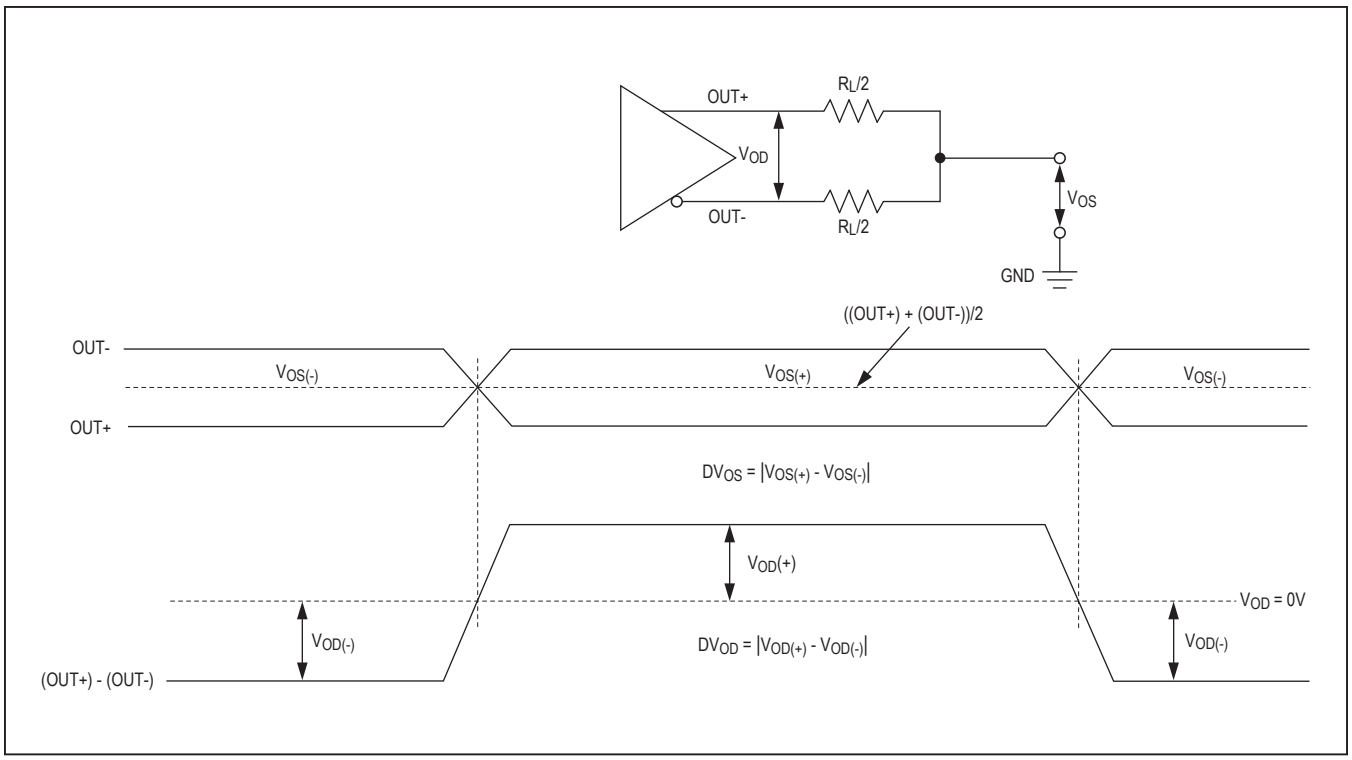


Figure 1. Serial-Output Parameters

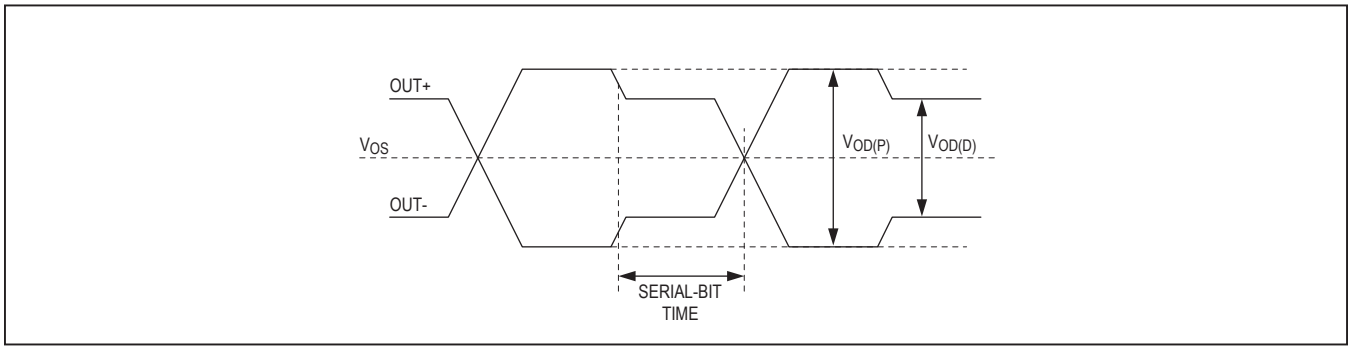


Figure 2. Output Waveforms at OUT+, OUT-

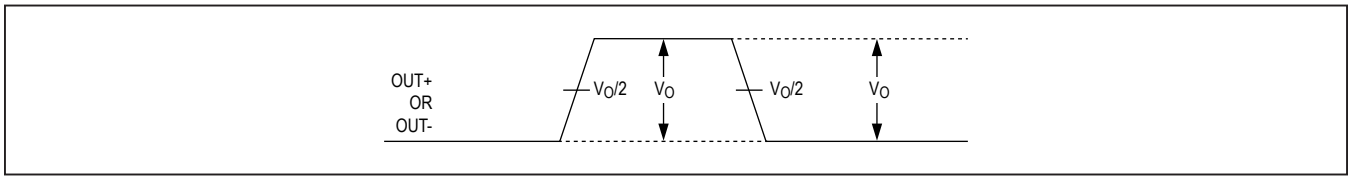


Figure 3. Single-Ended Output Template

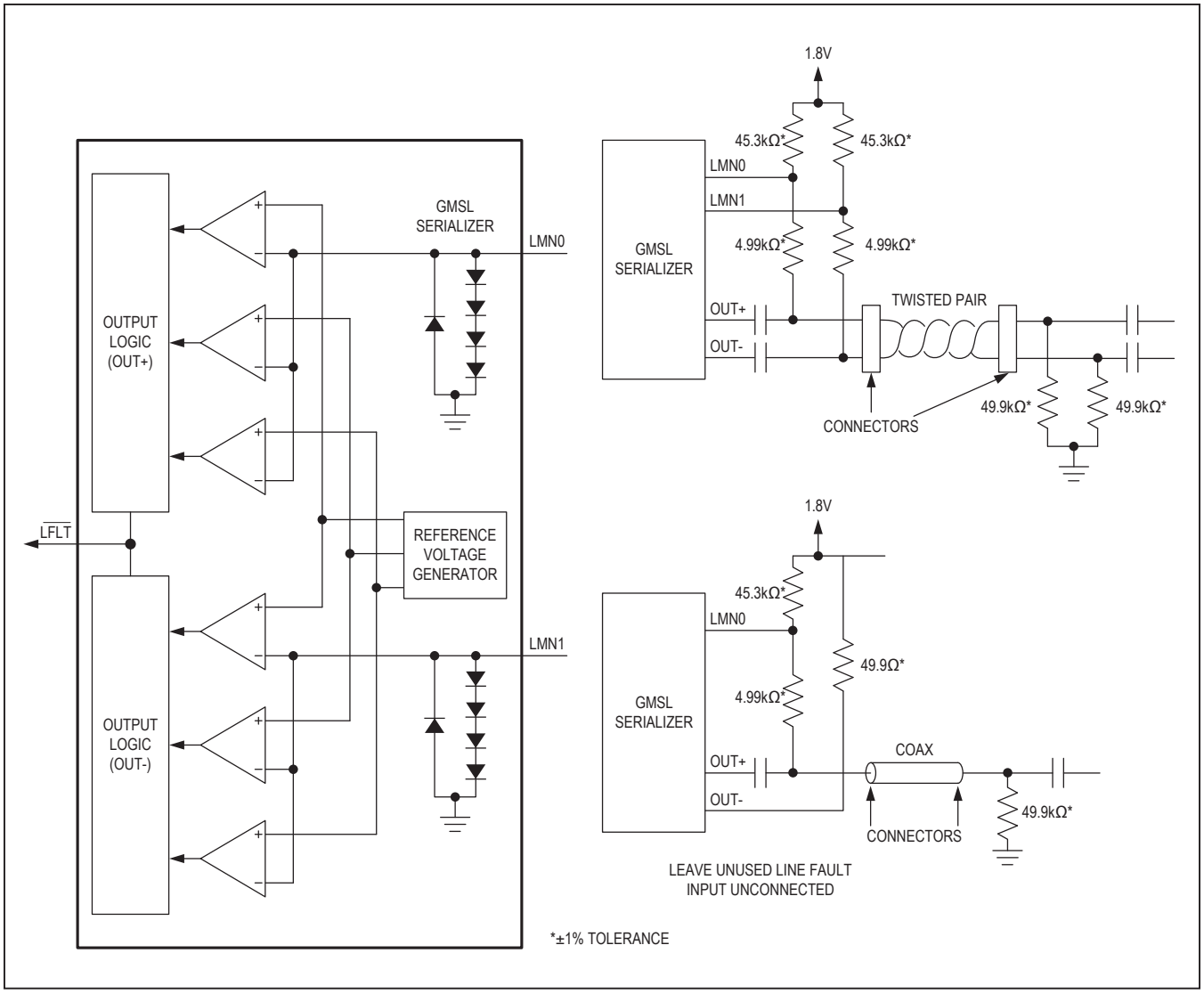


Figure 4. Line Fault Detector Circuit

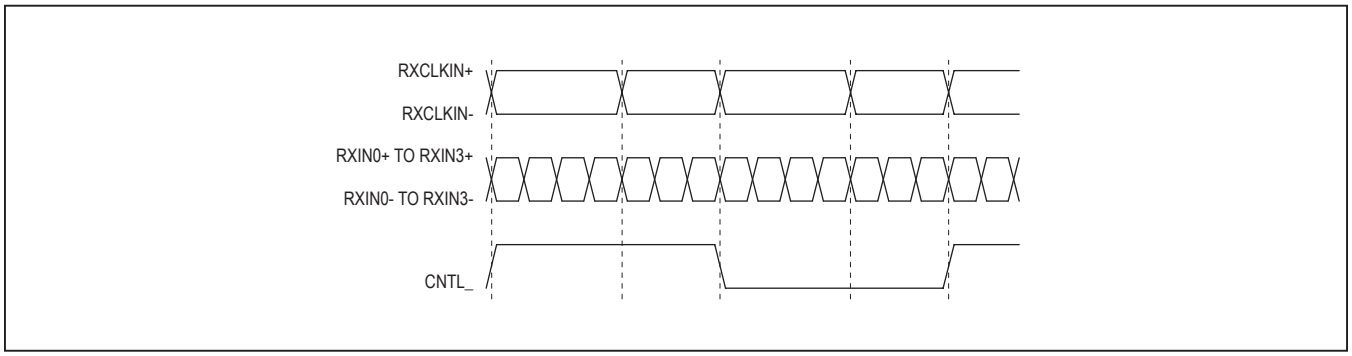


Figure 5. Worst-Case Pattern Input

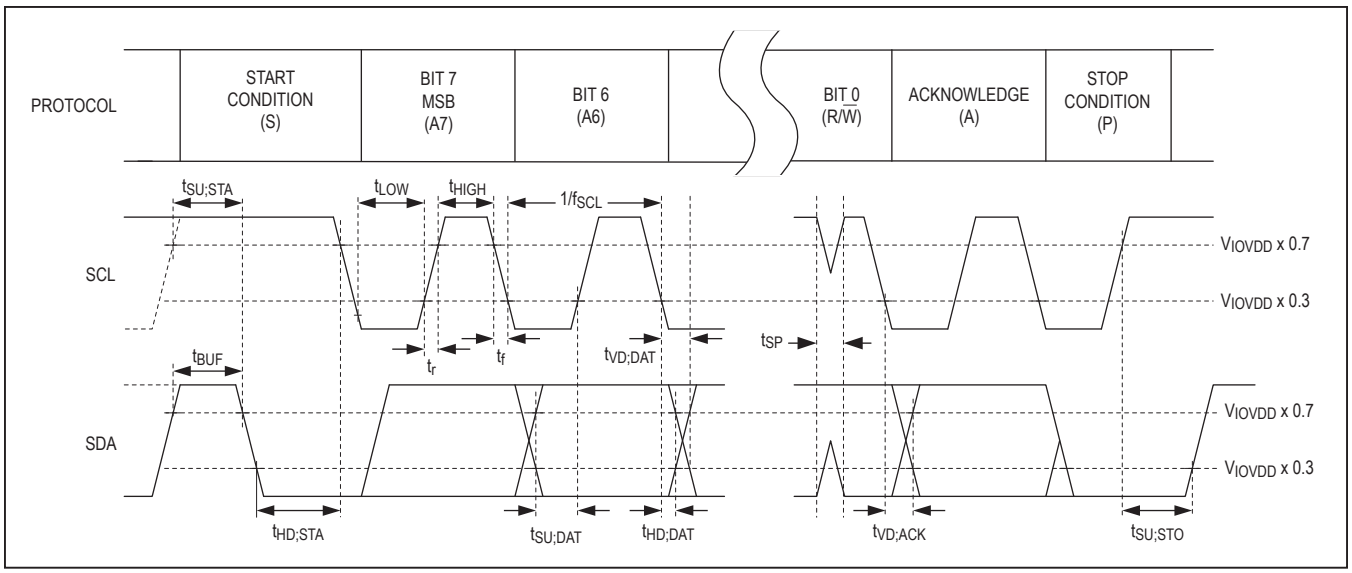


Figure 6. I²C Timing Parameters

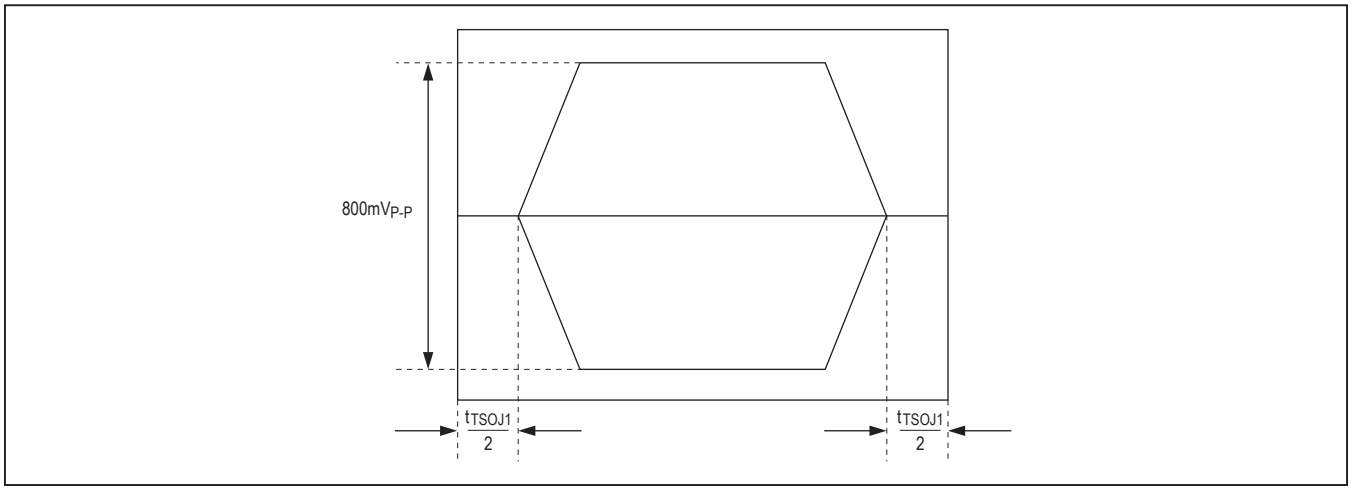


Figure 7. Differential Output Template

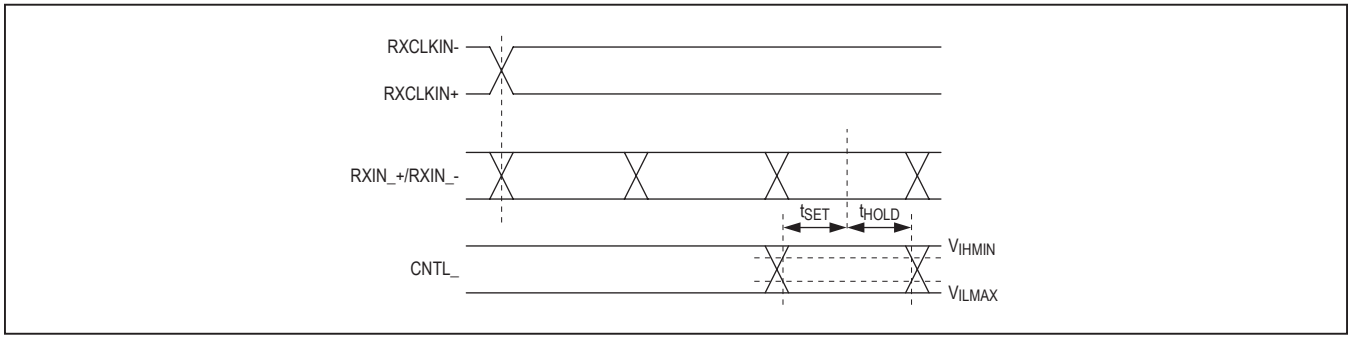


Figure 8. Input Setup and Hold Times

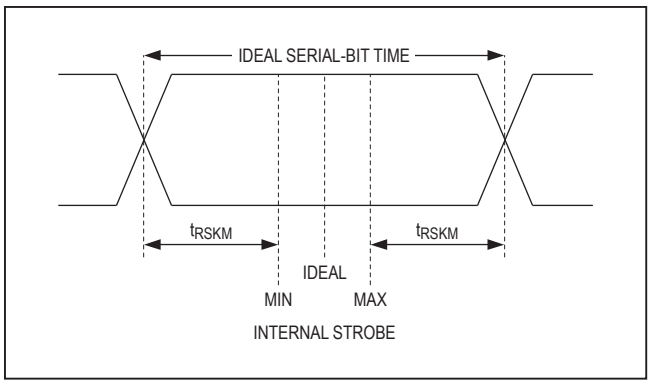


Figure 9. LVDS Receiver Input Skew Margin

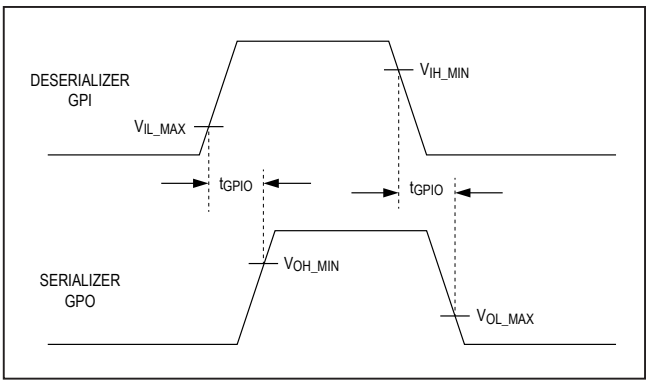


Figure 10. GPI-to-GPO Delay

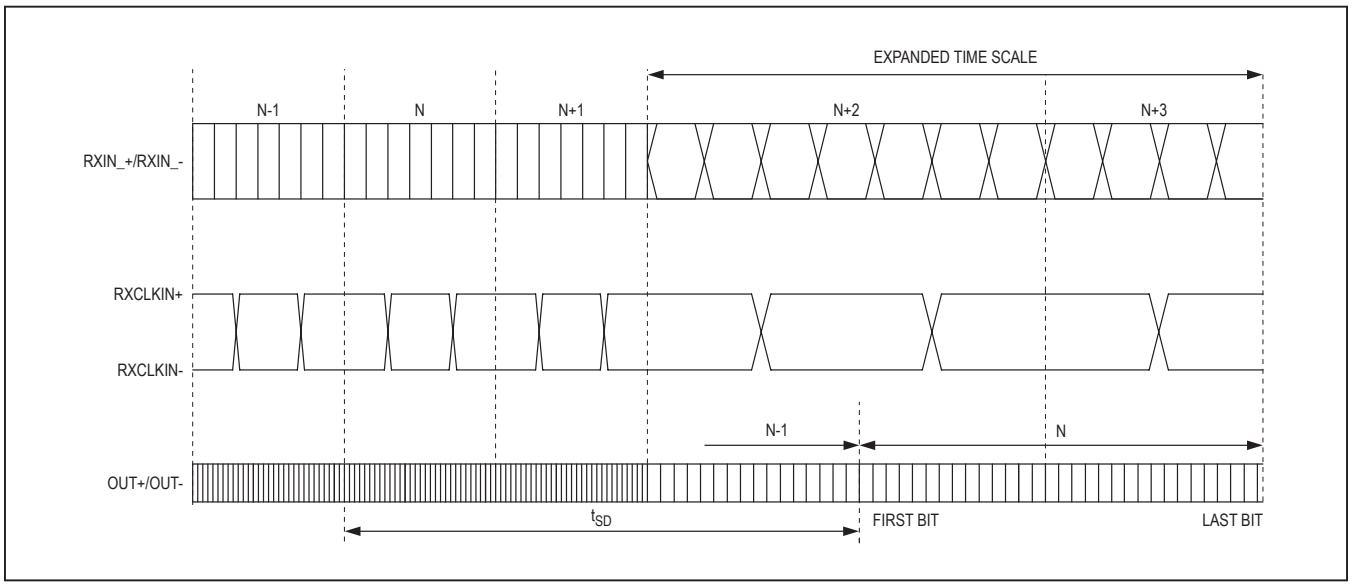


Figure 11. Serializer Delay

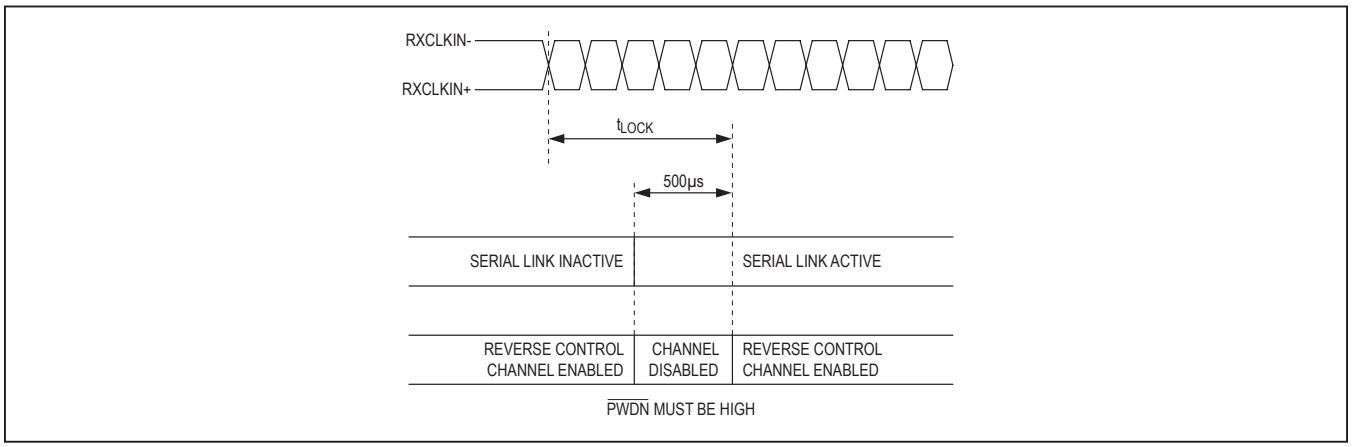


Figure 12. Link Startup Time

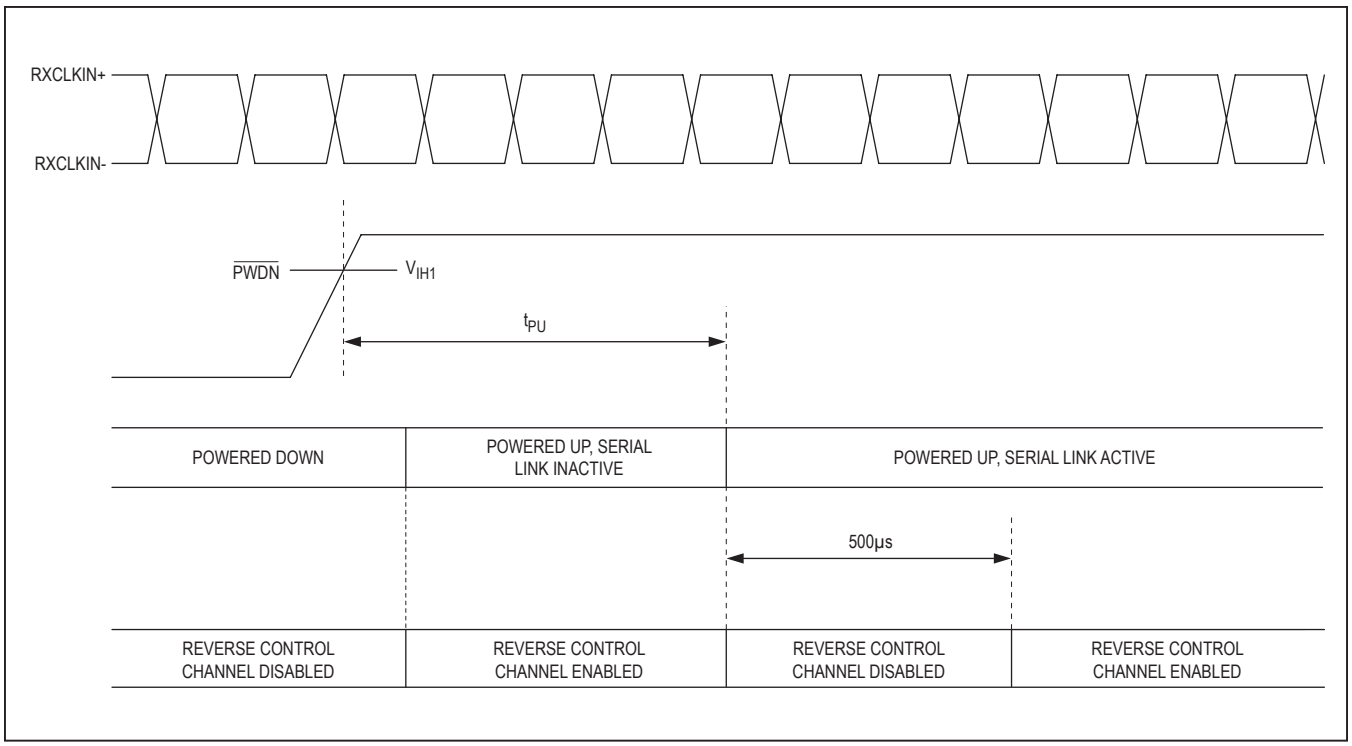


Figure 13. Power-Up Delay

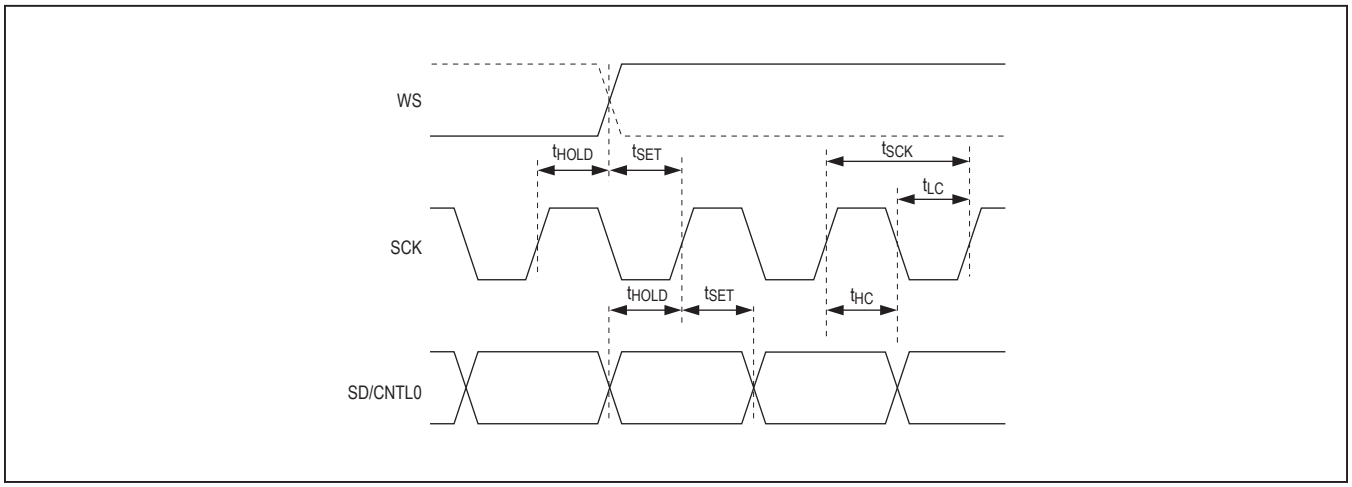


Figure 14. Input I²S Timing Parameters

Detailed Description

The MAX9277/MAX9281 serializers, when paired with the MAX9276/MAX9280 deserializers, provides the full set of operating features, but is backward compatible with the MAX9249–MAX9270 family of Gigabit Multimedia Serial Link (GMSL) devices, and have basic functionality when paired with any GMSL device. The MAX9281 has High-bandwidth Digital Content Protection (HDCP) while the MAX9277 does not.

The serializer has a maximum serial-bit rate of 3.12Gbps for up to 15m of cable and operates up to a maximum output clock of 104MHz in 24-bit, 3-channel mode and 27-bit high-bandwidth mode, or 78MHz in 32-bit, 4-channel mode. This bit rate and output flexibility support a wide range of displays, from QVGA (320 x 240) to 1920 x 720 and higher with 24-bit color, as well as megapixel image sensors. An encoded audio channel supports L-PCM I²S stereo and up to 8 channels of L-PCM in TDM mode. Sample rates of 32kHz to 192kHz are supported with sample depth from 8 to 32 bits. Output pre/deemphasis, combined with GMSL deserializer equalization, extends the cable length and enhances link reliability.

The control channel enables a µC to program the serializer and deserializer registers and program registers on peripherals. The control channel is also used to perform HDCP functions (MAX9281 only). The µC can be located at either end of the link, or when using two µCs, at both ends. Two modes of control-channel operation are available. Base mode uses either I²C or GMSL UART protocol, while bypass mode uses a user-defined UART protocol. UART protocol allows full-duplex communication, while I²C allows half-duplex communication.

Spread spectrum is available to reduce EMI on the serial output. The serial output and LVDS input complies with ISO 10605 and IEC 61000-4-2 ESD protection standards.

Register Mapping

Registers set the operating conditions of the serializers and are programmed using the control channel in base mode. The MAX9277/MAX9281 holds its own device address and the device address of the deserializer with which it is paired. Similarly, the deserializer holds its own device address and the address of the MAX9277/MAX9281. Whenever a device address is changed be sure to write the new address to both devices. The default device address of the serializer is set by the ADD[1:0] (see Table 1). Registers 0x00 and 0x01 in both devices hold the device addresses.

Table 1. Device Address Defaults (Register 0x00, 0x01)

PIN		DEVICE ADDRESS (bin)								SERIALIZER DEVICE ADDRESS (hex)	DESERIALIZER DEVICE ADDRESS (hex)
ADD1	ADD0	D7	D6	D5	D4	D3	D2	D1	D0		
Low	Low	1	0	0	X*	0	0	0	R/$\overline{W}$	80	90
Low	High	1	0	0	X*	0	1	0	R/$\overline{W}$	84	94
Low	Open	1	0	0	X*	1	0	0	R/$\overline{W}$	88	98
High	Low	1	1	0	X*	0	0	0	R/$\overline{W}$	C0	D0
High	High	1	1	0	X*	0	1	0	R/$\overline{W}$	C4	D4
High	Open	1	1	0	X*	1	0	0	R/$\overline{W}$	C8	D8
Open	Low	0	1	0	X*	0	0	0	R/$\overline{W}$	40	50
Open	High	0	1	0	X*	0	1	0	R/$\overline{W}$	44	54
Open	Open	0	1	0	X*	1	0	0	R/$\overline{W}$	48	58

**X = 0 for the serializer address, X = 1 for the deserializer address.*

Input Bit Map

The input bit width depends on settings of the bus width (BWS) pin. Table 2 lists the bit map.

Table 2. Input Map (See Figure 15, Figure 16)

MODE		3-CHANNEL MODE (BWS = LOW)	HIGH-BANDWIDTH MODE (BWS = MID)	4-CHANNEL MODE (BWS = HIGH)
SIGNAL	INPUT PIN/ BIT POSITION			
R[5:0]	DIN[5:0]	Used	Used	Used
G[5:0]	DIN [11:6]	Used	Used	Used
B[5:0]	DIN [17:12]	Used	Used	Used
HS, VS, DE	DIN18/HS, DIN19/VS, DIN20/DE	Used**	Used**	Used**
R[7:6]	DIN [22:21]	Not used	Used	Used
G[7:6]	DIN [24:23]	Not used	Used	Used
B[7:6]	DIN [26:25]	Not used	Used	Used
RES, CNTL[2:1]	RES, CNTL[2:1]	Not used	Used*,**	Used**
CNTL3, CNTL0	CDS/CNTL3, MS/CNTL0	Not used	Used*,**	Not used
I²S/TDM	WS, SCK, SD	Used	Used	Used
AUX SIGNAL		Used	Used	Used

**See the High-Bandwidth Mode section for details on timing requirements.*

***Not encrypted when HDCP is enabled (MAX9281 only).*

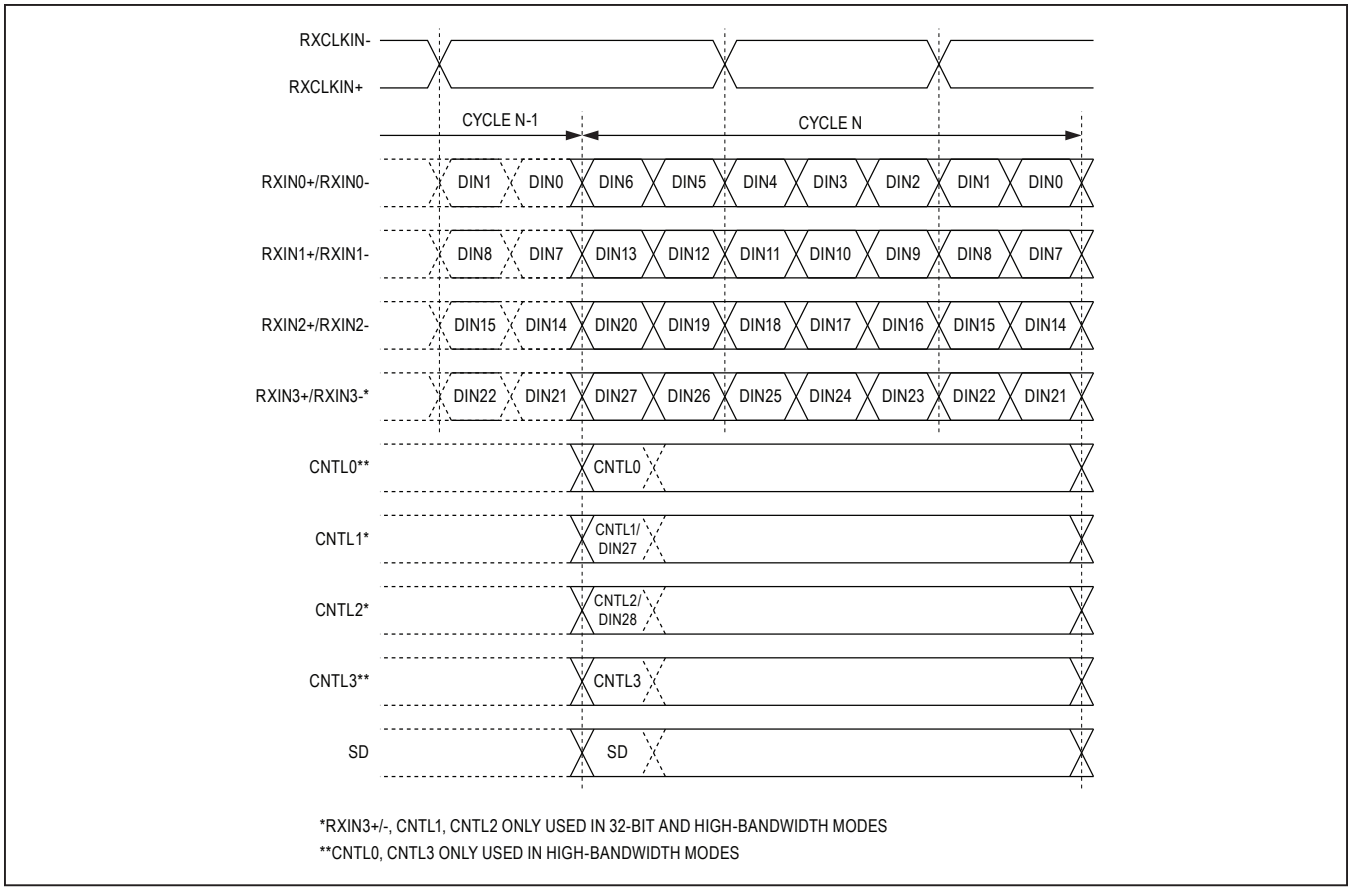


Figure 15. LVDS Input Timing

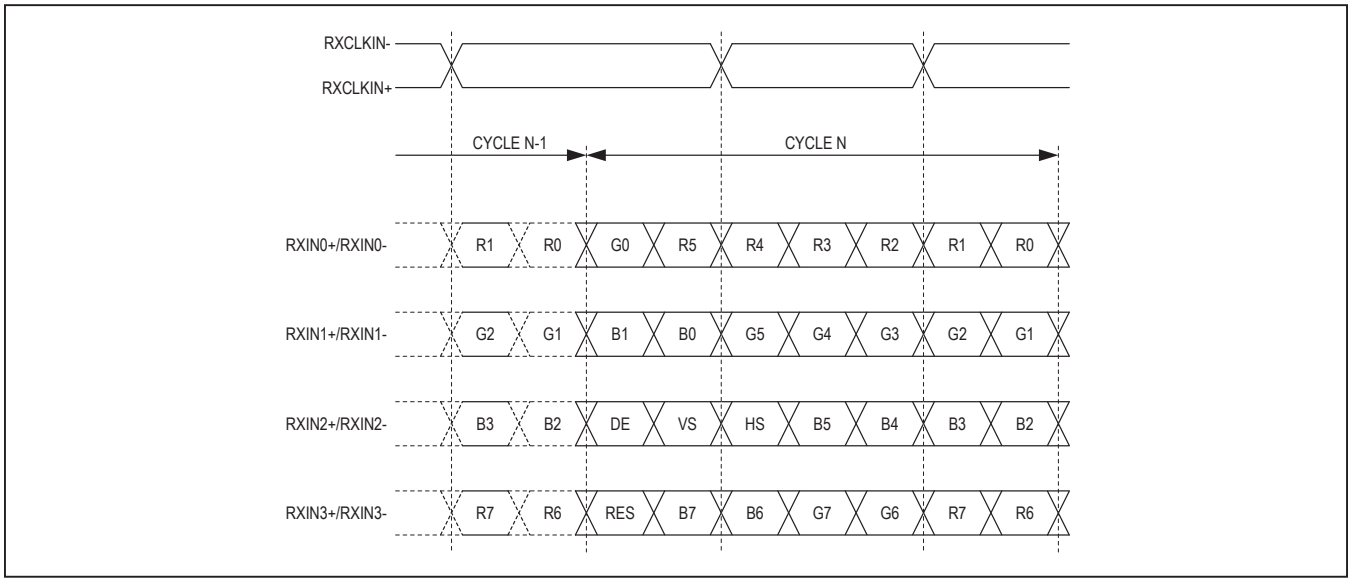


Figure 16. LVDS Clock and Bit Assignment

**VESA and oLDI define naming conventions with regards to MSB and LSB.*

Serial Link Signaling and Data Format

The serializer uses differential CML signaling to drive twisted-pair cable and single-ended CML to drive coaxial cable with programmable pre/deemphasis and AC-coupling. The deserializer uses AC-coupling and programmable channel equalization.

Input data is scrambled and then 8b/10b coded (9b10b in high-bandwidth mode). The deserializer recovers the embedded serial clock, then samples, decodes, and descrambles the data. In 3-channel mode, the first 21 bits contain video data. In 4-channel mode, the first 29 bits contain video data. In high-bandwidth mode, the first 24 bits contain video data, or special control signal packets. The last 3 bits contain the embedded audio channel, the embedded forward control channel, the parity bit of the serial word (see Figure 17 and Figure 18).

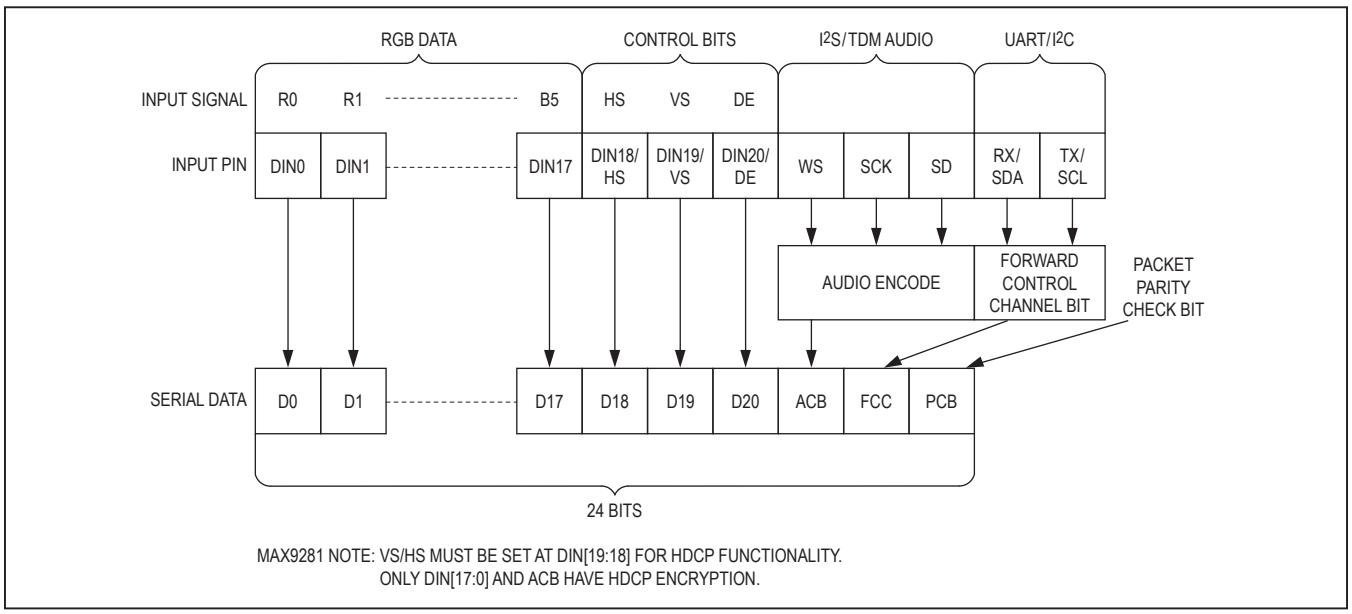


Figure 17. 3-Channel Mode Serial Data Format

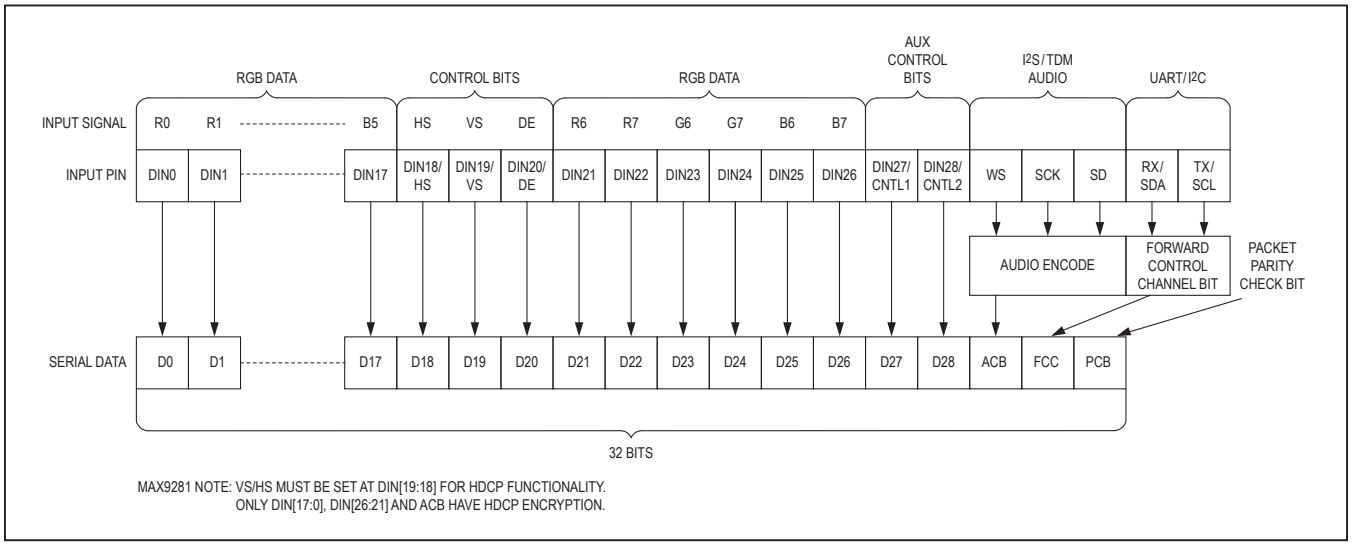


Figure 18. 4-Channel Mode Serial Data Format

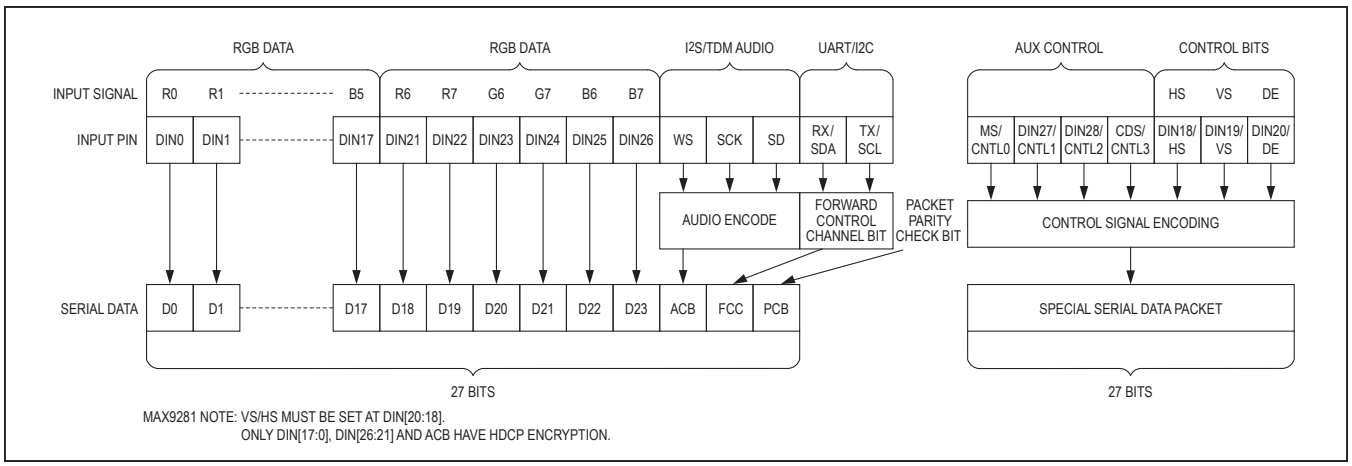


Figure 19. High-Bandwidth Mode Serial Data Format

Table 3. Data-Rate Selection Table

DRS BIT SETTING	BWS PIN SETTING	RXCLKIN_ RANGE (MHz)
0 (high data rate)	Low (3-channel mode)	16.66 to 104
	Mid (high bandwidth mode)	36.66 to 104
	High (4-channel mode)	12.5 to 78
1 (low data rate)	Low	8.33 to 16.66
	Mid	18.33 to 36.66
	High	6.25 to 12.5

Reserved Bit (RES)/CNTL1

In 4-channel mode, the serializer by default serializes RES to serial data bit 27. Set DISRES (D4 of register 0x0D) = 1 to map CNTL1 to serial data bit 27.

Data-Rate Selection

The serializer uses the DRS bit, and BWS input to set the RXCLKIN_ frequency range (Table 3). Set DRS = 1 for low data rate RXCLKIN_ frequency range of 6.25MHz to 16.66MHz. Set DRS = 0 for high data rate RXCLKIN_ frequency range of 12.5MHz to 104MHz.

High-Bandwidth Mode

The serializer uses a 27-bit high-bandwidth mode to support 24-Bit RGB at 104MHz pixel clock. Set BWS = open in both the serializer and deserializer to use high-bandwidth mode. In high-bandwidth mode, the serializer encodes HS, VS, DE and CNTL[3:0] to special packets. Packets are sent by replacing a pixel before the rising edge and after the falling edge of HS, VS, DE signals. However, for CNTL[3:0], which is not always continuously sampled, packets always replace a pixel before the transition of the sampled CNTL[3:0]. Keep HS, VS, and DE low pulse widths at least two pixel clock cycles. By default, CNTL[3:0] are sampled continuously when DE is low. CNTL[3:0] are sampled only on HS/VS transitions when DE is high. If DE triggering of encoded packets is not desired, set the serializer's DISDETRIG = 0 and the CNTLTRIG bits to their desired value (register 0x15) to change the CNTL triggering behavior. Set DETREN = 0 on the deserializer when DE is not periodic.

Audio Channel

The audio channel supports 8kHz to 192kHz audio sampling rates and audio word lengths from 8 bits to 32 bits (2 channel I^2S) or 64 to 256 bits (TDM64 to TDM256). The audio bit clock (SCK) does not have to be synchronized with RXCLKIN_. The serializer automatically encodes audio data into a single bit stream synchronous with RXCLKIN_. The deserializer decodes the audio stream and stores audio words in a FIFO. Audio rate detection uses an internal oscillator to continuously determine the audio data rate and output the audio in I^2S format. The audio channel is enabled by default. When the audio channel is disabled, the SD is treated as an auxiliary control signal.

Since the encoded audio data sent through the serial link is synchronized with RXCLKIN_ (through ACB), low RXCLKIN_ frequencies limit the maximum audio sampling rate. Table 4 lists the maximum audio sampling rate for various RXCLKIN_ frequencies. Spread-spectrum settings do not affect the I^2S/TDM data rate or WS clock frequency.

Table 4. Maximum Audio WS Frequency (kHz) for Various RXCLKIN_ Frequencies

CHANNELS	BITS PER CHAN	RXCLKIN_ FREQUENCY (DRS = 0*) (MHz)										
		12.5	15.0	16.6	20.0	25.0	30.0	35.0	40.0	45.0	50.0	100
2	8	+	+	+	+	+	+	+	+	+	+	+
	16	+	+	+	+	+	+	+	+	+	+	+
	18	185.5	+	+	+	+	+	+	+	+	+	+
	20	174.6	+	+	+	+	+	+	+	+	+	+
	24	152.2	182.7	+	+	+	+	+	+	+	+	+
	32	123.7	148.4	164.3	+	+	+	+	+	+	+	+
4	8	+	+	+	+	+	+	+	+	+	+	+
	16	123.7	148.4	164.3	+	+	+	+	+	+	+	+
	18	112.0	134.4	148.8	179.2	+	+	+	+	+	+	+
	20	104.2	125.0	138.3	166.7	+	+	+	+	+	+	+
	24	88.6	106.3	117.7	141.8	177.2	+	+	+	+	+	+
	32	69.9	83.8	92.8	111.8	139.7	167.6	+	+	+	+	+
6	8	152.2	182.7	+	+	+	+	+	+	+	+	+
	16	88.6	106.3	117.7	141.8	177.2	+	+	+	+	+	+
	18	80.2	93.3	106.6	128.4	160.5	+	+	+	+	+	+
	20	73.3	88.0	97.3	117.3	146.6	175.9	+	+	+	+	+
	24	62.5	75.0	83.0	100	125	150	175	+	+	+	+
	32	48.3	57.9	64.1	77.2	96.5	115.9	135.2	154.5	173.8	+	+
8	8	123.7	148.4	164.3	+	+	+	+	+	+	+	+
	16	69.9	83.8	92.8	111.8	139.7	167.6	+	+	+	+	+
	18	62.5	75.0	83.0	100.0	125.0	150.0	175.0	+	+	+	+
	20	57.1	68.5	75.8	91.3	114.2	137.0	159.9	182.7	+	+	+
	24	48.3	57.9	64.1	77.2	96.5	115.9	135.2	154.5	173.8	+	+
	32	37.1	44.5	49.3	59.4	74.2	89.1	103.9	118.8	133.6	148.4	+

COLOR CODING
<48kHz
48kHz to 96kHz
96kHz to 192kHz
>192kHz

+ Max WS rate is greater than 192kHz.

**DRS = 0 RXCLKIN_ frequency is equal to 2x the DRS = 1 RXCLKIN_ frequency.*

Audio Channel Input

The audio channel input works with 8-channel TDM and stereo I2S, as well as non-standard formats. The input format is shown in Figure 20.

The period of the WS can be 8 to 256 SCK periods. The WS frame starts with the falling edge and can be low for 1 to 255 SCK periods. SD is one SCK period, sampled on the rising edge. MSB/LSB order, zero padding or any other significance assigned to the serial data does not affect operation of the audio channel. The polarity for WS and SCK edges is programmable.

The following are examples of acceptable input formats:

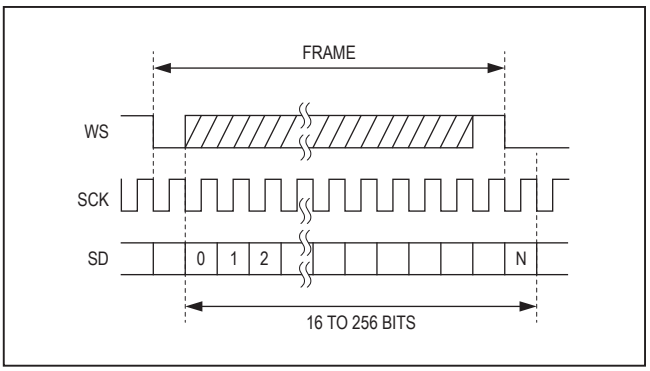


Figure 20. Audio Channel Input Format

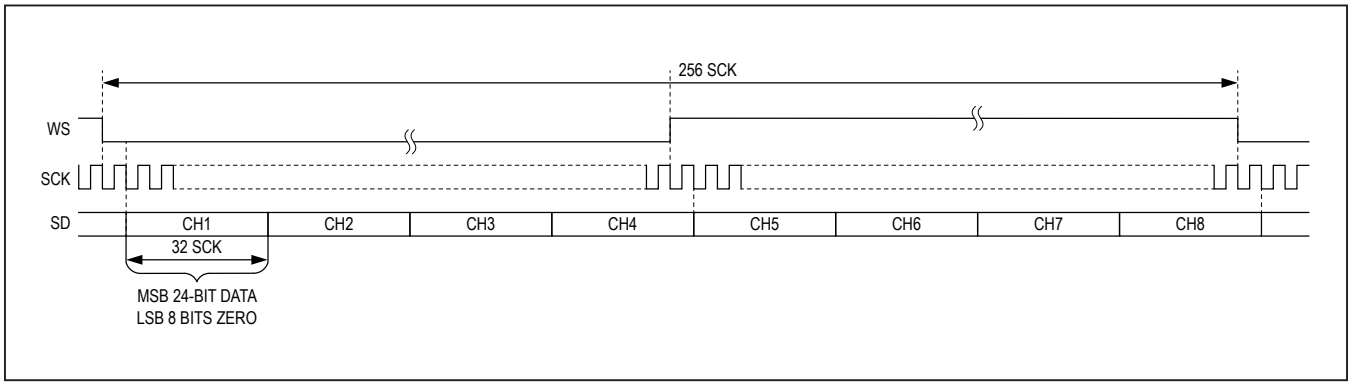


Figure 21. 8-Channel TDM (24-Bit Samples, Padded with Zeros)

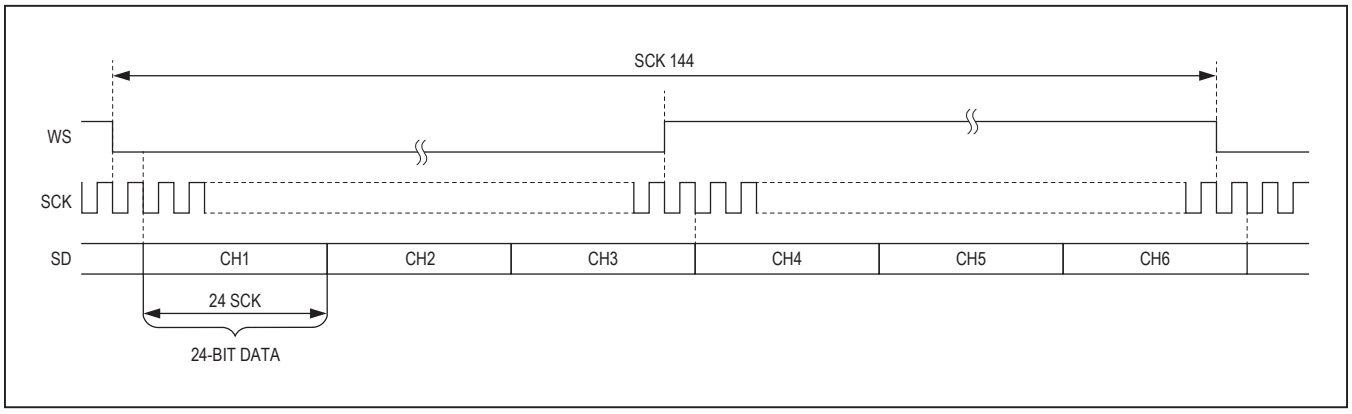


Figure 22. 6-Channel TDM (24-Bit Samples, No Padding)

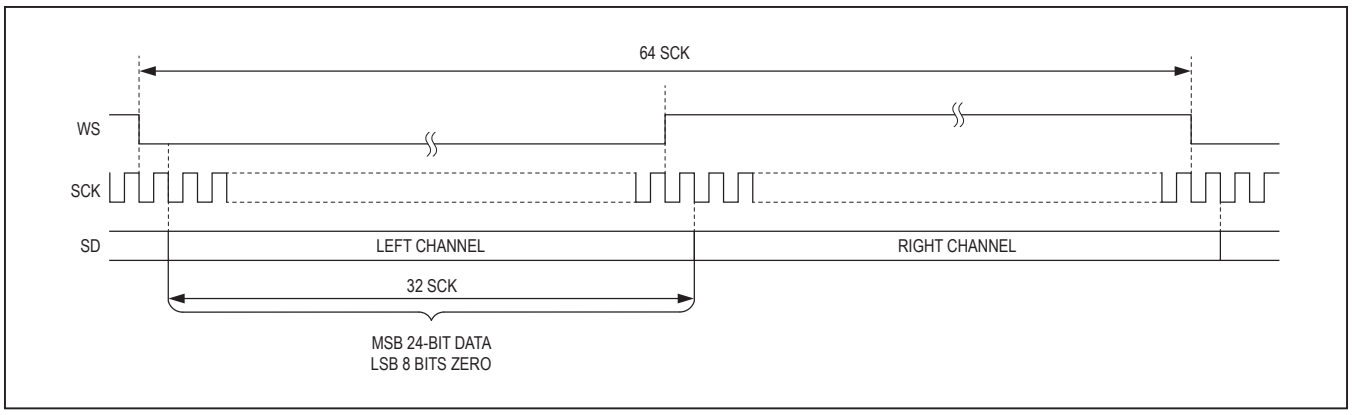


Figure 23. Stereo I²S (24-Bit Samples, Padded with Zeros)

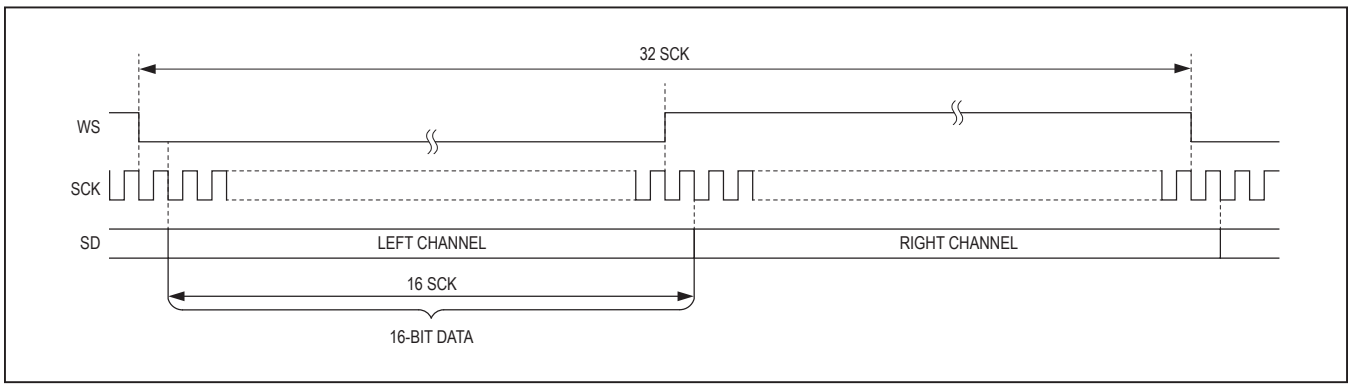


Figure 24. Stereo I²S (16-Bit Samples, No Padding)

Reverse Control Channel

The serializer uses the reverse control channel to receive I²C/UART, MS, and GPO signals from the deserializer in the opposite direction of the video stream. The reverse control channel and forward video data coexist on the same serial cable forming a bidirectional link. The reverse control channel operates independently from the forward control channel. The reverse control channel is available 2ms after power-up. The serializer temporarily disables the reverse control channel for 500µs after starting/stopping the forward serial link.

Control Channel and Register Programming

The control channel is available for the µC to send and receive control data over the serial link simultaneously with the high-speed data. The µC controls the link from either the serializer or the deserializer side to support video-display or image-sensing applications. The control channel between the µC and serializer or deserializer runs in base mode or bypass mode according to the mode selection (MS) input of the device connected to the µC. Base mode is a half-duplex control channel and the bypass mode is a full-duplex control channel. The total maximum forward or reverse control channel delay is 2µs (UART) or 2 bit times (I^2C) from the input of one device to the output of the other. I^2C delay is measured from a START condition to START condition.

UART Interface

In base mode, the µC is the host and can access the registers of both the serializer and deserializer from either side of the link using the GMSL UART protocol. The µC can also program the peripherals on the remote side by sending the UART packets to the serializer or deserializer, with the UART packets converted to I^2C by the device on the remote side of the link. The µC communicates with a UART peripheral in base mode (through INTTYPE register settings), using the half-duplex default GMSL UART protocol of the serializer/deserializer. The device addresses of the serializer and deserializer in base mode are programmable.

When the peripheral interface is I^2C, the serializer/deserializer converts UART packets to I^2C that have device addresses different from those of the serializer or deserializer. The converted I^2C bit rate is the same as the original UART bit rate.

The deserializer uses differential line coding to send signals over the reverse channel to the serializer. The bit rate of the control channel is 9.6kbps to 1Mbps in both directions. The serializer and deserializer automatically detect the control-channel bit rate in base mode. Packet bit rate changes can be made in steps of up to 3.5 times higher or lower than the previous bit rate. See *Changing the Clock Frequency* for more information.

Figure 25 shows the UART protocol for writing and reading in base mode between the µC and the serializer/deserializer.

Figure 26 shows the UART data format (even parity is used). Figure 27 and Figure 28 detail the formats of the SYNC byte (0x79) and the ACK byte (0xC3). The µC and the connected slave chip generate the SYNC byte and ACK byte, respectively. Events such as device wake-up and GPI generate transitions on the control channel that can be ignored by the µC. Data written to the serializer registers do not take effect until after the acknowledge byte is sent. This allows the µC to verify that write commands are received without error, even if the result of the write command directly affects the serial link. The slave uses the SYNC byte to synchronize with the host UART's data rate. If the GPI or MS inputs of the deserializer toggle while there is control-channel communication, or if a line fault occurs, the control-channel communication will be corrupted. In the event of a missed or delayed acknowledge (~1ms due to control channel timeout), the µC should assume there was an error in the packet transmission or response. In base mode, the µC must keep the UART Tx/Rx lines high no more than 4 bit times between bytes in a packet. Keep the UART Tx/Rx lines high for at least 16 bit-times before starting to send a new packet.

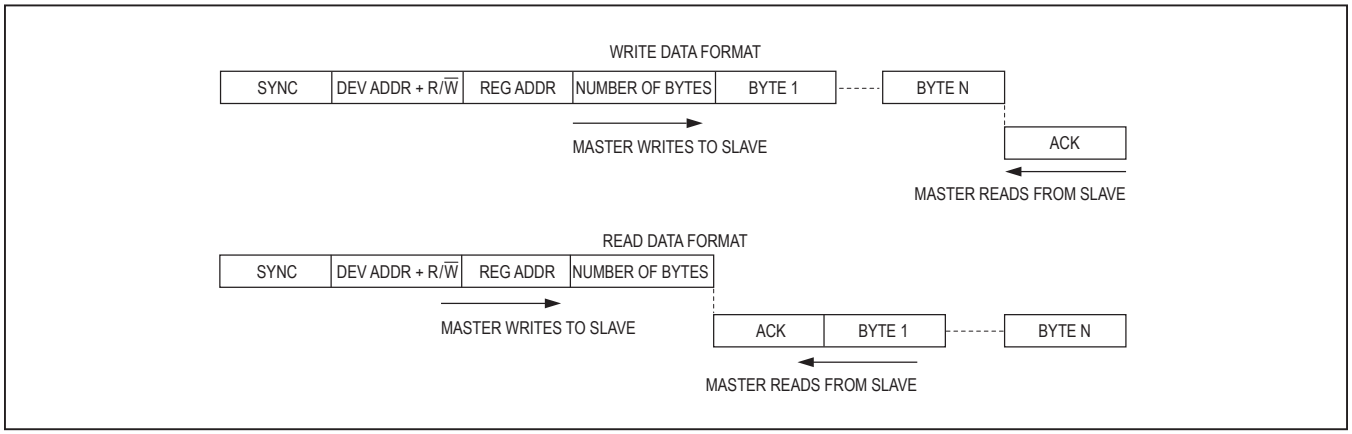


Figure 25. GMSL UART Protocol for Base Mode

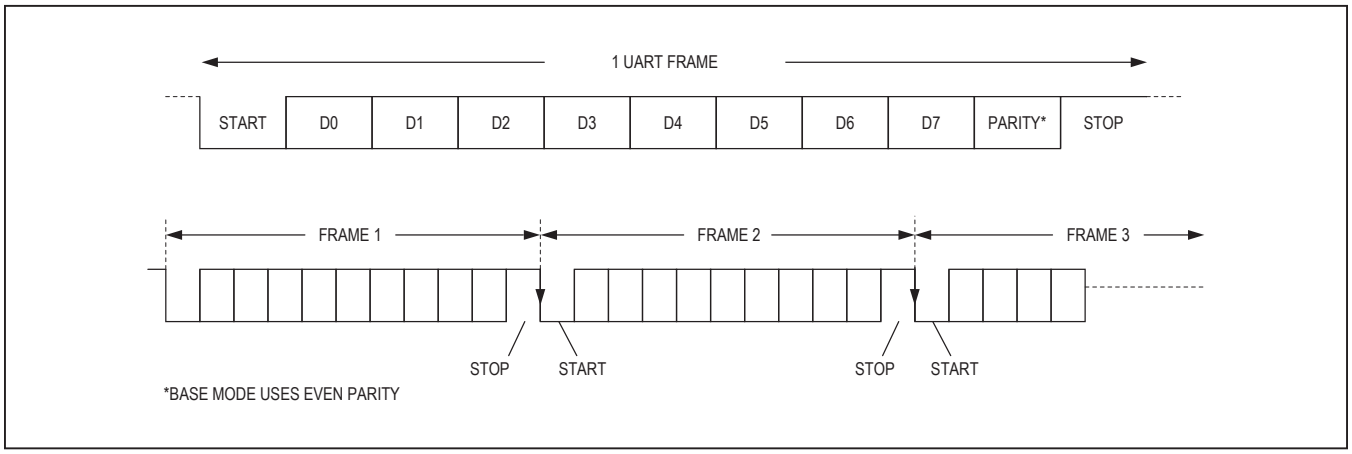


Figure 26. GMSL UART Data Format for Base Mode

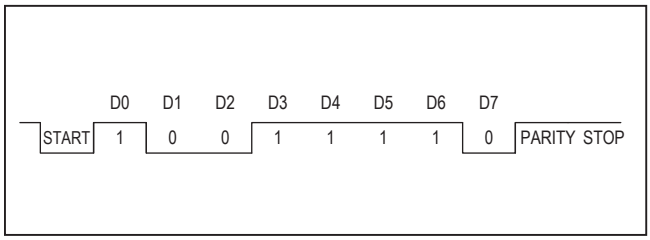


Figure 27. Sync Byte (0x79)

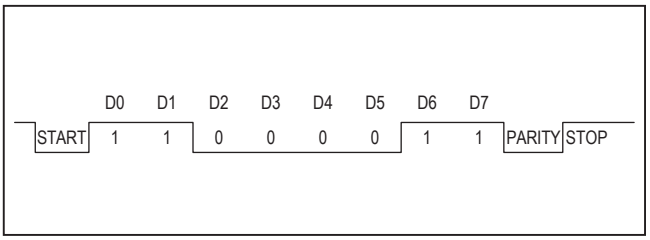


Figure 28. ACK Byte (0xC3)

As shown in Figure 30, the remote-side device converts packets going to or coming from the peripherals from UART format to I²C format and vice versa. The remote device removes the byte number count and adds or receives the ACK between the data bytes of I²C. The I²C bit rate is the same as the UART bit rate.

Interfacing Command-Byte-Only I²C Devices With UART

The serializers' UART-to-I²C conversion can interface with devices that do not require register addresses, such as the MAX7324 GPIO expander. In this mode, the I²C master ignores the register address byte and directly reads/writes the subsequent data bytes (Figure 30). Change the communication method of the I²C master using the I2CMETHOD bit. I2CMETHOD = 1 sets command-byte-only mode, while I2CMETHOD = 0 sets normal mode where the first byte in the data stream is the register address.

UART Bypass Mode

In bypass mode, the serializers ignore UART commands from the µC and the µC communicates with the peripherals directly using its own defined UART protocol. The µC cannot access the serializer/deserializer's registers in this mode. Peripherals accessed through the forward control channel using the UART interface need to handle at least one RXCLKIN_ period ±10ns of jitter due to the asynchronous sampling of the UART signal by RXCLKIN_. Set MS = high in the serializer to put the control channel into bypass mode. For applications with the µC connected to the deserializer, set the MS pin on the deserializer. There is a 1ms wait time between switching MS high and the bypass control channel being active; do not send a UART command during this time. There is no delay time when switching to bypass mode when the µC is connected to the serializer. Although MS on either serializer or deserializer sets the control channel bypass mode, only the local side device (connected to the µC) should be used to set bypass mode. Do not switch MS while a UART command is being sent. Do not send a logic-low value longer than 100µs to ensure proper GPO functionality. Bypass mode accepts bit rates down to 10kbps in either direction. See the *GPO/GPI Control* section for GPI functionality limitations. The control-channel data pattern should not be held low longer than 100µs if GPI control is used.

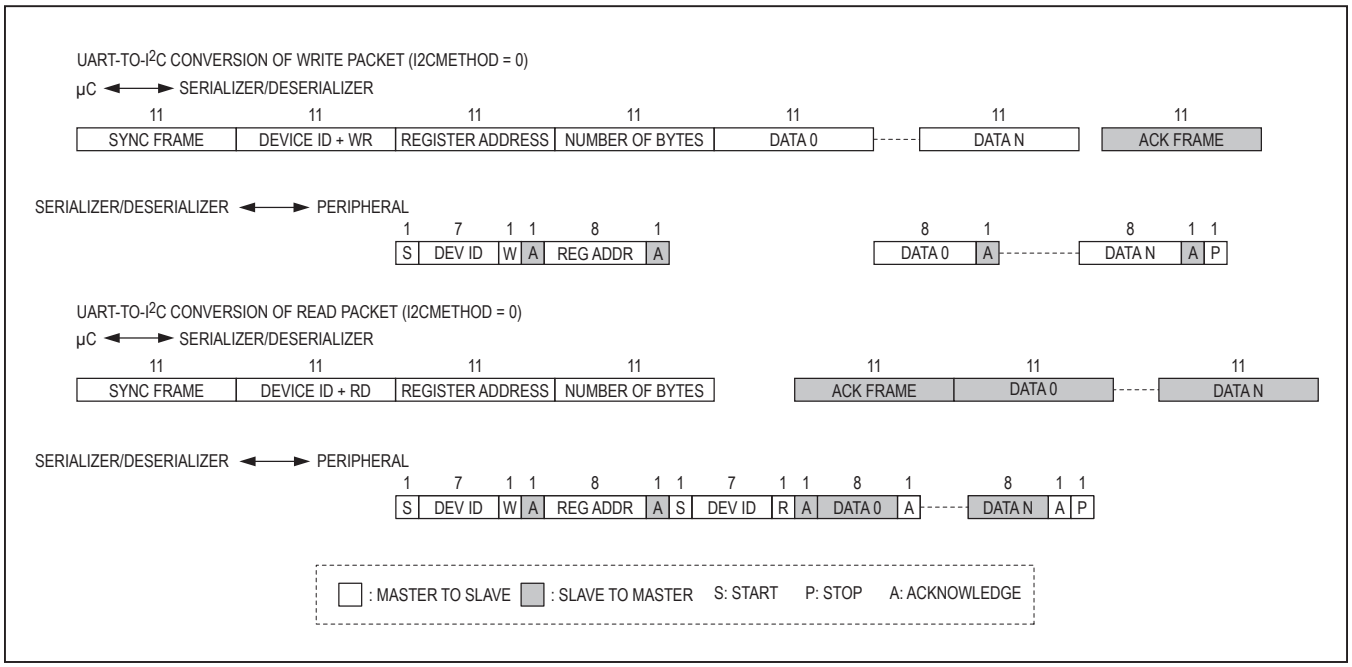


Figure 29. Format Conversion between GMSL UART and I²C with Register Address (I2CMETHOD = 0)

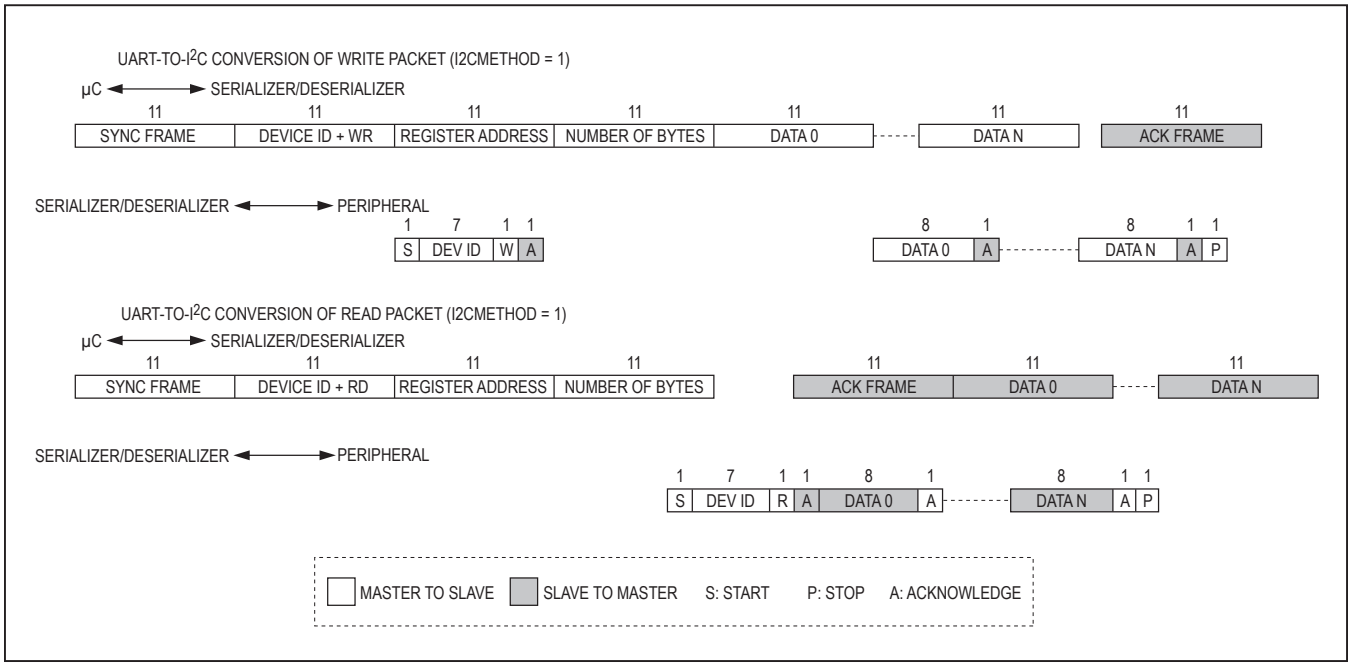


Figure 30. Format Conversion between GMSL UART and I²C without Register Address (I2CMETHOD = 1)

I²C Interface

In I²C to I²C Mode, the serializer's control channel interface sends and receives data through an I²C-compatible 2-wire interface. The interface uses a serial-data line (SDA) and a serial-clock line (SCL) to achieve bidirectional communication between master and slave(s). A µC master initiates all data transfers to and from the device and generates the SCL clock that synchronizes the data transfer. When an I²C transaction starts on the local side device's control channel port, the remote side device's control channel port becomes an I²C master that interfaces with remote side I²C peripherals. The I²C master must accept clock-stretching which is imposed by the serializer (holding SCL low). The SDA and SCL lines operate as both an input and an open-drain output. Pullup resistors are required on SDA and SCL. Each transmission consists of a START condition (Figure 6) sent by a master, followed by the device's 7-bit slave address plus a R/$\overline{W}$ bit, a register address byte, one or more data bytes, and finally a STOP condition.

START and STOP Conditions

Both SCL and SDA remain high when the interface is not busy. A master signals the beginning of a transmission with a START (S) condition by transitioning SDA from high to low while SCL is high (see Figure 31). When the master has finished communicating with the slave, it issues a STOP (P) condition by transitioning SDA from low to high while SCL is high. The bus is then free for another transmission.

Bit Transfer

One data bit is transferred during each clock pulse (Figure 32). The data on SDA must remain stable while SCL is high.

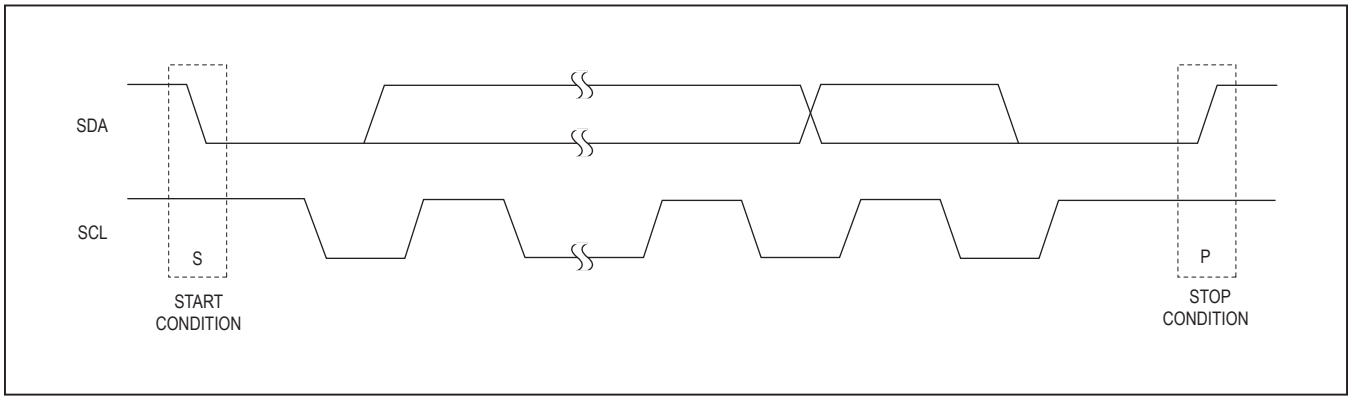


Figure 31. START and STOP Conditions

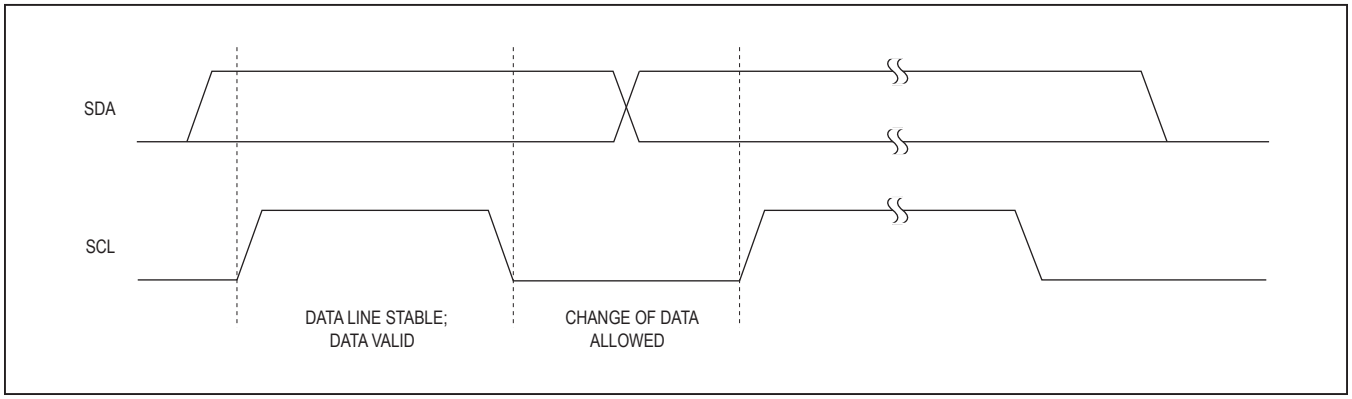


Figure 32. Bit Transfer

Acknowledge

The acknowledge bit is a clocked ninth bit that the recipient uses to handshake receipt of each byte of data (Figure 33). Thus, each byte transferred effectively requires nine bits. The master generates the ninth clock pulse, and the recipient pulls down SDA during the acknowledge clock pulse. The SDA line is stable low during the high period of the clock pulse. When the master is transmitting to the slave device, the slave device generates the acknowledge bit because the slave device is the recipient. When the slave device is transmitting to the master, the master generates the acknowledge bit because the master is the recipient. The device generates an acknowledge even when the forward control channel is not active. To prevent acknowledge generation when the forward control channel is not active, set the I2CLOCACK bit low.

Slave Address

The serializers have 7-bit long slave addresses. The bit following a 7-bit slave address is the R/$\overline{W}$ bit, which is low for a write command and high for a read command. The slave address for the serializer is XX00XX01 for read commands and XX00XX00 for write commands. See Figure 34.

Bus Reset

The device resets the bus with the I2C START condition for reads. When the R/$\overline{W}$ bit is set to 1, the serializers transmit data to the master, thus the master is reading from the device.

Format for Writing

Writes to the serializers comprise the transmission of the slave address with the R/$\overline{W}$ bit set to zero, followed by at least one byte of information. The first byte of information is the register address or command byte. The register address determines which register of the device is to be written by the next byte, if received. If a STOP (P) condition is detected after the register address is received, the device takes no further action beyond storing the register address (Figure 35). Any bytes received after the register address are data bytes. The first data byte goes into the register selected by the register address, and subsequent data bytes go into subsequent registers (Figure 36). If multiple data bytes are transmitted before a STOP condition, these bytes are stored in subsequent registers because the register addresses autoincrements.

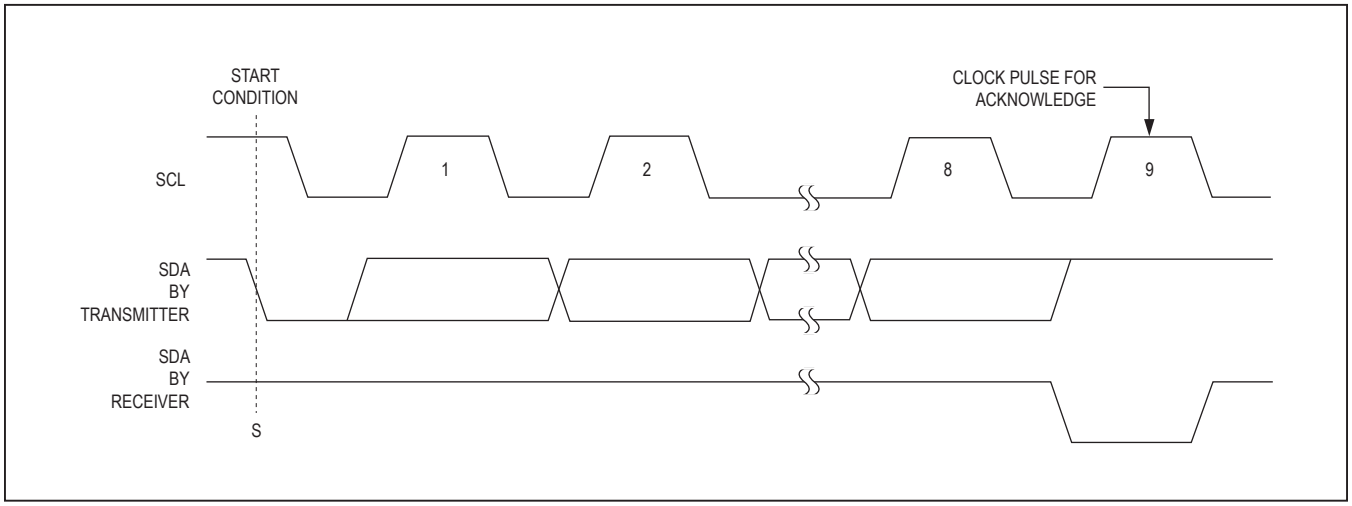


Figure 33. Acknowledge

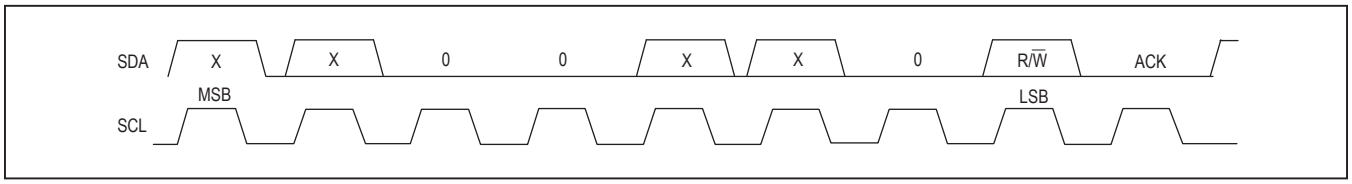


Figure 34. Slave Address

Format for Reading

The serializers are read using the internally stored register address as an address pointer, the same way the stored register address is used as an address pointer for a write. The pointer autoincrements after each data byte is read using the same rules as for a write. Thus, a read is initiated by first configuring the register address by performing a write (Figure 37). The master can now read consecutive bytes from the device, with the first data byte being read from the register address pointed by the previously written register address. Once the master sends a NACK, the device stops sending valid data.

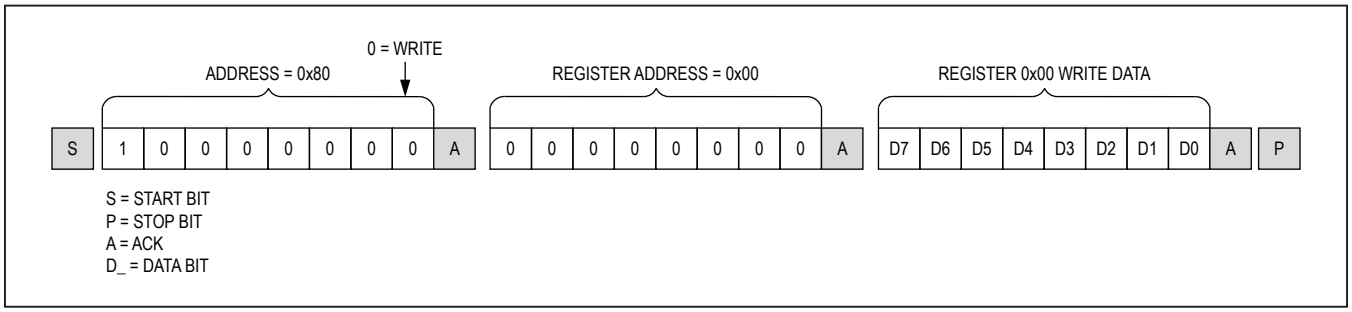


Figure 35. Format for I²C Write

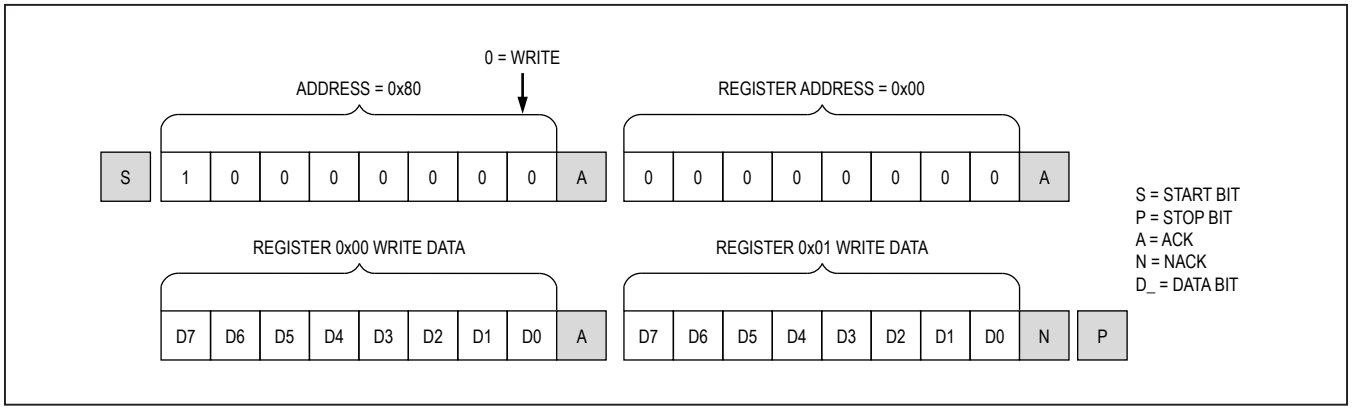


Figure 36. Format for Write to Multiple Registers

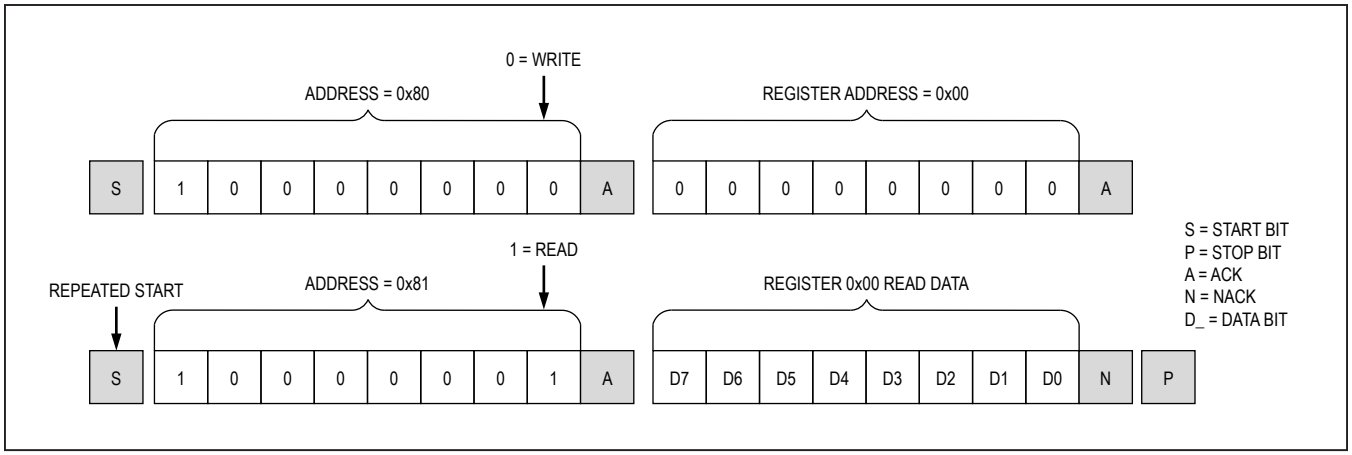


Figure 37. Format for I²C Read

I²C Communication with Remote Side Devices

The serializers support I²C communication with a peripheral on the remote side of the communication link using SCL clock stretching. While multiple masters can reside on either side of the communication link, arbitration is not provided. The connected masters need to support SCL clock stretching. The remote side I²C bit-rate range must be set according to the local side I²C bit rate. Supported remote side bit rates can be found in Table 5. Set the I2CMSTBT (register 0x13) to set the remote I²C bit rate. If using a bit rate different from 400kbps, local and remote side I²C setup and hold times should be adjusted by setting the I2CSLVSH register settings on both sides.

I²C Address Translation

The serializers support I²C address translation for up to two device addresses. Use address translation to assign unique device addresses to peripherals with limited I²C addresses. Source addresses (address to translate from) are stored in registers 0x0F and 0x11. Destination addresses (address to translate to) are stored in registers 0x10 and 0x12.

In a multilink situation, these devices support broadcast commands to control these multiple devices. Select an unused device address to use as a broadcast device address. Program all the remote side devices to translate the broadcast device address (source address stored in registers 0x0F, 0x11) to the peripherals' address (destination address stored in registers 0x10, 0x12). Any commands sent to the broadcast address (selected unused address) will be sent to all devices whose addresses match the translated broadcast address.

GPO/GPI Control

GPO on the serializer follows GPI transitions on the deserializer. This GPO/GPI function can be used to transmit signals such as a frame sync in a surround-view camera system. The GPI to GPO delay is 0.35ms (max). Keep time between GPI transitions to a minimum 0.35ms. This includes transitions from the other deserializer in coax splitter mode. Bit D4 of register 0x06 in the deserializer stores the GPI input state. GPO is low after power-up. The µC can set GPO by writing to the SETGPO register bit. Do not send a logic-low value on the deserializer RX/SDA input (UART mode) longer than 100µs in either base or bypass mode to ensure proper GPO/GPI functionality. GPO/GPI commands will override and corrupt an I²C/UART command in progress.

Pre/Deemphasis Driver

The serial line driver employs current-mode logic (CML) signaling. The driver is differential when programmed for twisted-pair. When programmed for coax, one side of the CML driver is used. The line driver has programmable pre/deemphasis which modifies the output to compensate for cable length. There are 13 preemphasis settings as shown in Table 6. Negative preemphasis levels are deemphasis levels in which the preemphasized swing level is the same as normal swing, but the no-transition data is deemphasized. Program the preemphasis levels through register 0x05 D[3:0] of the serializer. This preemphasis function compensates the high frequency loss of the cable and enables reliable transmission over longer link distances. Current drive for both TP and coax modes is programmable. CMLLVL bits (0x05, D[5:4]) program drive current in TP mode. CMLLVLCX bits (0x14,D[7:4]) program drive current in coax mode.

Spread Spectrum

To reduce the EMI generated by the transitions on the serial link, the serializer output is programmable for spread spectrum. If the deserializer paired with the MAX9277/MAX9281 has programmable spread spectrum, do not enable spread for both at the same time or their interaction will cancel benefits. The deserializer will track the serializer spread and will pass the spread to the deserializer output. The programmable spread-spectrum amplitudes are ±0.5%, ±1%, ±1.5%, ±2%, ±3%, and ±4% (Table 7). Some spread-spectrum amplitudes can only be used at lower RXCLKIN frequencies (Table 8). There is no RXCLKIN frequency limit for the ±0.5% spread rate.

Table 5. I²C Bit-Rate Ranges

LOCAL BIT RATE	REMOTE BIT-RATE RANGE	I2CMSTBT SETTING
f > 50kbps	Up to 1Mbps	Any
20kbps > f > 50kbps	Up to 400kbps	Up to 110
f < 20kbps	Up to 10kbps	000

Table 6. TP/COAX Drive Current (400mV Output Drive Levels)

PREEMPHASIS LEVEL (dB)*	PREEMP SETTING (0x06, D[3:0])	I_{CML} (mA)	I_{PRE} (mA)	SINGLE-ENDED VOLTAGE SWING	
				MAX (mV)	MIN (mV)
-6.0	0100	12	4	400	200
-4.1	0011	13	3	400	250
-2.5	0010	14	2	400	300
-1.2	0001	15	1	400	350
0	0000	16	0	400	400
1.1	1000	16	1	425	375
2.2	1001	16	2	450	350
3.3	1010	16	3	475	325
4.4	1011	16	4	500	300
6.0	1100	15	5	500	250
8.0	1101	14	6	500	200
10.5	1110	13	7	500	150
14.0	1111	12	8	500	100

**Negative preemphasis levels denote deemphasis.*

Table 7. Serial Output Spread

SS	SPREAD (%)
000	No spread spectrum. Power-up default depends on CONF[1:0].
001	±0.5% spread spectrum. Power-up default depends on CONF[1:0].
010	±1.5% spread spectrum
011	±2% spread spectrum
100	No spread spectrum
101	±1% spread spectrum
110	±3% spread spectrum
111	±4% spread spectrum

Table 8. Spread Limitations

3-CHANNEL OR HIGH-BANDWIDTH MODE RXCLKIN FREQUENCY (MHz)	4-CHANNEL MODE RXCLKIN FREQUENCY (MHz)	SERIAL LINK BIT-RATE (Mbps)	AVAILABLE SPREAD RATES
< 33.3	< 25	< 1000	All rates available
33.3 to < 66.7	25 to < 50	1000 to < 2000	1.5%, 1.0%, 0.5%
66.7+	50+	2000+	0.5%

When the spread spectrum is turned on or off the serial link stops for several microseconds and then restarts in order for the deserializer to lose and re-lock to the new serial data stream.

The serializer includes a sawtooth divider to control the spread modulation rate. Auto detection of the RXCLKIN_ operation range guarantees a spread-spectrum modulation frequency within 20kHz to 40kHz. Additionally, manual configuration of the sawtooth divider (SDIV: 0x03, D[6:0]) allows the user to set a modulation frequency according to the RXCLKIN_ frequency. When ranges are manually selected, program the SDIV value for a fixed modulation frequency around 20kHz.

Manual Programming of the Spread-Spectrum Divider

The modulation rate relates to the RXCLKIN_ frequency as follows:

$$f_M = (1 + DRS)\ f_{RXCLKIN\_}/(MOD \times SDIV)$$

where:

f_M = Modulation frequency

DRS = DRS value (0 or 1)

$f_{RXCLKIN\_}$ = RXCLKIN_ frequency

MOD = Modulation coefficient given in Table 9

SDIV = 6-bit SDIV setting, manually programmed by the µC

To program the SDIV setting, first look up the modulation coefficient according to the desired bus-width and spread-spectrum settings. Solve the above equation for SDIV using the desired pixel clock and modulation frequencies. If the calculated SDIV value is larger than the maximum allowed SDIV value in Table 9, set SDIV to the maximum value.

Serial Output

The driver output is programmable for two kinds of cable: 100Ω twisted pair and 50Ω coax. (Contact the factory for devices compatible with 75Ω cables).

Coax Splitter Mode

In coax mode OUT+ and OUT- of the serializer are active. This enables the use as a 1:2 splitter (Figure 38). In coax mode, connect OUT+ to IN+ of the deserializer. Connect OUT- to IN- of the second deserializer. Control channel data is broadcast from the serializer to both deserializers and their attached peripherals. Assign a unique address to send control data to one deserializer. Leave all unused IN_ pins unconnected, or connect them to ground through 50Ω and a capacitor for increased power supply rejection.

If OUT- is not used, connect OUT- to V_{DD} through a 50Ω resistor (Figure 39). When there are µCs at the serializer, and at each deserializer, only one µC can communicate at a time. Disable forward and reverse channel links according to the communicating deserializer connection to prevent contention in I^2C to I^2C mode and UART to I^2C mode. Use ENREVP or ENREVN register bits to disable/enable the control channel link. In UART mode, the serializer provides arbitration of the control channel link.

Configuration Inputs

Several configuration inputs determine the power-up values of the serializer. CONF[1:0] set the control channel mode (I2CSEL), data rate select (DRS), and spread spectrum enable (SSEN) (Table 10). DRS and spread spectrum can be changed after power-up by writing to the appropriate register bits.

High-Immunity Reverse Control Channel Mode

The serializer contains a high-immunity reverse control channel mode, which has increased robustness at half the bit rate over the standard GMSL reverse control channel link (Table 11). Set GPO/HIM on the serializer, and on the deserializer to use high-immunity mode at power-up. Set the HIGHIMM bit high in both the serializer and deserializer to enable high-immunity mode at any time after power-up. Set the HIGHIMM bit low in both the serializer and deserializer to use the legacy reverse control channel mode.

Table 9. Modulation Coefficients and Maximum SDIV Settings

BIT WIDTH MODE	SPREAD SPECTRUM SETTING (%)	MODULATION COEFFICIENT MOD (dec)	SDIV UPPER LIMIT (dec)
4-channel mode	1	104	40
	0.5	104	63
	3	152	27
	1.5	152	54
	4	204	15
	2	204	30
3-channel or high-bandwidth mode	1	80	52
	0.5	80	63
	3	112	37
	1.5	112	63
	4	152	21
	2	152	42

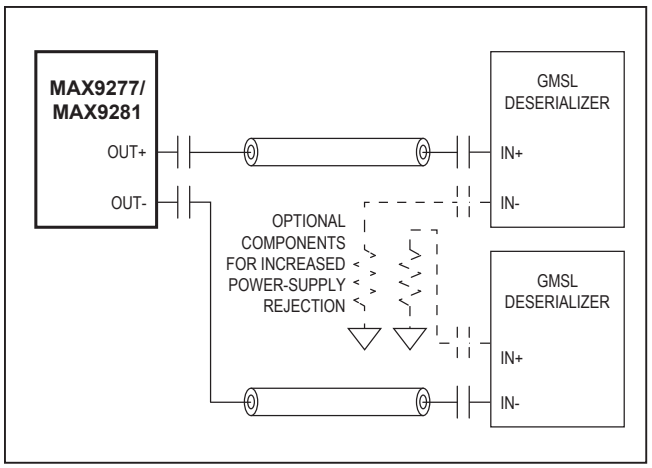


Figure 38. 2:1 Coax Splitter Connection Diagram

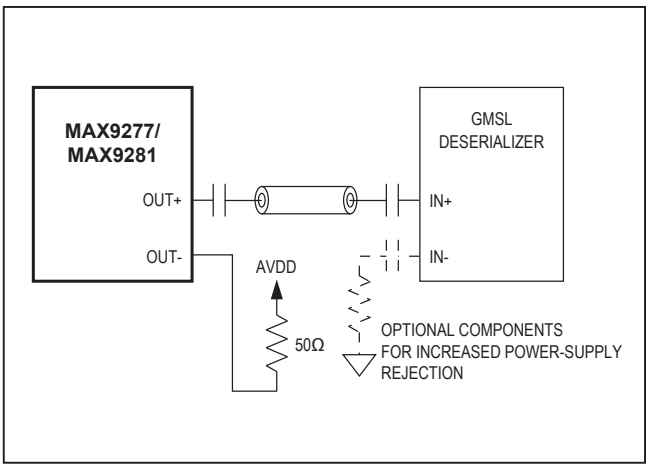


Figure 39. Coax Connection Diagram

Table 10. CONF[1:0] Input Map

CONF1	CONF0	CONTROL CHANNEL MODE (I2CSEL)	SPREAD ENABLE (SSEN)	DATA RATE SELECT (DRS)
Low	Low	UART (0)	Disabled (0)	High rate (0)
Low	High	UART	Disabled	Low rate (1)
High	Low	UART	Enabled (1)	High rate
High	High	UART	Enabled	Low rate
Mid	Low/Mid	I²C (1)	Disabled	High rate
Low	Mid	I²C	Disabled	Low rate
High	Mid	I²C	Enabled	High rate
Mid	High	I²C	Enabled	Low rate

The serializer reverse channel mode is not available for 500µs/1.92ms after the reverse control channel mode is changed through the serializer/deserializer's HIGHIMM bit setting respectively. The user must set GPO/HIM or the HIGHIMM bits to the same value for proper reverse control channel communication.

In high-immunity mode, Set HPFTUNE = 00 in the equalizer, if the serial bit rate = [RXCLKIN_ x 30 (BWS = low or open) or 40 (BWS = high)] is larger than 1Gbps when BWS is low or high. When BWS = open, set HPFTUNE = 00 when the serial bit rate is larger than 2Gbps. In addition, use 47nF AC-coupling capacitors. Note that legacy reverse control channel mode may not function when using 47nF AC-coupling capacitors.

By default, high immunity mode uses a 500kbps bit rate. Set REVFAST =1 (D7 in register 0x1A in the serializer and register 0x11 in the deserializer) in both devices to use a 1Mbps bit rate. Certain limitations apply when using the fast high-immunity mode (Table 12).

Table 11. Reverse Control Channel Modes

HIGHIMM BIT OR GPO/HIM PIN SETTING	REVFAST BIT	REVERSE CONTROL CHANNEL MODE	MAX UART/I²C BIT RATE (kbps)
LOW (1)	X	Legacy reverse control channel mode (compatible with all GMSL devices)	1000
HIGH (1)	0	High-immunity mode	500
	1	Fast high-immunity mode	1000

X = Don't care

Sleep Mode

The serializers have sleep mode to reduce power consumption when powered up. The devices enter or exit sleep mode by a command from a local µC or a remote µC using the control channel. Set the SLEEP bit to 1 to initiate sleep mode. Entering sleep mode resets the HDCP registers, but not the configuration registers. The serializer sleeps immediately after setting its SLEEP = 1. The serial outputs has a wake-up receiver to accept wake-up commands from the attached deserializer. Wake-up from the remote side is not supported in coax splitter mode. Disable the wake-up receiver (through DISRWAKE), if wake-up from remote side is not used in order to reduce sleep mode current. If the wake-up receiver is disabled, the device can only be woken up from the local control channel. See the *Link Startup Procedure* section for details on waking up the device for different µC and starting conditions.

To wake up from the local or remote side, send an arbitrary control channel command to serializer, wait for 5ms for the chip to power up and then write 0 to SLEEP register bit to make the wake-up permanent.

The serializer cannot power up into sleep mode when CDS = 0 (for LCD applications), however after power-up, the device can be put to sleep.

Table 12. Fast High-Immunity Mode Requirements

BWS SETTING	ALLOWED RXCLKIN_ FREQUENCY (MHz)
Low	> 41.66
High	> 30
Open	> 83.33

Fast high-immunity mode requires DRS = 0.

Power-Down Mode

The serializers have a power-down mode which further reduces power consumption compared to Sleep Mode. Set $\overline{\text{PWDN}}$ low to enter power-down mode. In power-down, the serial outputs remain high impedance. Entering power-down resets the device's registers. Upon exiting power-down, the state of external pins CONF[1:0], ADD[2:0], CX/TP, GPO/HIM and BWS are latched.

Configuration Link

The control channel can operate in a low-speed mode called configuration link in the absence of a clock input. This allows a microprocessor to program configuration registers before starting the video link. An internal oscillator provides the clock for the configuration link. Set CLINKEN = 1 on the serializer to enable configuration link. Configuration link is active until the video link is enabled. The video link overrides the configuration link and attempts to lock when SEREN = 1.

Link Startup Procedure

Table 13 lists the startup procedure for display applications (CDS = Low). Table 14 lists the startup procedure for image-sensing applications (CDS = High). The control channel is available after the video link or the configuration link is established. If the deserializer powers up after the serializer, the control channel becomes unavailable for 2ms after power-up.

Table 13. Startup Procedure for Video-Display Applications (CDS = Low)

NO.	µC	SERIALIZER		DESERIALIZER
		(AUTOSTART ENABLED)	(AUTOSTART DISABLED)	
—	µC connected to serializer	Set all configuration inputs. Set $\overline{\text{AUTOS}}$ low. If any configuration inputs are available on one end of the link but not the other, always connects that configuration input low	Set all configuration inputs. Set $\overline{\text{AUTOS}}$ high. If any configuration inputs are available on one end of the link but not the other, always connects that configuration input low	Set all configuration inputs. If any configuration inputs are available on one end of the link but not the other, always connects that configuration input low
1	Powers up	Powers up and loads default settings. Establishes video link when valid RXCLK available	Powers up and loads default settings.	Powers up and loads default settings. Locks to video link signal if available
2	Enables serial link by setting SEREN = 1 or configuration link by setting SEREN = 0 and CLINKEN = 1 (if valid RXCLK not available) and gets an acknowledge. Waits for link to be establish (~3ms)	—	Establishes configuration or video link	Locks to configuration or video link signal
3	Writes configuration bits in the serializer/deserializer and gets an acknowledge.	Configuration changed from default settings		Configuration changed from default settings
4	If not already enabled, sets SEREN = 1, gets an acknowledge and waits for video link to be established (~3ms)	Establishes video link when valid RXCLK available (if not already enabled).		Locks to video link signal (if not already locked)
5	Begin sending video data to input	Video data serialized and sent across serial link.		Video data received and deserialized

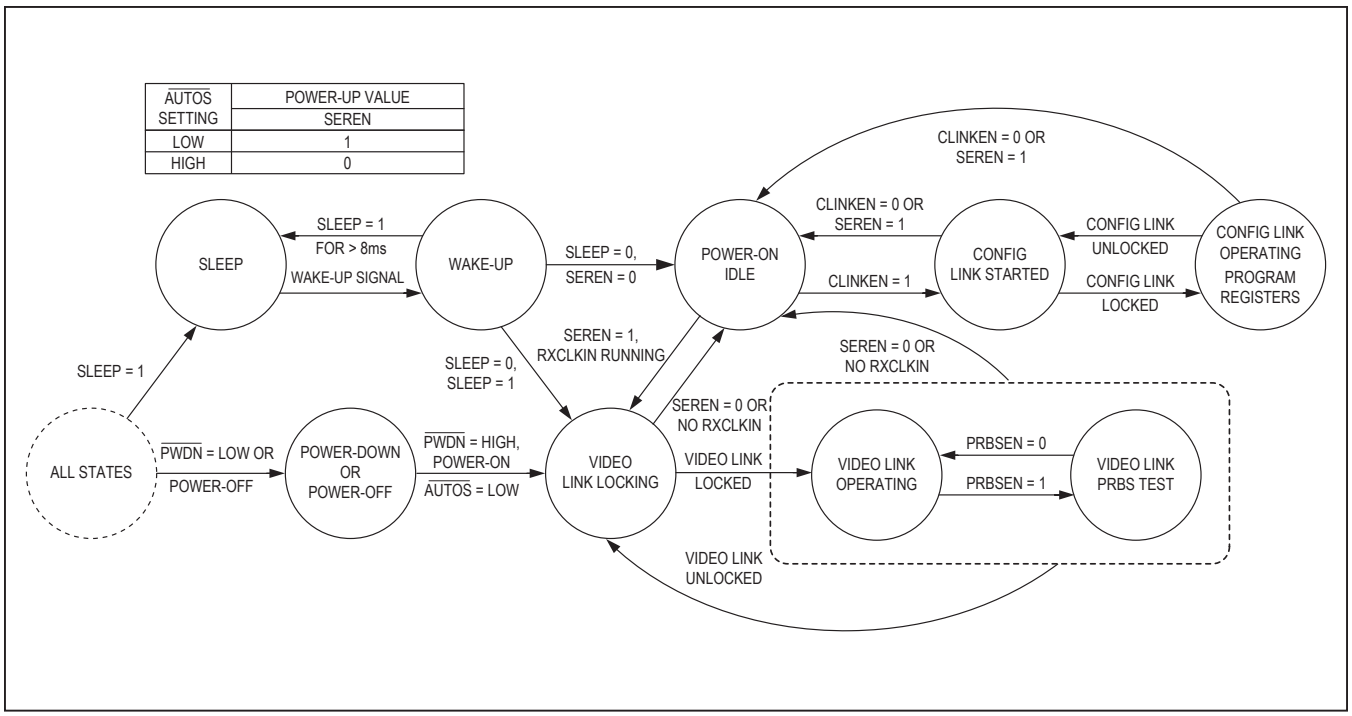


Figure 40. State Diagram, CDS = LOW (Video Display Application)

Table 14. Startup Procedure for Image-Sensing Applications

NO.	µC	SERIALIZER		DESERIALIZER
		(AUTOSTART ENABLED)	(AUTOSTART DISABLED)	
—	µC connected to deserializer	Set all configuration inputs. Set $\overline{AUTOS}$ low.	Set all configuration inputs. Set $\overline{AUTOS}$ high.	Set all configuration inputs.
1	Powers up	Powers up and loads default settings. Establishes video link when valid RXCLK available	Powers up and loads default settings. Goes to sleep after 8ms	Powers up and loads default settings. Locks to video link signal if available
2	Writes deserializer configuration bits and gets an acknowledge.	—	—	Configuration changed from default settings
3	Wakes up the serializer by sending dummy packet, and then writing SLEEP = 0 within 8 ms. May not get an acknowledge (or gets a dummy acknowledge) if not locked.	—	Wakes up	—

Table 14. Startup Procedure for Image-Sensing Applications (continued)

NO.	µC	SERIALIZER		DESERIALIZER
		(AUTOSTART ENABLED)	(AUTOSTART DISABLED)	
4	Writes serializer configuration bits. May not get an acknowledge (or gets a dummy acknowledge) if not locked.	Configuration changed from default settings		—
5	If not already enabled, sets SEREN = 1, gets an acknowledge and waits for serial link to be established (~3ms)	Establishes video link when valid RXCLK available (if not already enabled).		Locks to video link signal (if not already locked)
6	Begin sending video data to input	Video data serialized and sent across serial link.		Video data received and deserialized

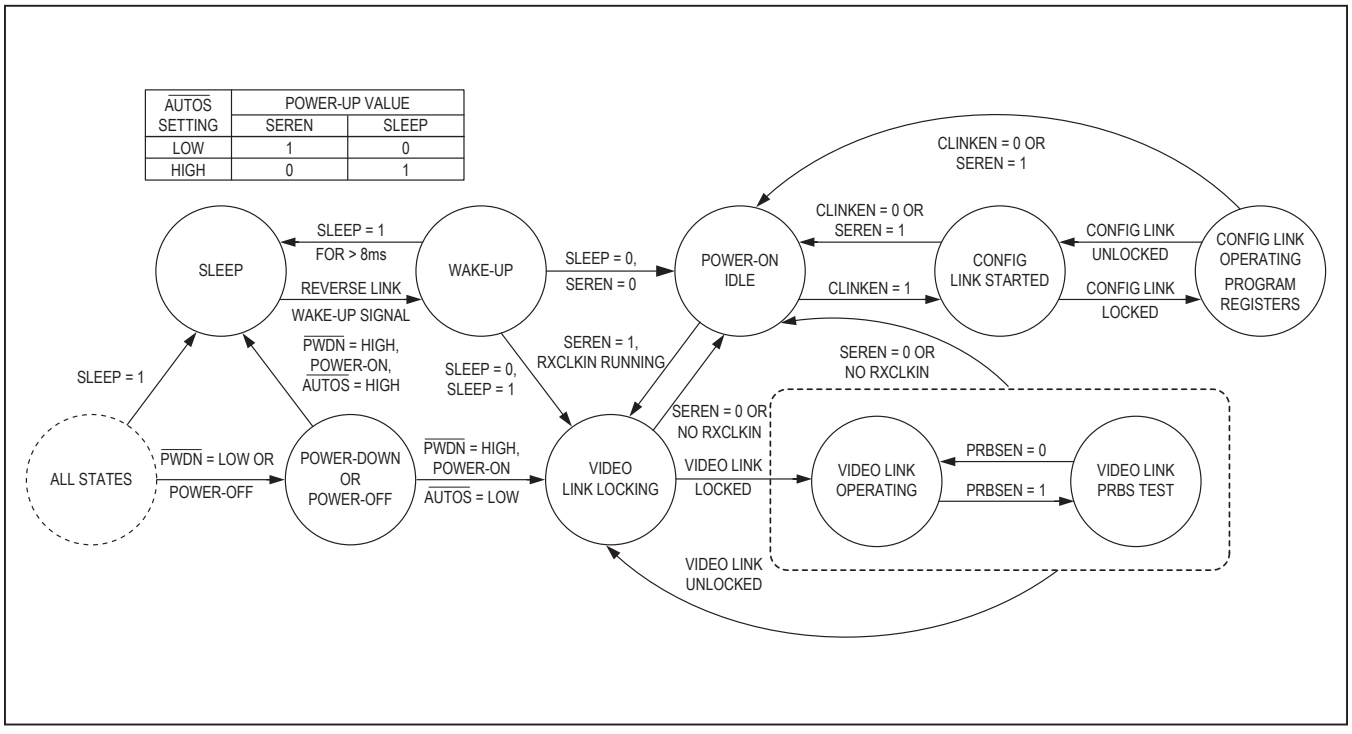


Figure 41. State Diagram, CDS = HIGH (Image Sensing Application)

High-Bandwidth Digital Content Protection (HDCP)

Note: The explanation of HDCP operation in this data sheet is provided as a guide for general understanding. Implementation of HDCP in a product must meet the requirements given in the HDCP System v1.3 Amendment for GMSL, which is available from DCP.

HDCP has two main phases of operation: authentication and the link integrity check. The µC starts authentication by writing to the START_AUTHENTICATION bit in the GMSL serializer. The GMSL serializer generates a 64-bit random number. The host µC first reads the 64-bit random number from the GMSL serializer and writes it to the deserializer. The µC then reads the GMSL serializer public key selection vector (AKSV) and writes it to the deserializer. The µC then reads the deserializer KSV (BKSV) and writes it to the GMSL serializer. The µC begins checking BKSV against the revocation list. Using the cipher, the GMSL serializer and deserializer calculate a 16-bit response value, R0 and R0', respectively. The GMSL amendment for HDCP reduces the 100ms minimum wait time allowed for the receiver to generate R0' (specified in HDCP rev 1.3) to 128 pixel clock cycles in the GMSL amendment.

There are two response-value comparison modes: internal comparison and µC comparison. Set EN_INT_COMP = 1 to select internal comparison mode. Set EN_INT_COMP = 0 to select µC comparison mode. In internal comparison mode, the µC reads the deserializer response R0' and writes it to the GMSL serializer. The GMSL serializer compares R0' to its internally generated response value R0, and sets R0_RI_MATCHED. In µC comparison mode, the µC reads and compares the R0/R0' values from the GMSL serializer/deserializer.

During response-value generation and comparison, the host µC checks for a valid BKSV (having 20 1s and 20 0s is also reported in BKSV_INVALID) and checks BKSV against the revocation list. If BKSV is not on the list and the response values match, the host authenticates the link. If the response values do not match, the µC resamples the response values (as described in HDCP rev 1.3, Appendix C). If resampling fails, the µC restarts authentication by setting the RESET_HDCP bit in the GMSL serializer. If BKSV appears on the revocation list, the host cannot transmit data that requires protection. The host knows when the link is authenticated and decides when to output data requiring protection. The µC performs a link integrity check every 128 frames or every 2s ±0.5s. The GMSL serializer/deserializer generate response values every 128 frames. These values are compared internally (internal comparison mode) or can be compared in the host µC.

In addition, the GMSL serializer/deserializer provide response values for the enhanced link verification. Enhanced link verification is an optional method of link verification for faster detection of loss-of-synchronization. For this option, the GMSL serializer and deserializer generate 8-bit enhanced link-verification response values (PJ and PJ') every 16 frames. The host must detect three consecutive PJ/PJ' mismatches before resampling.

Encryption Enable

The GMSL link transfers either encrypted or nonencrypted data. To encrypt data, the host µC sets the encryption enable (ENCRYPTION_ENABLE) bit in both the GMSL serializer and deserializer. The µC must set ENCRYPTION_ENABLE in the same VSYNC cycle in both the GMSL serializer and deserializer (no internal VSYNC falling edges between the two writes). The same timing applies when clearing ENCRYPTION_ENABLE to disable encryption.

Note: ENCRYPTION_ENABLE enables/disables encryption on the GMSL irrespective of the content. To comply with HDCP, the µC must not allow content requiring encryption to cross the GMSL unencrypted.

The µC must complete the authentication process before enabling encryption. In addition, encryption must be disabled before starting a new authentication session.

Synchronization of Encryption

The video vertical sync (VSYNC) synchronizes the start of encryption. Once encryption has started, the GMSL generates a new encryption key for each frame and each line, with the internal falling edge of VSYNC and HSYNC. Rekeying is transparent to data and does not disrupt the encryption of video or audio data.

Repeater Support

The GMSL serializer/deserializer include features to build an HDCP repeater. An HDCP repeater receives and decrypts HDCP content and then encrypts and transmits on one or more downstream links. A repeater can also use decrypted HDCP content (e.g., to display on a screen). To support HDCP repeater-authentication protocol, the deserializer has a REPEATER register bit. This register bit must be set to 1 by a µC (most likely on the repeater module). Both the GMSL serializer and deserializer use SHA-1 hash-value calculation over the assembled KSV lists. HDCP GMSL links support a maximum of 15 receivers (total number including the ones in repeater modules). If the total number of downstream receivers exceeds 14, the µC must set the MAX_DEVS_EXCEEDED register bit when it assembles the KSV list.

HDCP Authentication Procedures

The GMSL serializer generates a 64-bit random number exceeding the HDCP requirement. The GMSL serializer/deserializer internal one-time programmable (OTP) memories contain a unique HDCP keyset programmed at the factory. The host µC initiates and controls the HDCP authentication procedure. The GMSL serializer and deserializer generate HDCP authentication response values for the verification of authentication. Use the following procedures to authenticate the HDCP GMSL encryption (refer to the HDCP 1.3 Amendment for GMSL for details).

The µC must perform link integrity checks while encryption is enabled (see Table 16). Any event that indicates that the deserializer has lost link synchronization should retrigger authentication. The µC must first write 1 to the RESET_HDCP bit in the GMSL serializer before starting a new authentication attempt.

HDCP Protocol Summary

Table 15, Table 16, and Table 17 list the summaries of the HDCP protocol. These tables serve as an implementation guide only. Meet the requirements in the GMSL amendment for HDCP to be in full compliance.

Table 15. Startup, HDCP Authentication, and Normal Operation (Deserializer is not a Repeater)—First Part of the HDCP Authentication Protocol

NO.	µC	HDCP GMSL SERIALIZER	HDCP GMSL DESERIALIZER
1	Initial state after power-up.	Powers up waiting for HDCP authentication.	Powers up waiting for HDCP authentication.
2	Makes sure that A/V data not requiring protection (low-value content) is available at the GMSL serializer inputs (such as blue or informative screen). Alternatively, uses the FORCE_VIDEO and FORCE_AUDIO bits of the GMSL serializer to mask A/V data at the input of the GMSL serializer. Starts the link by writing SEREN = H or link starts automatically if $\overline{\text{AUTOS}}$ is low.	—	—
3	—	Starts serialization and transmits low-value content A/V data.	Locks to incoming data stream and outputs low-value content A/V data.
4	Reads the locked bit of the deserializer and makes sure the link is established.	—	—
5	Optionally writes a random-number seed to the GMSL serializer.	Combines seed with internally generated random number. If no seed provided, only internal random number is used.	—
6	If HDCP encryption is required, starts authentication by writing 1 to the START_AUTHENTICATION bit of the GMSL serializer.	Generates (stores) AN, and resets the START_AUTHENTICATION bit to 0.	—
7	Reads AN and AKSV from the GMSL serializer and writes to the deserializer.	—	Generates R0' triggered by the µC's write of AKSV.
8	Reads the BKSV and REPEATER bit from the deserializer and writes to the GMSL serializer.	Generates R0, triggered by the µC's write of BKSV.	—

Table 15. Startup, HDCP Authentication, and Normal Operation (Deserializer is not a Repeater)—First Part of the HDCP Authentication Protocol (continued)

NO.	µC	HDCP GMSL SERIALIZER	HDCP GMSL DESERIALIZER
9	Reads the INVALID_BKSV bit of the GMSL serializer and continues with authentication if it is 0. Authentication can be restarted if it fails (set RESET_HDCP = 1 before restarting authentication).	—	—
10	Reads R0' from the deserializer and reads R0 from the GMSL serializer. If they match, continues with authentication; otherwise, retries up to two more times (optionally, GMSL serializer comparison can be used to detect if R0/R0' match). Authentication can be restarted if it fails (set RESET_HDCP = 1 before restarting authentication).	—	—
11	Waits for the VSYNC falling edge (internal to the GMSL serializer) and then sets the ENCRYPTION_ENABLE bit to 1 in the deserializer and GMSL serializer (if the µC is not able to monitor VSYNC, it can utilize the VSYNC_DET bit in the GMSL serializer).	Encryption enabled after the next VSYNC falling edge.	Decryption enabled after the next VSYNC falling edge.
12	Checks that BKSV is not in the Key Revocation list and continues if it is not. Authentication can be restarted if it fails. **Note:** Revocation list check can start after BKSV is read in step 8.	—	—
13	Starts transmission of A/V content that needs protection.	Performs HDCP encryption on high-value content A/V data.	Performs HDCP decryption on high-value content A/V data.

Table 16. Link Integrity Check (Normal)—Performed Every 128 Frames After Encryption is Enabled

NO.	µC	HDCP GMSL SERIALIZER	HDCP GMSL DESERIALIZER
1	—	Generates Ri and updates the RI register every 128 VSYNC cycles.	Generates Ri' and updates the RI' register every 128 VSYNC cycles.
2	—	Continues to encrypt and transmit A/V data.	Continues to receive, decrypt, and output A/V data.
3	Every 128 video frames (VSYNC cycles) or every 2s.	—	—
4	Reads RI from the GMSL serializer.	—	—
5	Reads RI' from the deserializer.	—	—
6	Reads RI again from the GMSL serializer and makes sure it is stable (matches the previous RI that it has read from the GMSL serializer). If RI is not stable, go back to step 5.	—	—
7	If RI matches RI', the link integrity check is successful; go back to step 3.	—	—
8	If RI does not match RI', the link integrity check fails. After the detection of failure of link integrity check, the µC makes sure that A/V data not requiring protection (low-value content) is available at the GMSL serializer inputs (such as blue or informative screen). Alternatively, the FORCE_VIDEO and FORCE_AUDIO bits of the GMSL serializer can be used to mask A/V data input of the GMSL serializer.	—	—
9	Writes 0 to the ENCRYPTION_ENABLE bit of the GMSL serializer and deserializer.	Disables encryption and transmits low-value content A/V data.	Disables decryption and outputs low-value content A/V data.
10	Restarts authentication by writing 1 to the RESET_HDCP bit followed by writing 1 to the START_AUTHENTICATION bit in the GMSL serializer.	—	—

Table 17. Optional Enhanced Link Integrity Check—Performed Every 16 Frames After Encryption is Enabled

NO.	µC	HDCP GMSL SERIALIZER	HDCP GMSL DESERIALIZER
1	—	Generates Pj and updates the PJ register every 16 VSYNC cycles.	Generates Pj' and updates the PJ' register every 16 VSYNC cycles.
2	—	Continues to encrypt and transmit A/V data.	Continues to receive, decrypt, and output A/V data.
3	Every 16 video frames, reads PJ from the GMSL serializer and PJ' from the deserializer.	—	—
4	If PJ matches PJ', the enhanced link integrity check is successful; go back to step 3.	—	—
5	If there is a mismatch, retry up to two more times from step 3. Enhanced link integrity check fails after 3 mismatches. After the detection of failure of enhanced link integrity check, the µC makes sure that A/V data not requiring protection (low-value content) is available at the GMSL serializer inputs (such as blue or informative screen). Alternatively, the FORCE_VIDEO and FORCE_AUDIO bits of the GMSL serializer can be used to mask A/V data input of the GMSL serializer.	—	—
6	Writes 0 to the ENCRYPTION_ENABLE bit of the GMSL serializer and deserializer.	Disables encryption and transmits low-value content A/V data.	Disables decryption and outputs low-value content A/V data.
7	Restarts authentication by writing 1 to the RESET_HDCP bit followed by writing 1 to the START_AUTHENTICATION bit in the GMSL serializer.	—	—

Example Repeater Network—Two µCs

The example shown in Figure 42 has **one repeater and two µCs**. Table 18 summarizes the authentication operation.

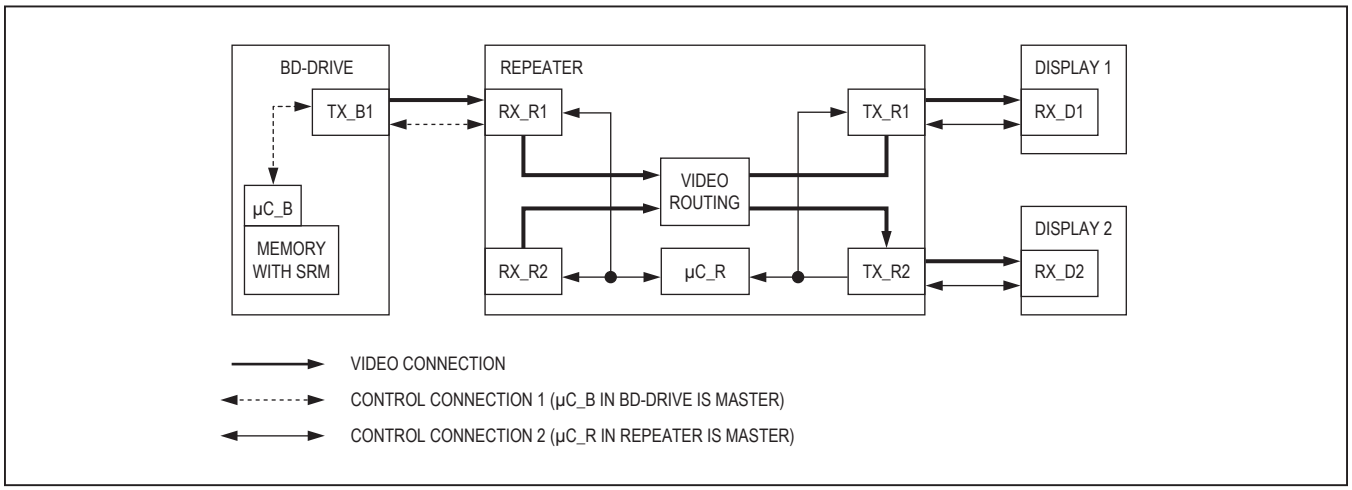


Figure 42. Example Network with One Repeater and Two µCs (Tx = GMSL Serializers, Rx = Deserializers)

Table 18. HDCP Authentication and Normal Operation (One Repeater, Two µCs)—First and Second Parts of the HDCP Authentication Protocol

NO.	µC_B	µC_R	HDCP GMSL SERIALIZER (TX_B1, TX_R1, TX_R2)	HDCP GMSL DESERIALIZER (RX_R1, RX_D1, RX_D2)
			TX_B1 CDS = 0 TX_R1 CDS = 0 TX_R2 CDS = 0	**RX_R1 CDS = 1 RX_D1 CDS = 0 RX_D2 CDS = 0**
1	Initial state after power-up.	Initial state after power-up.	All: Power-up waiting for HDCP authentication.	All: Power-up waiting for HDCP authentication.
2	—	Writes REPEATER = 1 in RX_R1. Retries until proper acknowledge frame received. **Note:** This step must be completed before the first part of authentication is started between TX_B1 and RX_R1 by the µC_B (step 7). For example, to satisfy this requirement, RX_R1 can be held at power-down until µC_R is ready to write the REPEATER bit, or µC_B can poll µC_R before starting authentication.	—	—

Table 18. HDCP Authentication and Normal Operation (One Repeater, Two µCs)—First and Second Parts of the HDCP Authentication Protocol (continued)

NO.	µC_B	µC_R	HDCP GMSL SERIALIZER (TX_B1, TX_R1, TX_R2)	HDCP GMSL DESERIALIZER (RX_R1, RX_D1, RX_D2)
			TX_B1 CDS = 0 TX_R1 CDS = 0 TX_R2 CDS = 0	**RX_R1 CDS = 1 RX_D1 CDS = 0 RX_D2 CDS = 0**
3	Makes sure that A/V data not requiring protection (low-value content) is available at the TX_B1 inputs (such as blue or informative screen). Alternatively, the FORCE_VIDEO and FORCE_AUDIO bits of TX_B1 can be used to mask A/V data input of TX_B1. Starts the link between TX_B1 and RX_R1 by writing SEREN = H to TX_B1, or link starts automatically if $\overline{\text{AUTOS}}$ is low.	—	TX_B1: Starts serialization and transmits low-value content A/V data.	RX_R1: Locks to incoming data stream and outputs low-value content A/V data.
4	—	Starts all downstream links by writing SEREN = H to TX_R1, TX_R2, or links start automatically if $\overline{\text{AUTOS}}$ of transmitters are low.	TX_R1, TX_R2: Starts serialization and transmits low-value content A/V data.	RX_D1, RX_D2: Locks to incoming data stream and outputs low-value content A/V data.
5	Reads the locked bit of RX_R1 and makes sure the link between TX_B1 and RX_R1 is established.	Reads the locked bit of RX_D1 and makes sure the link between TX_R1 and RX_D1 is established. Reads the locked bit of RX_D2 and makes sure the link between TX_R2 and RX_D2 is established.	—	—
6	Optionally, writes a random number seed to TX_B1.	Writes 1 to the GPIO_0_FUNCTION and GPIO_1_FUNCTION bits in RX_R1 to change GPIO functionality used for HDCP purpose. Optionally, writes a random-number seed to TX_R1 and TX_R2.	—	—
7	Starts and completes the first part of the authentication protocol between TX_B1, RX_R1 (see steps 6–10 in Table 15).	—	TX_B1: According to commands from µC_B, generates AN, computes R0.	RX_R1: According to commands from µC_B, computes R0'.

Table 18. HDCP Authentication and Normal Operation (One Repeater, Two µCs)—First and Second Parts of the HDCP Authentication Protocol (continued)

NO.	µC_B	µC_R	HDCP GMSL SERIALIZER (TX_B1, TX_R1, TX_R2)	HDCP GMSL DESERIALIZER (RX_R1, RX_D1, RX_D2)
			TX_B1 CDS = 0 TX_R1 CDS = 0 TX_R2 CDS = 0	**RX_R1 CDS = 1 RX_D1 CDS = 0 RX_D2 CDS = 0**
8	—	When GPIO_1 = 1 is detected, starts and completes the first part of the authentication protocol between the (TX_R1, RX_D1) and (TX_R2, RX_D2) links (see steps 6–10 in Table 15).	TX_R1, TX_R2: According to commands from µC_R, generates AN, computes R0.	RX_D1, RX_D2: According to commands from µC_R, computes R0'.
9	Waits for the VSYNC falling edge and then enables encryption on the (TX_B1, RX_R1) link. Full authentication is not complete yet so it makes sure A/V content that needs protection is not transmitted. Since REPEATER = 1 was read from RX_R1, the second part of authentication is required.	—	TX_B1: Encryption enabled after next VSYNC falling edge.	RX_R1: Decryption enabled after next VSYNC falling edge.
10	—	When GPIO_0 = 1 is detected, enables encryption on the (TX_R1, RX_D1) and (TX_R2, RX_D2) links.	TX_R1, TX_R2: Encryption enabled after next VSYNC falling edge.	RX_D1, RX_D2: Decryption enabled after next VSYNC falling edge.
11	Waits for some time to allow µC_R to make the KSV list ready in RX_R1. Then polls (reads) the KSV_LIST_READY bit of RX_R1 regularly until proper acknowledge frame is received and bit is read as 1.	Blocks control channel from µC_B side by setting REVCCEN = FWDCCEN = 0 in RX_R1. Retries until proper acknowledge frame received.	—	RX_R1: Control channel from serializer side (TX_B1) is blocked after FWDCCEN = REVCCEN = 0 is written.
12		Writes BKSVs of RX_D1 and RX_D2 to the KSV list in RX_R1. Then, calculates and writes the BINFO register of RX_R1.	—	RX_R1: Triggered by µC_R's write of BINFO, calculates hash value (V') on the KSV list, BINFO and the secret-value M0'.
13		Writes 1 to the KSV_LIST_READY bit of RX_R1 and then unblocks the control channel from the µC_B side by setting REVCCEN = FWDCCEN = 1 in RX_R1.	—	RX_R1: Control channel from the serializer side (TX_B1) is unblocked after FWDCCEN = REVCCEN = 1 is written.

Table 18. HDCP Authentication and Normal Operation (One Repeater, Two µCs)—First and Second Parts of the HDCP Authentication Protocol (continued)

NO.	µC_B	µC_R	HDCP GMSL SERIALIZER (TX_B1, TX_R1, TX_R2)	HDCP GMSL DESERIALIZER (RX_R1, RX_D1, RX_D2)
			TX_B1 CDS = 0 TX_R1 CDS = 0 TX_R2 CDS = 0	**RX_R1 CDS = 1 RX_D1 CDS = 0 RX_D2 CDS = 0**
14	Reads the KSV list and BINFO from RX_R1 and writes them to TX_B1. If any of the MAX_DEVS_EXCEEDED or MAX_CASCADE_EXCEEDED bits is 1, then authentication fails. **Note:** BINFO must be written after the KSV list.	—	TX_B1: Triggered by µC_B's write of BINFO, calculates hash value (V) on the KSV list, BINFO and the secret-value M0.	—
15	Reads V from TX_B1 and V' from RX_R1. If they match, continues with authentication; otherwise, retries up to two more times.	—	—	—
16	Searches for each KSV in the KSV list and BKSV of RX_R1 in the Key Revocation list.	—	—	—
17	If keys are not revoked, the second part of the authentication protocol is completed.	—	—	—
18	Starts transmission of A/V content that needs protection.	—	All: Perform HDCP encryption on high-value A/V data.	All: Perform HDCP decryption on high-value A/V data.

Detection and Action Upon New Device Connection

When a new device is connected to the system, the device must be authenticated and the device's KSV checked against the revocation list. The downstream µCs can set the NEW_DEV_CONN bit of the upstream receiver and invoke an interrupt to notify upstream µCs.

Notification of Start of Authentication and Enable of Encryption to Downstream Links

HDCP repeaters do not immediately begin authentication upon startup or detection of a new device, but instead wait for an authentication request from the upstream transmitter/repeaters.

Use the following procedure to notify downstream links of the start of a new authentication request:

- Host µC begins authentication with the HDCP repeater's input receiver.
- When AKSV is written to HDCP repeater's input receiver, its AUTH_STARTED bit is automatically set and its GPIO1 goes high (if GPIO1_FUNCTION is set to high).
- HDCP repeater's µC waits for a low-to-high transition on HDCP repeater input receiver's AUTH_STARTED bit and/or GPIO1 (if configured) and starts authentication downstream.
- HDCP repeater's µC resets the AUTH_STARTED bit.

Set GPIO0_FUNCTION to high to have GPIO0 follow the ENCRYPTION_ENABLE bit of the receiver. The repeater µC can use this function for notification when encryption is enabled/disabled by an upstream µC.

Applications Information

Self PRBS Test

The serializers include a PRBS pattern generator which works with bit-error verification in the deserializer. To run the PRBS test, first disable HDCP encryption. Next, set DISHSFILT, DISVSFILT and DISDEFILT to '1', to disable glitch filter in the deserializer. Then, set PRBSEN = 1 (0x04, D5) in the serializer and then in the deserializer. To exit the PRBS test, set PRBSEN = 0 (0x04, D5) in the deserializer and then in the serializer.

Dual µC Control

Usually systems have one microcontroller to run the control channel, located on the serializer side for display applications or on the deserializer side for image-sensing applications. However, a µC can reside on each side simultaneously, and trade off running the control channel. In this case, each µC can communicate with the serializer and deserializer and any peripheral devices.

Contention will occur if both µCs attempt to use the control channel at the same time. It is up to the user to prevent this contention by implementing a higher level protocol. In addition, the control channel does not provide arbitration between I^2C masters on both sides of the link. An acknowledge frame is not generated when communication fails due to contention. If communication across the serial link is not required, the µCs can disable the forward and reverse control channel using the FWDCCEN and REVCCEN bits (0x04, D[1:0]) in the serializer/deserializer. Communication across the serial link is stopped and contention between µCs cannot occur.

As an example of dual µC use in an image-sensing application, the serializer can be in sleep mode and waiting for wake-up by µC on the deserializer side. After wake-up, the serializer-side µC assumes master control of the serializer's registers.

Jitter-Filtering PLL

In some applications, the clock input (RXCLKIN) includes noise, which reduces link reliability. The clock input has a programmable narrowband jitter-filter PLL that attenuates frequencies higher than 100kHz (typical). Enable the jitter-filter by setting DISJITFILT = 0 (0x05, D6).

RXCLKIN Spread Tracking

The serializers can operate with a spread RXCLKIN signal. When using a spread RXCLKIN, disable the jitter-filter by setting DISJITFILT = 1 (0x05, D6) and set X7PLLHIBW =1 (0x0C, D7). Do not exceed 0.5% spread for $f_{RXCLKIN}$ > 50MHz, and 1% spread for $f_{RXCLKIN}$ < 50MHz, and keep modulation less than 40kHz. In addition, turn off spread spectrum in the serializer and deserializer. The serializer and deserializer track the spread on RXCLKIN.

Changing the Clock Frequency

It is recommended that the serial link be enabled after the video clock ($f_{RXCLKIN\_}$) and the control-channel clock ($f_{UART}/f_{\mu C}$) are stable. When changing the clock frequency, stop the video clock for 5µs, apply the clock at the new frequency, then restart the serial link or toggle SEREN. On-the-fly changes in clock frequency are possible if the new frequency is immediately stable and without glitches. The reverse control channel remains unavailable for 500µs after serial link start or stop. When using the UART interface, limit on-the-fly changes in f_{UART} to factors of less than 3.5 at a time to ensure that the device recognizes the UART sync pattern. For example, when lowering the UART frequency from 1Mbps to 100kbps, first send data at 333kbps then at 100kbps for reduction ratios of 3 and 3.333, respectively.

Providing a Frame Sync (Camera Applications)

The GPI/GPO provide a simple solution for camera applications that require a Frame Sync signal from the ECU (e.g. surround view systems). Connect the ECU Frame Sync signal to the GPI input, and connect GPO output to the camera Frame Sync input. GPI/GPO has a typical delay of 275µs. Skew between multiple GPI/GPO channels is typically 115µs. If a lower skew signal is required, connect the camera's frame sync input one of the deserializer's GPIOs and use an I²C broadcast write command to change the GPIO output state. This has a maximum skew of 0.5µs + 1 I²C bit time.

Software Programming of the Device Addresses

The serializers and deserializers have programmable device addresses. This allows multiple GMSL devices, along with I²C peripherals, to coexist on the same control channel. The serializer device address is in register 0x00 of each device, while the deserializer device address is in register 0x01 of each device. To change a device address, first write to the device whose address changes (register 0x00 of the serializer for serializer device address change, or register 0x01 of the deserializer for deserializer device address change). Then write the same address into the corresponding register on the other device (register 0x00 of the deserializer for serializer device address change, or register 0x01 of the serializer for deserializer device address change).

3-Level Configuration Inputs

CONF[1:0], ADD[1:0] and BWS are 3-level inputs that control the serial interface configuration and power-up defaults. Connect 3-level inputs through a pullup resistor to IOVDD to set a high level, a pulldown resistor to GND to set a low level, or open to set a mid level. For digital control, use three-state logic to drive the 3-level logic input.

Configuration Blocking

The serializers can block changes to registers. Set CFGBLOCK to make registers 0x00 to registers 0x1F as read only. Once set, the registers remain blocked until the supplies are removed or until $\overline{PWDN}$ is low.

Compatibility with other GMSL Devices

The serializers are designed to pair with the MAX9276–MAX9282 deserializers but interoperates with any GMSL deserializers. See Table 19 for operating limitations.

Key Memory

Each device has a unique HDCP key set that is stored in secure nonvolatile memory (NVM). The HDCP key set consists of forty 56-bit private keys and one 40-bit public key. The NVM is qualified for automotive applications.

Table 19. MAX9277/MAX9281 Feature Compatibility

MAX9277/MAX9281 FEATURE	GMSL DESERIALIZER
HDCP (MAX9281 only)	If feature not supported in deserializer, must not be turned on in the MAX9281.
High-bandwidth mode	If feature not supported in deserializer, must only use 24-bit and 32-bit modes.
I²C to I²C	If feature not supported in deserializer, must use UART to I²C or UART to UART.
Coax	If feature not supported in deserializer, must connect unused serial input through 200nF and 50Ω in series to V_{DD} and set the reverse control channel amplitude to 100mV.
High-immunity control channel	If feature not supported in deserializer, must use the legacy reverse control channel mode
TDM encoding	If feature not supported in deserializer, must use I²S encoding (with 50% WS duty cycle), if supported.
I²S encoding	If feature not supported in deserializer must disable I²S in the MAX9277/MAX9281.

HS/VS/DE Inversion

The serializer uses an active high HS, VS, and DE for encoding and HDCP encryption. Set INVHSYNC, INVVSYNC, and INVDE in the serializer (registers 0x0D, 0x0E) to invert active low input signals for use with the GMSL devices. Set INVHSYNC, INVVSYNC, and INVDE in the deserializer to output active-low signals for use with downstream devices.

WS/SCK Inversion

The serializer uses standard polarities for I²S. Set INVWS, INVSCK in the serializer (register 0x1B) to invert opposite polarity signals for use with the GMSL devices. Set INVWS, INVSCK in the deserializer (register 0x1D) to output reverse polarity signals for downstream use.

Line-Fault Detection

The line-fault detector in the serializer monitors for line failures such as short to ground, short to battery, and open link for system fault diagnosis. Figure 4 shows the required external resistor connections. $\overline{LFLT}$ = low when a line fault is detected and $\overline{LFLT}$ goes high when the line returns to normal. The line-fault type is stored in 0x08 D[3:0] of the serializer. Filter $\overline{LFLT}$ with the µC to reduce the detector's susceptibility to short ground shifts. The fault detector threshold voltages are referenced to the serializer ground. Additional passive components set the DC level of the cable (Figure 4). If the serializer and GMSL deserializer grounds are different, the link DC voltage during normal operation can vary and cross one of the fault-detection thresholds.

For the fault-detection circuit, select the resistor's power rating to handle a short to the battery. In coax mode, leave the unused line fault inputs unconnected. To detect the short-together case, refer to Application Note 4709: *MAX9259 GMSL Line Fault Detection*.

Table 20 lists the mapping for line-fault types.

Internal Input Pulldowns

The control and configuration inputs (except 3-level inputs) include a pulldown resistor to GND. External pulldown resistors are not needed.

Choosing I²C/UART Pullup Resistors

I²C and UART open-drain lines require a pullup resistor to provide a logic-high level. There are tradeoffs between power dissipation and speed, and a compromise may be required when choosing pullup resistor values. Every device connected to the bus introduces some capacitance even when the device is not in operation. I²C specifies 300ns rise times (30% to 70%) for fast mode, which is defined for data rates up to 400kbps (see the I²C specifications in the *AC Electrical Characteristics* table for details). To meet the fast-mode rise-time requirement, choose the pullup resistors so that rise time t_R = 0.85 x R_{PULLUP} x C_{BUS} < 300ns. The waveforms are not recognized if the transition time becomes too slow. The device supports I²C/UART rates up to 1Mbps.

Table 20. Line Fault Mapping

REGISTER ADDRESS	BITS	NAME	VALUE	LINE FAULT TYPE
0X08	D[3:2]	LFNEG	00	Negative cable wire shorted to supply voltage
			01	Negative cable wire shorted to ground
			10	Normal operation
			11	Negative cable wire disconnected
	D[1:0]	LFPOS	00	Positive cable wire shorted to supply voltage
			01	Positive cable wire shorted to ground
			10	Normal operation
			11	Positive cable wire disconnected

AC-Coupling

AC-coupling isolates the receiver from DC voltages up to the voltage rating of the capacitor. Capacitors at the serializer output and at the deserializer input are needed for proper link operation and to provide protection if either end of the cable is shorted to a battery. AC-coupling blocks low-frequency ground shifts and low-frequency common-mode noise.

Selection of AC-Coupling Capacitors

Voltage droop and the digital sum variation (DSV) of transmitted symbols cause signal transitions to start from different voltage levels. Because the transition time is fixed, starting the signal transition from different voltage levels causes timing jitter. The time constant for an AC-coupled link needs to be chosen to reduce droop and jitter to an acceptable level. The RC network for an AC-coupled link consists of the CML/coax receiver termination resistor (RTR), the CML/coax driver termination resistor (RTD), and the series AC-coupling capacitors (C). The RC time constant for four equal-value series capacitors is (C x (RTD + RTR))/4. RTD and RTR are required to match the transmission line impedance (usually 100Ω differential, 50Ω single ended). This leaves the capacitor selection to change the system time constant. Use at 0.22µF (using legacy reverse control channel), 47nF (using high-immunity reverse control channel), or larger high-frequency surface-mount ceramic capacitors, with sufficient voltage rating to withstand a short to battery, to pass the lower speed reverse control-channel signal. Use capacitors with a case size less than 3.2mm x 1.6mm to have lower parasitic effects to the high-speed signal.

Power-Supply Circuits and Bypassing

The serializers use an AVDD and DVDD of 1.7V to 1.9V and an LVDSVDD of 3.0V to 3.6V. All single-ended inputs and outputs except for the serial output derive power from an IOVDD of 1.7V to 3.6V, which scale with IOVDD. Proper voltage-supply bypassing is essential for high-frequency circuit stability.

Power-Supply Table

Power supply currents shown in the *Electrical Characteristics* table is the sum of the currents from LVDSVDD, AVDD, DVDD, and IOVDD. Typical currents from the individual power supplies are shown in Table 21. HDCP operation (MAX9281 only) draws additional current. This is shown in Table 22.

Table 21. Typical Power-Supply Currents (Using Worst-Case Input Pattern, V_{AVDD} = V_{DVDD} = V_{IOVDD} = 1.8V, $V_{LVDSVDD}$ = 3.3V, T_A = +25°C, SSEN = High, No HDCP)

BWS	RXCLK (MHz)	AVDD (mA)	DVDD (mA)	IOVDD (mA)	LVDSVDD (mA)
Low	16.6	88	11.4	0.029	24
	33.3	90.7	15.6	0.029	24
	66.6	98.3	23.9	0.029	24
	104	112.2	33.2	0.029	24
Open	36.6	91.7	19.7	0.029	29
	104	112.1	38.8	0.030	29

Table 22. Additional Supply Current from HDCP (MAX9281 Only)

RXCLK (MHZ)	MAX HDCP CURRENT (mA)
16.6	25
33.3	30
66.6	45
104	70

Table 23. Suggested Connectors and Cables for GMSL

VENDOR	CONNECTOR	CABLE	TYPE
Rosenberger	59S2AX-400A5-Y	RG174	Coax
Rosenberger	D4S10A-40ML5-Z	Dacar 535-2	STP
Nissei	GT11L-2S	F-2WME AWG28	STP
JAE	MX38-FF	A-BW-Lxxxxx	STP

Cables and Connectors

Interconnect for CML typically has a differential impedance of 100Ω. Use cables and connectors that have matched differential impedance to minimize impedance discontinuities. Coax cables typically have a characteristic impedance of 50Ω. Contact the factory for 75Ω operation. Table 23 lists the suggested cables and connectors used in the GMSL link.

Board Layout

Separate LVCMOS logic signals, LVDS and CML/coax high-speed signals to prevent crosstalk. Use a four-layer PCB with separate layers for power, ground, LVDS/CML/coax, and LVCMOS logic signals. Layout PCB traces close to each other for a 100Ω differential characteristic impedance for STP. The trace dimensions depend on the type of trace used (microstrip or stripline). Note that two 50Ω PCB traces do not have 100Ω differential impedance when brought close together—the impedance goes down when the traces are brought closer. Use a 50Ω trace for the single-ended output when driving coax.

Route the PCB traces for differential LVDS/CML channels in parallel to maintain the differential characteristic impedance. Avoid vias. Keep PCB traces that make up a differential pair equal length to avoid skew within the differential pair.

ESD Protection

ESD tolerance is rated for Human Body Model, IEC 61000-4-2, and ISO 10605. The ISO 10605 and IEC 61000-4-2 standards specify ESD tolerance for electronic systems. The serial link inputs are rated for ISO 10605 ESD protection and IEC 61000-4-2 ESD protection. All pins are tested for the Human Body Model. The Human Body Model discharge components are C_S = 100pF and R_D = 1.5kΩ (Figure 43). The IEC 61000-4-2 discharge components are C_S = 150pF and R_D = 330Ω (Figure 44). The ISO 10605 discharge components are C_S = 330pF and R_D = 2kΩ (Figure 45).

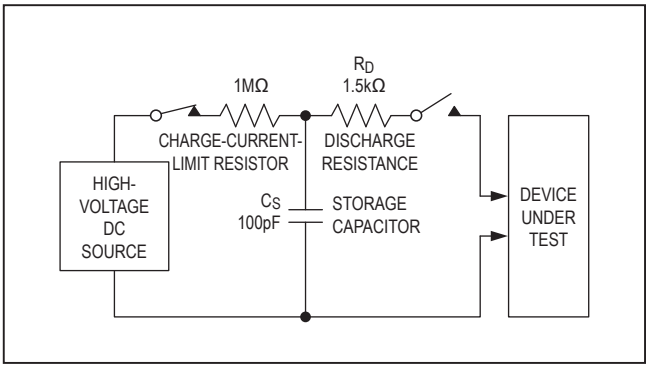


Figure 43. Human Body Model ESD Test Circuit

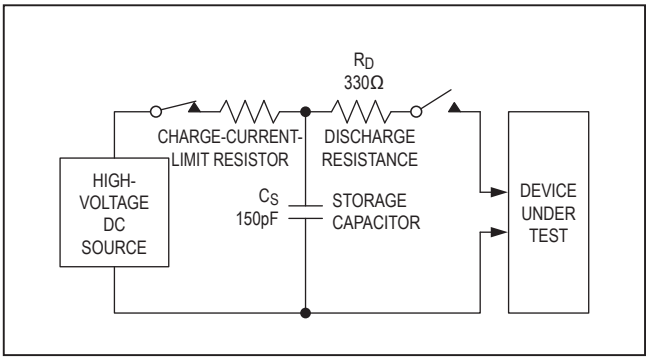


Figure 44. IEC 61000-4-2 Contact Discharge ESD Test Circuit

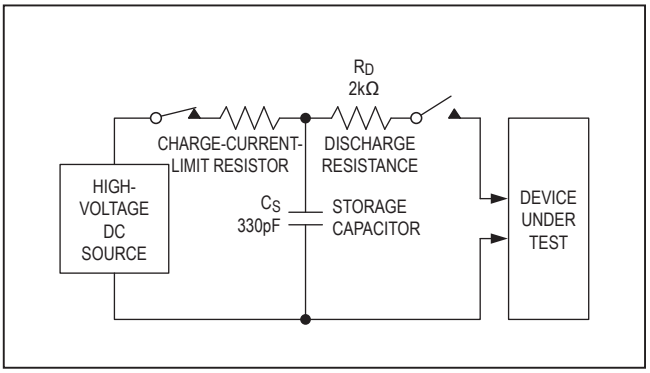


Figure 45. ISO 10605 Contact Discharge ESD Test Circuit

Table 24. Register Table

REGISTER ADDRESS	BITS	NAME	VALUE	FUNCTION	DEFAULT VALUE
0x00	D[7:1]	SERID	XXXXXXX	Serializer device address (power-up default value depends on latched address pin level)	XX00XX0
	D0	CFGBLOCK	0	Normal operation	0
			1	Registers 0x00 to 0x1F are read only	
0x01	D[7:1]	DESID	XXXXXXX	Deserializer device address address (power-up default value depends on latched address pin level)	XX01XX0
	D0	—	0	Reserved	0
0x02	D[7:5]	SS	000	No spread spectrum. (Power-up default values depend on values of CONF[1:0] at power-up)	000, 001
			001	±0.5% spread spectrum (Power-up default values depend on values of CONF[1:0] at power-up)	
			010	±1.5% spread spectrum	
			011	±2% spread spectrum	
			100	No spread spectrum	
			101	±1% spread spectrum	
			110	±3% spread spectrum	
			111	±4% spread spectrum	
	D4	AUDIOEN	0	Disable I²S/TDM channel	1
			1	Enable I²S/TDM channel	
	D[3:2]	PRNG	00	12.5MHz to 25MHz pixel clock	11
			01	25MHz to 50MHz pixel clock	
			10	50MHz to 104MHz pixel clock	
			11	Automatically detect the pixel clock range	
	D[1:0]	SRNG	00	0.5 to 1Gbps serial bit rate	11
			01	1 to 2Gbps serial bit rate	
			10	2 to 3.12Gbps serial bit rate	
			11	Automatically detect serial bit rate	
0x03	D[7:6]	AUTOFM	00	Calibrate spread modulation rate only once after locking	00
			01	Calibrate spread modulation rate every 2ms after locking	
			10	Calibrate spread modulation rate every 16ms after locking	
			11	Calibrate spread modulation rate every 256ms after locking	
	D[5:0]	SDIV	000000	Auto calibrate sawtooth divider	000000
			XXXXXX	Manual SDIV setting. See *Manual Programming of the Spread-Spectrum Divider* section.	

Table 24. Register Table (continued)

REGISTER ADDRESS	BITS	NAME	VALUE	FUNCTION	DEFAULT VALUE
0x04	D7	SEREN	0	Disable serial link. Power-up default when $\overline{AUTOS}$ = high. Reverse control channel communication remains unavailable for 500µs after the serializer starts/stops the serial link	0, 1
			1	Enable serial link. Power-up default when $\overline{AUTOS}$ = low. Reverse control channel communication remains unavailable for 500µs after the serializer starts/stops the serial link	
	D6	CLINKEN	0	Disable configuration link	0
			1	Enable configuration link	
	D5	PRBSEN	0	Disable PRBS test	0
			1	Enable PRBS test	
	D4	SLEEP	0	Normal mode (power-up default value depends on CDS/CNTL3 and $\overline{AUTOS}$ pin values at power-up).	0, 1
			1	Activate sleep mode. (power-up default value depends on CDS/CNTL3 and $\overline{AUTOS}$ pin values at power-up)	
	D[3:2]	INTTYPE	00	Base mode uses I^2C interface when I2CSEL = 0, CDS = 1	00
			01	Base mode uses UART interface when I2CSEL = 0, CDS = 1	
			10, 11	Local control channel disabled	
	D1	REVCCEN	0	Disable reverse control channel from deserializer (receiving)	1
			1	Enable reverse control channel from deserializer (receiving)	
	D0	FWDCCEN	0	Disable forward control channel to deserializer (sending)	1
			1	Enable forward control channel to deserializer (sending)	
0x05	D7	I2CMETHOD	0	I^2C conversion sends the register address when converting UART to I^2C	0
			1	Disable sending of I^2C register address when converting UART to I^2C (command-byte-only mode)	
	D6	DISJITFILT	0	Enable jitter filter	1
			1	Disable jitter filter	
	D[5:4]	CMLLVL	00	100mV CML twisted pair output level (see Table 6).	11
			01	200mV CML twisted pair output level	
			10	300mV CML twisted pair output level	
			11	400mV CML twisted pair output level	

Table 24. Register Table (continued)

REGISTER ADDRESS	BITS	NAME	VALUE	FUNCTION	DEFAULT VALUE
0x05	D[3:0]	PREEMP	0000	Preemphasis off	0000
			0001	-1.2dB Preemphasis	
			0010	-2.5dB Preemphasis	
			0011	-4.1dB Preemphasis	
			0100	-6.0dB Preemphasis	
			0101	Do not use	
			0110	Do not use	
			0111	Do not use	
			1000	1.1dB Preemphasis	
			1001	2.2dB Preemphasis	
			1010	3.3dB Preemphasis	
			1011	4.4dB Preemphasis	
			1100	6.0dB Preemphasis	
			1101	8.0dB Preemphasis	
			1110	10.5dB Preemphasis	
			1111	14.0dB Preemphasis	
0x06	D[7:0]	—	01000000	Reserved	01000000
0x07	D[7:0]	—	00100010	Reserved	00100010
0x08	D[7:4]	—	0000	Reserved	0000 (Read only)
	D[3:2]	LFNEG	00	Negative cable wire shorted to supply voltage	10 (Read only)
			01	Negative cable wire shorted to ground	
			10	Normal operation	
			11	Negative cable wire disconnected	
	D[1:0]	LFPOS	00	Positive cable wire shorted to supply voltage	10 (Read only)
			01	Positive cable wire shorted to ground	
			10	Normal operation	
			11	Positive cable wire disconnected	
0x09	D[7:0]	—	XXXXXXXX	Reserved	(Read only)
0x0A	D[7:0]	—	XXXXXXXX	Reserved	(Read only)
0x0B	D[7:0]	—	XXXXXXXX	Reserved	(Read only)
0x0C	D7	X7PLLHIBW	0	Set X7PLL to normal bandwidth	0
			1	Set X7PLL to high bandwidth	
	D[6:0]	—	0100000	Reserved	0100000

Table 24. Register Table (continued)

REGISTER ADDRESS	BITS	NAME	VALUE	FUNCTION	DEFAULT VALUE
0x0D	D7	SETGPO	0	Set GPO to output low	0
			1	Set GPO to output high	
	D6	INVVSYNC	0	Do not invert VSYNC input	0
			1	Invert VSYNC input	
	D5	INVHSYNC	0	Do not invert HSYNC input	0
			1	Invert HSYNC input	
	D4	DISRES	0	RES bit transmitted to deserializer	0
			1	CNTL1 transmitted to deserializer	
	D[3:0]	SKEWADJ	0000	Adjust X7PLL clock skew +50ps	1111
			0001	Adjust X7PLL clock skew +100ps	
			0010	Adjust X7PLL clock skew +200ps	
			0011	Adjust X7PLL clock skew +250ps	
			0100	Adjust X7PLL clock skew +300ps	
			0101	Adjust X7PLL clock skew +350ps	
			0110	Adjust X7PLL clock skew +400ps	
			0111	Do not use	
			1000	Adjust X7PLL clock skew -50ps	
			1001	Adjust X7PLL clock skew -100ps	
			1010	Adjust X7PLL clock skew -200ps	
			1011	Adjust X7PLL clock skew -250ps	
			1100	Adjust X7PLL clock skew -300ps	
			1101	Adjust X7PLL clock skew -350ps	
			1110	Adjust X7PLL clock skew -400ps	
			1111	Do not Adjust X7PLL clock skew	
0x0E	D7	INVDE	0	Do not invert DE input	0
			1	Invert DE input	
	D[6:0]	—	0000010	Reserved	0000010
0x0F	D[7:1]	I2CSRCA	XXXXXXX	I²C address translator source A	0000000
	D0	—	0	Reserved	0
0x10	D[7:1]	I2CDSTA	XXXXXXX	I²C address translator destination A	0000000
	D0	—	0	Reserved	0
0x11	D[7:1]	I2CSRCB	XXXXXXX	I²C address translator source B	0000000
	D0	—	0	Reserved	0
0x12	D[7:1]	I2CDSTB	XXXXXXX	I²C address translator destination B	0000000
	D0	—	0	Reserved	0

Table 24. Register Table (continued)

REGISTER ADDRESS	BITS	NAME	VALUE	FUNCTION	DEFAULT VALUE
0x13	D7	I2CLOCACK	0	Acknowledge not generated when forward channel is not available	1
			1	I²C to I²C-slave generates local acknowledge when forward channel is not available	
	D[6:5]	I2CSLVSH	00	352ns/117ns I²C setup/hold time	01
			01	469ns/234ns I²C setup/hold time	
			10	938ns/352ns I²C setup/hold time	
			11	1046ns/469ns I²C setup/hold time	
	D[4:2]	I2CMSTBT	000	8.47kbps (typ) I²C to I²C-master bit rate setting	101
			001	28.3kbps (typ) I²C to I²C-master bit rate setting	
			010	84.7kbps (typ) I²C to I²C-master bit rate setting	
			011	105kbps (typ) I²C to I²C-master bit rate setting	
			100	173kbps (typ) I²C to I²C-master bit rate setting	
			101	339kbps (typ) I²C to I²C-master bit rate setting	
			110	533kbps (typ) I²C to I²C-master bit rate setting	
			111	837kbps (typ) I²C to I²C-master bit rate setting	
	D[1:0]	I2CSLVTO	00	64µs (typ) I²C to I²C-slave remote timeout	10
			01	256µs (typ) I²C to I²C-slave remote timeout	
			10	1024µs (typ) I²C to I²C-slave remote timeout	
			11	No I²C to I²C-slave remote timeout	
0x14	D[7:4]	CMLLVLCX	0000	Do not use	1010
			0001	50mV CML coax output level	
			0010	100mV CML coax output level	
			0011	150mV CML coax output level	
			0100	200mV CML coax output level	
			0101	250mV CML coax output level	
			0110	300mV CML coax output level	
			0111	350mV CML coax output level	
			1000	400mV CML coax output level	
			1001	450mV CML coax output level	
			1010	500mV CML coax output level	
			1011	Do not use	
			11XX	Do not use	
	D[3:1]	—	000	Reserved	000
	D0	DISRWAKE	0	Enable wake-up receiver (enable remote wakeup)	0
			1	Disable wake-up receiver (disable remote wakeup)	

Table 24. Register Table (continued)

REGISTER ADDRESS	BITS	NAME	VALUE	FUNCTION	DEFAULT VALUE
0x15	D7	DISDETRIG	0	Enable DE trigger of encoded packets in high-bandwidth mode	0
			1	Disable DE trigger of encoded packets in high-bandwidth mode	
	D[6:5]	CNTLTRIG	00	No trigger of encoded CNTL packets in high-bandwidth mode	10
			01	Always trigger encoded CNTL packets in high-bandwidth mode	
			10	Trigger encoded CNTL packets in high-bandwidth mode when DE is low	
			11	Trigger encoded CNTL packets in high-bandwidth mode when HS is low	
	D4	ENREVP	0	Disable reverse channel from positive input with coax cable	1
			1	Enable reverse channel from positive input with coax cable	
	D3	ENREVN	0	Disable reverse channel from negative input with coax cable	0
			1	Enable reverse channel from negative input with coax cable	
	D[2:0]	—	010	Reserved	010
0x16	D[7:0]	—	XXXXXXXX	Reserved	XXXXXXXX
0x17	D7	HIGHIMM	0	Set reverse channel to legacy mode. (power-up default value depends on GPO/HIM pin value at power-up)	0, 1
			1	Set reverse channel to high-immunity mode (power-up default value depends on GPO/HIM pin value at power-up)	
	D[6:0]	—	0011111	Reserved	0011111
0x18	D[7:0]	—	XXXXXXXX	Reserved	(Read only)
0x19	D[7:0]	—	01001010	Reserved	01001010
0x1A	D7	REVFAST	0	High Immunity Reverse Channel Mode uses 500kbps bit rate	0
			1	High Immunity Reverse Channel Mode uses 1Mbps bit rate	
	D6	—	0	Reserved	0
	D5	MDCNTL0	0	MS/CNTL0 functions as MS input	0
			1	MS/CNTL0 functions as CNTL0 input	
	D4	CDSCNTL3	0	CDS/CNTL3 functions as CDS input	0
			1	CDS/CNTL3 functions as CNTL3 input	
	D[3:1]	—	000	Reserved	000
	D0	REVARBTO	0	256µs reverse channel arbitration time out duration (coax splitter mode only)	0
			1	4ms reverse channel arbitration time out duration (coax splitter mode only)	

Table 24. Register Table (continued)

REGISTER ADDRESS	BITS	NAME	VALUE	FUNCTION	DEFAULT VALUE
0x1B	D7	INVSCK	0	Do not invert SCK input	0
			1	Invert SCK input	
	D6	INVWS	0	Do not invert WS input	0
			1	Invert WS input	
	D[5:0]	—	010000	Reserved	010000
0x1E	D[7:0]	ID	00100011	Device is a MAX9277 (0x23)	00100X11 (Read only)
			00100111	Device is a MAX9281 (0x27)	
0x1F	D[7:5]	—	000	Reserved	000 (Read only)
	D4	CAPS	0	Not HDCP capable (MAX9277)	(Read only)
			1	HDCP capable (MAX9281)	
	D[3:0]	REVISION	XXXX	Device revision	(Read only)

**X = don't care*

Table 25. HDCP Register Table (MAX9281 Only)

REGISTER ADDRESS	SIZE (Bytes)	NAME	READ/ WRITE	FUNCTION	DEFAULT VALUE (hex)
0x80 to 0x84	5	BKSV	Read/write	HDCP receiver KSV	0x0000000000
0x85 to 0x86	2	RI/RI'	Read/write	RI (read only) of the transmitter when EN_INT_COMP = 0 RI' (read/write) of the receiver when EN_INT_COMP = 1	0xFFFF
0x87	1	PJ/PJ'	Read/write	PJ (read only) of the transmitter when EN_INT_COMP = 0 PJ' (read/write) of the receiver when EN_INT_COMP = 1	0xFF
0x88 to 0x8F	8	AN	Read only	Session random number	(Read only)
0x90 to 0x94	5	AKSV	Read only	HDCP transmitter KSV	(Read only)
0x95	1	ACTRL	Read/write	D7 = PD_HDCP 1 = Power-down HDCP circuits 0 = HDCP circuits normal	0x00
				D6 = EN_INT_COMP 1 = Internal comparison mode 0 = µC comparison mode	
				D5 = FORCE_AUDIO 1 = Force audio data to 0 0 = Normal operation	
				D4 = FORCE_VIDEO 1 = Force video data DFORCE value 0 = Normal operation	

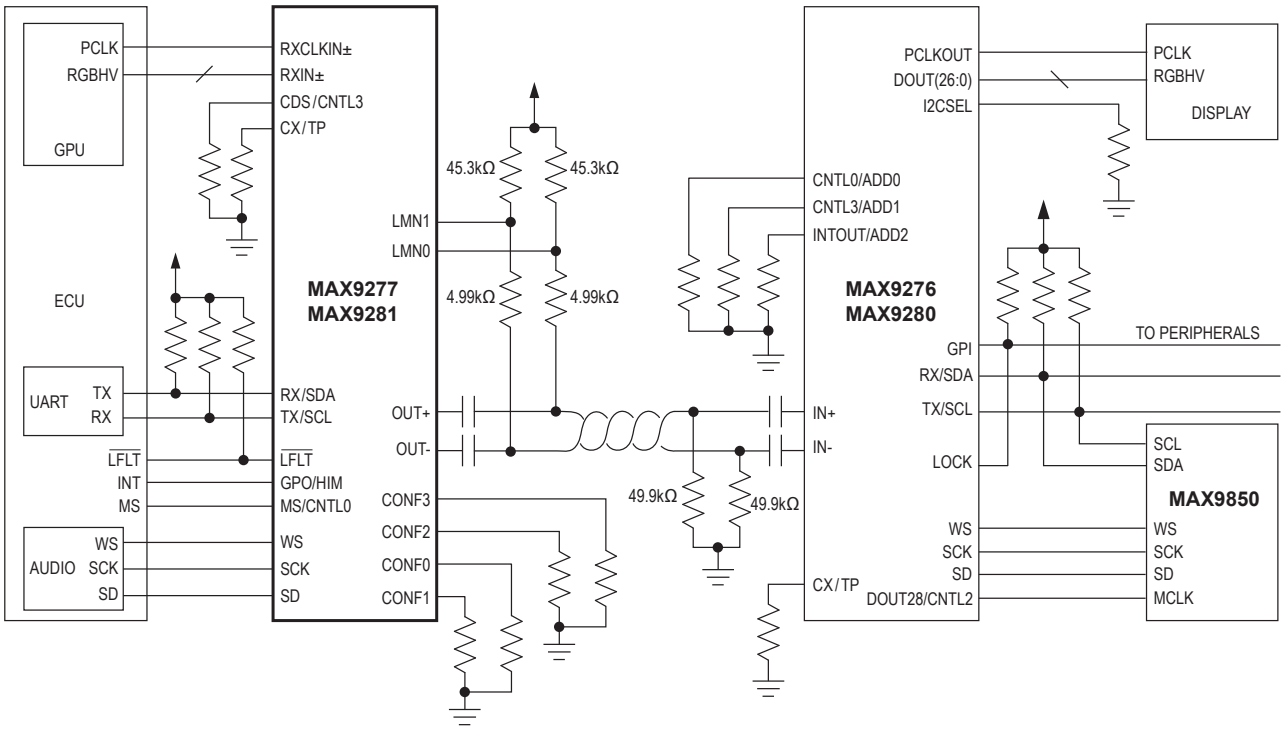
Table 25. HDCP Register Table (MAX9281 Only) (continued)

REGISTER ADDRESS	SIZE (Bytes)	NAME	READ/ WRITE	FUNCTION	DEFAULT VALUE (hex)
0x95	1	ACTRL	Read/write	D3 = RESET_HDCP 1 = Reset HDCP circuits. Automatically set to 0 upon completion. 0 = Normal operation	0x00
				D2 = START_AUTHENTICATION 1 = Start authentication. Automatically set to 0 once authentication starts. 0 = Normal operation	
				D1 = VSYNC_DET 1 = Internal falling edge on VSYNC detected 0 = No falling edge detected	
				D0 = ENCRYPTION_ENABLE 1 = Enable encryption 0 = Disable encryption	
0x96	1	ASTATUS	Read only	D[7:4] = Reserved	0x00 (Read only)
				D3 = V_MATCHED 1 = V matches V' (when EN_INT_COMP = 1) 0 = V does not match V' or EN_INT_COMP = 0	
				D2 = PJ_MATCHED 1 = PJ matches PJ' (when EN_INT_COMP = 1) 0 = PJ does not match PJ' or EN_INT_COMP = 0	
				D1 = R0_RI_MATCHED 1 = RI matches RI' (when EN_INT_COMP = 1) 0 = RI does not match RI' or EN_INT_COMP = 0	
				D0 = BKSV_INVALID 1 = BKSV is not valid 0 = BKSV is valid	
0x97	1	BCAPS	Read/write	D[7:1] = RESERVED	0x00
				D0 = REPEATER 1 = Set to one if device is a repeater 0 = Set to zero if device is not a repeater	
0x98 to 0x9C	5	ASEED	Read/write	internal random number generator optional seed value	0x0000000000
0x9D to 0x9F	3	DFORCE	Read/write	Forced video data transmitted when FORCE_VIDEO = 1. R[7:0] = DFORCE[7:0] G[7:0] = DFORCE[15:8] B[7:0] = DFORCE[23:16]	0x000000
0xA0 to 0xA3	4	V.H0, V'.H0	Read/write	H0 part of SHA-1 hash value. V (read only) of the transmitter when EN_INT_COMP = 0 V' (read/write) of the receiver when EN_INT_COMP = 1	0x00000000

Table 25. HDCP Register Table (MAX9281 Only) (continued)

REGISTER ADDRESS	SIZE (Bytes)	NAME	READ/ WRITE	FUNCTION	DEFAULT VALUE (hex)
0xA4 to 0xA7	4	V.H1, V'.H1	Read/write	H1 part of SHA-1 hash value. V (read only) of the transmitter when EN_INT_COMP = 0 V' (read/write) of the receiver when EN_INT_COMP = 1	0x00000000
0xA8 to 0xAB	4	V.H2, V'.H2	Read/write	H2 part of SHA-1 hash value. V (read only) of the transmitter when EN_INT_COMP = 0 V' (read/write) of the receiver when EN_INT_COMP = 1	0x00000000
0xAC to 0xAF	4	V.H3, V'.H3	Read/write	H3 part of SHA-1 hash value. V (read only) of the transmitter when EN_INT_COMP = 0 V' (read/write) of the receiver when EN_INT_COMP = 1	0x00000000
0xB0 to 0xB3	4	V.H4, V'.H4	Read/write	H4 part of SHA-1 hash value. V (read only) of the transmitter when EN_INT_COMP = 0 V' (read/write) of the receiver when EN_INT_COMP = 1	0x00000000
0xB4 to 0xB5	2	BINFO	Read/write	D[15:12] = Reserved	0x0000
				D11 = MAX_CASCADE_EXCEEDED 1 = Set to one if more than 7 cascaded devices attached 0 = Set to zero if 7 or fewer cascaded devices attached	
				D[10:8] = DEPTH Depth of cascaded devices	
				D7 = MAX_DEVS_EXCEEDED 1 = Set to one if more than 14 devices attached 0 = Set to zero if 14 or fewer devices attached	
				D[6:0] = DEVICE_COUNT Number of devices attached	
0xB6	1	GPMEM	Read/write	General purpose memory byte	0x00
0xB7 to 0xB9	3	—	Read only	Reserved	0x000000
0xBA to 0xFF	70	KSV_LIST	Read/write	List of KSVs downstream repeaters and receivers (Maximum of 14 devices)	All Zero

Typical Application Circuit



NOTE: NOT ALL PULLUP/PULLDOWN RESISTORS ARE SHOWN. SEE PIN DESCRIPTION FOR DETAILS.

VIDEO-DISPLAY APPLICATION

Ordering Information

PART	TEMP RANGE	PIN-PACKAGE	HDCP
MAX9277GTM+	-40°C to +105°C	48 TQFN-EP*	NO
MAX9277GTM/V+	-40°C to +105°C	48 TQFN-EP*	NO
MAX9277GTM/VY+	-40°C to +105°C	48 TQFN-SW-EP*	NO
MAX9281GTM+	-40°C to +105°C	48 TQFN-EP*	YES**
MAX9281GTM/V+	-40°C to +105°C	48 TQFN-EP*	YES**
MAX9281GTM/VY+***	-40°C to +105°C	48 TQFN-SW-EP*	YES**

+Denotes a lead(Pb)-free/RoHS-compliant package.
/V denotes an automotive qualified product.
Y denotes wettable flank.
**EP = Exposed pad.*
***HDCP parts require registration with Digital Content Protection, LLC.*
****Future product - contact factory for availability.*

Chip Information

PROCESS: CMOS

Package Information

For the latest package outline information and land patterns (footprints), go to **www.maximintegrated.com/packages**. Note that a "+", "#", or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

PACKAGE TYPE	PACKAGE CODE	OUTLINE NO.	LAND PATTERN NO.
48 TQFN-EP	T4877+6	21-0144	90-0130
48 TQFN-SW-EP	T4877Y+4	21-100045	90-100016

Revision History

REVISION NUMBER	REVISION DATE	DESCRIPTION	PAGES CHANGED
0	8/13	Initial release	—
1	11/13	Fixed errors and clarified functions	18, 20, 22, 31, 33, 37, 38, 49, 50, 60, 74
2	7/15	Removed future product designations from *Ordering Information*	74
3	10/17	Fixed typos, clarified feature descriptions, removed old/unnecessary content (e.g., Table 1), general improvements	12, 13, 17–20, 22, 26, 27–30, 31, 33, 34, 36, 38, 39, 43–50, 52–59, 61–74
4	8/19	Added optional wettable flank package to *General Description*, *Ordering Information*, and *Package Information*.	1, 72
4.1		Corrected broken link in *Package Information* section	72

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MAX9281GTM/V+TGG7 MAX9281GTM/V+GG7 MAX9281COAXEVKIT#