MAX5882

14-Bit, 4.6Gsps Cable Downstream Direct RF Synthesis DAC

General Description

The MAX5882 14-bit, 4.6Gsps digital-to-analog converter (DAC) is designed for direct RF synthesis of multicarrier quadrature amplitude modulation (QAM) signals in cable modem termination systems (CMTS) and edge QAM (EQAM) devices. The DAC features excellent spurious, noise, and adjacent-channel power (ACP) performance, and directly synthesizes multiple carriers in the 47MHz to 1003MHz cable downstream band, as defined by the Data-Over-Cable Service Interface Specification (DOCSISM). The 4.6Gsps update rate allows digital generation of signals with more than 2GHz bandwidth.

The device has four 14-bit, multiplexed, low-voltage differential signaling (LVDS) input ports that each operate at up to 1150Mwps in double data rate (DDR) or single data rate (SDR) mode. The inputs also accept differential high-speed transceiver logic (DHSTL) input levels. The device accepts a clock at 1/2 the DAC update rate, as conversion is triggered on both rising and falling clock edges. The input data rate on each port is 1/4 the DAC update rate or 1/2 of the clock rate. The device contains a delay-locked loop (DLL) that simplifies the interface to FPGA or ASIC devices. Using the DLL, the phase of the output clock (DATACLK) is adjusted to ensure that the input LVDS data bus has the proper timing relationship to the on-chip clock used to latch the data.

The device is a current-steering DAC with an integrated 50I differential output termination to ensure optimum dynamic performance. Operating from 3.3V and 1.8V power supplies, the device consumes 2.3W at 4.6Gsps. The device is specified over the extended temperature range (-40NC to +85NC) and is offered in a 256 CSBGA lead(Pb)-free/RoHS-compliant package.

Applications

- DOCSIS-Compliant Edge QAM Devices
- Cable Modem Termination Systems (CMTS)
- Broadcast Video Modulators
- Video-On-Demand (VOD)
- Coax Media Converters
- Remote PHY

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Features

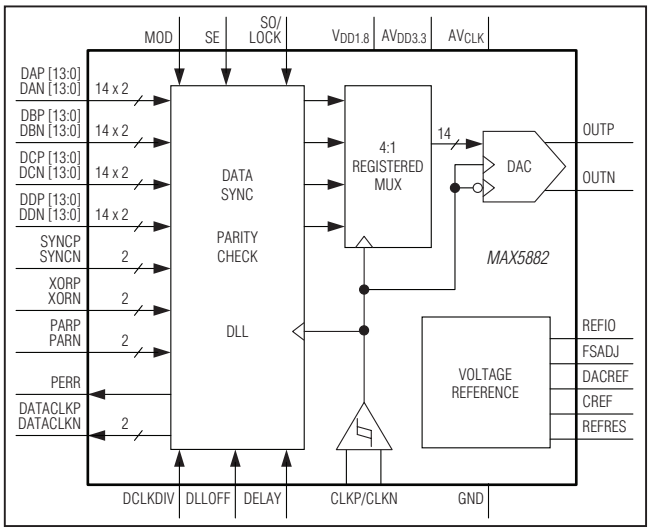
- 4.6Gsps Output Update Rate
  - Direct RF Synthesis from 47MHz to 1003MHz
  - No Aliasing of HD3 into Cable Band
- Industry-Leading DOCSIS 3.0 Performance Noise Floor
  - -70dBc at f_{OUT} = 900MHz, 8 Channel (256 QAM)
  - -66dBc at f_{OUT} = 900MHz, 16 Channel (256 QAM)
  - -62dBc at f_{OUT} = 900MHz, 32 Channel (256 QAM)
  - -57dBc at f_{OUT} = 500MHz, 128 Channel (256 QAM)
- High Output Power 9dBm (CW)
  - Enables Low Solution Power
- 4:1 Multiplexed LVDS Inputs
  - Up to 1150Mwps Each Port
  - Double Data Rate (DDR) Mode
- On-Chip DLL for Input Data Synchronization
- Parity Error Flag
- Internal 50Ω Differential Output Termination
- Input Register Scan Mode
- Compact 17mm x 17mm, 256 CSBGA Package
- Evaluation Kit Available (Order MAX5882EVKIT+)

Ordering Information

PART	TEMP RANGE	PIN-PACKAGE
MAX5882EXF+D	-40°C to +85°C	256 CSBGA

+Denotes a lead(Pb)-free/RoHS-compliant package.
D = Dry pack.

Functional Diagram



maxim integrated™

Absolute Maximum Ratings

$AV_{DD3.3}$ to GND, DACREF ..... -0.3V to 3.6V
$V_{DD1.8}$, AV_{CLK} to GND, DACREF ..... -0.3V to 2.0V
REFIO, FSADJ to GND, DACREF ..... -0.3V to $AV_{DD3.3}$ + 0.3V
OUTP, OUTN to GND, DACREF ..... -0.3V to $AV_{DD3.3}$ + 1.0V
CREF to GND, DACREF ..... -0.3V to $V_{DD1.8}$ + 0.3V
SE, DCLKDIV, DLLOFF, MOD, DELAY, REFRES TO GND, DACREF ..... -0.3V to $AV_{DD3.3}$ + 0.3V
CLKP, CLKN to GND, DACREF ..... -0.3V to AV_{CLK} + 0.3V
DAP0–DAP13, DBP0–DBP13, DCP0–DCP13 to GND, DACREF ..... -0.3V to $V_{DD1.8}$ + 0.3V
DDP0–DDP13, XORP, SYNCP, PARP to GND, DACREF ..... -0.3V to $V_{DD1.8}$ + 0.3V
DAN0–DAN13, DBN0–DBN13, DCN0–DCN13 to GND, DACREF ..... -0.3V to $V_{DD1.8}$ + 0.3V
DDN0–DDN13, XORN, SYNCN, PARN to GND, DACREF ..... -0.3V to $V_{DD1.8}$ + 0.3V
DATACLKP, DATACLKN to GND, DACREF ..... -0.3V to $V_{DD1.8}$ + 0.3V
SO/LOCK, PERR to GND, DACREF ..... -0.3V to $V_{DD1.8}$ + 0.3V
SO/LOCK, PERR Continuous Current 8mA
DATACLKP, DATACLKN Continuous Current 8mA
Continuous Power Dissipation (T_A = +70°C)
256 CSBGA (derate 38.6mW/°C above +70°C) 3088.8mW
Operating Temperature Range ..... -40°C to +85°C
Junction Temperature ..... +150°C
Storage Temperature Range ..... -65°C to +150°C
Soldering Temperature (reflow) ..... +260°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Electrical Characteristics

($V_{AVDD3.3}$ = 3.3V, $V_{DD1.8}$ = V_{AVCLK} = 1.8V, R_{SET} = 2kΩ, V_{REFIO} = external 1.25V, V_{MOD} = $V_{DCLKDIV}$ = V_{DLLOFF} = 0V, V_{DELAY} = 1.8V, R_{REFRES} = 500Ω, transformer-coupled differential output, $T_{A(MIN)}$ = -40°C, $T_{J(MAX)}$ = +110°C, unless otherwise noted. Typical values are at T_J = +65°C.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
STATIC PERFORMANCE						
Resolution				14		Bits
Full-Scale Output Current Range	I_{OUT}	(Note 2)	10		80	mA
Output-Power Gain Error	GE		-0.7		+0.7	dB
Output-Power Drift		Internal reference		-0.003		dB/°C
		External reference		-0.0025		
Full-Scale Output Power	P_{OUT}	Differential, into 50Ω load, f_{OUT} = 103.5MHz, f_{DAC} = 4.608Gsps		9		dBm
Output Resistance	R_{OUT}	Differential		50		Ω
DYNAMIC PERFORMANCE (Note 3)						
Minimum Clock Rate	f_{CLK}				10	MHz
Maximum Clock Rate	f_{CLK}		2304			MHz
Minimum Output Update Rate	f_{DAC}				20	Msps
Maximum Output Update Rate	f_{DAC}		4608			Msps

Electrical Characteristics (continued)

($V_{AVDD3.3}$ = 3.3V, $V_{DD1.8}$ = V_{AVCLK} = 1.8V, R_{SET} = 2kΩ, V_{REFIO} = external 1.25V, V_{MOD} = $V_{DCLKDIV}$ = V_{DLLOFF} = 0V, V_{DELAY} = 1.8V, R_{REFRES} = 500Ω, transformer-coupled differential output, $T_{A(MIN)}$ = -40°C, $T_{J(MAX)}$ = +110°C, unless otherwise noted. Typical values are at T_J = +65°C.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Out-of-Band Noise and Spurious, Eight 6MHz QAM Channels, Average Total Power = -10dBFS		f_{OUT} = 400MHz, f_{DAC} = 4608Msps	Adjacent channel (750kHz from channel block edge to 6MHz from channel block edge)		-71	-64	dBc
			Next-adjacent channel (6MHz from channel block edge to 12MHz from channel block edge)		-73	-66	
			Third-adjacent channel (12MHz from channel block edge to 18MHz from channel block edge)		-73	-66	
			Noise in any other channel (Note 4)		-73		
		f_{OUT} = 860MHz, f_{DAC} = 4608Msps	Adjacent channel (750kHz from channel block edge to 6MHz from channel block edge)		-67		
			Next-adjacent channel (6MHz from channel block edge to 12MHz from channel block edge)		-66		
			Third-adjacent channel (12MHz from channel block edge to 18MHz from channel block edge)		-66		
			Noise in any other channel (Note 4)		-65		
		f_{OUT} = 1000MHz, f_{DAC} = 4608Msps	Adjacent channel (750kHz from channel block edge to 6MHz from channel block edge)		-67		
			Next-adjacent channel (6MHz from channel block edge to 12MHz from channel block edge)		-67		
			Third-adjacent channel (12MHz from channel block edge to 18MHz from channel block edge)		-67		
			Noise in any other channel (Note 4)		-66		

Electrical Characteristics (continued)

($V_{AVDD3.3}$ = 3.3V, $V_{DD1.8}$ = V_{AVCLK} = 1.8V, R_{SET} = 2kΩ, V_{REFIO} = external 1.25V, V_{MOD} = $V_{DCLKDIV}$ = V_{DLLOFF} = 0V, V_{DELAY} = 1.8V, R_{REFRES} = 500Ω, transformer-coupled differential output, $T_{A(MIN)}$ = -40°C, $T_{J(MAX)}$ = +110°C, unless otherwise noted. Typical values are at T_J = +65°C.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Harmonic Distortion, Block of Four 6MHz QAM Channels, Average Total Power = -10dBFS		f_{OUT} = 300MHz, f_{DAC} = 4.6Gsps	In each of eight 6MHz channels coinciding with 2nd-harmonic components		-72	-64	dBc
			In each of twelve 6MHz channels coinciding with 3rd-harmonic components		-72	-65	
Gain Flatness	GF	Over any single 6MHz channel			0.05		dB
		Within 47MHz to 1003MHz band			1.6		
Clock Spurs		f_{DAC} = 4.6Gsps, eight QAM channels	f_{DAC}/4 spur		-80		dBm
			f_{DAC}/8 spur		-100		
$f_{DAC}/2 - f_{OUT}$ Image		f_{DAC} = 4.6Gsps, eight QAM channels covering the band from 952MHz to 1000MHz			-40		dBc
$f_{DAC}/2 - 2f_{OUT}$ Spurious		f_{DAC} = 4.6Gsps, eight QAM channels covering the band from 952MHz to 1000MHz			-64		dBc
REFERENCE							
Internal Reference Voltage Range	V_{REFIO}			1.1	1.2	1.3	V
Reference Input-Voltage Compliance Range	V_{REFIOR}			0.5		1.8	V
Reference Input Resistance	R_{REFIO}				10		kΩ
Reference Voltage Drift	TCO_{REF}				50		ppm/°C
ANALOG OUTPUT TIMING							
Output Fall Time	t_{FALL}	90% to 10% (Note 5)			300		ps
Output Rise Time	t_{RISE}	10% to 90% (Note 5)			300		ps
Settling Time	t_S	Settling to 0.1%			1		ns
		Settling to 0.025%			2.5		
Output Bandwidth	BW	(Note 6)			2.0		GHz
Output Propagation Delay	t_{PD}	(Note 7)			1.5		ns
Output Data Latency	t_{DL}	DAP[13:0]/DAN[13:0] to output			11.5		Clock Cycles
		DBP[13:0]/DBN[13:0] to output			12		
		DCP[13:0]/DCN[13:0] to output			12.5		
		DDP[13:0]/DDN[13:0] to output			13		
TIMING CHARACTERISTICS							
DLL Frequency Range	f_{DLL}	f_{DLL} = $f_{CLK}/2$	DLLOFF = Low, DELAY = High	1075		1152	MHz
			DLLOFF = Low, DELAY = Open	950		1075	
			DLLOFF = Open, DELAY = Low	825		950	
			DLLOFF = Open, DELAY = High	700		825	
			DLLOFF = Open, DELAY = Open	625		700	
			DLLOFF = Res, DELAY = Low	550		625	
			DLLOFF = Res, DELAY = High	475		550	
			DLLOFF = Res, DELAY = Open	400		475	

Electrical Characteristics (continued)

($V_{AVDD3.3}$ = 3.3V, $V_{DD1.8}$ = V_{AVCLK} = 1.8V, R_{SET} = 2kΩ, V_{REFIO} = external 1.25V, V_{MOD} = $V_{DCLKDIV}$ = V_{DLLOFF} = 0V, V_{DELAY} = 1.8V, R_{REFRES} = 500Ω, transformer-coupled differential output, $T_{A(MIN)}$ = -40°C, $T_{J(MAX)}$ = +110°C, unless otherwise noted. Typical values are at T_J = +65°C.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Input Data Skew vs. SYNC	t_{SKEW}	Allowed skew of any LVDS inputs (DAP[13:0]/DAN[13:0], DBP[13:0]/DBN[13:0], DCP[13:0]/DCN[13:0], DDP[13:0]/DDN[13:0], XORP/XORN, and PARP/PARN), with respect to the SYNC input; this parameter only applies when DLLOFF is not driven high (Note 8)	$T_{A(MIN)}$ = 0°C, $T_{J(MAX)}$ = +110°C	-324		+307	ps
			$T_{A(MIN)}$ = -40°C, $T_{J(MAX)}$ = +110°C	-300		+300	
Input Data to Clock Setup Time	t_{SETUP}	DLLOFF = 1.8V; data on the LVDS input pins must be stable for t_{SETUP} before the next edge of DATACLKP/DATACLKN; this parameter only applies when DLLOFF is driven high (Note 8)	$T_{A(MIN)}$ = 0°C, $T_{J(MAX)}$ = +110°C	1.52			ns
			$T_{A(MIN)}$ = -40°C, $T_{J(MAX)}$ = +110°C	1.53			
Input Data to Clock Hold Time	t_{HOLD}	DLLOFF = 1.8V; data on the LVDS input pins must remain stable for t_{HOLD} after an edge of DATACLKP/DATACLKN; this parameter only applies when DLLOFF is driven high (Note 8)	$T_{A(MIN)}$ = 0°C, $T_{J(MAX)}$ = +110°C	-0.85			ns
			$T_{A(MIN)}$ = -40°C, $T_{J(MAX)}$ = +110°C	-0.9			
Parity Error Pulse Width	t_{ERR}	Pulse width of PERR when a parity error is detected			48		Data Clock Cycles
Parity Pipeline Delay	$t_{PIPE, PARITY}$	Pipeline delay in the internal parity calculation; delay the incoming PARP/PARN bit by this amount		3		3	Data Clock Cycles
XOR Pipeline Delay	$t_{PIPE, XOR}$	Pipeline delay in the XOR path; delay the incoming XORP/XORN bit by this amount		1		1	Data Clock Cycles

Electrical Characteristics (continued)

($V_{AVDD3.3}$ = 3.3V, $V_{DD1.8}$ = V_{AVCLK} = 1.8V, R_{SET} = 2kΩ, V_{REFIO} = external 1.25V, V_{MOD} = $V_{DCLKDIV}$ = V_{DLLOFF} = 0V, V_{DELAY} = 1.8V, R_{REFRES} = 500Ω, transformer-coupled differential output, $T_{A(MIN)}$ = -40°C, $T_{J(MAX)}$ = +110°C, unless otherwise noted. Typical values are at T_J = +65°C.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
DIFFERENTIAL LOGIC INPUTS (DAP[13:0], DAN[13:0], DBP[13:0], DBN[13:0], DCP[13:0], DCN[13:0], DDP[13:0], DDN[13:0], XORP, XORN, PARP, PARN, SYNCP, SYNCN) SPECIFIED FOR LVDS INPUT						
Differential Input Logic-High	V_{IH}		100			mV
Differential Input Logic-Low	V_{IL}				-100	mV
Input Common-Mode Voltage Range	V_{COM}		1.125		1.375	V
Differential Input Resistance	R_{IN}		85	107	125	Ω
Input Capacitance	C_{IN}			1.5		pF
DIFFERENTIAL LOGIC INPUTS (DAP[13:0], DAN[13:0], DBP[13:0], DBN[13:0], DCP[13:0], DCN[13:0], DDP[13:0], DDN[13:0], XORP, XORN, PARP, PARN, SYNCP, SYNCN) SPECIFIED FOR DIFFERENTIAL-HSTL INPUT						
Differential Input Logic-High	$V_{IH(DC)}$		160			mV
Differential Input Logic-Low	$V_{IL(DC)}$				-160	mV
Input Common-Mode Voltage Range	V_{COM}		0.456		1.0	V
Differential Input Resistance	R_{IN}		85	107	125	Ω
Input Capacitance	C_{IN}			1.5		pF
1.8V CMOS LOGIC INPUTS (DCLKDIV, SE, MOD)						
Input Logic-High	$V_{IH1.8}$		0.7 x $V_{DD1.8}$			V
Input Logic-Low	$V_{IL1.8}$				0.3 x $V_{DD1.8}$	V
Input Leakage Current	$I_{IN1.8}$		-5		+5	µA
Input Capacitance	$C_{IN1.8}$			3		pF
1.8V 4-LEVEL LOGIC INPUTS (DLLOFF, DELAY)						
Input 4-Level Logic-Open	V_{OC4}		23/32 x $V_{DD1.8}$ + 50mV		29/32 x $V_{DD1.8}$ - 50mV	V
Input 4-Level Logic-Res	V_{RC4}		7/32 x $V_{DD1.8}$ + 50mV		23/32 x $V_{DD1.8}$ - 50mV	V
Input 4-Level Logic-High	V_{IH4}		29/32 x $V_{DD1.8}$ + 50mV		$V_{DD1.8}$	V
Input 4-Level Logic-Low	V_{IL4}		0		7/32 x $V_{DD1.8}$ - 50mV	V
Input Pullup Current	I_{PU4}		8	11.3	15	µA
Input Pulldown Current	I_{PD4}		32		64	µA
Input Capacitance	C_{IN4}			3		pF

Electrical Characteristics (continued)

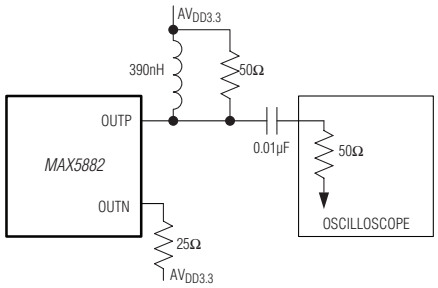
($V_{AVDD3.3}$ = 3.3V, $V_{DD1.8}$ = V_{AVCLK} = 1.8V, R_{SET} = 2kΩ, V_{REFIO} = external 1.25V, V_{MOD} = $V_{DCLKDIV}$ = V_{DLLOFF} = 0V, V_{DELAY} = 1.8V, R_{REFRES} = 500Ω, transformer-coupled differential output, $T_{A(MIN)}$ = -40°C, $T_{J(MAX)}$ = +110°C, unless otherwise noted. Typical values are at T_J = +65°C.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
1.8V CMOS LOGIC OUTPUTS (SO/LOCK, PERR)						
Output Logic-High	$V_{OH1.8}$	I_{SOURCE} = 200µA	$V_{DD1.8}$ - 0.2			V
Output Logic-Low	$V_{OL1.8}$	I_{SINK} = 200µA			0.2	V
1.8V LVDS OUTPUTS (DATACLKP, DATACLKN)						
Differential Swing	$V_{DIFF, LVDS}$	$V_{DIFF,LVDS}$ = $V_{DATACLKP}$ - $V_{DATACLKN}$ with 100Ω differential termination	±250	±350	±450	mV
Output Rise and Fall Time	t_R, t_F	With 100Ω differential termination		0.3		ns
Common-Mode Voltage	$V_{COM, LVDS}$		1.125	1.28	1.375	V
CLOCK INPUTS (CLKP, CLKN)						
Minimum Clock Input Power	$P_{CLK, MIN}$	(Note 9)		6		dBm
Maximum Clock Input Power	$P_{CLK, MAX}$	Power measured into the MAX5882 clock input with 100Ω external differential termination resistor		12		dBm
Common-Mode Voltage	V_{COMCLK}	Input is self-biased		AV_{CLK}/3		V
Input Resistance	R_{CLK}	Differential		100		Ω
Input Capacitance	C_{CLK}			2		pF
POWER SUPPLIES						
Analog Supply Voltage Range	$AV_{DD3.3}$		3.2	3.3	3.5	V
1.8V Supply Voltage Range	$V_{DD1.8}$		1.7	1.8	1.9	V
Clock Supply Voltage Range	AV_{CLK}		1.7	1.8	1.9	V
Analog Supply Current	$I_{AVDD3.3}$	f_{DAC} = 4608Msps, f_{OUT} = 400MHz, 8-channel QAM (Note 3)		335	360	mA
1.8V Supply Current	$I_{VDD1.8}$	f_{DAC} = 4608Msps, f_{OUT} = 400MHz, 8-channel QAM (Note 3)		250	290	mA
Clock Supply Current	I_{AVCLK}	f_{DAC} = 4608Msps, f_{OUT} = 400MHz, 8-channel QAM (Note 3)		440	500	mA
Power Dissipation	P_{DISS}	f_{DAC} = 4608Msps, f_{OUT} = 400MHz, 8-channel QAM (Note 3)		2.3	2.6	W

Electrical Characteristics (continued)

($V_{AVDD3.3}$ = 3.3V, $V_{DD1.8}$ = V_{AVCLK} = 1.8V, R_{SET} = 2kΩ, V_{REFIO} = external 1.25V, V_{MOD} = $V_{DCLKDIV}$ = V_{DLLOFF} = 0V, V_{DELAY} = 1.8V, R_{REFRES} = 500Ω, transformer-coupled differential output, $T_{A(MIN)}$ = -40°C, $T_{J(MAX)}$ = +110°C, unless otherwise noted. Typical values are at T_J = +65°C.) (Note 1)

Note 1: All specifications are guaranteed via test at T_J = +65°C and T_J = +110°C to an accuracy of ±15°C, unless otherwise noted. Specifications at T_J < +65°C are guaranteed by design and characterization. Timing specifications are guaranteed by design and characterization.
Note 2: Nominal full-scale current I_{OUT} = 128 x I_{REF}.
Note 3: CLK input = +9dBm, AC-coupled sine wave.
Note 4: Excludes clock, clock images, $f_{DAC}/2 - f_{OUT}$, and $f_{DAC}/2 - 2f_{OUT}$ spurs, which are specified separately.
Note 5: Measured single-ended into a double-terminated 50Ω load.



Note 6: Excludes impulse-response dependent rolloff inherent in the DAC.
Note 7: Referenced to rising edge of DAC update clock—excludes data latency.
Note 8: Guaranteed by design and characterization.
Note 9: Transformer-coupled clock input (Figure 4).

Thermal Characteristics

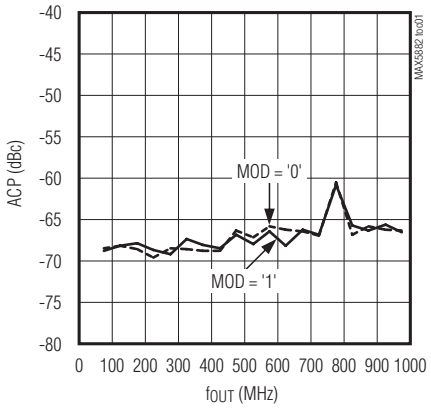
PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Ambient Temperature	T_A	(Note 10)	-40		+85	°C
Junction Temperature	T_J		-40		+110	°C
Thermal Resistance, Junction-to-Ambient (Note 10)	θ_{JA}	Air flow 0m/s		31.9		°C/W
		Air flow 1m/s		27.7		
Thermal Resistance, Junction-to-Case	θ_{JC}			3.4		°C/W
Thermal Resistance, Junction-to-Board	θ_{JB}			24		°C/W
Thermal Characterization Parameter, Junction-to-Board	Ψ_{JB}	Air flow 0m/s		25.5		°C/W
		Air flow 1m/s		23.7		
Thermal Characterization Parameter, Junction-to-Top	Ψ_{JT}	Air flow 0m/s		8.1		°C/W
		Air flow 1m/s		1.7		

Note 10: The package is mounted on a four-layer JEDEC-standard test board, dissipating maximum power.

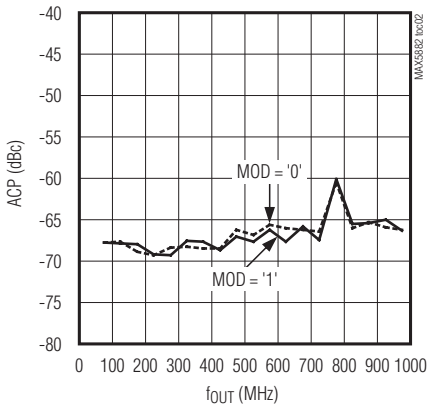
Typical Operating Characteristics

($V_{AVDD3.3}$ = 3.3V, $V_{DD1.8}$ = V_{AVCLK} = 1.8V, R_{SET} = 2kΩ, V_{REFIO} = external 1.25V, V_{MOD} = $V_{DCLKDIV}$ = V_{DLLOFF} = 0V, V_{DELAY} = 1.8V, R_{REFRES} = 500Ω, transformer-coupled differential output, tested at T_J = +60°C, unless otherwise noted.)

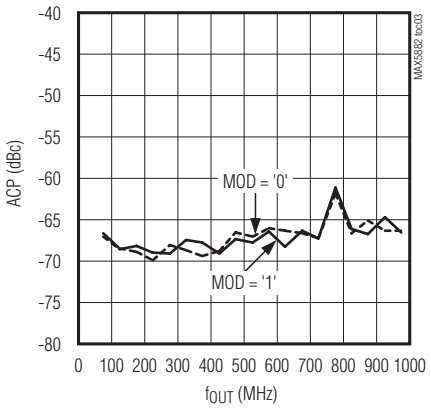
8-CHANNEL 256 QAM ACP vs. OUTPUT FREQUENCY (f_{DAC} = 4.6Gsps, 750kHz TO 6MHz FROM CHANNEL BLOCK EDGE)



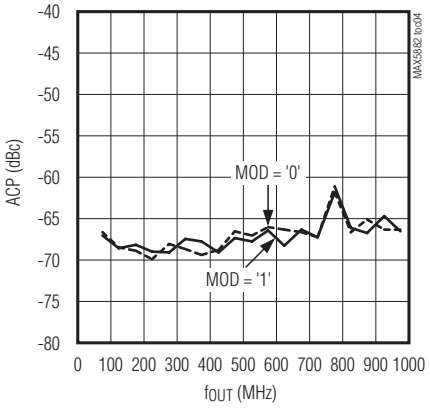
8-CHANNEL 256 QAM ACP vs. OUTPUT FREQUENCY (f_{DAC} = 4.6Gsps, 6MHz TO 12MHz FROM CHANNEL BLOCK EDGE)



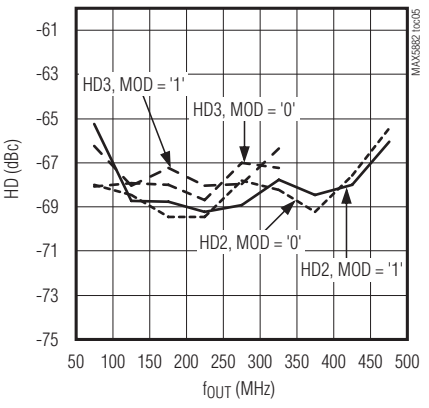
8-CHANNEL 256 QAM ACP vs. OUTPUT FREQUENCY (f_{DAC} = 4.6Gsps, 12MHz TO 18MHz FROM CHANNEL BLOCK EDGE)



8-CHANNEL 256 QAM ACP vs. OUTPUT FREQUENCY (f_{DAC} = 4.6Gsps, 18MHz TO 24MHz FROM CHANNEL BLOCK EDGE)



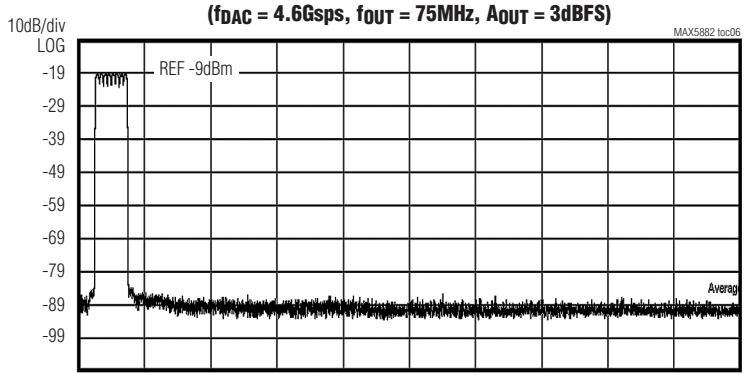
8-CHANNEL 256 QAM HARMONIC DISTORTION vs. OUTPUT FREQUENCY (f_{DAC} = 4.605Gsps)



Typical Operating Characteristics (continued)

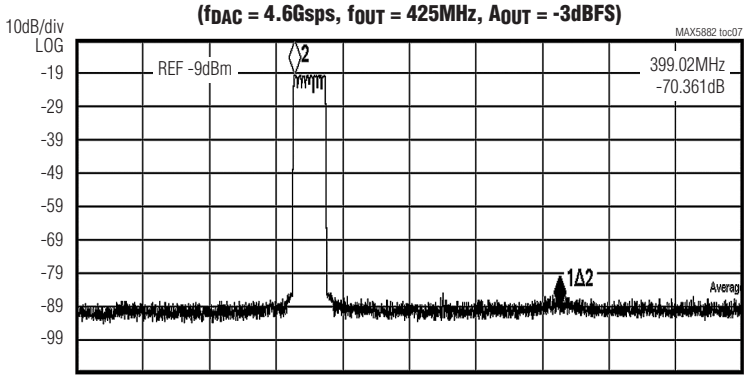
($V_{AVDD3.3}$ = 3.3V, $V_{DD1.8}$ = V_{AVCLK} = 1.8V, R_{SET} = 2kΩ, V_{REFIO} = external 1.25V, V_{MOD} = $V_{DCLKDIV}$ = V_{DLLOFF} = 0V, V_{DELAY} = 1.8V, R_{REFRES} = 500Ω, transformer-coupled differential output, tested at T_J = +60°C, unless otherwise noted.)

8-CHANNEL 256 QAM (DOCSIS)
(f_{DAC} = 4.6Gsps, f_{OUT} = 75MHz, A_{OUT} = 3dBFS)



CENTER = 525MHz, SPAN = 1GHz, RBW = 1MHz,
VBW = 1MHz, SWEEP = 5s

8-CHANNEL 256 QAM (DOCSIS)
(f_{DAC} = 4.6Gsps, f_{OUT} = 425MHz, A_{OUT} = -3dBFS)

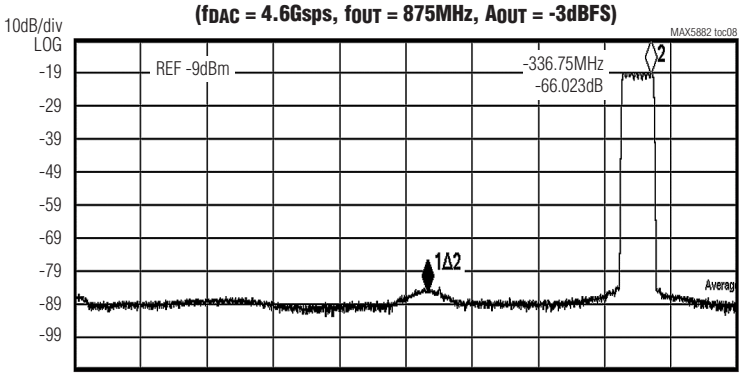


CENTER = 525MHz, SPAN = 1GHz, RBW = 1MHz,
VBW = 1MHz, SWEEP = 6s

Typical Operating Characteristics (continued)

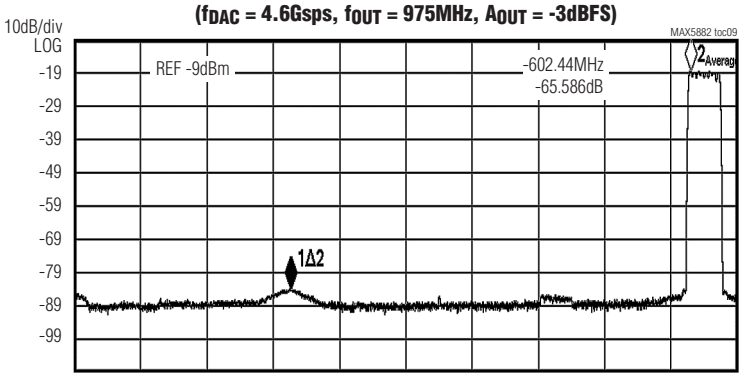
($V_{AVDD3.3}$ = 3.3V, $V_{DD1.8}$ = V_{AVCLK} = 1.8V, R_{SET} = 2kΩ, V_{REFIO} = external 1.25V, V_{MOD} = $V_{DCLKDIV}$ = V_{DLLOFF} = 0V, V_{DELAY} = 1.8V, R_{REFRES} = 500Ω, transformer-coupled differential output, tested at T_J = +60°C, unless otherwise noted.)

8-CHANNEL 256 QAM (DOCSIS)
(f_{DAC} = 4.6Gsps, f_{OUT} = 875MHz, A_{OUT} = -3dBFS)



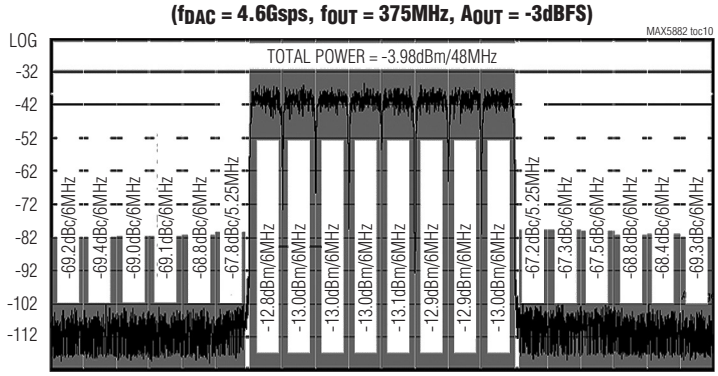
CENTER = 525MHz, SPAN = 1GHz, RBW = 2MHz,
VBW = 8MHz, SWEEP = 6s

8-CHANNEL 256 QAM (DOCSIS)
(f_{DAC} = 4.6Gsps, f_{OUT} = 975MHz, A_{OUT} = -3dBFS)



CENTER = 525MHz, SPAN = 1GHz, RBW = 2MHz,
VBW = 8MHz, SWEEP = 6s

8-CHANNEL 256 QAM (DOCSIS) ACP
(f_{DAC} = 4.6Gsps, f_{OUT} = 375MHz, A_{OUT} = -3dBFS)

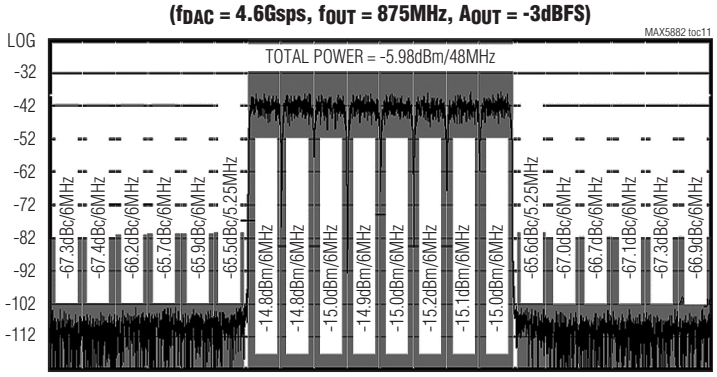


CENTER = 375MHz, SPAN = 120MHz, RBW = 10kHz,
VBW = 100kHz, SWEEP = 5s

Typical Operating Characteristics (continued)

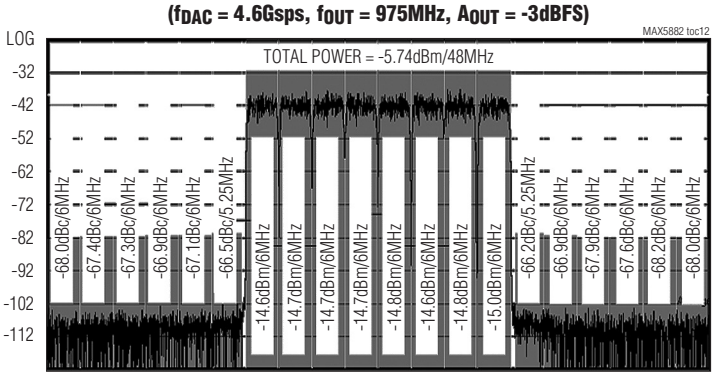
($V_{AVDD3.3}$ = 3.3V, $V_{DD1.8}$ = V_{AVCLK} = 1.8V, R_{SET} = 2kΩ, V_{REFIO} = external 1.25V, V_{MOD} = $V_{DCLKDIV}$ = V_{DLLOFF} = 0V, V_{DELAY} = 1.8V, R_{REFRES} = 500Ω, transformer-coupled differential output, tested at T_J = +60°C, unless otherwise noted.)

8-CHANNEL 256 QAM (DOCSIS) ACP
(f_{DAC} = 4.6Gsps, f_{OUT} = 875MHz, A_{OUT} = -3dBFS)



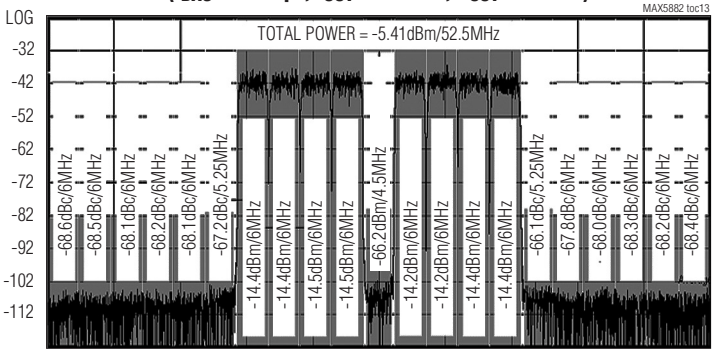
CENTER = 874.9MHz, SPAN = 120MHz, RBW = 10kHz,
VBW = 100kHz, SWEEP = 6s

8-CHANNEL 256 QAM (DOCSIS) ACP
(f_{DAC} = 4.6Gsps, f_{OUT} = 975MHz, A_{OUT} = -3dBFS)



CENTER = 975MHz, SPAN = 120MHz, RBW = 10kHz,
VBW = 100kHz, SWEEP = 5s

8-CHANNEL 256 QAM (DOCSIS) ACP
(f_{DAC} = 4.6Gsps, f_{OUT} = 860MHz, A_{OUT} = -3dBFS)

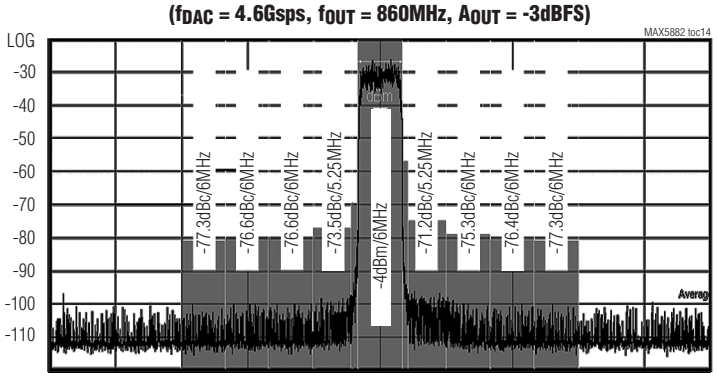


CENTER = 860MHz, SPAN = 126MHz, RBW = 10kHz,
VBW = 100kHz, SWEEP = 5s

Typical Operating Characteristics (continued)

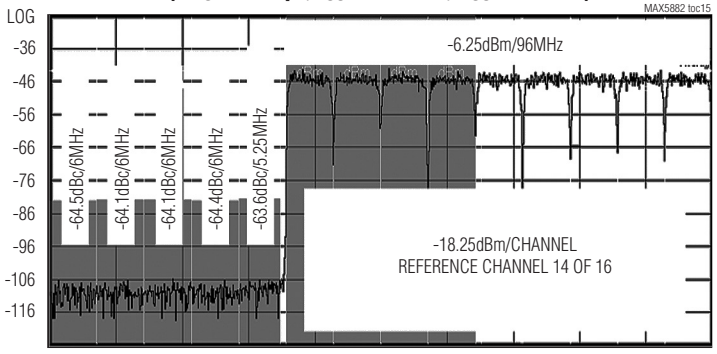
($V_{AVDD3.3}$ = 3.3V, $V_{DD1.8}$ = V_{AVCLK} = 1.8V, R_{SET} = 2kΩ, V_{REFIO} = external 1.25V, V_{MOD} = $V_{DCLKDIV}$ = V_{DLLOFF} = 0V, V_{DELAY} = 1.8V, R_{REFRES} = 500Ω, transformer-coupled differential output, tested at T_J = +60°C, unless otherwise noted.)

SINGLE-CHANNEL 256 QAM (DOCSIS) ACP
(f_{DAC} = 4.6Gsps, f_{OUT} = 860MHz, A_{OUT} = -3dBFS)



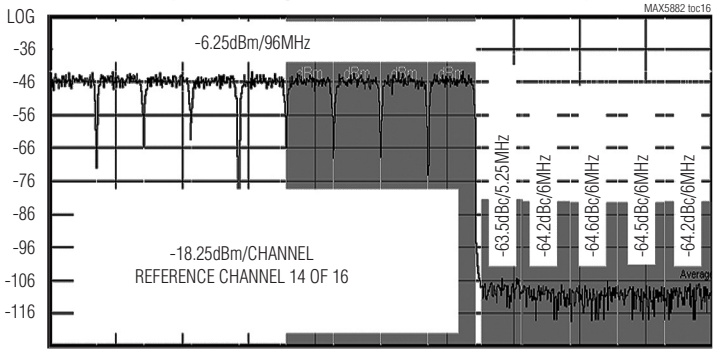
CENTER = 860MHz, SPAN = 90MHz, RBW = 10kHz,
VBW = 100kHz, SWEEP = 4.445s

16-CHANNEL 256 QAM (DOCSIS) ACP LOWER ADJACENT CHANNELS
(f_{DAC} = 4.6Gsps, f_{OUT} = 860MHz, A_{OUT} = -3dBFS)



CENTER = 824MHz, SPAN = 84MHz, RBW = 10kHz,
VBW = 100kHz, SWEEP = 5s

16-CHANNEL 256 QAM (DOCSIS) ACP UPPER ADJACENT CHANNELS
(f_{DAC} = 4.6Gsps, f_{OUT} = 860MHz, A_{OUT} = -3dBFS)

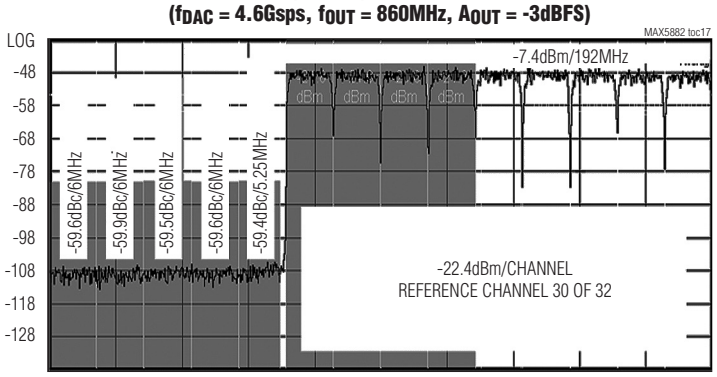


CENTER = 896MHz, SPAN = 84MHz, RBW = 10kHz,
VBW = 100kHz, SWEEP = 5s

Typical Operating Characteristics (continued)

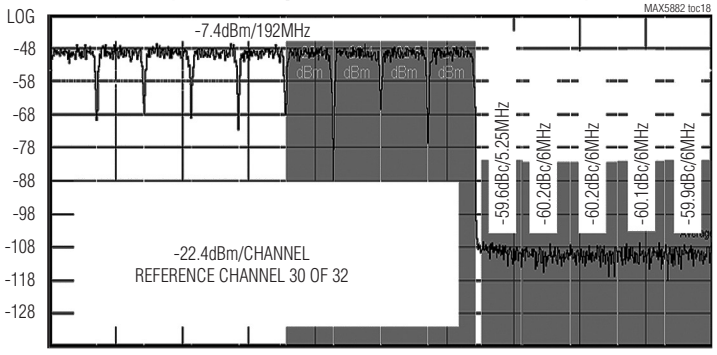
($V_{AVDD3.3}$ = 3.3V, $V_{DD1.8}$ = V_{AVCLK} = 1.8V, R_{SET} = 2kΩ, V_{REFIO} = external 1.25V, V_{MOD} = $V_{DCLKDIV}$ = V_{DLLOFF} = 0V, V_{DELAY} = 1.8V, R_{REFRES} = 500Ω, transformer-coupled differential output, tested at T_J = +60°C, unless otherwise noted.)

32-CHANNEL 256 QAM (DOCSIS) ACP LOWER ADJACENT CHANNELS
(f_{DAC} = 4.6Gsps, f_{OUT} = 860MHz, A_{OUT} = -3dBFS)



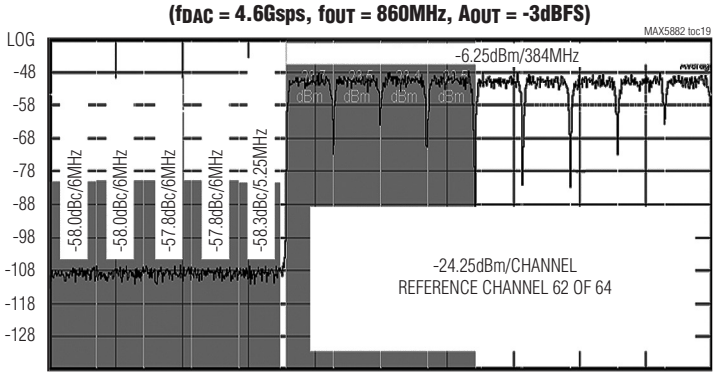
CENTER = 716MHz, SPAN = 84MHz, RBW = 10kHz,
VBW = 100kHz, SWEEP = 5s

32-CHANNEL 256 QAM (DOCSIS) ACP UPPER ADJACENT CHANNELS
(f_{DAC} = 4.6Gsps, f_{OUT} = 860MHz, A_{OUT} = -3dBFS)



CENTER = 884MHz, SPAN = 84MHz, RBW = 10kHz,
VBW = 100kHz, SWEEP = 5s

64-CHANNEL 256 QAM (DOCSIS) ACP LOWER ADJACENT CHANNELS
(f_{DAC} = 4.6Gsps, f_{OUT} = 860MHz, A_{OUT} = -3dBFS)

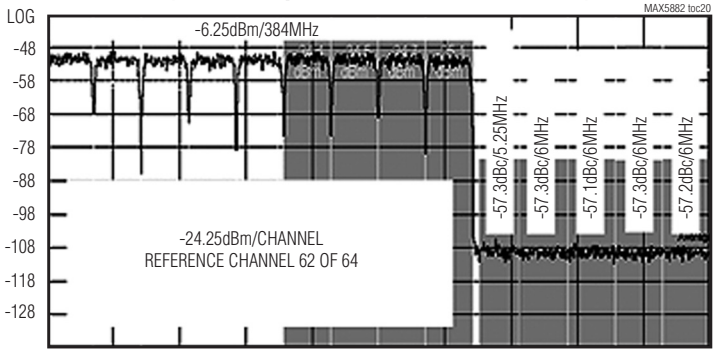


CENTER = 620MHz, SPAN = 72MHz, RBW = 30kHz,
VBW = 300kHz, SWEEP = 5s

Typical Operating Characteristics (continued)

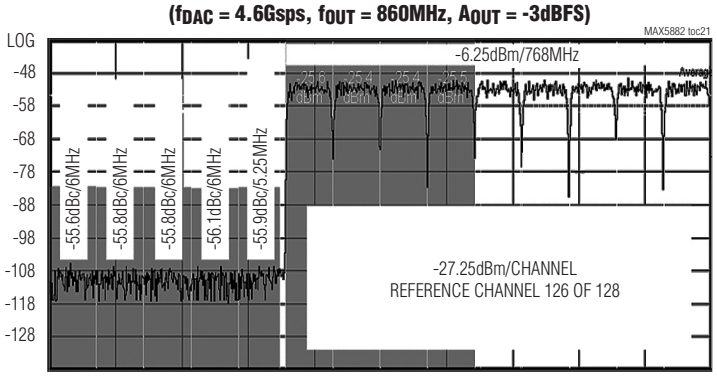
($V_{AVDD3.3}$ = 3.3V, $V_{DD1.8}$ = V_{AVCLK} = 1.8V, R_{SET} = 2kΩ, V_{REFIO} = external 1.25V, V_{MOD} = $V_{DCLKDIV}$ = V_{DLLOFF} = 0V, V_{DELAY} = 1.8V, R_{REFRES} = 500Ω, transformer-coupled differential output, tested at T_J = +60°C, unless otherwise noted.)

64-CHANNEL 256 QAM (DOCSIS) ACP UPPER ADJACENT CHANNELS (f_{DAC} = 4.6Gsps, f_{OUT} = 860MHz, A_{OUT} = -3dBFS)



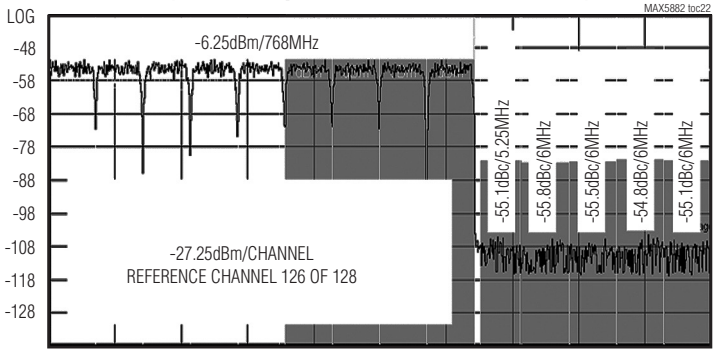
CENTER = 980MHz, SPAN = 84MHz, RBW = 10kHz,
VBW = 100kHz, SWEEP = 5s

128-CHANNEL 256 QAM (DOCSIS) ACP LOWER ADJACENT CHANNELS (f_{DAC} = 4.6Gsps, f_{OUT} = 860MHz, A_{OUT} = -3dBFS)



CENTER = 128MHz, SPAN = 84MHz, RBW = 10kHz,
VBW = 100kHz, SWEEP = 5s

128-CHANNEL 256 QAM (DOCSIS) ACP UPPER ADJACENT CHANNELS (f_{DAC} = 4.6Gsps, f_{OUT} = 860MHz, A_{OUT} = -3dBFS)

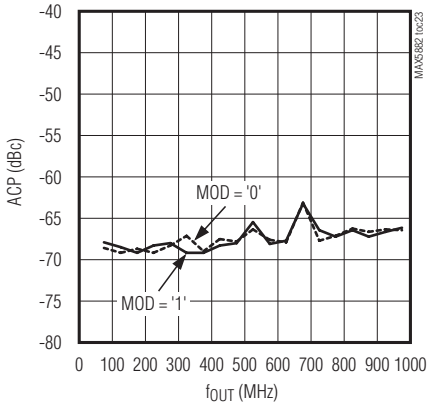


CENTER = 872MHz, SPAN = 84MHz, RBW = 10kHz,
VBW = 100kHz, SWEEP = 5s

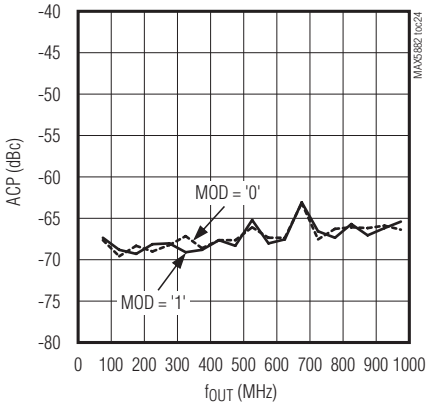
Typical Operating Characteristics (continued)

($V_{AVDD3.3}$ = 3.3V, $V_{DD1.8}$ = V_{AVCLK} = 1.8V, R_{SET} = 2kΩ, V_{REFIO} = external 1.25V, V_{MOD} = $V_{DCLKDIV}$ = V_{DLLOFF} = 0V, V_{DELAY} = 1.8V, R_{REFRES} = 500Ω, transformer-coupled differential output, tested at T_J = +60°C, unless otherwise noted.)

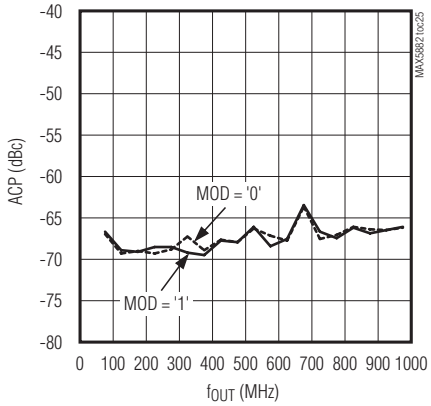
8-CHANNEL 256 QAM ACP vs. OUTPUT FREQUENCY (f_{DAC} = 4.096Gsps, 750kHz TO 6MHz FROM CHANNEL BLOCK EDGE)



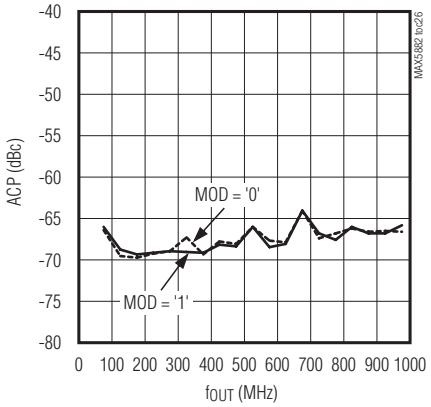
8-CHANNEL 256 QAM ACP vs. OUTPUT FREQUENCY (f_{DAC} = 4.096Gsps, 6MHz TO 12MHz FROM CHANNEL BLOCK EDGE)



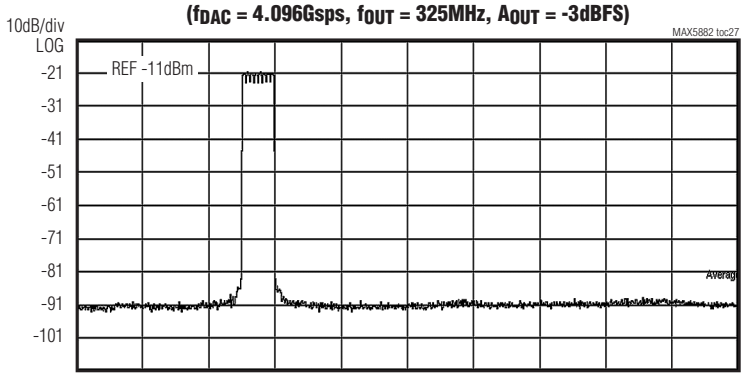
8-CHANNEL 256 QAM ACP vs. OUTPUT FREQUENCY (f_{DAC} = 4.096Gsps, 12MHz TO 18MHz FROM CHANNEL BLOCK EDGE)



8-CHANNEL 256 QAM ACP vs. OUTPUT FREQUENCY (f_{DAC} = 4.096Gsps, 18MHz TO 24MHz FROM CHANNEL BLOCK EDGE)



8-CHANNEL 256 QAM (DOCSIS) (f_{DAC} = 4.096Gsps, f_{OUT} = 325MHz, A_{OUT} = -3dBFS)

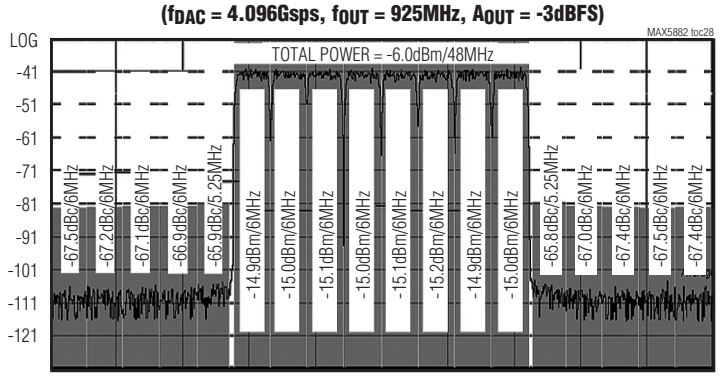


CENTER = 525MHz, SPAN = 1GHz, RBW = 1MHz,
VBW = 1MHz, SWEEP = 5s

Typical Operating Characteristics (continued)

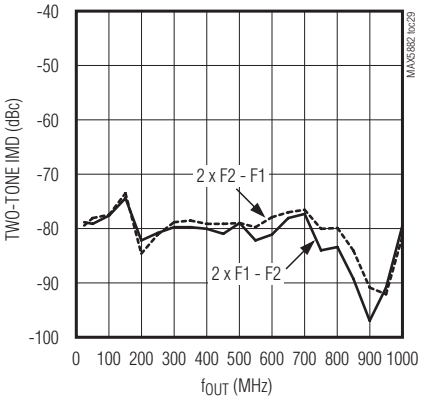
($V_{AVDD3.3}$ = 3.3V, $V_{DD1.8}$ = V_{AVCLK} = 1.8V, R_{SET} = 2kΩ, V_{REFIO} = external 1.25V, V_{MOD} = $V_{DCLKDIV}$ = V_{DLLOFF} = 0V, V_{DELAY} = 1.8V, R_{REFRES} = 500Ω, transformer-coupled differential output, tested at T_J = +60°C, unless otherwise noted.)

8-CHANNEL 256 QAM (DOCSIS) ACP
(f_{DAC} = 4.096Gsps, f_{OUT} = 925MHz, A_{OUT} = -3dBFS)

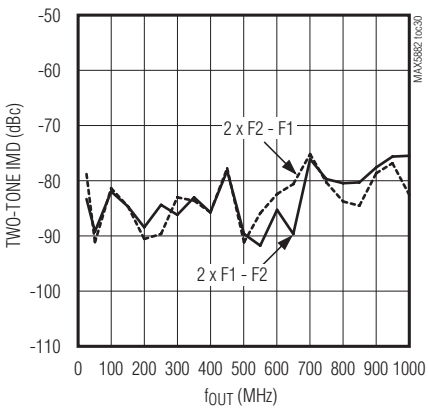


CENTER = 900MHz, SPAN = 108MHz, RBW = 10kHz,
VBW = 100kHz, SWEEP = 5s

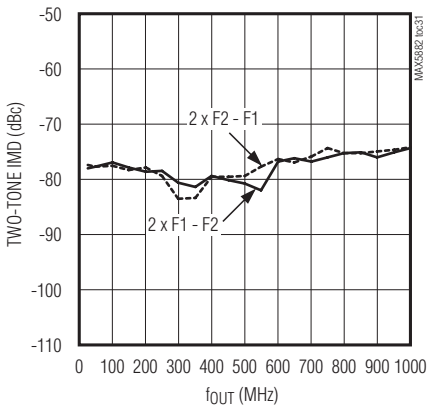
TWO-TONE IMD vs. OUTPUT FREQUENCY
(f_{DAC} = 4.6Gsps, A_{OUT} = -12dBFS PER TONE, 6MHz CARRIER SPACING)



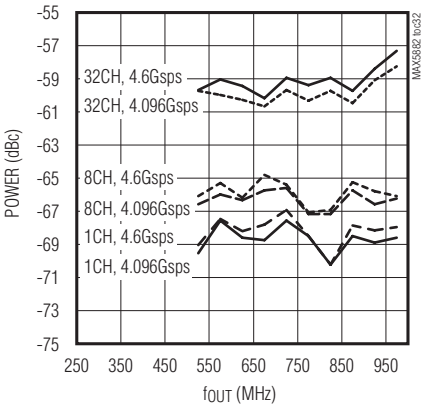
TWO-TONE IMD vs. OUTPUT FREQUENCY
(f_{DAC} = 4.096Gsps, A_{OUT} = -12dBFS PER TONE, 6MHz CARRIER SPACING)



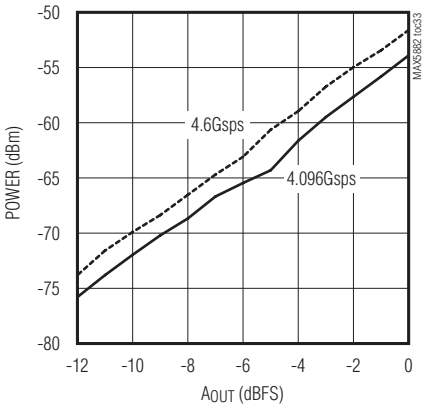
TWO-TONE IMD vs. OUTPUT FREQUENCY
(f_{DAC} = 2.4Gsps, A_{OUT} = -12dBFS PER TONE, 6MHz CARRIER SPACING)



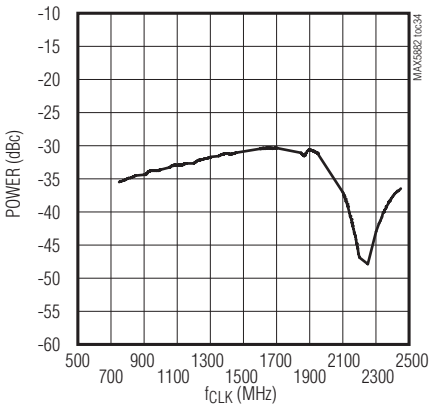
256 QAM f_{CLK} - 2 x f_{OUT} IMAGE vs. OUTPUT FREQUENCY (HIGHEST RELATIVE IMAGE POWER)



CW f_{CLK} - 2 x f_{OUT} IMAGE vs. OUTPUT AMPLITUDE (f_{OUT} = 900MHz)



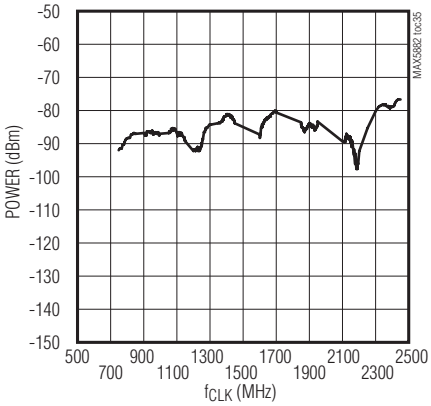
CLOCK FEEDTHROUGH vs. CLOCK FREQUENCY (f_{OUT} = 100MHz, A_{OUT} = -0.1dBFS)



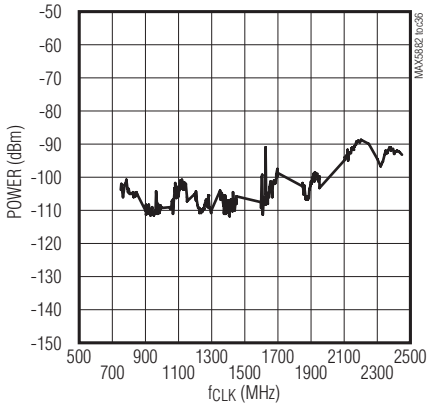
Typical Operating Characteristics (continued)

($V_{AVDD3.3}$ = 3.3V, $V_{DD1.8}$ = V_{AVCLK} = 1.8V, R_{SET} = 2kΩ, V_{REFIO} = external 1.25V, V_{MOD} = $V_{DCLKDIV}$ = V_{DLLOFF} = 0V, V_{DELAY} = 1.8V, R_{REFRES} = 500Ω, transformer-coupled differential output, tested at T_J = +60°C, unless otherwise noted.)

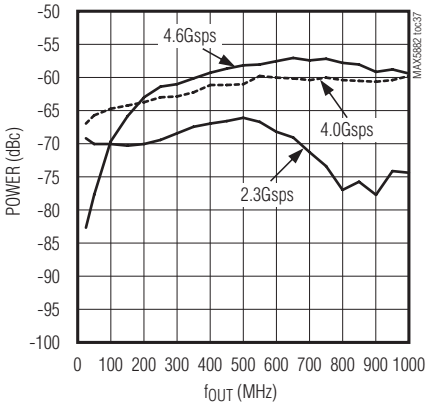
CLOCK/2 FEEDTHROUGH vs. CLOCK FREQUENCY (f_{OUT} = 100MHz, A_{OUT} = -0.1dBFS)



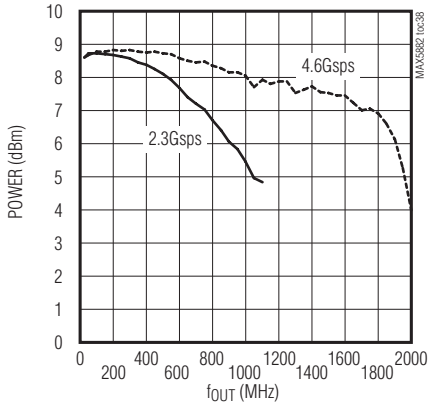
CLOCK/4 FEEDTHROUGH vs. CLOCK FREQUENCY (f_{OUT} = 100MHz, A_{OUT} = -0.1dBFS)



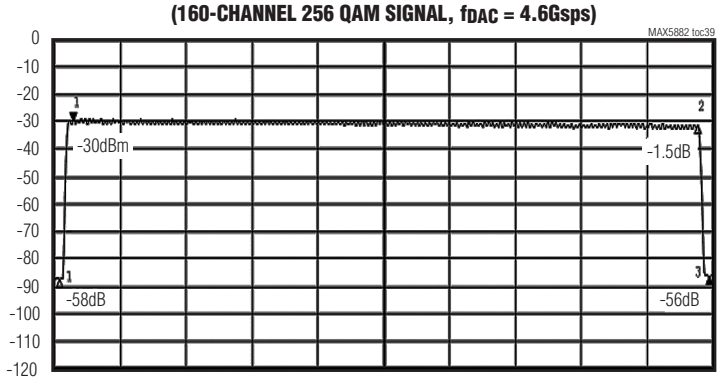
CW f_{CLK} - 2 x f_{OUT} IMAGE vs. OUTPUT FREQUENCY (A_{OUT} = -0.1dBFS)



CW OUTPUT POWER vs. OUTPUT FREQUENCY (A_{OUT} = -0.1dBFS)



OUTPUT POWER vs. OUTPUT FREQUENCY (160-CHANNEL 256 QAM SIGNAL, f_{DAC} = 4.6Gsps)

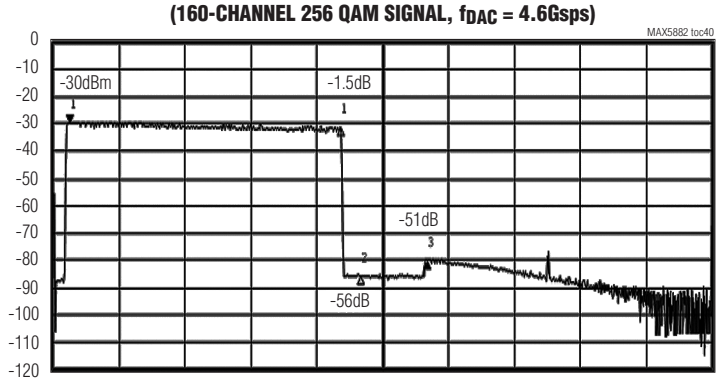


CENTER = 527MHz, SPAN = 1GHz, RBW = 3MHz,
VBW = 100kHz, SWEEP = 5.6s

Typical Operating Characteristics (continued)

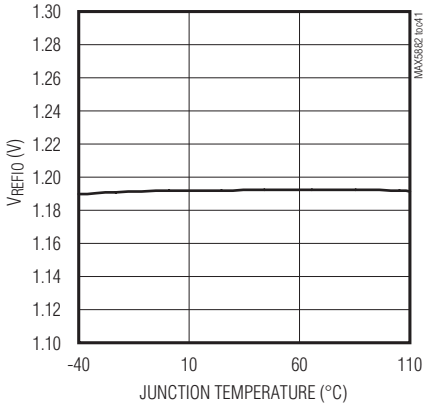
($V_{AVDD3.3}$ = 3.3V, $V_{DD1.8}$ = V_{AVCLK} = 1.8V, R_{SET} = 2kΩ, V_{REFIO} = external 1.25V, V_{MOD} = $V_{DCLKDIV}$ = V_{DLLOFF} = 0V, V_{DELAY} = 1.8V, R_{REFRES} = 500Ω, transformer-coupled differential output, tested at T_J = +60°C, unless otherwise noted.)

OUTPUT POWER vs. OUTPUT FREQUENCY (160-CHANNEL 256 QAM SIGNAL, f_{DAC} = 4.6Gsps)

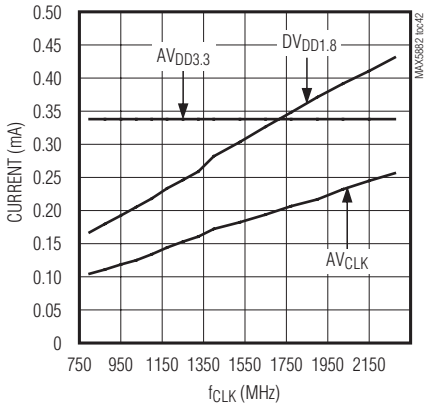


CENTER = 1.15GHz, SPAN = 2.3GHz, RBW = 3MHz, VBW = 100kHz, SWEEP = 5.6s

INTERNAL REFERENCE (REFIO) VOLTAGE vs. JUNCTION TEMPERATURE



SUPPLY CURRENT vs. CLK FREQUENCY (f_{OUT} = 100MHz, A_{OUT} = -0.1dBFS, 80mA FSR)



Ball Configuration

TOP VIEW

MAX5882

CREF A1	DACREF A2	REFIO A3	FSADJ A4	REFRES A5	$AV_{DD3.3}$ A6	GND A7	$AV_{DD3.3}$ A8	$AV_{DD3.3}$ A9	OUTN A10	OUTP A11	$AV_{DD3.3}$ A12	$AV_{DD3.3}$ A13	GND A14	GND A15	GND A16
GND B1	GND B2	GND B3	GND B4	GND B5	GND B6	GND B7	$AV_{DD3.3}$ B8	$AV_{DD3.3}$ B9	OUTN B10	OUTP B11	$AV_{DD3.3}$ B12	$AV_{DD3.3}$ B13	GND B14	AV_{CLK} B15	AV_{CLK} B16
$V_{DD1.8}$ C1	$V_{DD1.8}$ C2	$V_{DD1.8}$ C3	$V_{DD1.8}$ C4	$V_{DD1.8}$ C5	GND C6	GND C7	GND C8	GND C9	GND C10	GND C11	GND C12	GND C13	GND C14	AV_{CLK} C15	CLKN C16
SE D1	SO/LOCK D2	PERR D3	GND D4	DELAY D5	GND D6	GND D7	GND D8	GND D9	GND D10	GND D11	GND D12	GND D13	GND D14	AV_{CLK} D15	CLKP D16
GND E1	DCLKDIV E2	GND E3	DLLOFF E4	MOD E5	GND E6	GND E7	GND E8	GND E9	GND E10	GND E11	GND E12	GND E13	GND E14	AV_{CLK} E15	AV_{CLK} E16
GND F1	GND F2	GND F3	GND F4	GND F5	GND F6	GND F7	GND F8	GND F9	GND F10	GND F11	GND F12	GND F13	GND F14	GND F15	GND F16
$V_{DD1.8}$ G1	$V_{DD1.8}$ G2	$V_{DD1.8}$ G3	$V_{DD1.8}$ G4	GND G5	GND G6	GND G7	GND G8	GND G9	GND G10	GND G11	GND G12	GND G13	GND G14	GND G15	GND G16
DAP13 H1	DAN13 H2	DAP12 H3	DAN12 H4	DAP11 H5	DAN11 H6	DAP10 H7	DAN10 H8	GND H9	GND H10	GND H11	GND H12	$V_{DD1.8}$ H13	$V_{DD1.8}$ H14	$V_{DD1.8}$ H15	$V_{DD1.8}$ H16
DAP9 J1	DAN9 J2	DAP8 J3	DAN8 J4	DAP7 J5	DAN7 J6	DAP6 J7	DAN6 J8	DDP13 J9	DDN13 J10	DDP12 J11	DDN12 J12	DDP11 J13	DDN11 J14	DDP10 J15	DDN10 J16
DAP5 K1	DAN5 K2	DAP4 K3	DAN4 K4	DAP3 K5	DAN3 K6	DAP2 K7	DAN2 K8	DDP9 K9	DDN9 K10	DDP8 K11	DDN8 K12	DDP7 K13	DDN7 K14	DDP6 K15	DDN6 K16
DAP1 L1	DAN1 L2	DAP0 L3	DAN0 L4	GND L5	GND L6	GND L7	GND L8	DDP5 L9	DDN5 L10	DDP4 L11	DDN4 L12	DDP3 L13	DDN3 L14	DDP2 L15	DDN2 L16
DBP13 M1	DBN13 M2	DBP12 M3	DBN12 M4	DBP11 M5	DBN11 M6	DBP10 M7	DBN10 M8	DDP1 M9	DDN1 M10	DDP0 M11	DDN0 M12	GND M13	GND M14	GND M15	GND M16
DBP9 N1	DBN9 N2	DBP8 N3	DBN8 N4	DBP7 N5	DBN7 N6	DBP6 N7	DBN6 N8	DCP13 N9	DCN13 N10	DCP12 N11	DCN12 N12	DCP11 N13	DCN11 N14	DCP10 N15	DCN10 N16
DBP5 P1	DBN5 P2	DBP4 P3	DBN4 P4	DBP3 P5	DBN3 P6	DBP2 P7	DBN2 P8	DCP9 P9	DCN9 P10	DCP8 P11	DCN8 P12	DCP7 P13	DCN7 P14	DCP6 P15	DCN6 P16
DBP1 R1	DBN1 R2	DBP0 R3	DBN0 R4	PARP R5	PARN R6	SYNCP R7	SYNCN R8	DCP5 R9	DCN5 R10	DCP4 R11	DCN4 R12	DCP3 R13	DCN3 R14	DCP2 R15	DCN2 R16
GND T1	GND T2	GND T3	GND T4	DATACLKP T5	DATACLKN T6	XORP T7	XORN T8	DCP1 T9	DCN1 T10	DCP0 T11	DCN0 T12	GND T13	GND T14	GND T15	GND T16

Ball Description

BALL	NAME	FUNCTION
A1	CREF	Noise Bypass Pin. A 1µF capacitor between CREF and DACREF band limits the phase noise of the device.
A2	DACREF	Current-Set Resistor Return Path. For 80mA full-scale output current, connect a 2kΩ resistor between FSADJ and DACREF. DACREF is internally connected to GND. **Do not connect DACREF to external ground.**

Ball Description (continued)

BALL	NAME	FUNCTION
A3	REFIO	Reference Input/Output. Output pin for the internal 1.2V bandgap reference. REFIO has a 10kΩ series resistance and can be driven using an external reference. Connect a 1µF capacitor between REFIO and DACREF.
A4	FSADJ	Full-Scale Adjust Input. Sets the full-scale output current of the DAC. For 80mA full-scale output current, connect a 2kΩ resistor between FSADJ and DACREF.
A5	REFRES	Connect a 500Ω resistor between REFRES and $AV_{DD3.3}$.
A6, A8, A9, A12, A13, B8, B9, B12, B13	$AV_{DD3.3}$	Analog 3.3V Supply Voltage. Connect 47nF bypass capacitors between each $AV_{DD3.3}$ pin and GND.
A7, A14, A15, A16, B1–B7, B14, C6–C14, D4, D6–D14, E1, E3, E6–E14, F1–F16, G5–G16, H9–H12, L5–L8, M13–M16, T1–T4, T13–T16	GND	Analog Ground. Connect to ground plane with minimum inductance.
A10, B10	OUTN	Negative Terminal of Differential DAC Output. OUTN has an internal 25Ω resistor to $AV_{DD3.3}$.
A11, B11	OUTP	Positive Terminal of Differential DAC Output. OUTP has an internal 25Ω resistor to $AV_{DD3.3}$.
B15, B16, C15, D15, E15, E16	AV_{CLK}	Clock 1.8V Supply Voltage. Connect 47nF bypass capacitors between AV_{CLK} and GND.
C1–C5, G1–G4, H13–H16	$V_{DD1.8}$	1.8V Supply Voltage. Connect 47nF bypass capacitors between each $V_{DD1.8}$ pin and GND.
D16	CLKP	Positive Converter Clock Input. There is an internal 100Ω termination resistor between CLKP and CLKN.
C16	CLKN	Negative Converter Clock Input. There is an internal 100Ω termination resistor between CLKP and CLKN.
D1	SE	Scan Enable. 1.8V CMOS logic input. During normal operation, SE should be connected to GND, and this makes the SO/LOCK pin a DLL LOCK indicator output. When SE is high (1.8V), the parallel input register is configured as a shift register, allowing the contents of the input register to be shifted out on SO/LOCK.
D2	SO/LOCK	1.8V CMOS Logic Output SE = high: SO/LOCK is a scan data output SE = low: SO/LOCK is a DLL locking indicator output, and logic high indicates DLL is locked
D3	PERR	1.8V CMOS Logic Level Parity Error Output. When a parity error is detected in the DAC input data, this pin is set high for a minimum of 48 LVDS data periods. This can be used to provide failure monitoring for the system. Note that this pin can pulse high when power is initially applied and before the DLL is locked.

Ball Description (continued)

BALL	NAME	FUNCTION
D5	DELAY	Data Clock Mode Control DELAY = 0: No clock delay when DLLOFF = 1 DELAY = 1: One f_{CLK} period delay added to DATACLKP/DATACLKN when DLLOFF = 1 DLLOFF ≠ 1: DELAY is a 4-level input pin used along with DLLOFF (see Table 1 for details) DELAY is a 1.8V, 3.3V tolerant, 4-level logic input
E2	DCLKDIV	Data Clock Divider Mode Input DCLKDIV = 1: DATACLKP/DATACKLN is $f_{DAC}/8$ DCLKDIV = 0: DATACLKP/DATACKLN is $f_{DAC}/4$ DCLKDIV is a 1.8V, 3.3V tolerant, CMOS input with an internal pulldown resistor
E4	DLLOFF	Data Clock Mode Control DLLOFF ≠ 1: DLL is enabled as a 4-level logic input pin used along with the DELAY pin (see Table 1 for details) DLLOFF = 1: DLL is disabled DLLOFF is a 1.8V, 3.3V tolerant, 4-level logic input
E5	MOD	$f_{DAC}/2$ (f_{CLK}) Modulation Control Input MOD = 0: Modulation off MOD = 1: Modulation on MOD is a 1.8V, 3.3V tolerant, CMOS input with an internal pulldown resistor
H1, H3, H5, H7, J1, J3, J5, J7, K1, K3, K5, K7, L1, L3	DAP[13:0]	Positive Terminals of the A-Channel LVDS Data Inputs (Offset Binary Format). DAP13 is the MSB.
H2, H4, H6, H8, J2, J4, J6, J8, K2, K4, K6, K8, L2, L4	DAN[13:0]	Negative Terminals of the A-Channel LVDS Data Inputs
M1, M3, M5, M7, N1, N3, N5, N7, P1, P3, P5, P7, R1, R3	DBP[13:0]	Positive Terminals of the B-Channel LVDS Data Inputs (Offset Binary Format). DBP13 is the MSB.
M2, M4, M6, M8, N2, N4, N6, N8, P2, P4, P6, P8, R2, R4	DBN[13:0]	Negative Terminals of the B-Channel LVDS Data Inputs
N9, N11, N13, N15, P9, P11, P13, P15, R9, R11, R13, R15, T9, T11	DCP[13:0]	Positive Terminals of the C-Channel LVDS Data Inputs (Offset Binary Format). DCP13 is the MSB.

Ball Description (continued)

BALL	NAME	FUNCTION
N10, N12, N14, N16, P10, P12, P14, P16, R10, R12, R14, R16, T10, T12	DCN[13:0]	Negative Terminals of the C-Channel LVDS Data Inputs
J9, J11, J13, J15, K9, K11, K13, K15, L9, L11, L13, L15, M9, M11	DDP[13:0]	Positive Terminals of the D-Channel LVDS Data Inputs (Offset Binary Format). DDP13 is the MSB.
J10, J12, J14, J16, K10, K12, K14, K16, L10, L12, L14, L16, M10, M12	DDN[13:0]	Negative Terminals of the D-Channel LVDS Data Inputs
R5	PARP	Positive Terminal of the Parity LVDS Data Input. The parity input data is used internally to provide detection of bit errors between the data source and the DAC and can be used for system monitoring. PARP/PARN should be delayed three DATACLKP/DATACLKN cycles.
R6	PARN	Negative Terminal of parity LVDS Data Input
R7	SYNCP	Positive Terminal of the Synchronization LVDS Data Input. The SYNCP/SYNCN pair should be driven synchronously with the DAC data input pairs and should be a pseudo-random sequence.
R8	SYNCN	Negative Terminal of the Synchronization LVDS Data Input
T5	DATACLKP	Positive Terminal of the LVDS Data Clock Output
T6	DATACLKN	Negative Terminal of the LVDS Data Clock Output
T7	XORP	Positive Terminal of the XOR LVDS Data Input. The A-, B-, C-, and D-channel data bits are logically exclusive ORed by the data on the XORP/XORN pin internally. This function can be used for whitening spurious signals that can be present in the input data. XORP/XORN should be delayed one DATACLKP/DATACLKN cycle. To disable the XOR function, drive a logic 0 into the XORP/XORN input pair.
T8	XORN	Negative Terminal of XOR LVDS Data Input

Detailed Description

The MAX5882 is a high-performance, high-speed, 14-bit current-steering DAC with an integrated 50Ω differential output termination to the 3.3V supply. The DAC operates with a clock rate (f_{CLK}) up to 2.3GHz. The DAC output is updated on each edge of the input clock resulting in a DAC update rate (f_{DAC}) of 4.6Gsps.

The device employs an edge-triggered 4:1 input data multiplexer and a delay-locked loop (DLL) to ease the interface requirements to FPGA or ASIC data sources. The SYNCP/SYNCN signal provides timing information to the internal DLL. The XORP/XORN signal allows whitening the spectral content of the input data stream. The data interface also provides parity validation for verification of the data transmission.

The analog output is a current-steering circuit capable of generating differential full-scale currents in the 10mA to 80mA range. An integrated 1.2V bandgap reference, control amplifier, and user-selectable external resistor determine the data converter's full-scale range.

Internal 25Ω termination resistors on each output, in combination with an external termination, convert the differential current into a voltage. The internal termination resistors are connected to the 3.3V analog supply, $AV_{DD3.3}$.

Reference System

The device supports operation with the on-chip 1.2V bandgap reference or an external reference voltage source. REFIO serves as the input for an external, low-impedance reference source and as the output if the DAC is operating with the internal reference. For stable operation with the internal reference, decouple REFIO to DACREF with a 1µF capacitor. Since REFIO has a 10kΩ series resistance, buffer REFIO with an external amplifier to drive external loads.

The device's reference circuit (Figure 1) employs a control amplifier that regulates the full-scale current I_{OUT} for the differential current outputs of the DAC. The bandwidth of the control amplifier is typically less than 100kHz. The DAC full-scale output current can be calculated as follows:

$$I_{OUT} = 128 \times I_{REF}$$

where I_{REF} is the reference output current ($I_{REF} = V_{REFIO}/R_{SET}$) and I_{OUT} is the full-scale output current of the DAC. With an external reference voltage of 1.25V, R_{SET} is typically set to 2kΩ, resulting in a full-scale current of 80mA and maximum 9dBm output power for a continuous-wave (CW) signal. Generally, the dynamic performance of the DAC improves with increasing full-scale current.

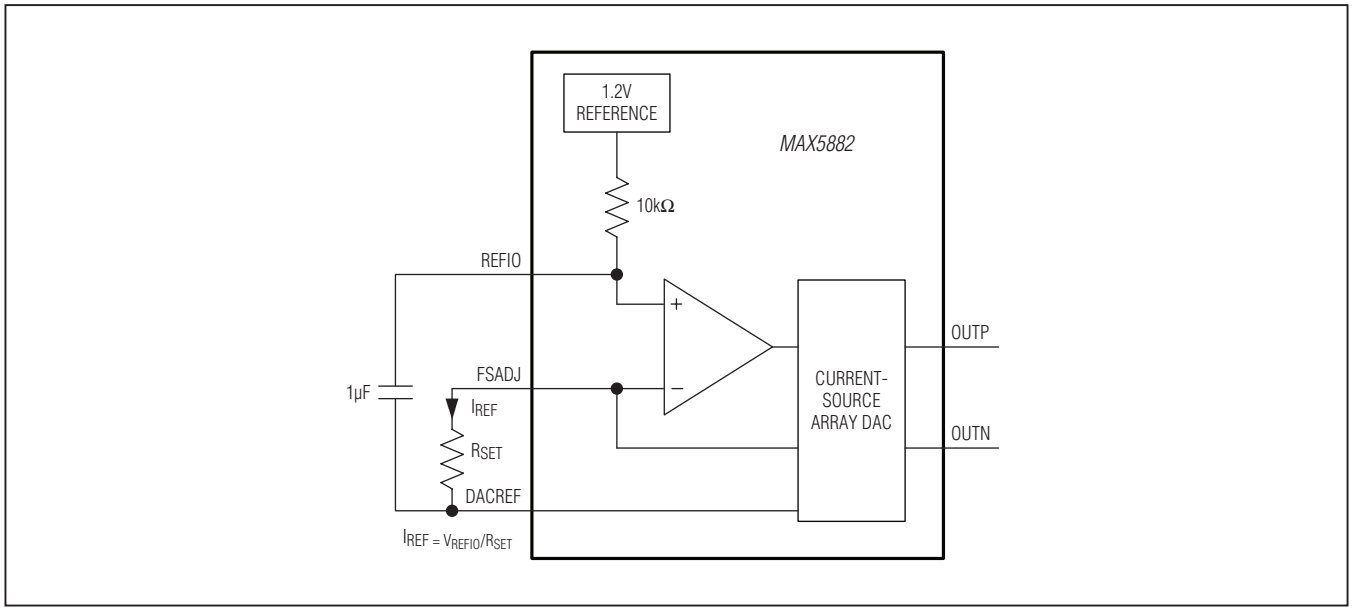


Figure 1. Reference Architecture, Internal Reference Configuration

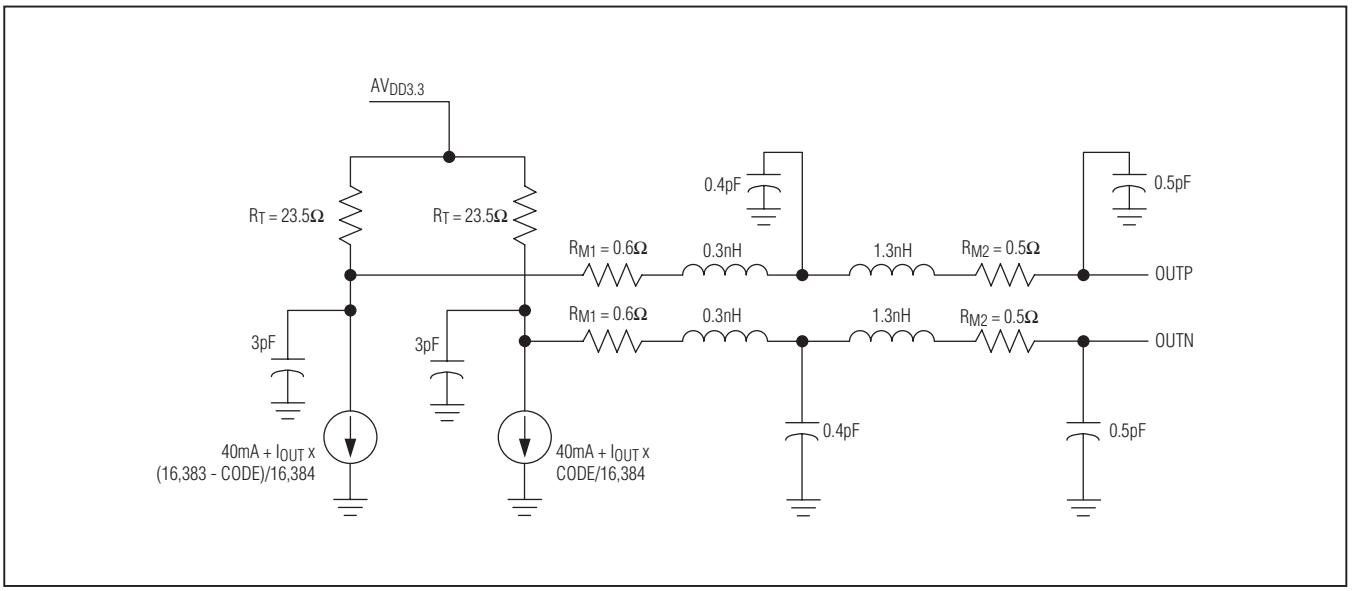


Figure 2. Equivalent Output Circuit

Analog Output

The device is a differential current-steering DAC with built-in output termination resistors. The outputs are terminated to $AV_{DD3.3}$ providing a 50Ω differential output resistance. In addition to the signal current, a constant 40mA current sink is connected to each DAC output. Figure 2 shows an equivalent circuit of the internal output structure of the device. The circuit has some resistive, capacitive, and inductive elements. These elements limit the output bandwidth to 2GHz with a resistive differential 50Ω load.

The outputs need to be pulled up externally to $AV_{DD3.3}$. It is recommended that inductors be used for this purpose, as shown in Figure 3. The use of discrete inductors and capacitors allows for near perfect symmetry in the output circuit layout. An external 50Ω differential load is also required to avoid excessive voltage swings at the DAC output pins.

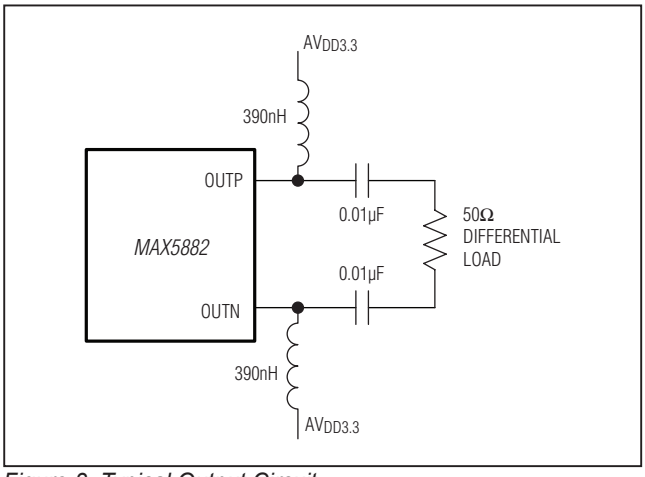


Figure 3. Typical Output Circuit

Clock Inputs

The device has a universal, differential clock input (CLKP, CLKN) operating from a separate power supply (AV_{CLK}) to achieve the best possible jitter performance. The two clock inputs should be driven from a differential clock source. A sine-wave or square-wave signal can be used.

For the highest speeds and highest performance, a sinusoidal clock should be used. At rates where it is feasible, an LVDS or PECL clock can also be utilized. The LVDS or PECL clock must be AC-coupled to the device. Each pin is internally DC-biased to 1/3 the supply voltage, AV_{CLK}. The clock input has an internal 100Ω differential termination resistor. For 50Ω differential termination at high clock frequencies, an additional external termination resistor is required between CLKP and CLKN. The balanced input should be AC-coupled unless the common mode of the clock source is within the specifications for the device's clock input. An example of a well-balanced, single-ended-to-differential application circuit using three baluns is shown in Figure 4.

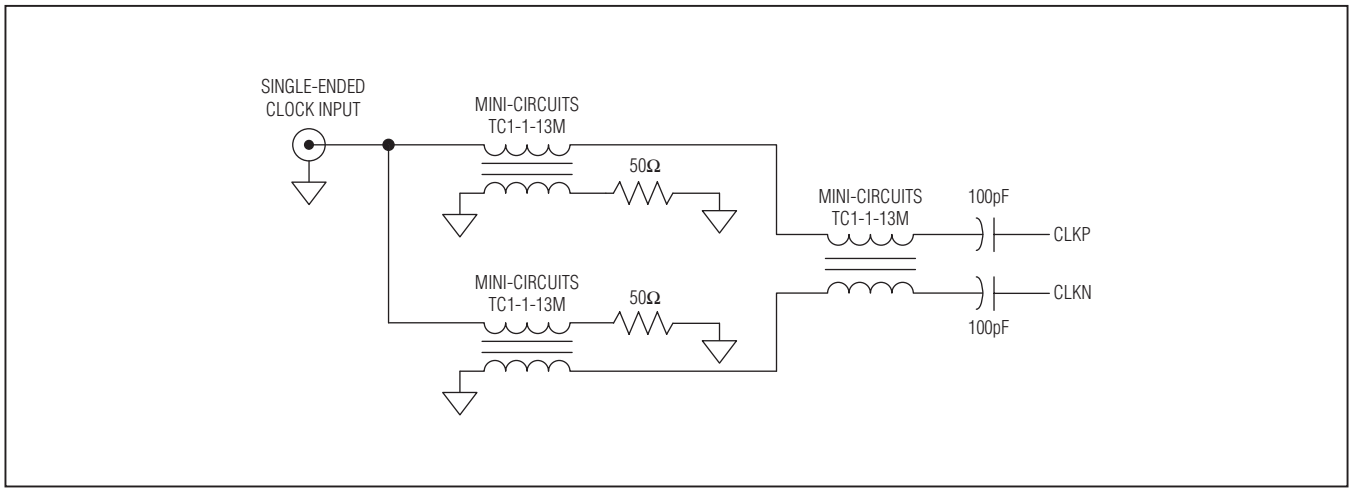


Figure 4. Balanced Clock Interface Circuit

Clock Duty Cycle

The device input clock is supplied at a frequency (f_{CLK}) that is 1/2 the DAC update rate (f_{DAC}). The DAC output updates on both edges of the clock. Deviation from a balanced duty cycle contributes to images in the output spectrum. The magnitude of the images is dependent on the absolute value of the deviation from an ideal 50% duty cycle. These artifacts occur at the following frequencies:

$$f_{IMAGE} = \frac{f_{DAC}}{2} \pm f_{OUT}$$

To minimize the image at $f_{DAC}/2 - f_{OUT}$, the clock duty cycle should be close to 50%. A filtered sine wave has this characteristic. An offset voltage at the input of the clock input buffer causes a duty-cycle change. The duty-cycle change in percent is approximately $(100/\pi) \times V_{OFS}/Ampl$, where V_{OFS} is the offset voltage and Ampl is the peak clock input amplitude. With clock amplitude of 1V peak (differential), an offset of 3.14mV shifts the duty cycle from 50.0% to 50.1/49.9%. Alternatively, the amplitude of the odd and even input data channels can be adjusted to remove the $f_{DAC}/2 - f_{OUT}$ component. For example, the gain of the digital data into channels A and C can be slightly adjusted up or down to remove the $f_{DAC}/2 - f_{OUT}$ image.

Data Inputs

The device supports both single data rate (SDR) and double data rate (DDR) data interfaces. The data inputs (DAP[13:0], DAN[13:0], DBP[13:0], DBN[13:0], DCP[13:0], DCN[13:0], DDP[13:0], DDN[13:0], XORP, XORN, PARP, PARN, SYNCP, and SYNCN) all accept LVDS or differential-HSTL signal levels.

Figure 5 shows a simplified block diagram for a clocking scheme using a Xilinx® FPGA and the device's DLL. The $f_{DAC}/2$ input clock to the device is divided by two to produce a $f_{DAC}/4$ clock that is equal to the input data rate. The $f_{DAC}/4$ clock feeds a variable delay line and an optional divide-by-two block to produce the DATACLK signal that is sent to the FPGA. By adjusting the delay of the DATACLK signal, the phase of the input data can be adjusted. The device's DLL is used to lock the phase of the incoming data to the internal clock that is used to latch the data. The incoming SYNC signal is used to close the DLL loop and is a replica of the other data lines, but with a data pattern guaranteed to have active data.

The DCM_ADV DLL loop inside the Virtex®-5 FPGA should not be used and is not needed for clocking the output data and OSERDES to the DAC. However, the DCM_ADV can be used to generate internal clocks, locked to the DATACLK, for any data FIFO and internal logic. The buffered DATACLK without the DCM is used to clock the OSERDES. One OSERDES, with its data wired in such a manner as to reduce its function to that of a simple buffer, is used to match the timing of the SYNCP/SYNCN signal to the FPGA output data. This adds between 1ns and 3ns delay on SYNC referenced to the device's DATACLKP/DATACLKN output.

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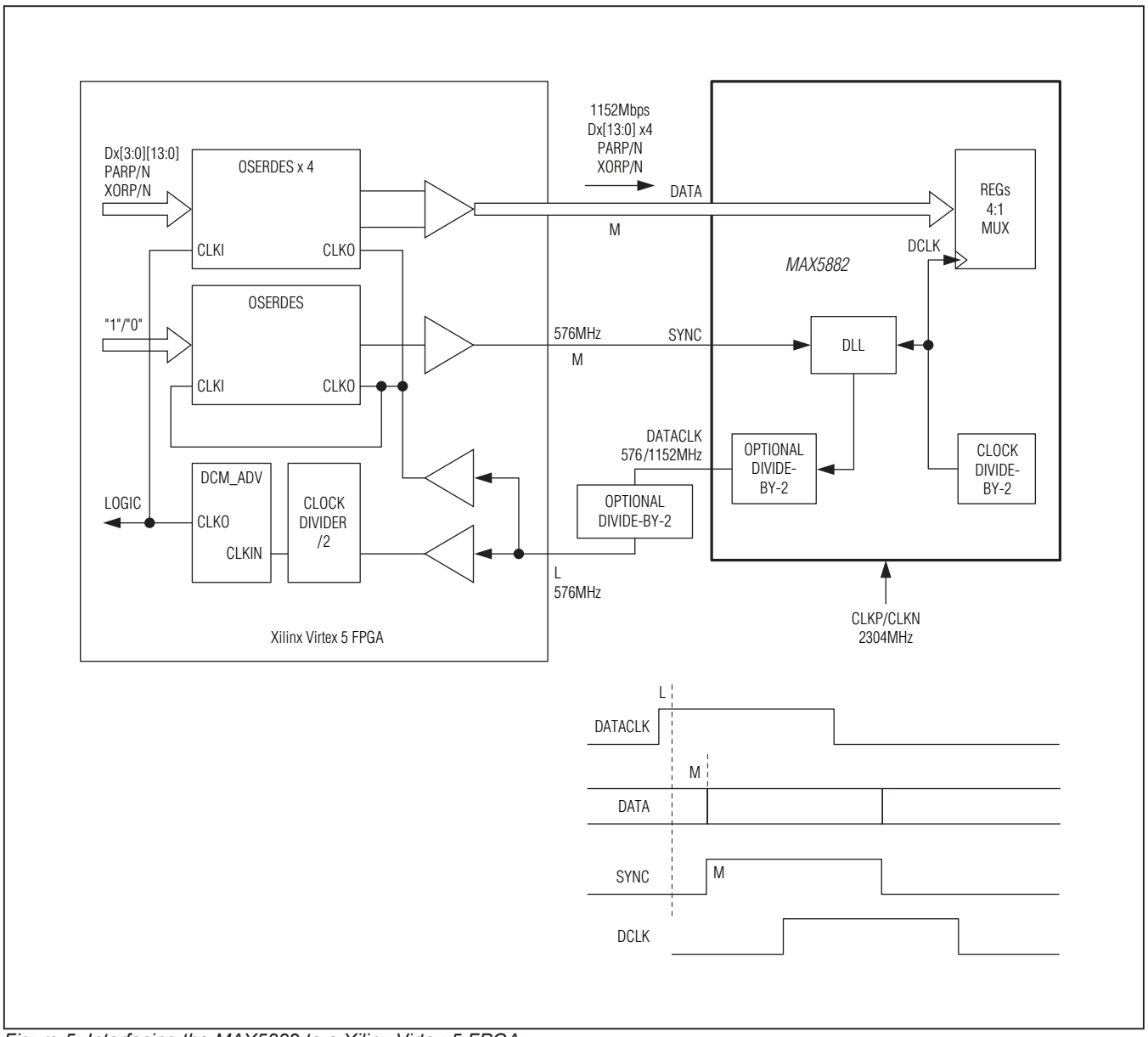

Figure 5. Interfacing the MAX5882 to a Xilinx Virtex-5 FPGA

An alternate clocking architecture using an Altera® Stratix® III FPGA is shown in Figure 6. As with the Xilinx solution, the DAC supplies a DATACLK to the FPGA that is one quarter the DAC update rate. Notice that the Stratix PLL is placed inside the device DLL loop. The bandwidth differential between the device's DLL and the Stratix III PLL is sufficient to allow for this configuration.

When the device is configured with the optional, internal divide-by-two turned off, the output clock rate must be divided by two externally with the current generation of FPGAs (Stratix IV or Virtex-6). Placing the divide-by-two external to the device may reduce a fixed $f_{DAC}/8$ spur.

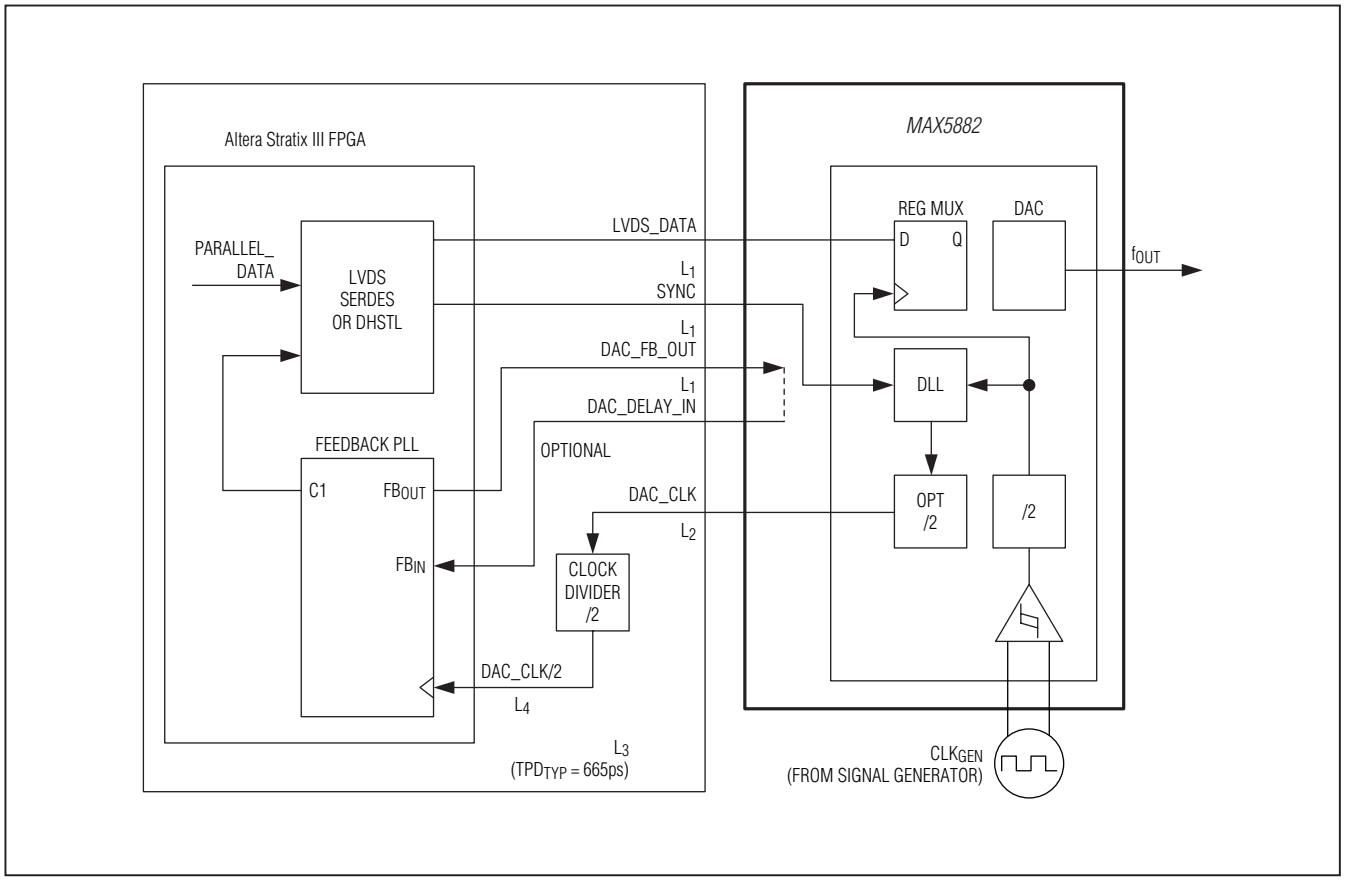

Figure 6. Interfacing the MAX5882 to an Altera Stratix III FPGA

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DLL Frequency Selection and 4-Level Inputs

Two external pins (DLLOFF and DELAY) have 4-level inputs (high, low, open, and resistor to ground) that perform the following functions:

- Turn DLL on or off
- Select operating frequency range of DLL

Table 1 defines the functionality of the DLLOFF and DELAY controls. Figure 7 shows the block diagram of the 4-level input circuitry.

Reset the DLL circuitry at power-up and each time the frequency range is changed. Set DLLOFF = 1 prior to selecting the range to perform the reset.

Table 1. Pin Function (DLLOFF, DELAY)

DLLOFF	DELAY	MAX5882 f_{CLK} (MHz)	OPERATION
High	High	10 to 2304	DLL disabled (one DAC clock period delay added to the DATACLKP/DATACLKN outputs)
High	Low	10 to 2304	DLL disabled (no delay added to the DATACLKP/DATACLKN outputs)
Low	High	2150 to 2304	DLL enabled
Low	Open	1900 to 2150	DLL enabled
Open	Low	1650 to 1900	DLL enabled
Open	High	1400 to 1650	DLL enabled
Open	Open	1250 to 1400	DLL enabled
Resistor to ground	Low	1100 to 1250	DLL enabled
Resistor to ground	High	950 to 1100	DLL enabled
Resistor to ground	Open	800 to 950	DLL enabled

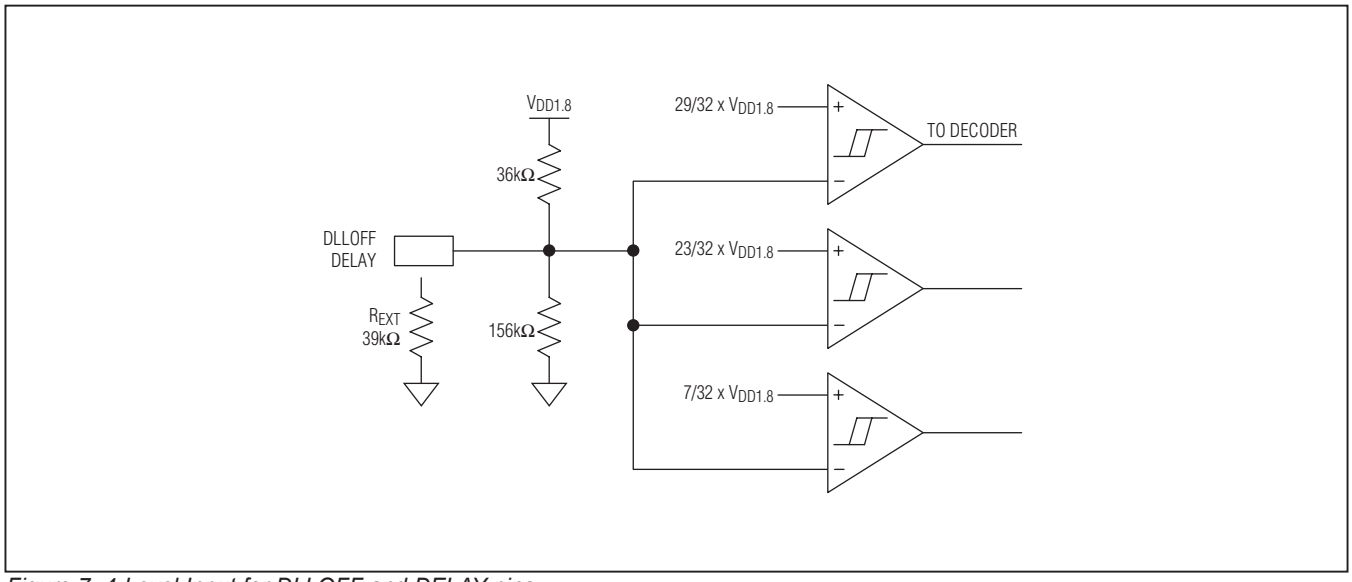

Figure 7. 4-Level Input for DLLOFF and DELAY pins

XOR and Parity Inputs

The device includes an XOR data function that can be used to whiten the spectral content of the data bits. Figure 8 shows the XOR and parity calculation. The block labeled “parity calculation” returns a 1 when there is an odd number of 1s in the DAC data. The parity is calculated by the device and compared to the received parity from the FPGA. When the received and calculated parity bits do not match, PERR is set high and held for 48 DATACLK cycles to make it easier for the FPGA or supervisory microcontroller to monitor asynchronously. Note that the FPGA also XORs the parity bit before sending it to the device. This ensures that corruption of the XOR bit results in detected parity errors.

The XORP/XORN and PARP/PARN signals include pipeline delays internal to the device. These delays must be compensated for in the data source for them to align to the data within the device. XORP/XORN requires one DATACLK cycle delay and PARP/PARN requires three.

f_{DAC}/2 Modulation (MOD)

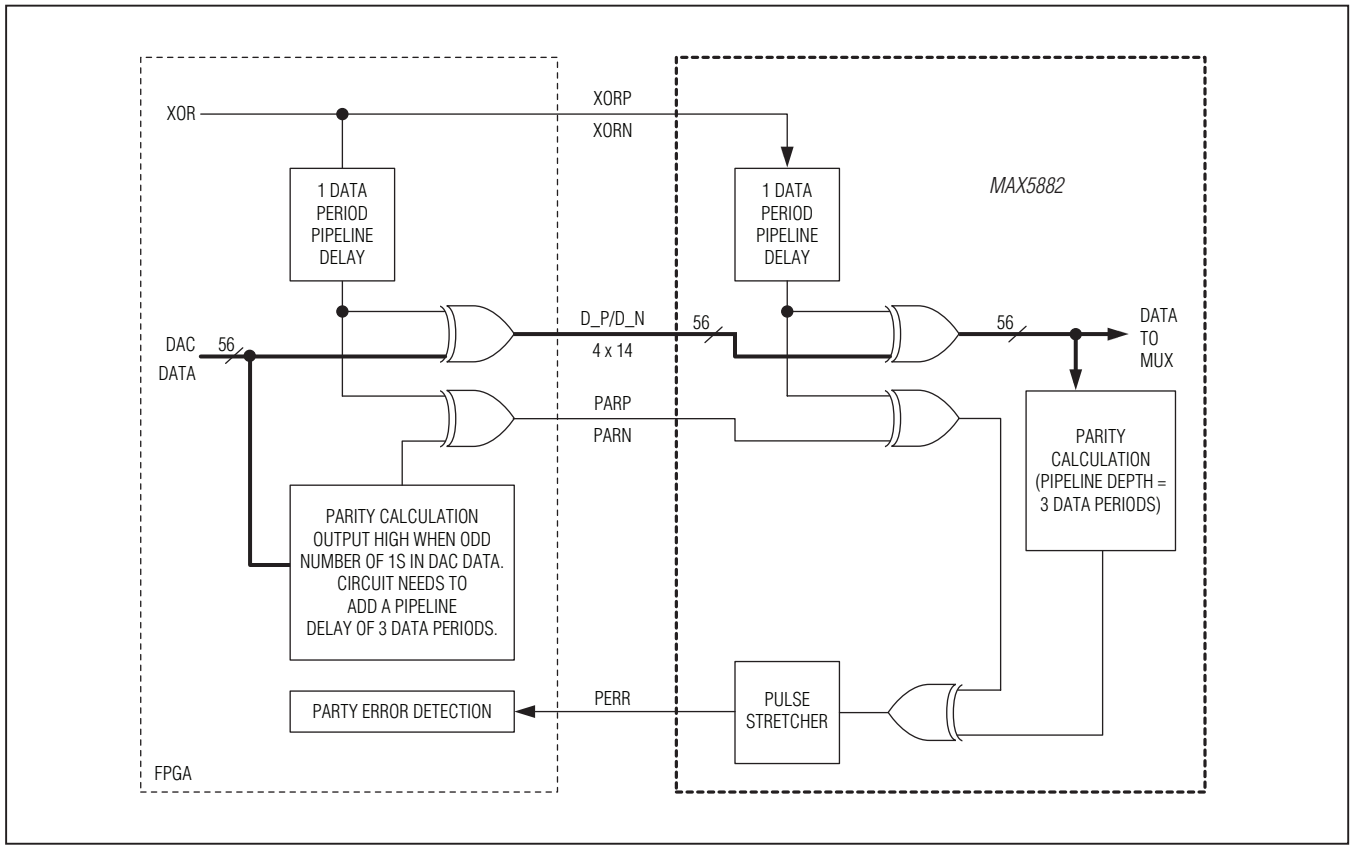

Figure 8. XOR and Parity Functions

The device's MOD input provides $f_{DAC}/2$ (or f_{CLK}) modulation when it is set to logic-high, as shown in Figure 9. MOD is a 1.8V, 3.3V tolerant, CMOS input with an internal pulldown resistor. Setting MOD to logic-high inverts data on channels B and D inside the device.

SO/LOCK Signal

The SO/LOCK pin is a dual-mode output signal. When SE is logic-low (0V), the SO/LOCK signal indicates the lock condition of the DLL circuit; SO/LOCK is logic-high (1.8V) when the DLL is locked.

The second function of the SO/LOCK signal is an output of the data input register on the device. Setting SE to logic 1 configures the input data register flip-flops into a 56-bit shift register connected to the SO/LOCK output, as shown in Figure 10. The contents of the shift register are output on the SO/LOCK pin allowing verification of connectivity in the data interface.

A timing diagram for the scan operation is shown in Figure 11. Known input data is applied to the DAC data inputs on the first DATACLK pulse, and the input register is loaded

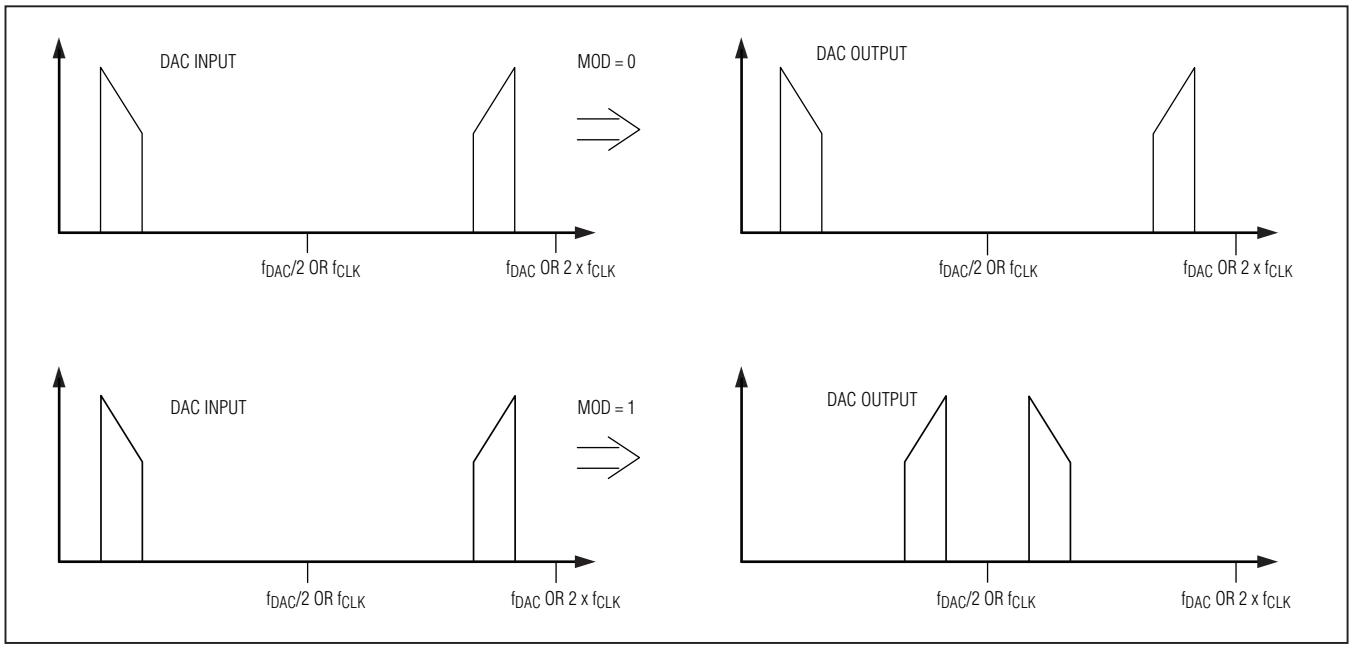

Figure 9. $f_{DAC}/2$ Modulation Using the MOD Input

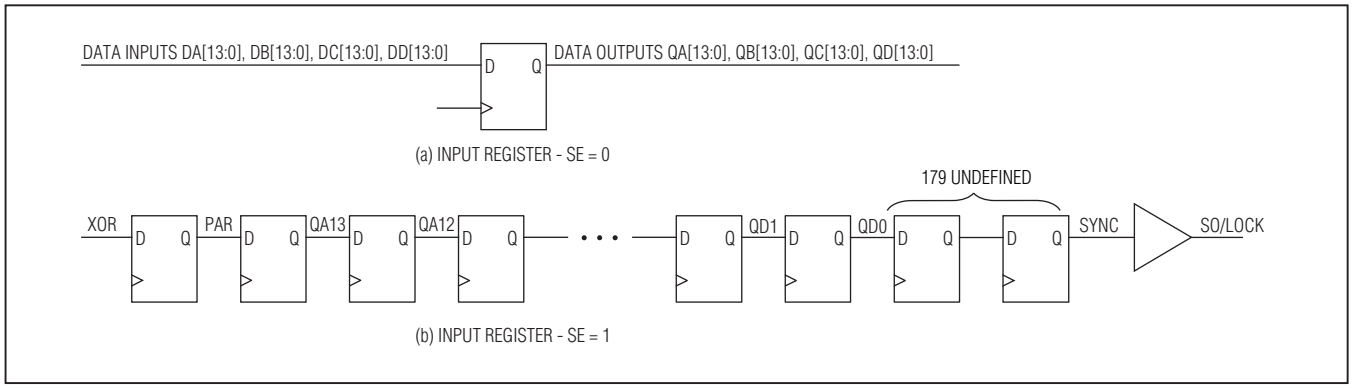

Figure 10. Input Register Flip-Flops in Normal Operation (a) and Scan Mode (b)

in a parallel fashion. Note that the input data needs one clock cycle to propagate before SE can be set to logic-high. When SE is set to logic-high, the input shift register is activated and the serial-data stream is output at the SO/LOCK pin at the input data rate (f_{DATA}). The bit order of the output stream is SYNC, 179 undefined states, QD[0:13], QC[0:13], QB[0:13], QA[0:13], PAR, and XOR. Any additional data out of the SO/LOCK pin is undefined and should be ignored. Set SE to logic-low to return the SO/LOCK pin to the LOCK functionality.

SE and SO/LOCK are a 1.8V CMOS logic interface intended for low-frequency operation. The DAC input clock frequency should be lower than normal when using the scan functionality.

Applications Information

Startup Conditions

The device employs a protection circuit to prevent damage to the DAC outputs. The internal clock circuitry is disabled when the reference voltage (V_{REFIO}) is less than 0.4V. The DATACLK outputs do not operate when the protection circuit is active. If the data source requires the DATACLK present to function normally, then the reference voltage must remain above 0.4V.

The device's DLL circuit requires an active, stable clock input and stable power supplies to perform accurately. After initial power is applied and the clock has stabilized, the DLL circuit should be reset by setting the DLLOFF pin high. The state of DLLOFF and DELAY can then be changed to set the DLL frequency range as needed.

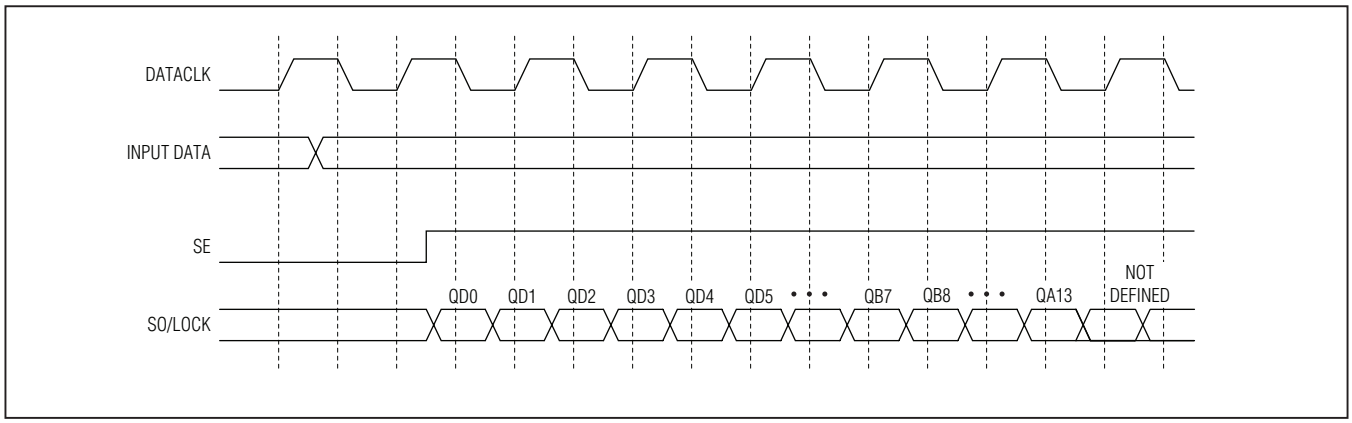

Figure 11. Timing Diagram (Scan Operation)

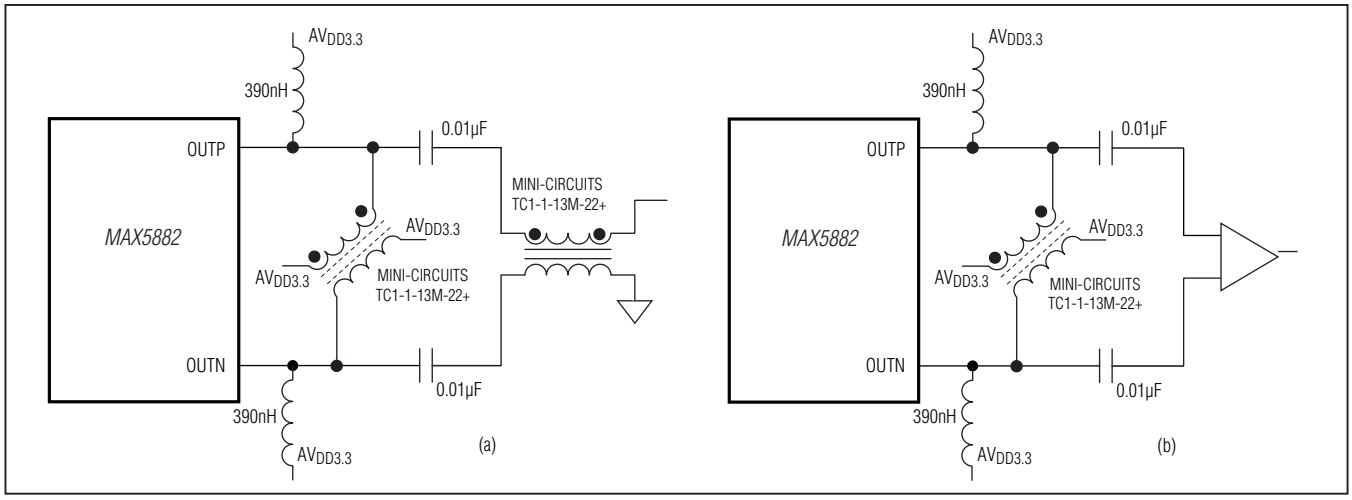

Figure 12. Balun Transformer Output (a) and Amplified Output Configuration (b)

Output Coupling

The differential voltage between OUTP and OUTN can be converted to a single-ended voltage using a transformer or a differential amplifier configuration. The DAC outputs should be pulled up to $AV_{DD3.3}$. It is recommended to use bias tees built from discrete inductors and capacitors for the pullups. Two recommended output circuit configurations are shown in Figure 12. To achieve the maximum bandwidth, minimize the inductance in the ground lead on the secondary side of the transformer. Use a very short trace and multiple vias for the connection to the ground plane.

Spectral Considerations

DAC Update Rate Selection

The 4.6Gsps maximum update rate of the device allows flexibility in system design. Several trade-offs exist in terms of update rate versus performance or circuit complexity, and these should be considered when selecting the DAC update rate.

An attenuated image of the desired DAC output is present at $f_{DAC}/2 - f_{OUT}$, due to the fact that the DAC output is updated on both edges of the clock. The DAC update rate must be at least four times higher than the highest frequency generated to keep this image outside of the cable band. Since DOCSIS (DRFI, annex A) defines the upper frequency as 1003MHz, the minimum DAC update rate to keep this spur out-of-band is 4012Msps. In some cases, a 1GHz lowpass filter is required to further attenuate this image. As the DAC update rate is reduced towards the lower requirement, the design of the filter becomes increasingly difficult. However, there are several potential advantages to using lower update rates. First, the overall spurious performance of the device improves as the update rate is reduced from the 4.6Gsps maximum towards 4Gsps. Second, the power requirement for the system solution will be lower; the device alone dissipates approximately 15% less power at 4Gsps versus 4.6Gsps. The power in the ASIC or FPGA will also be reduced for lower update rates. Another consideration is that timing margins are reduced at higher update rates and can be more difficult to meet.

Harmonic Distortion

The device features low harmonic distortion. Second harmonic distortion (HD2) and third harmonic distortion (HD3) are usually the dominant harmonics. The frequency of HD2 is below 1GHz for frequencies below 500MHz, and the frequency of HD3 is below 1GHz for output frequencies lower than 333MHz. When the DAC update rate is higher than 4Gsps, HD2 and HD3 never alias into the 45MHz to 1000MHz band.

Harmonics of Images around the Clock Frequency

The device has a spur at $f_{DAC}/2 - 2 \times f_{OUT}$. This spur is lower than the DOCSIS limit for channel counts greater than eight, but may violate DOCSIS DRFI spurious requirements for lower channel counts and high output frequencies. This spur is coincident with f_{OUT} for $f_{OUT} = f_{DAC}/6$. If necessary, this spur can be reduced using digital predistortion.

Grounding, Bypassing, Power-Supply, and Board-Layout Considerations

Grounding and power-supply decoupling can strongly influence the performance of the device. Unwanted digital crosstalk may couple through the input, reference, power-supply, and ground connections, affecting dynamic performance. Proper grounding and power-supply decoupling guidelines for high-speed, high-frequency applications should be closely followed. This reduces EMI and internal crosstalk that can significantly affect the dynamic performance of the device.

Use of a multilayer PCB with separate ground and power-supply planes is required. It is recommended that the analog output and the clock input are run as controlled-impedance microstrip lines on the top layer of the board, directly above a ground plane, and that no vias are used for the clock input (CLKP, CLKN) and the analog output (OUTP, OUTN) signals. Depending on the length of the traces, and the operating condition, a low-loss dielectric material (such as ROGERS RO4003) as the top layer dielectric may be advisable. The data clock (DATACLKP, DATACLKN) must be routed so that coupling into the clock input and the DAC output is minimized.

Digital input signals should be run as controlled-impedance striplines between ground planes. Digital signals should be kept as far away from sensitive analog inputs, reference input sense lines, common-mode inputs, and clock inputs as practical. It is particularly important to minimize coupling between digital signals and the clock to optimize dynamic performance for high output frequencies. Symmetric designs of the clock input and analog output lines are critical to minimize distortion and optimize the DAC's dynamic performance.

Digital signal paths should be kept short and run lengths matched to avoid data-delay mismatch.

The device supports three separate power-supply inputs for analog ($AV_{DD3.3}$), switching ($V_{DD1.8}$), and clock (AV_{CLK}) circuits. Each $AV_{DD3.3}$, $V_{DD1.8}$, and AV_{CLK} input should at least be decoupled with a separate 47nF capacitor as close as possible to the input, and their opposite ends with the shortest possible connection to the corresponding ground plane, to minimize loop inductance. All three power-supply voltages should also be decoupled at the point they enter the PCB.

Ferrite beads with additional decoupling capacitors forming a pi-network could also improve performance.

Static Performance Parameter Definitions

Offset Error

The offset error is the difference between the ideal and the actual offset current. For a DAC, the offset point is the average value at the output for the two mid-scale digital input codes, with respect to the full scale of the DAC. This error affects all codes by the same amount.

Gain Error

A gain error is the difference between the ideal and the actual full-scale output voltage on the transfer curve, after nullifying the offset error. This error alters the slope of the transfer function and corresponds to the same percentage error in each step.

Dynamic Performance Parameter Definitions

Settling Time

The settling time is the amount of time required from the start of a transition until the DAC output settles its new output value to within the specified accuracy.

Noise Spectral Density

The DAC output noise is the sum of the quantization noise and other noise sources. Noise spectral density is the noise power in a 1Hz bandwidth.

Two-/Four-Tone Intermodulation Distortion (IMD)

The two-/four-tone IMD is the ratio expressed in dBc (or dBFS) of the worst 3rd-order (or higher) IMD products to any output tone.

Adjacent Channel Power (ACP)

Adjacent channel power is commonly used in combination with DOCSIS-compliant QAM signals. ACP is the ratio in dB between the power in a channel at a specified frequency offset from the edge of the transmitted channel block, and power in the lowest frequency channel of the transmitted block. ACP provides a quantifiable method of determining out-of-band spectral energy and its influence on an adjacent channel when a bandwidth-limited RF signal passes through a nonlinear device.

Package Information

For the latest package outline information and land patterns (footprints), go to **www.maximintegrated.com/packages.** Note that a "+", "#", or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

PACKAGE TYPE	PACKAGE CODE	OUTLINE NO.	LAND PATTERN NO.
256 CSBGA	X25677-10	21-0474	90-0291

Revision History

REVISION NUMBER	REVISION DATE	DESCRIPTION	PAGES CHANGED
0	8/10	Initial release	—
1	3/12	Revised average total power on out-of-band noise and spurious and harmonic distortion parameters; revised t_{SKEW} limits based on improved test methodology; and added *Startup Conditions* section	3, 4, 5, 31
2	6/13	Revised *Ordering Information*, *Electrical Characteristics*, *Thermal Characteristics*, *Typical Operating Characteristics*, and Figure 10.	1–8, 19, 31

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