



# Dual, Audio, Log Taper Digital Potentiometers

## General Description

The MAX5408–MAX5411 dual, logarithmic taper digital potentiometers, with 32-tap points each, replace mechanical potentiometers in audio applications requiring digitally controlled resistors. The MAX5408/MAX5410 are dual potentiometers with one wiper per potentiometer. The MAX5409/MAX5411 are dual potentiometers with two wipers per potentiometer (see *Functional Diagram*). An SPI™-compatible serial interface controls the wiper positions. The MAX5408–MAX5411 have a factory-set resistance of 10kΩ per potentiometer. A zero-crossing detect feature minimizes the audible noise generated by wiper transitions. The MAX5408–MAX5411 have nominal temperature coefficients of 35ppm/°C end-to-end and 5ppm/°C ratiometric. The MAX5408–MAX5411 are available in 16-pin QSOP and 16-pin thin QFN packages and are specified over the extended temperature range (-40°C to +85°C).

## Applications

Stereo Volume Control  
Fading and Balancing Stereo Signals  
Mechanical Potentiometer Replacement

**Functional Diagram appears at end of data sheet.**

SPI is a trademark of Motorola, Inc.

## Features

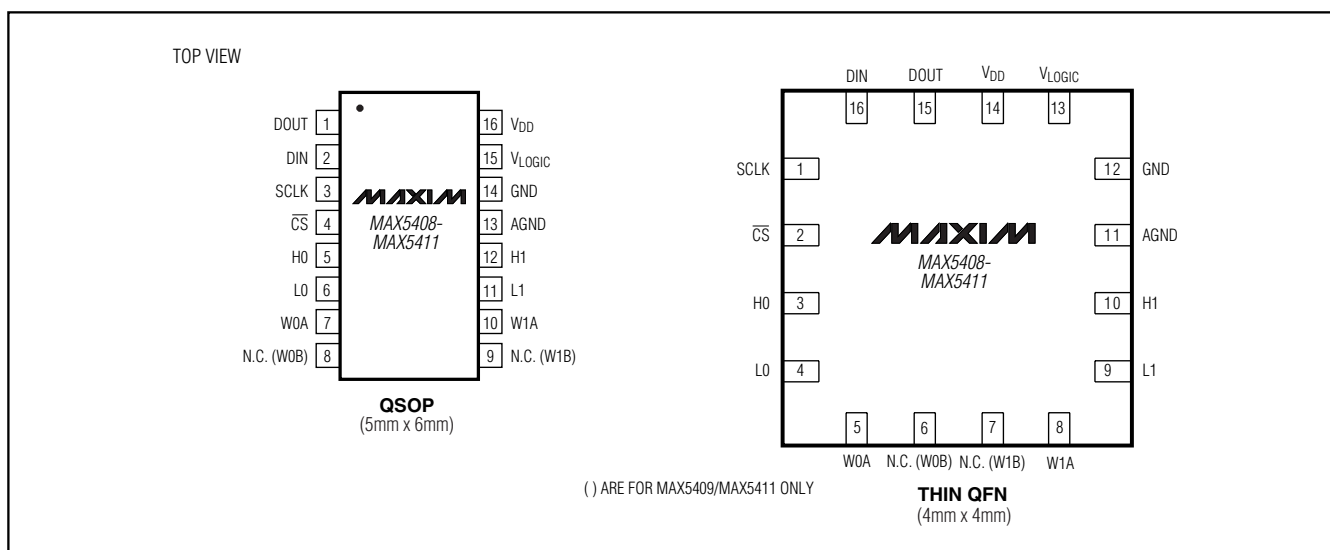
- ◆ Log Taper with 2dB Steps Between Taps
- ◆ 32-Tap Positions for Each Wiper
- ◆ Small 16-Pin QSOP/QFN Packages
- ◆ Single-Supply Voltage Operation
  - +2.7V to +3.6V (MAX5408/MAX5409)
  - +4.5V to +5.5V (MAX5410/MAX5411)
- ◆ Low 0.5μA Standby Supply Current
- ◆ Zero-Crossing Detection for Clickless Switching
- ◆ Mute Function to -90dB
- ◆ 10kΩ Fixed Resistance Value
- ◆ 3-Wire SPI-Compatible Serial Data Interface
- ◆ Power-On Reset: Wiper Goes to Maximum Attenuation
- ◆ Digital Output for Readback and Daisy-Chaining Capabilities

## Ordering Information

| PART       | TEMP RANGE     | PIN-PACKAGE | WIPERS PER RESISTOR |
|------------|----------------|-------------|---------------------|
| MAX5408EEE | -40°C to +85°C | 16 QSOP     | 1                   |
| MAX5408ETE | -40°C to +85°C | 16 Thin QFN | 1                   |
| MAX5409EEE | -40°C to +85°C | 16 QSOP     | 2                   |

Ordering Information continued at end of data sheet.

## Pin Configurations



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## ABSOLUTE MAXIMUM RATINGS

$V_{DD}$ ,  $V_{LOGIC}$ ,  $\overline{CS}$ , SCLK, DIN to GND ..... -0.3V to +6V  
 $H_{-}$ ,  $L_{-}$ , and  $W_{-}$  to GND ..... -0.3V to ( $V_{DD} + 0.3V$ )  
 DOUT to GND ..... -0.3V to ( $V_{DD} + 0.3V$ )  
 AGND to GND ..... -0.3V to +0.3V  
 Input and Output Latchup Immunity .....  $\pm 200mA$   
 Maximum Continuous Current into  $H_{-}$ ,  $L_{-}$ , and  $W_{-}$  .....  $\pm 500\mu A$

Continuous Power Dissipation ( $T_A = +70^{\circ}C$ )  
 16-Pin QSOP (derate 8.3mW/ $^{\circ}C$  above  $+70^{\circ}C$ ) ..... 666.7mW  
 16-Pin QFN (derate 18.5mW/ $^{\circ}C$  above  $+70^{\circ}C$ ) ..... 1481mW  
 Operating Temperature Range .....  $-40^{\circ}C$  to  $+85^{\circ}C$   
 Storage Temperature Range .....  $-60^{\circ}C$  to  $+150^{\circ}C$   
 Maximum Junction Temperature .....  $+150^{\circ}C$   
 Lead Temperature (soldering, 10s) .....  $+300^{\circ}C$

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

## ELECTRICAL CHARACTERISTICS

( $V_{DD} = +2.7V$  to  $+3.6V$  (MAX5408/MAX5409),  $V_{DD} = +4.5V$  to  $+5.5V$  (MAX5410/MAX5411),  $V_{H_{-}} = V_{DD}$ ,  $V_{L_{-}} = 0$ ,  $T_A = T_{MIN}$  to  $T_{MAX}$ . Typical values are at  $T_A = +25^{\circ}C$ , unless otherwise specified.)

| PARAMETER                                                | SYMBOL   | CONDITIONS                                    | MIN               | TYP        | MAX               | UNITS            |
|----------------------------------------------------------|----------|-----------------------------------------------|-------------------|------------|-------------------|------------------|
| End-to-End Resistance                                    |          |                                               | 7                 | 10         | 13                | k $\Omega$       |
| Maximum Bandwidth                                        |          | (Note 1) $C_{W_{-}} = 50pF$                   | 100               |            |                   | kHz              |
| Absolute Tolerance                                       |          |                                               |                   | $\pm 0.25$ |                   | dB               |
| Tap-to-Tap Tolerance                                     |          |                                               |                   | $\pm 0.1$  |                   | dB               |
| Total Harmonic Distortion + Noise                        | THD+N    | $V_{IN} = 1V_{RMS}$ , $f = 1kHz$ , tap = -6dB |                   | 0.002      |                   | %                |
| Channel Isolation                                        |          |                                               |                   | -100       |                   | dB               |
| Interchannel Matching                                    |          | $f = 20Hz$ to $20kHz$ , tap = -6dB            |                   | $\pm 0.5$  |                   | dB               |
| Mute Attenuation                                         |          |                                               |                   | -90        |                   | dB               |
| Power-Supply Rejection Ratio                             | PSRR     |                                               |                   | -80        |                   | dB               |
| Wiper Resistance                                         | $R_W$    |                                               |                   | 1000       | 1700              | $\Omega$         |
| Wiper Capacitance                                        | $C_W$    |                                               |                   | 10         |                   | pF               |
| Digital Clock Feedthrough                                |          | $f_{SCLK} = 20Hz$ to $20kHz$ , tap = -6dB     |                   | -90        |                   | dB               |
| End-to-End Resistance Temperature Coefficient            |          |                                               |                   | 35         |                   | ppm/ $^{\circ}C$ |
| Ratiometric Resistance Temperature Coefficient           |          |                                               |                   | 5          |                   | ppm/ $^{\circ}C$ |
| <b>DIGITAL INPUTS (<math>V_{LOGIC} &gt; 4.5V</math>)</b> |          |                                               |                   |            |                   |                  |
| Input High Voltage                                       | $V_{IH}$ |                                               | 2.4               |            |                   | V                |
| Input Low Voltage                                        | $V_{IL}$ |                                               |                   |            | 0.8               | V                |
| Input Leakage Current                                    |          |                                               |                   |            | $\pm 1$           | $\mu A$          |
| Input Capacitance                                        |          |                                               |                   | 5          |                   | pF               |
| <b>DIGITAL INPUTS (<math>V_{LOGIC} &lt; 4.5V</math>)</b> |          |                                               |                   |            |                   |                  |
| Input High Voltage                                       | $V_{IH}$ |                                               | 0.7 x $V_{LOGIC}$ |            |                   | V                |
| Input Low Voltage                                        | $V_{IL}$ |                                               |                   |            | 0.3 x $V_{LOGIC}$ | V                |
| Input Leakage Current                                    |          |                                               |                   |            | $\pm 1$           | $\mu A$          |
| Input Capacitance                                        |          |                                               |                   | 5          |                   | pF               |

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## ELECTRICAL CHARACTERISTICS (continued)

( $V_{DD} = +2.7V$  to  $+3.6V$  (MAX5408/MAX5409),  $V_{DD} = +4.5V$  to  $+5.5V$  (MAX5410/MAX5411),  $V_{H\_} = V_{DD}$ ,  $V_{L\_} = 0$ ,  $T_A = T_{MIN}$  to  $T_{MAX}$ . Typical values are at  $T_A = +25^\circ C$ , unless otherwise specified.)

| PARAMETER                                    | SYMBOL      | CONDITIONS                                   | MIN               | TYP | MAX | UNITS   |
|----------------------------------------------|-------------|----------------------------------------------|-------------------|-----|-----|---------|
| <b>DIGITAL OUTPUT</b>                        |             |                                              |                   |     |     |         |
| Output High Voltage                          | $V_{OH}$    | $I_{SOURCE} = 0.5mA$                         | $V_{LOGIC} - 0.5$ |     |     | V       |
| Output Low Voltage                           | $V_{OL}$    | $I_{SINK} = 2mA$                             |                   |     | 0.4 | V       |
| <b>TIMING CHARACTERISTICS</b> (Figure 1)     |             |                                              |                   |     |     |         |
| SCLK Clock Period                            | $t_{CP}$    |                                              | 100               |     |     | ns      |
| SCLK Pulse Width High                        | $t_{CH}$    |                                              | 40                |     |     | ns      |
| SCLK Pulse Width Low                         | $t_{CL}$    |                                              | 40                |     |     | ns      |
| $\overline{CS}$ Fall to SCLK Rise Setup Time | $t_{CSS}$   |                                              | 40                |     |     | ns      |
| SCLK Rise to $\overline{CS}$ Rise Hold Time  | $t_{CSH}$   |                                              | 0                 |     |     | ns      |
| DIN Setup Time                               | $t_{DS}$    |                                              | 40                |     |     | ns      |
| DIN Hold Time                                | $t_{DH}$    |                                              | 0                 |     |     | ns      |
| SCLK Fall to DOUT Valid Propagation Delay    | $t_{DO}$    | $C_{LOAD} = 200pF$                           |                   |     | 80  | ns      |
| $\overline{CS}$ Rise to SCLK Rise Hold Time  | $t_{CS1}$   |                                              | 40                |     |     | ns      |
| $\overline{CS}$ Pulse Width High             | $t_{CSW}$   |                                              | 100               |     |     | ns      |
| Wiper Settling Time                          | $t_{tW}$    | Zero-crossing detect disabled                |                   | 1   |     | $\mu s$ |
| <b>POWER SUPPLIES</b>                        |             |                                              |                   |     |     |         |
| Supply Voltage                               | $V_{DD}$    | MAX5408/MAX5409                              | 2.7               |     | 3.6 | V       |
|                                              |             | MAX5410/MAX5411                              | 4.5               |     | 5.5 |         |
| Active Supply Current                        | $I_{DD}$    | $f_{SCLK} = 2MHz$ (Note 2)                   |                   |     | 100 | $\mu A$ |
| Standby Supply Current                       |             | (Note 3)                                     |                   | 0.2 | 10  |         |
| Logic Supply Voltage                         | $V_{LOGIC}$ |                                              | 2.7               |     | 5.5 | V       |
| Logic Active Supply Current                  | $I_{LOGIC}$ | $f_{SCLK} = 2MHz$ , DOUT = floating (Note 2) |                   |     | 120 | $\mu A$ |
| Logic Standby Supply Current                 |             | DOUT = floating (Note 3)                     |                   | 0.5 | 10  |         |

**Note 1:** Guaranteed by design, not production tested.

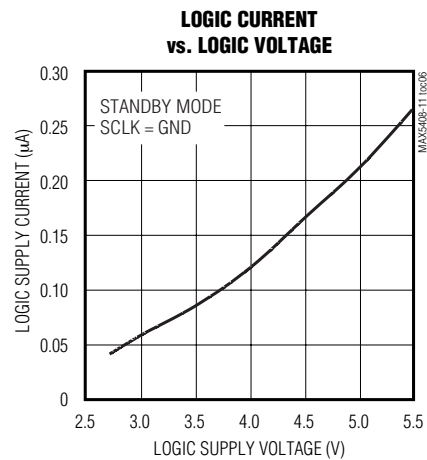
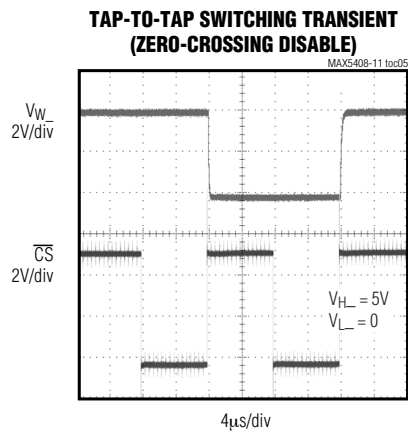
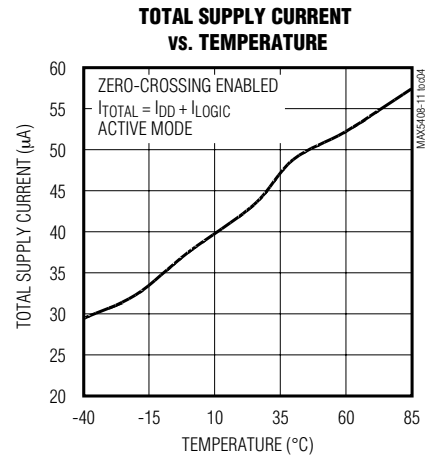
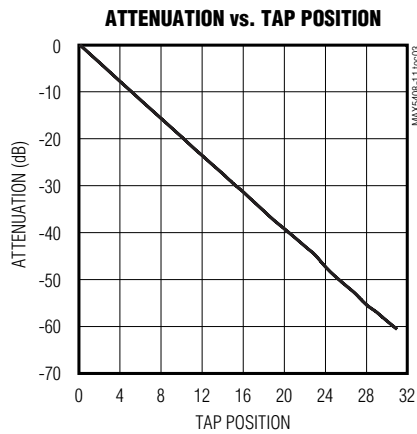
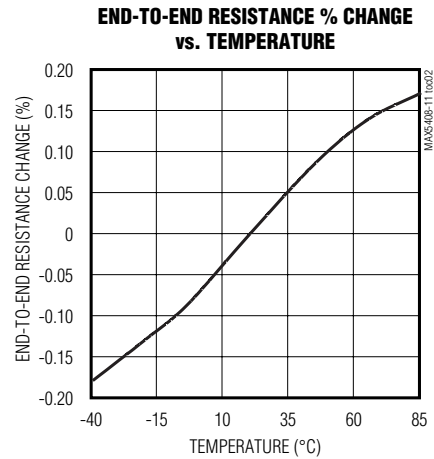
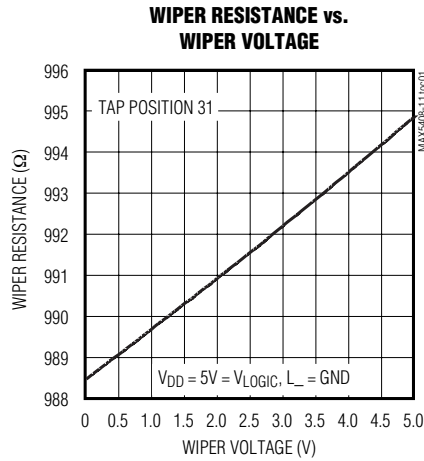
**Note 2:** Supply current measured while changing wiper position with zero crossing enabled.

**Note 3:** Supply current measured while wiper position is fixed.

# Dual, Audio, Log Taper Digital Potentiometers

## Typical Operating Characteristics

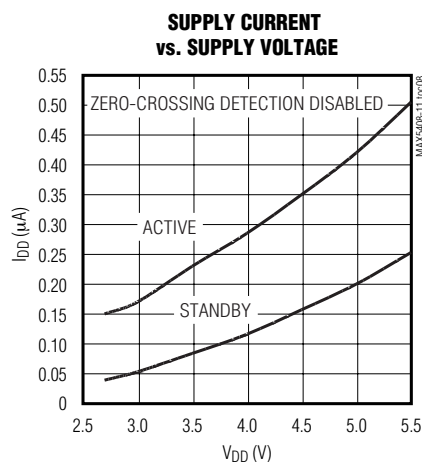
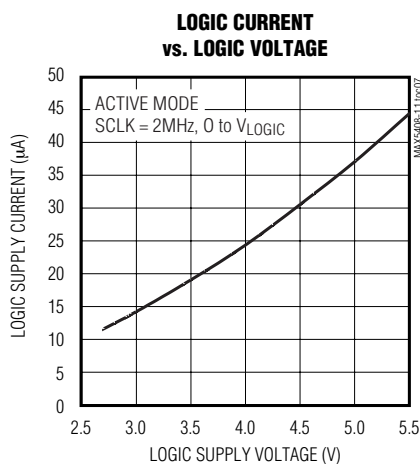
( $V_{DD} = +3V$  (MAX5408/MAX5409),  $V_{DD} = +5V$  (MAX5410/MAX5411),  $DOUT = \text{floating}$ )



# Dual, Audio, Log Taper Digital Potentiometers

## Typical Operating Characteristics (continued)

(V<sub>DD</sub> = +3V (MAX5408/MAX5409), V<sub>DD</sub> = +5V (MAX5410/MAX5411), DOUT = floating)



MAX5408-MAX5411

## Pin Description

| PIN                       |                            |                           |                            | NAME               | FUNCTION                                 |
|---------------------------|----------------------------|---------------------------|----------------------------|--------------------|------------------------------------------|
| MAX5408/<br>MAX5410 (QFN) | MAX5408/<br>MAX5410 (QSOP) | MAX5409/<br>MAX5411 (QFN) | MAX5409/<br>MAX5411 (QSOP) |                    |                                          |
| 1                         | 3                          | 1                         | 3                          | SCLK               | Serial Clock Input                       |
| 2                         | 4                          | 2                         | 4                          | CS                 | Chip-Select Input                        |
| 3                         | 5                          | 3                         | 5                          | H0                 | High Terminal of Resistor 0              |
| 4                         | 6                          | 4                         | 6                          | L0                 | Low Terminal of Resistor 0               |
| 5                         | 7                          | 5                         | 7                          | W0A                | Wiper Terminal A of Resistor 0           |
| —                         | —                          | 6                         | 8                          | W0B                | Wiper Terminal B of Resistor 0           |
| —                         | —                          | 7                         | 9                          | W1B                | Wiper Terminal B of Resistor 1           |
| 8                         | 10                         | 8                         | 10                         | W1A                | Wiper Terminal A of Resistor 1           |
| 9                         | 11                         | 9                         | 11                         | L1                 | Low Terminal of Resistor 1               |
| 10                        | 12                         | 10                        | 12                         | H1                 | High Terminal of Resistor 1              |
| 11                        | 13                         | 11                        | 13                         | AGND               | Analog Ground                            |
| 12                        | 14                         | 12                        | 14                         | GND                | Ground                                   |
| 13                        | 15                         | 13                        | 15                         | V <sub>LOGIC</sub> | Digital Logic Power Supply               |
| 14                        | 16                         | 14                        | 16                         | V <sub>DD</sub>    | Analog Power Supply                      |
| 15                        | 1                          | 15                        | 1                          | DOUT               | Serial Data Output                       |
| 16                        | 2                          | 16                        | 2                          | DIN                | Serial Data Input                        |
| 6, 7                      | 8, 9                       | —                         | —                          | N.C.               | No Connection. Not internally connected. |

# Dual, Audio, Log Taper Digital Potentiometers

**Table 1. Serial Interface Programming Commands for MAX5408/MAX5410**

| 8-BIT SERIAL WORD |    |    |                                                       | FUNCTION                                                                                                         |
|-------------------|----|----|-------------------------------------------------------|------------------------------------------------------------------------------------------------------------------|
| A0                | A1 | A2 | D4–D0                                                 |                                                                                                                  |
| 0                 | 0  | 0  | 5-bit DAC data                                        | Set position of wiper W0A                                                                                        |
| 0                 | 0  | 1  | 5-bit DAC data                                        | No change                                                                                                        |
| 0                 | 1  | 0  | 5-bit DAC data                                        | Set position of wiper W1A                                                                                        |
| 0                 | 1  | 1  | 5-bit DAC data                                        | No change                                                                                                        |
| 1                 | 0  | 0  | 4-bit mute data, D0 = “don’t care”                    | Data for mute register (see Table 3)                                                                             |
| 1                 | 0  | 1  | 4-bit zero-crossing detection data, D0 = “don’t care” | Data for zero-crossing detection register (see Table 5)                                                          |
| 1                 | 1  | 0  | 00000                                                 | Readback contents of wiper register for W0A at DOUT                                                              |
| 1                 | 1  | 0  | 00001                                                 | No change                                                                                                        |
| 1                 | 1  | 0  | 00010                                                 | Readback contents of wiper register for W1A at DOUT                                                              |
| 1                 | 1  | 0  | 00011                                                 | No change                                                                                                        |
| 1                 | 1  | 0  | 00100                                                 | Readback contents of mute register at DOUT                                                                       |
| 1                 | 1  | 0  | 00101                                                 | Readback contents of zero-crossing detection register at DOUT                                                    |
| 1                 | 1  | 1  | D4 = 0, D3–D0 = “don’t care”                          | Immediate update then analog power-down when zero crossing is enabled. No effect when zero crossing is disabled. |

## Detailed Description

### Digital Serial Interface

An SPI-compatible serial interface controls the MAX5408–MAX5411. The input word to the device is eight bits long, composed of three address bits (A0, A1, and A2), followed by five data bits, with MSB first (see Tables 1 and 2). The first three address bits set the value of internal registers. The five data bits control the wiper position. For certain commands, some of the five data bits are “don’t cares”, but must be sent to the device.

The serial data is listed in Tables 1 and 2.

The control code determines:

- Potentiometer to update or register to set.
- Data for mute register (Tables 3 and 4).
- Data for zero-crossing detection register (Tables 5 and 6).

The data bits control the position of the wiper (Table 7). A logic low on the chip-select input (CS) enables the device’s serial interface. A logic high on CS disables the interface control circuitry. See Figure 1 for serial-interface timing description.

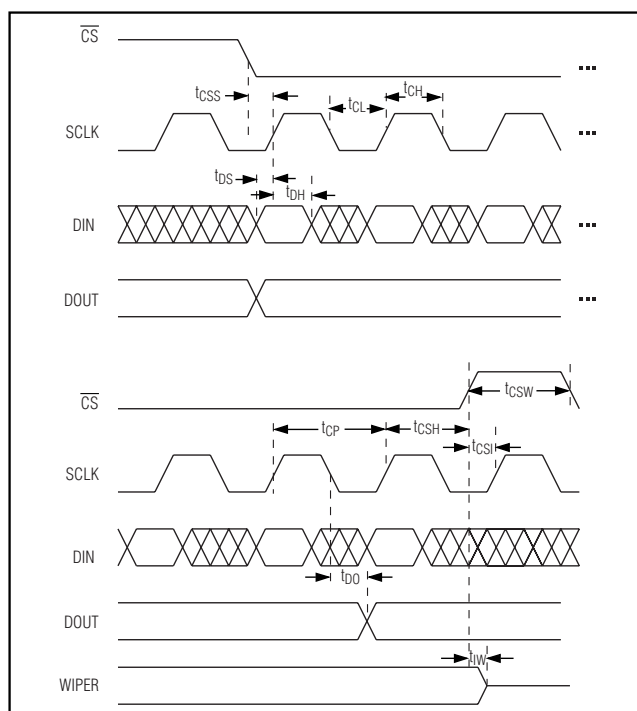


Figure 1. Serial Timing Diagram

# Dual, Audio, Log Taper Digital Potentiometers

MAX5408-MAX5411

**Table 2. Serial Interface Programming Commands for MAX5409/MAX5411**

| 8-BIT SERIAL WORD |    |    |                                                       | FUNCTION                                                      |
|-------------------|----|----|-------------------------------------------------------|---------------------------------------------------------------|
| A0                | A1 | A2 | D4-D0                                                 |                                                               |
| 0                 | 0  | 0  | 5-bit DAC data                                        | Set position of wiper W0A                                     |
| 0                 | 0  | 1  | 5-bit DAC data                                        | Set position of wiper W0B                                     |
| 0                 | 1  | 0  | 5-bit DAC data                                        | Set position of wiper W1A                                     |
| 0                 | 1  | 1  | 5-bit DAC data                                        | Set position of wiper W1B                                     |
| 1                 | 0  | 0  | 4-bit mute data, D0 = "don't care"                    | Data for mute register (see Table 4)                          |
| 1                 | 0  | 1  | 4-bit zero-crossing detection data, D0 = "don't care" | Data for zero-crossing detection register (see Table 6)       |
| 1                 | 1  | 0  | 00000                                                 | Readback contents of wiper register for W0A at DOUT           |
| 1                 | 1  | 0  | 00001                                                 | Readback contents of wiper register for W0B at DOUT           |
| 1                 | 1  | 0  | 00010                                                 | Readback contents of wiper register for W1A at DOUT           |
| 1                 | 1  | 0  | 00011                                                 | Readback contents of wiper register for W1B at DOUT           |
| 1                 | 1  | 0  | 00100                                                 | Readback contents of mute register at DOUT                    |
| 1                 | 1  | 0  | 00101                                                 | Readback contents of zero-crossing detection register at DOUT |
| 1                 | 1  | 1  | D4 = 0, D3-D0 = "don't care"                          | Analog power-down                                             |
| 1                 | 1  | 1  | D4 = 1, D3-D0 = "don't care"                          | Analog power-up                                               |

**Table 3. Mute Register Bit Definitions for MAX5408/MAX5410**

| DATA BIT | VALUE        | FUNCTION                                                 |
|----------|--------------|----------------------------------------------------------|
| D4       | 0            | Set wiper W0A to preprogrammed value (-62dB on power-up) |
|          | 1            | Set wiper W0A to mute (-90dB)                            |
| D3       | "don't care" | No change                                                |
| D2       | 0            | Set wiper W1A to preprogrammed value (-62dB on power-up) |
|          | 1            | Set wiper W1A to mute (-90dB)                            |
| D1       | "don't care" | No change                                                |
| D0       | "don't care" | No change                                                |

**Table 4. Mute Register Bit Definitions for MAX5409/MAX5411**

| DATA BIT | VALUE        | FUNCTION                                                 |
|----------|--------------|----------------------------------------------------------|
| D4       | 0            | Set wiper W0A to preprogrammed value (-62dB on power-up) |
|          | 1            | Set wiper W0A to mute (-90dB)                            |
| D3       | 0            | Set wiper W0B to preprogrammed value (-62dB on power-up) |
|          | 1            | Set wiper W0B to mute (-90dB)                            |
| D2       | 0            | Set wiper W1A to preprogrammed value (-62dB on power-up) |
|          | 1            | Set wiper W1A to mute (-90dB)                            |
| D1       | 0            | Set wiper W1B to preprogrammed value (-62dB on power-up) |
|          | 1            | Set wiper W1B to mute (-90dB)                            |
| D0       | "don't care" | No change                                                |

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**Table 5. Zero-Crossing Detection Register Bit Definitions for MAX5408/MAX5410**

| DATA BIT | VALUE        | FUNCTION                                          |
|----------|--------------|---------------------------------------------------|
| D4       | 0            | Disable wiper W0A zero-crossing detection circuit |
|          | 1            | Enable wiper W0A zero-crossing detection circuit  |
| D3       | “don’t care” | No change                                         |
| D2       | 0            | Disable wiper W1A zero-crossing detection circuit |
|          | 1            | Enable wiper W1A zero-crossing detection circuit  |
| D1       | “don’t care” | No change                                         |
| D0       | “don’t care” | No change                                         |

**Table 6. Zero-Crossing Detection Register Bit Definitions for MAX5409/MAX5411**

| DATA BIT | VALUE        | FUNCTION                                          |
|----------|--------------|---------------------------------------------------|
| D4       | 0            | Disable wiper W0A zero-crossing detection circuit |
|          | 1            | Enable wiper W0A zero-crossing detection circuit  |
| D3       | 0            | Disable wiper W0B zero-crossing detection circuit |
|          | 1            | Enable wiper W0B zero-crossing detection circuit  |
| D2       | 0            | Disable wiper W1A zero-crossing detection circuit |
|          | 1            | Enable wiper W1A zero-crossing detection circuit  |
| D1       | 0            | Disable wiper W1B zero-crossing detection circuit |
|          | 1            | Enable wiper W1B zero-crossing detection circuit  |
| D0       | “don’t care” | No change                                         |

**Table 7. Attenuation and Wiper Position**

| POSITION | OUTPUT LEVEL (dB) |
|----------|-------------------|
| 0        | 0                 |
| 1        | -2                |
| 2        | -4                |
| 3        | -6                |
| 4        | -8                |
| ⋮        | ⋮                 |
| 30       | -60               |
| 31       | -62               |
| MUTE     | <-90              |

The digital output, DOUT, lags the digital input signal, DIN by 8.5 clock cycles. Force  $\overline{CS}$  high to disable DOUT, placing DOUT in three-state mode. Force  $\overline{CS}$  low to enable DOUT and disable three-state mode.

Force  $\overline{CS}$  high, after a word has been written to the MAX5408–MAX5411 to make a readback request. The next  $\overline{CS}$  low period writes the requested data to DOUT.

A readback request overwrites any previous data in the shift register. Note that the data appears at DOUT in the order: A0, A1, A2, D4, D3, D2, D1, D0. A0 will be available after the first high-to-low transition of SCLK when  $\overline{CS}$  is low. The input continues to load the shift register while data is being read out of the MAX5408–MAX5411. The input data appears at DOUT 8.5 clock cycles later. A  $\overline{CS}$  transition from low-to-high latches the input data. For any control byte, the state of SCLK must be the same for both  $\overline{CS}$  low-to-high transitions and  $\overline{CS}$  high-to-low transitions in order to preserve the data at DOUT while  $\overline{CS}$  transitions. For proper operation, ensure that the input data remains valid on both the SCLK rising and falling edges when daisy chaining multiple devices.

## Zero-Crossing Detection

The zero-crossing detection register enables the zero-crossing detect feature. The zero-crossing detect feature reduces the audible noise (“clicks and pops”) that result from wiper transitions. The wiper changes position only when the voltage at L<sub>-</sub> is the same as the voltage at H<sub>-</sub>. Each wiper has a zero-crossing and timeout



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MAX5408-MAX5411

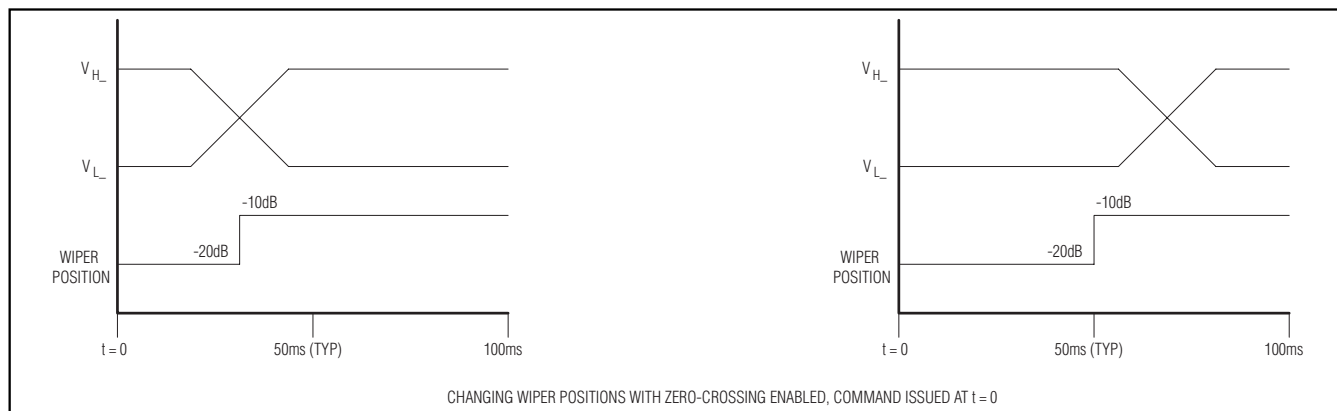


Figure 2. Zero-Crossing Timing Diagram

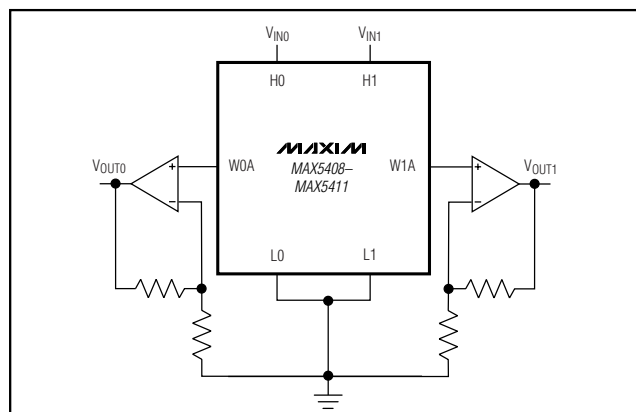


Figure 3. Attenuation Control

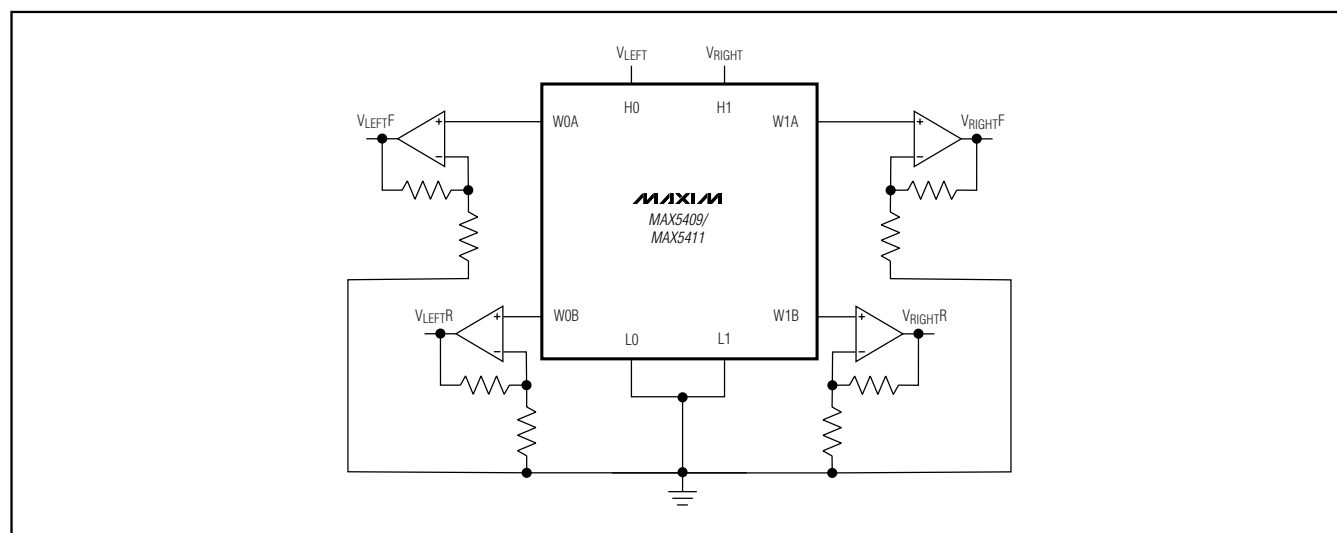


Figure 4. Stereo Volume Control with Front and Rear Fade

# Dual, Audio, Log Taper Digital Potentiometers

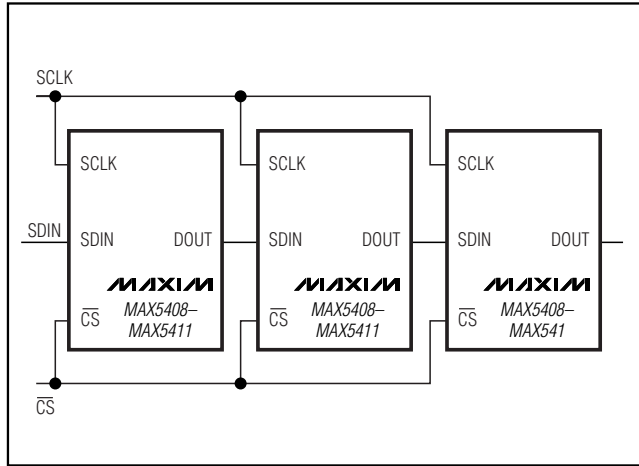


Figure 5. Daisy-Chaining of Serial Interfaces

circuit (see Figure 2). With zero-crossing enabled, the MAX5408-MAX5411 change wiper position after 50ms or when zero crossing is detected.

## Power-On Reset

The power-on reset (POR) feature sets all the wipers to the maximum attenuation (tap position 31, -62dB) at power-up. If either VDD or VLOGIC is zero volts, a power-on reset initiates when one of the supplies is brought back to the operating voltage.

## Mute Function

When mute is enabled, the wipers go to -90dB attenuation. When mute is disabled, the wiper returns to its position before mute was enabled. All wipers can be muted simultaneously or independently.

## Applications Information

### Attenuation Control

Figure 3 shows the application of an attenuation control. The op amps are connected in a follower configuration with a fixed gain. The digitally controlled potentiometer attenuates the input signal.

### Stereo Volume Control

Figure 4 shows the application of stereo volume control using MAX5409/MAX5411. The op amps are connected in a follower configuration with fixed gain. The digitally controlled potentiometer attenuates the input signals. The second wiper of each potentiometer controls the signal amplitude at the rear set of speakers.

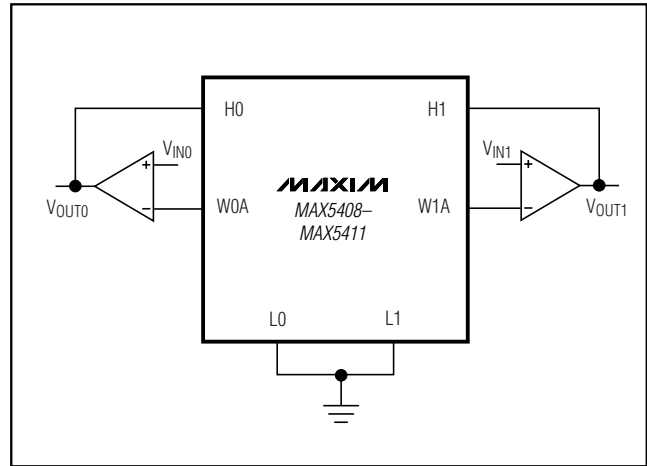


Figure 6. Gain Control

## Daisy-Chaining

Figure 5 shows an application daisy-chaining the serial-interfaces of the MAX5408-MAX5411. A single-write command updates multiple devices from a single digital port in this configuration (see *Digital Serial Interface* section).

## Gain Control

Figure 6 shows the application of a gain control. **Note:** Muting the potentiometer creates unpredictable behavior at the output of the op amp, and may seriously degrade the performance of the op amp.

## Ordering Information (continued)

| PART              | TEMP RANGE     | PIN-PACKAGE | WIPERS PER RESISTOR |
|-------------------|----------------|-------------|---------------------|
| MAX5409ETE        | -40°C to +85°C | 16 Thin QFN | 2                   |
| <b>MAX5410EEE</b> | -40°C to +85°C | 16 QSOP     | 1                   |
| MAX5410ETE        | -40°C to +85°C | 16 Thin QFN | 1                   |
| <b>MAX5411EEE</b> | -40°C to +85°C | 16 QSOP     | 2                   |
| MAX5411ETE        | -40°C to +85°C | 16 Thin QFN | 2                   |

## Chip Information

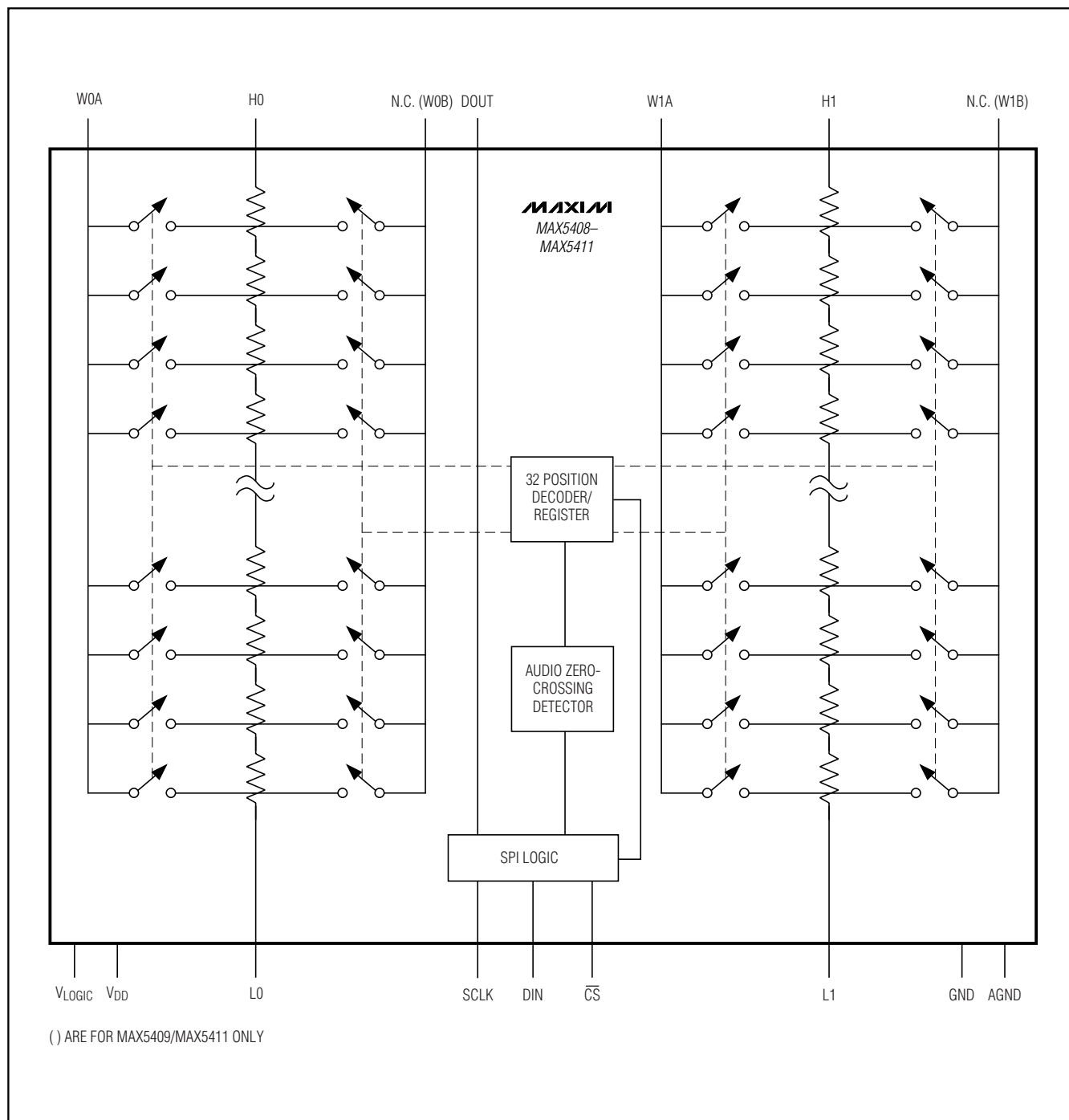
TRANSISTOR COUNT: 12,875

PROCESS: BiCMOS

# Dual, Audio, Log Taper Digital Potentiometers

## Functional Diagram

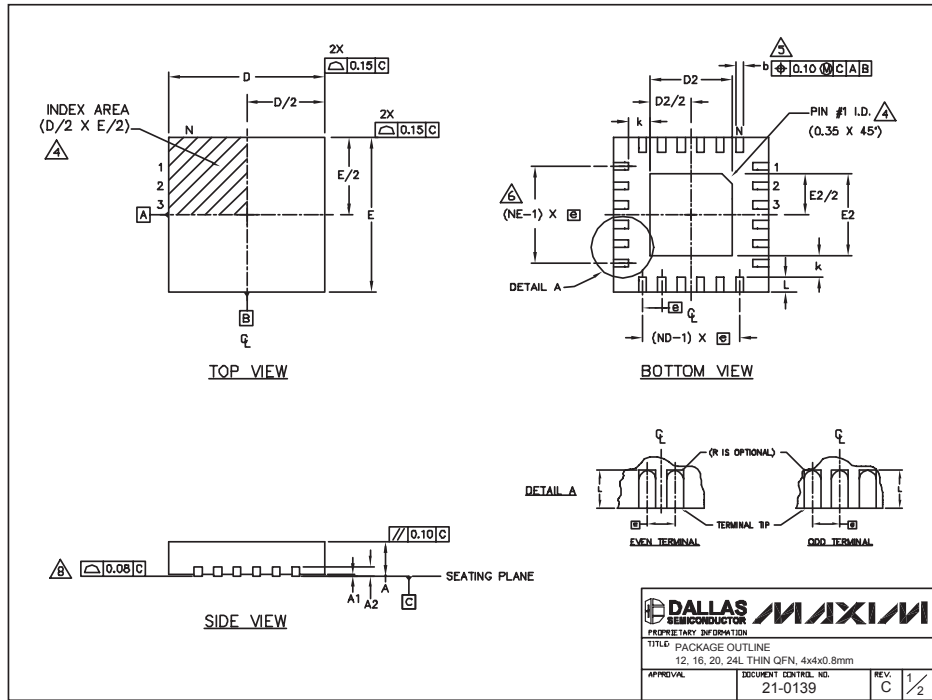
**MAX5408-MAX5411**



# Dual, Audio, Log Taper Digital Potentiometers

## Package Information

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information, go to [www.maxim-ic.com/packages](http://www.maxim-ic.com/packages).)



24L QFN THINLEPS

| COMMON DIMENSIONS |           |      |      |           |      |      |           |      |      |           |      |      |
|-------------------|-----------|------|------|-----------|------|------|-----------|------|------|-----------|------|------|
| PKG. REF.         | 12L 4x4   |      |      | 16L 4x4   |      |      | 20L 4x4   |      |      | 24L 4x4   |      |      |
|                   | MIN.      | NOM. | MAX. | MIN.      | NOM. | MAX. | MIN.      | NOM. | MAX. | MIN.      | NOM. | MAX. |
| A                 | 0.70      | 0.75 | 0.80 | 0.70      | 0.75 | 0.80 | 0.70      | 0.75 | 0.80 | 0.70      | 0.75 | 0.80 |
| Alt               | 0.0       | 0.02 | 0.05 | 0.0       | 0.02 | 0.05 | 0.0       | 0.02 | 0.05 | 0.0       | 0.02 | 0.05 |
| A2                | 0.20 REF. |      |      | 0.20 REF. |      |      | 0.20 REF. |      |      | 0.20 REF. |      |      |
| b                 | 0.25      | 0.30 | 0.35 | 0.25      | 0.30 | 0.35 | 0.25      | 0.30 | 0.35 | 0.18      | 0.23 | 0.30 |
| D                 | 3.90      | 4.00 | 4.30 | 3.90      | 4.00 | 4.10 | 3.90      | 4.00 | 4.30 | 3.90      | 4.00 | 4.10 |
| E                 | 3.90      | 4.00 | 4.30 | 3.90      | 4.00 | 4.10 | 3.90      | 4.00 | 4.30 | 3.90      | 4.00 | 4.10 |
| e                 | 0.80 BSC. |      |      | 0.65 BSC. |      |      | 0.50 BSC. |      |      | 0.50 BSC. |      |      |
| k                 | 0.25      | -    | -    | 0.25      | -    | -    | 0.25      | -    | -    | 0.25      | -    | -    |
| L                 | 0.45      | 0.55 | 0.65 | 0.45      | 0.55 | 0.65 | 0.45      | 0.55 | 0.65 | 0.30      | 0.40 | 0.50 |
| N                 | 12        |      |      | 16        |      |      | 20        |      |      | 24        |      |      |
| ND                | 3         |      |      | 4         |      |      | 5         |      |      | 6         |      |      |
| NE                | 3         |      |      | 4         |      |      | 5         |      |      | 6         |      |      |
| Ver.              | WGGB      |      |      | WGGB      |      |      | WGGB-1    |      |      | WGGB-2    |      |      |

| EXPOSED PAD VARIATIONS |      |      |      |      |      |      |
|------------------------|------|------|------|------|------|------|
| PKG. CODES             | D2   |      |      | E2   |      |      |
|                        | MIN. | NOM. | MAX. | MIN. | NOM. | MAX. |
| T1244-2                | 1.95 | 2.10 | 2.25 | 1.95 | 2.10 | 2.25 |
| T1244-3                | 1.95 | 2.10 | 2.25 | 1.95 | 2.10 | 2.25 |
| T1244-4                | 1.95 | 2.10 | 2.25 | 1.95 | 2.10 | 2.25 |
| T1644-2                | 1.95 | 2.10 | 2.25 | 1.95 | 2.10 | 2.25 |
| T1644-3                | 1.95 | 2.10 | 2.25 | 1.95 | 2.10 | 2.25 |
| T1644-4                | 1.95 | 2.10 | 2.25 | 1.95 | 2.10 | 2.25 |
| T2044-1                | 1.95 | 2.10 | 2.25 | 1.95 | 2.10 | 2.25 |
| T2044-2                | 1.95 | 2.10 | 2.25 | 1.95 | 2.10 | 2.25 |
| T2044-3                | 1.95 | 2.10 | 2.25 | 1.95 | 2.10 | 2.25 |
| T2444-1                | 2.45 | 2.60 | 2.63 | 2.45 | 2.60 | 2.63 |
| T2444-2                | 1.95 | 2.10 | 2.25 | 1.95 | 2.10 | 2.25 |
| T2444-3                | 2.45 | 2.60 | 2.63 | 2.45 | 2.60 | 2.63 |
| T2444-4                | 2.45 | 2.60 | 2.63 | 2.45 | 2.60 | 2.63 |

### NOTES:

1. DIMENSIONING & TOLERANCING CONFORM TO ASME Y14.5M-1994.
2. ALL DIMENSIONS ARE IN MILLIMETERS. ANGLES ARE IN DEGREES.
3. N IS THE TOTAL NUMBER OF TERMINALS.

△ THE TERMINAL #1 IDENTIFIER AND TERMINAL NUMBERING CONVENTION SHALL CONFORM TO JEDEC 95-1 SFP-012. DETAILS OF TERMINAL #1 IDENTIFIER ARE OPTIONAL, BUT MUST BE LOCATED WITHIN THE ZONE INDICATED. THE TERMINAL #1 IDENTIFIER MAY BE EITHER A MOLD OR MARKED FEATURE.

△ DIMENSION b APPLIES TO METALLIZED TERMINAL AND IS MEASURED BETWEEN 0.25 mm AND 0.30 mm FROM TERMINAL TIP.

△ ND AND NE REFER TO THE NUMBER OF TERMINALS ON EACH D AND E SIDE RESPECTIVELY.

△ DEPOPULATION IS POSSIBLE IN A SYMMETRICAL FASHION.

△ COPLANARITY APPLIES TO THE EXPOSED HEAT SINK SLUG AS WELL AS THE TERMINALS.

9. DRAWING CONFORMS TO JEDEC MO220, EXCEPT FOR T2444-1, T2444-3 AND T2444-4.

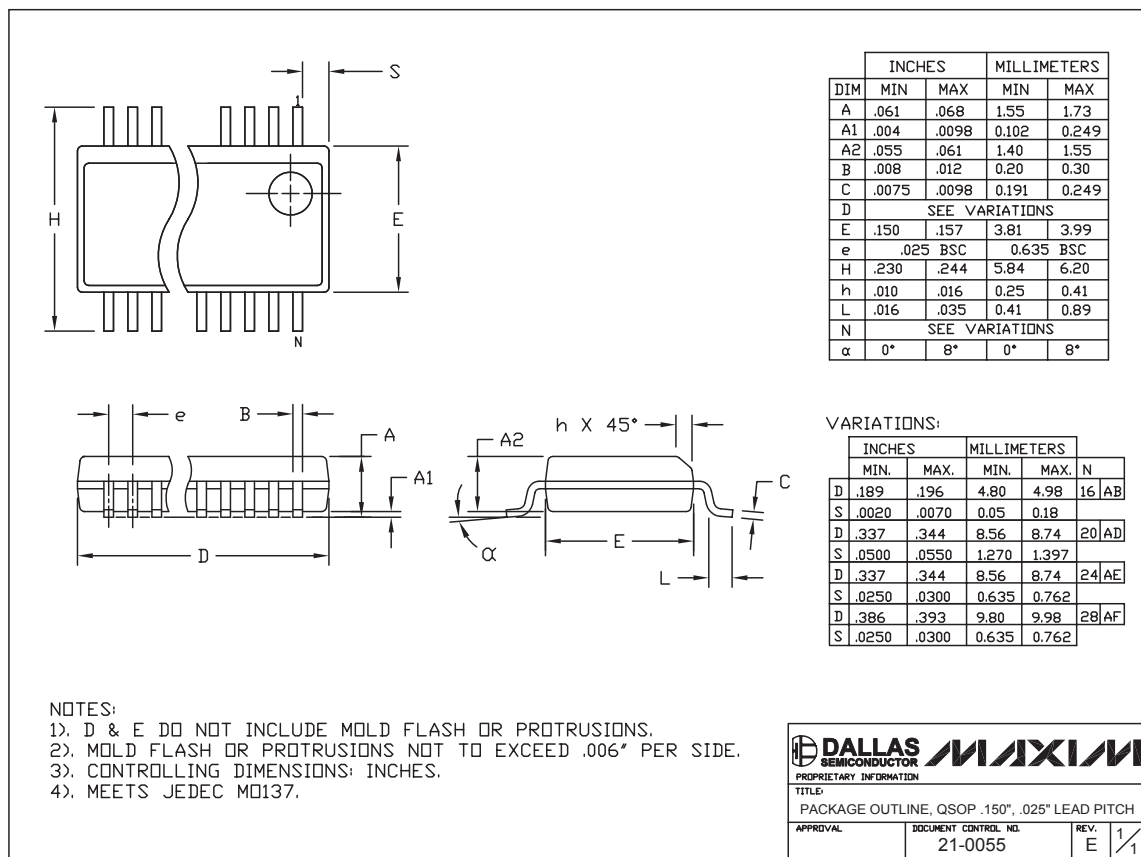
| DALLAS SEMICONDUCTOR                |                      |  |  |      |     |  |
|-------------------------------------|----------------------|--|--|------|-----|--|
| PROPRIETARY INFORMATION             |                      |  |  |      |     |  |
| TITLE PACKAGE OUTLINE               |                      |  |  |      |     |  |
| 12, 16, 20, 24L THIN QFN, 4x4x0.8mm |                      |  |  |      |     |  |
| APPROVAL                            | DOCUMENT CONTROL NO. |  |  | REV. |     |  |
|                                     | 21-0139              |  |  | C    | 2/2 |  |

# Dual, Audio, Log Taper Digital Potentiometers

## Package Information (continued)

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MAX5408-MAX5411



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