



Up to 8.0Gbps Dual Passive Switches

General Description

The MAX4888B/MAX4888C dual double-pole/double-throw (2 x DPDT), high-speed passive switches are ideal for switching two half-lanes of PCI Express® (PCIe) data between two possible destinations. These devices feature a dual digital control input to switch signal paths. The MAX4888C is intended for use in systems where both the input and output are capacitively coupled (e.g., SAS, SATA, XAUI, and PCIe) and provides a 10µA (typ) source current and a 60kΩ (typ) internal biasing resistor to GND at the AOUT_ and BOUT_ pins.

The devices are fully specified to operate from a single +3.3V (typ) power supply. Both devices are available in an industry-standard 3.5mm x 5.5mm, 28-pin TQFN package. They operate over the -40°C to +85°C extended temperature range.

Applications

Desktop PCs
Notebook PCs
Servers

Features

- ◆ Single +3.3V Power-Supply Voltage
- ◆ Supports PCIe Gen I, Gen II, and Gen III Data Rates
- ◆ Supports Up To and Including 6.0Gbps SAS/SATA Signals
- ◆ Supports Other High-Speed Interfaces (e.g., XAUI)
- ◆ Superior Bandwidth Return Loss
- ◆ Small, 3.5mm x 5.5mm, 28-Pin TQFN Package

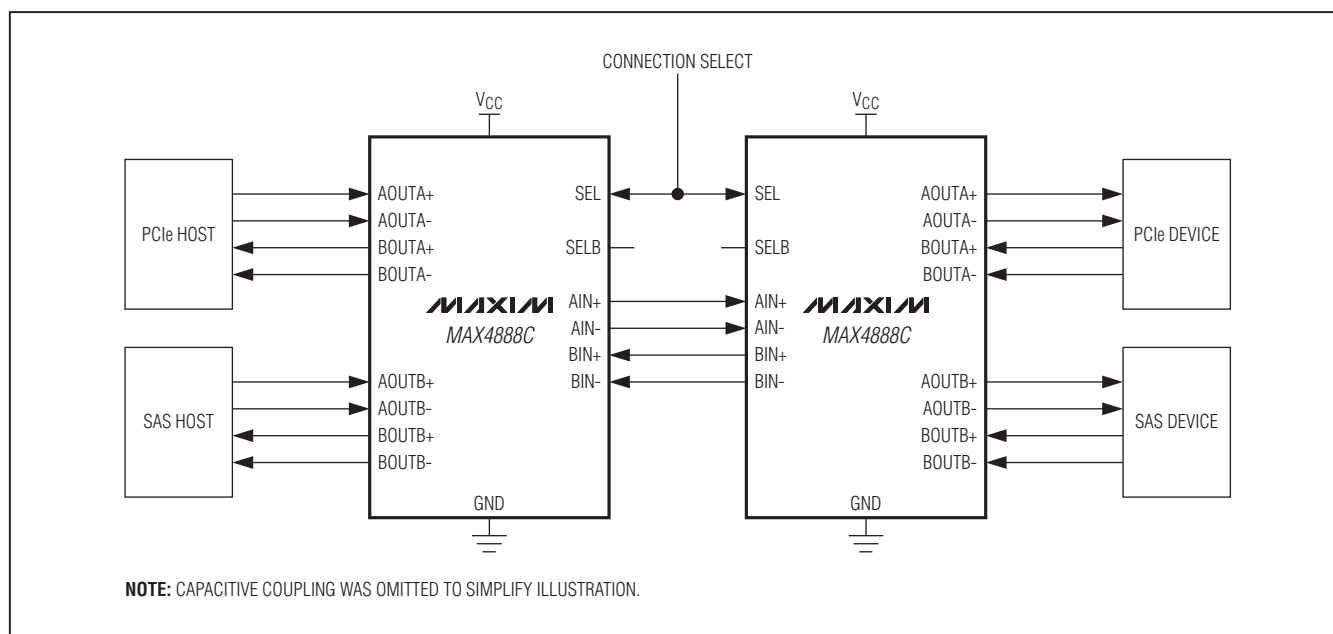
Ordering Information

PART	TEMP RANGE	PIN-PACKAGE
MAX4888BETI+	-40°C to +85°C	28 TQFN-EP*
MAX4888CETI+	-40°C to +85°C	28 TQFN-EP*

+ Denotes a lead(Pb)-free/RoHS-compliant package.

*EP = Exposed pad.

Typical Operating Circuit



PCI Express is a registered trademark of PCI-SIG Corp.

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ABSOLUTE MAXIMUM RATINGS

(All voltages referenced to GND, unless otherwise noted.)

V_{CC}.....-0.3V to +4V

SEL, SELB, AIN+, AIN-, BIN+, BIN-, AOUTA+,

AOUTA-, AOUTB+, AOUTB-, BOUTA+,

BOUTA-, BOUTB+, BOUTB- (Note 1) .. -0.3V to (V_{CC} + 0.3V)

Continuous Current (AIN_ to AOUTA_/AOUTB_,

BIN_ to BOUTA_/BOUTB_)..... ±15mA

Peak Current (AIN_ to AOUTA_/AOUTB_,

BIN_ to BOUTA_/BOUTB_) ..

(pulsed at 1ms, 10% duty cycle) ±70mA

Continuous Current (SEL, SELB) ±10mA

Peak Current (SEL, SELB)

(pulsed at 1ms, 10% duty cycle) ±10mA

Continuous Power Dissipation (T_A = +70°C)

TQFN (derate 28.6mW/°C above +70°C)..... 2286mW

Operating Temperature Range..... -40°C to +85°C

Junction Temperature +150°C

Storage Temperature Range..... -65°C to +150°C

Lead Temperature (soldering, 10s) +300°C

Soldering Temperature (reflow) +260°C

Note 1: Signals on SEL, SELB, AIN_, BIN_, AOUTA_, AOUTB_, BOUTA_, and BOUTB_ exceeding V_{CC} or GND are clamped by internal diodes. Limit forward-diode current to maximum current rating.

PACKAGE THERMAL CHARACTERISTICS (Note 2)

TQFN

Junction-to-Ambient Thermal Resistance (θ_{JA}) 35°C/W

Junction-to-Case Thermal Resistance (θ_{JC}) 2°C/W

Note 2: Package thermal resistances were obtained using the method described in JEDEC specification JESD51-7, using a four-layer board. For detailed information on package thermal considerations, refer to www.maxim-ic.com/thermal-tutorial.

Stresses beyond those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(V_{CC} = 3.3V ±10%, T_A = -40°C to +85°C, unless otherwise noted. Typical values are at V_{CC} = 3.3V, T_A = +25°C, unless otherwise noted.) (Note 3)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
DC PERFORMANCE						
Analog-Signal Range	V _{INPUT}	AIN_, BIN_, AOUTA_, BOUTA_, AOUTB_, BOUTB_	-0.3		V _{CC} - 1.8	V
On-Resistance	R _{ON}	V _{CC} = +3.0V, I _{AIN_} = I _{BIN_} = 15mA, V _{OUTA_} = V _{OUTB_} = 0V, 1.2V		6.4	8.4	Ω
On-Resistance Match Between Channels	ΔR _{ON}	V _{CC} = +3.0V, I _{AIN_} = I _{BIN_} = 15mA, V _{OUTA_} = V _{OUTB_} = 0V (Note 4)		0.2	1.5	Ω
On-Resistance Flatness	R _{FLAT(ON)}	V _{CC} = +3.0V, I _{AIN_} = I _{BIN_} = 15mA, V _{OUTA_} = V _{OUTB_} = 0V, 1.2V (Note 5)		0.3	1	Ω
OUTA or _OUTB_ Off-Leakage Current	I _{OUTA_(OFF)} , I _{OUTB_(OFF)}	V _{CC} = +3.6V, V _{AIN_} = V _{BIN_} = 0V, 1.2V; V _{OUTA_} or V _{OUTB_} = 1.2V, 0V (MAX4888B)	-1		+1	μA
AIN_, BIN_ On-Leakage Current	I _{AIN_(ON)} , I _{BIN_(ON)}	V _{CC} = +3.6V, V _{AIN_} = V _{BIN_} = 0V, 1.2V; V _{OUTA_} or V _{OUTB_} = V _{AIN_} = V _{BIN_} or unconnected (MAX4888B)	-1		+1	μA
Output Short-Circuit Current		All other ports are unconnected (MAX4888C)	5		15	μA
Output Open-Circuit Voltage		All other ports are unconnected (MAX4888C)	0.2	0.6	0.9	V

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MAX4888B/MAX4888C

ELECTRICAL CHARACTERISTICS (continued)

(V_{CC} = 3.3V ±10%, T_A = -40°C to +85°C, unless otherwise noted. Typical values are at V_{CC} = 3.3V, T_A = +25°C, unless otherwise noted.) (Note 3)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
AC PERFORMANCE						
Switch Turn-On Time	tON_SEL	ZS = ZL = 50Ω	65		ns	
Switch Turn-Off Time	tOFF_SEL	ZS = ZL = 50Ω, Figure 1, measured at 500MHz	7		ns	
Propagation Delay	tPD	ZS = ZL = 50Ω, Figure 2, measured at 500MHz	43		ps	
Output Skew Between Pairs	tSK1	ZS = ZL = 50Ω, Figure 2, measured at 500MHz	8		ps	
Output Skew Between Same Pair	tSK2	ZS = ZL = 50Ω, Figure2	10		ps	
Differential Return Loss (Note 6)	SDD11	0Hz < f ≤ 2.8GHz	-14		dB	
		2.8GHz < f ≤ 5.0GHz	-8			
		5.0GHz < f ≤ 8.0GHz	-5			
		f > 8.0GHz	-1			
Differential Insertion Loss	SDD21	Table 1			dB	
Bandwidth	SDD12/SDD21		8		GHz	
Differential Crosstalk (Note 6)	SDDCTK	0Hz < f ≤ 2.5GHz	-30		dB	
		2.5GHz < f ≤ 5.0GHz	-25			
		5.0GHz < f ≤ 8.0GHz	-35			
		f > 8.0GHz	-35			
Differential Off-Isolation (Note 6)	SDD21_OFF	0Hz < f ≤ 2.5GHz	-15		dB	
		2.5GHz < f ≤ 5.0GHz	-12			
		5.0GHz < f ≤ 8.0GHz	-12			
		f > 8.0GHz	-12			
CONTROL INPUT						
Input Logic-High	VIH		1.4		V	
Input Logic-Low	VIL		0.6		V	
Input Logic Hysteresis	VHYST		130		mV	
POWER SUPPLY						
Power-Supply Range	VCC		3.0	3.6	V	
VCC Supply Current	ICC		1		mA	

Note 3: All units are 100% production tested at T_A = +85°C. Limits over the operating temperature range are guaranteed by design and characterization and are not production tested.

Note 4: ΔRON = RON(MAX) - RON(MIN).

Note 5: Flatness is defined as the difference between the maximum and minimum value of on-resistance as measured over the specified analog-signal range.

Note 6: Guaranteed by design; not production tested.

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Test Circuits/Timing Diagrams

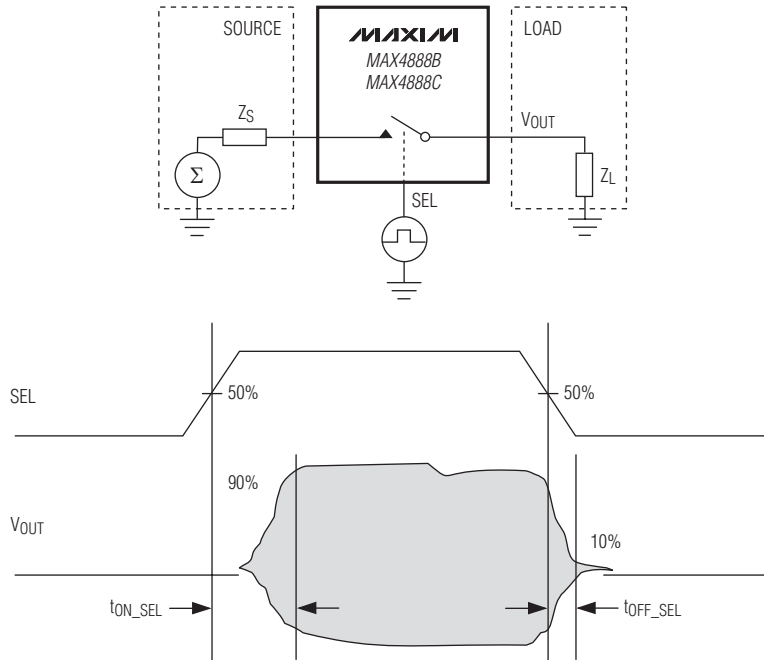


Figure 1. Switching Time

Table 1. Insertion Loss Mask

FREQUENCY RANGE (GHz)	MAXIMUM INSERTION LOSS (dB)
0 to 2.5	$1/3 \times f_{\text{GHz}} + 17/30$
2.5 to 5	$2/5 \times f_{\text{GHz}} - 2/5$
5 to 8	$18/5 \times f_{\text{GHz}} - 4/15$
Greater than 8	$2 \times f_{\text{GHz}} - 12$

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Test Circuits/Timing Diagrams (continued)

MAX4888B/MAX4888C

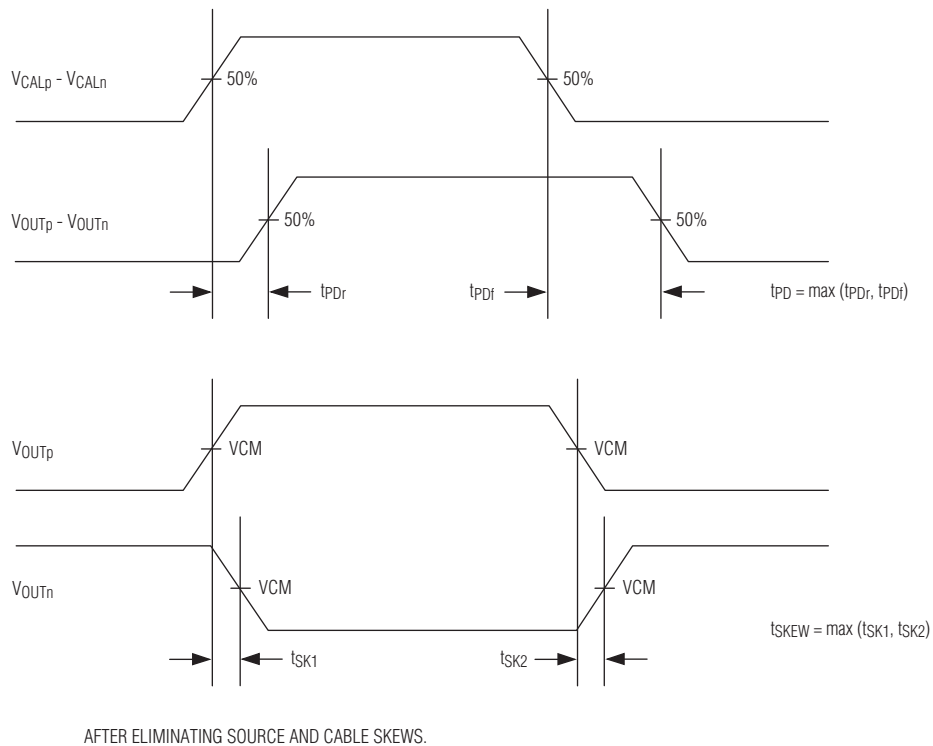
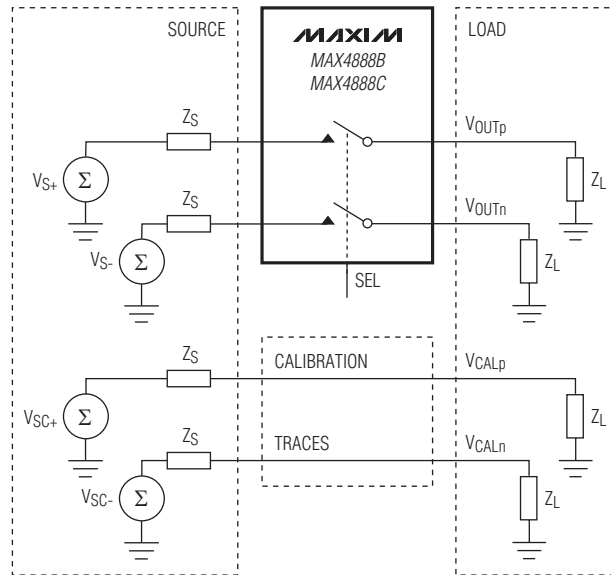
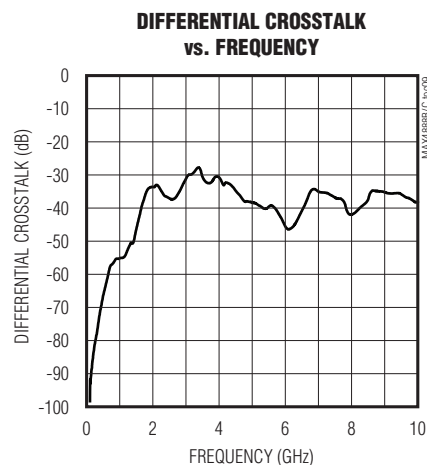
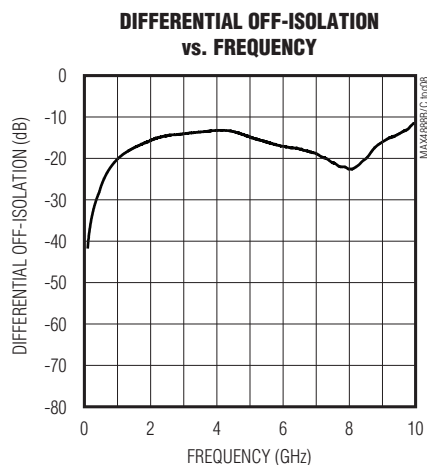
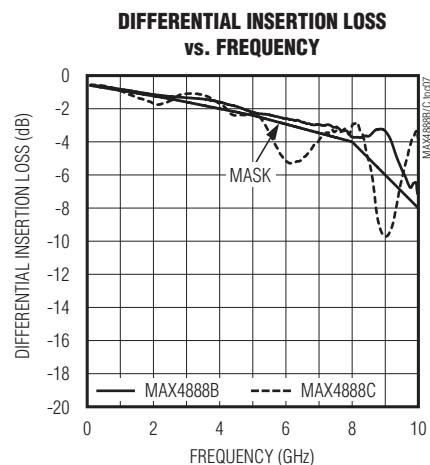
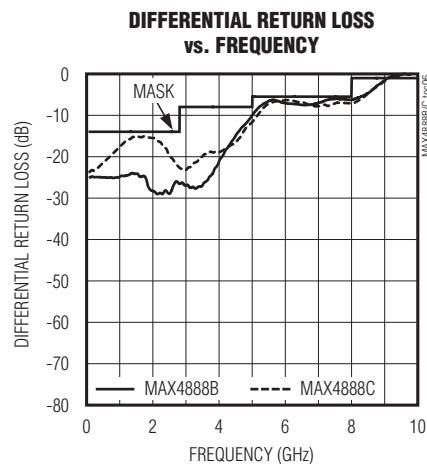
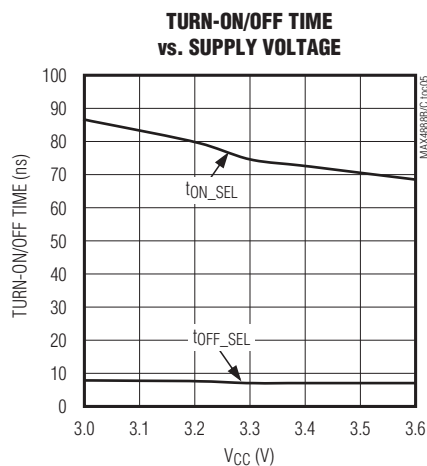
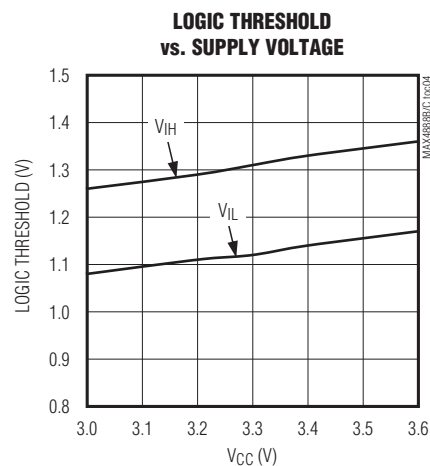
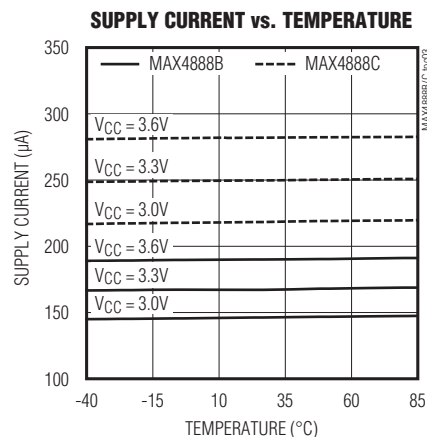
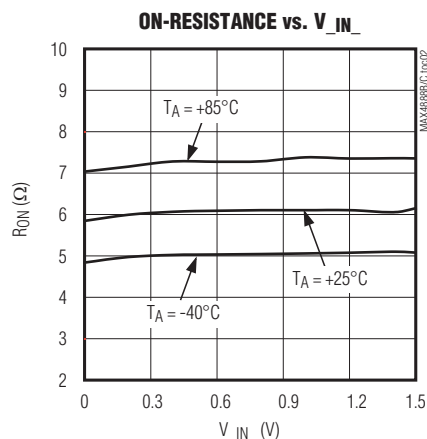
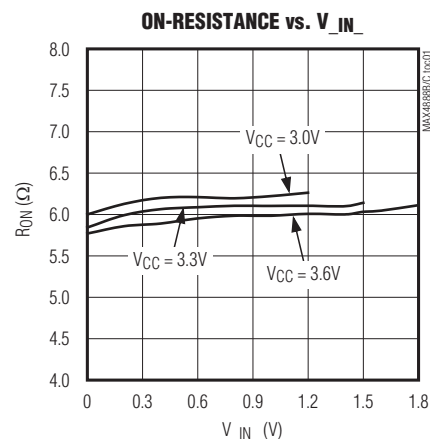


Figure 2. Propagation Delay and Output Skew

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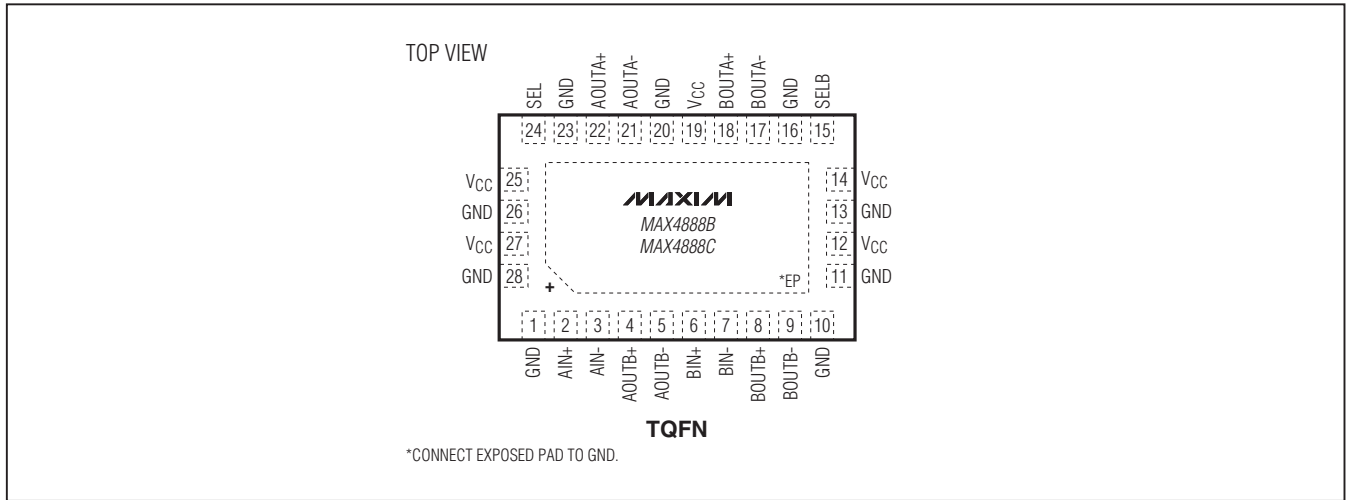
Typical Operating Characteristics

($V_{CC} = 3.3V$, $T_A = +25^\circ C$, unless otherwise noted.)



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Pin Configuration



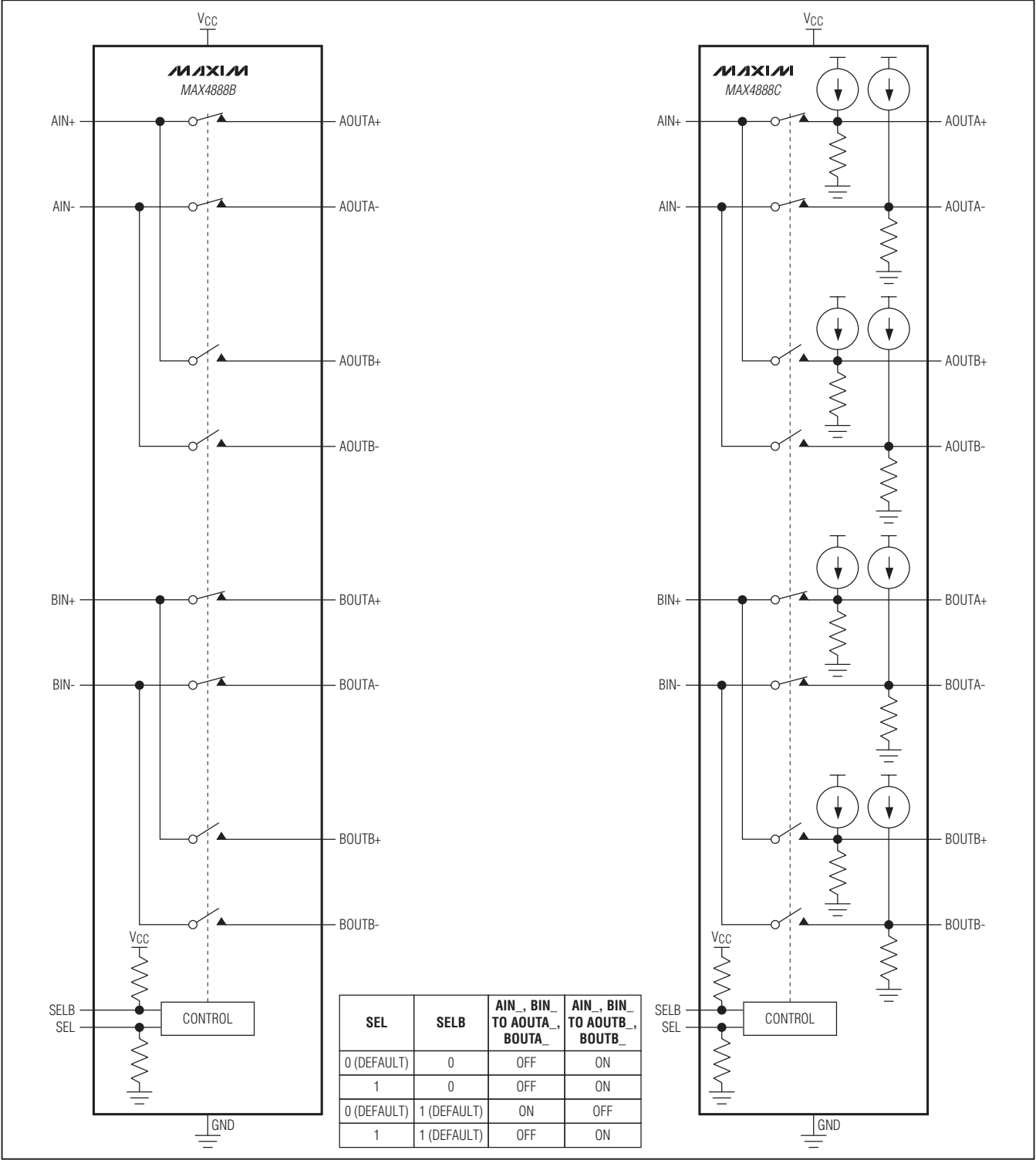
Pin Description

PIN	NAME	FUNCTION
1, 10, 11, 13, 16, 20, 23, 26, 28	GND	Ground
2	AIN+	Analog Switch 1, Common Positive Terminal
3	AIN-	Analog Switch 1, Common Negative Terminal
4	AOUTB+	Analog Switch 1, Normally Open Positive Terminal
5	AOUTB-	Analog Switch 1, Normally Open Negative Terminal
6	BIN+	Analog Switch 2, Common Positive Terminal
7	BIN-	Analog Switch 2, Common Negative Terminal
8	BOUTB+	Analog Switch 2, Normally Open Positive Terminal
9	BOUTB-	Analog Switch 2, Normally Open Negative Terminal
12, 14, 19, 25, 27	VCC	Positive Supply-Voltage Input. Connect VCC to a 3.0V to 3.6V supply voltage. Bypass VCC to GND with a 0.1μF ceramic capacitor placed as close as possible to the device. See the <i>Board Layout</i> section.
15	SELB	Control Signal Input. SELB has a 70kΩ (typ) pullup resistor to VCC. If SELB is not in use, leave unconnected.
17	BOUTA-	Analog Switch 2, Normally Closed Negative Terminal
18	BOUTA+	Analog Switch 2, Normally Closed Positive Terminal
21	AOUTA-	Analog Switch 1, Normally Closed Negative Terminal
22	AOUTA+	Analog Switch 1, Normally Closed Positive Terminal
24	SEL	Control Signal Input. SEL has a 70kΩ (typ) pulldown resistor to GND.
—	EP	Exposed Pad. Connect EP to GND.

MAX4888B/MAX4888C

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Functional Diagram/Truth Table



Up to 8.0Gbps Dual Passive Switches

Detailed Description

The MAX4888B high-speed passive switch routes high-speed differential signals such as PCIe, SAS, SATA, and XAUI from one source to two possible destinations or vice versa. The MAX4888B is ideal for routing PCIe signals to change the system configuration. The MAX4888C features a 10 μ A (typ) source current and a 60k Ω (typ) internal biasing resistor to GND at the AOUTA_, BOUTA_, AOUTB_, and BOUTB_ terminals. The MAX4888C is ideal for circuits that are capacitively coupled at both the output and input. These devices are protocol independent and can be used to switch two different protocol signals over the same physical lane. They feature dual digital control inputs (SEL, SELB) to switch signal paths. SEL has a 70k Ω (typ) pulldown resistor to GND and SELB has a 70k Ω (typ) pullup resistor to VCC.

These devices are fully specified to operate from a single 3.0V to 3.6V power supply.

Digital Control Input (SEL, SELB)

The devices provide dual digital control inputs (SEL, SELB) to select the signal path between the AIN_, BIN_ and AOUTA_, BOUTA_ or AOUTB_, BOUTB_ channels. In most cases SEL is chosen and SELB is unconnected. The truth table for the devices is depicted in the *Functional Diagram/Truth Table*. SEL has a 70k Ω (typ) pulldown resistor to GND and SELB has a 70k Ω (typ) pullup resistor to VCC.

Analog-Signal Levels

The devices accept signals from -0.3V to (VCC - 1.8V). Signals on the AIN+ and BIN+ channels are routed to either the AOUTA+, BOUTA+ or AOUTB+, BOUTB+ channels. Signals on the AIN- and BIN- channels are routed to either the AOUTA-, BOUTA- or AOUTB-, BOUTB- channels. The devices are bidirectional switches, allowing AIN_, BIN_ and AOUTA_, BOUTA_, AOUTB_, and BOUTB_ to be used as either inputs or outputs.

Applications Information

High-Speed Switching

The devices' primary applications are aimed at sharing resources. For example, a single lane of PCIe or SAS can be shared between a single host and two devices. This could be used for redundancy or to share resources such as a physical lane or route a lane between one host and two devices or two hosts and one device.

Board Layout

High-speed switches require proper layout and design procedures for optimum performance. Keep controlled impedance PCB traces as short as possible or follow impedance layouts per the PCIe specification. Ensure that power-supply bypass capacitors are placed as close as possible to the device. Multiple bypass capacitors are recommended. Connect all grounds and the exposed pad to a large ground plane.

Chip Information

PROCESS: CMOS

Package Information

For the latest package outline information and land patterns, go to www.maxim-ic.com/packages. Note that a "+", "#", or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

PACKAGE TYPE	PACKAGE CODE	OUTLINE NO.	LAND PATTERN NO.
28 TQFN-EP	T283555+1	21-0184	90-0123

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Revision History

REVISION NUMBER	REVISION DATE	DESCRIPTION	PAGES CHANGED
0	12/10	Initial release	—

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