



Single/Dual/Quad, Low-Cost, UCSP/SOT23, Low-Power, Rail-to-Rail I/O Op Amps

General Description

The MAX4322/MAX4323/MAX4326/MAX4327/MAX4329 family of operational amplifiers combines wide bandwidth and excellent DC accuracy with Rail-to-Rail® operation at the inputs and outputs. These devices consume only 650µA per amplifier and operate from either a single supply (2.4V to 6.5V) or dual supplies ($\pm 1.2V$ to $\pm 3.25V$). These unity-gain-stable amplifiers are capable of driving 250Ω loads and have a 5MHz gain-bandwidth product. The MAX4323 and MAX4327 feature a low-power shutdown mode that reduces supply current to 25µA and places the outputs in a high-impedance state.

With their rail-to-rail input common-mode range and output swing, these amplifiers are ideal for low-voltage, single-supply operation. In addition, low offset voltage and high speed make them the ideal signal-conditioning stages for precision, low-voltage data-acquisition systems.

The MAX4323 is offered in a small 6-bump chip-scale package (UCSP™). The MAX4322/MAX4323 are also available in space-saving SOT23 packages.

Selector Guide

PART	BW (MHz)	NO. OF AMPS	PIN/BUMP-PACKAGE	SHUTDOWN
MAX4322	5	1	5 SOT23, 8 µMAX/SO	—
MAX4323	5	1	6 SOT23/UCSP, 8 µMAX/SO	Yes
MAX4326	5	2	8 µMAX/SO	—
MAX4327	5	2	10 µMAX, 14 SO	Yes
MAX4329	5	4	14 SO	—

Applications

Battery-Powered Instruments	Data-Acquisition Systems
RSSI Systems	Signal Conditioning
PA Biasing	Portable Equipment
Low-Power, Low-Voltage Applications	

Rail-to-Rail is a registered trademark of Nippon Motorola, Ltd.

UCSP is a trademark of Maxim Integrated Products, Inc.

Features

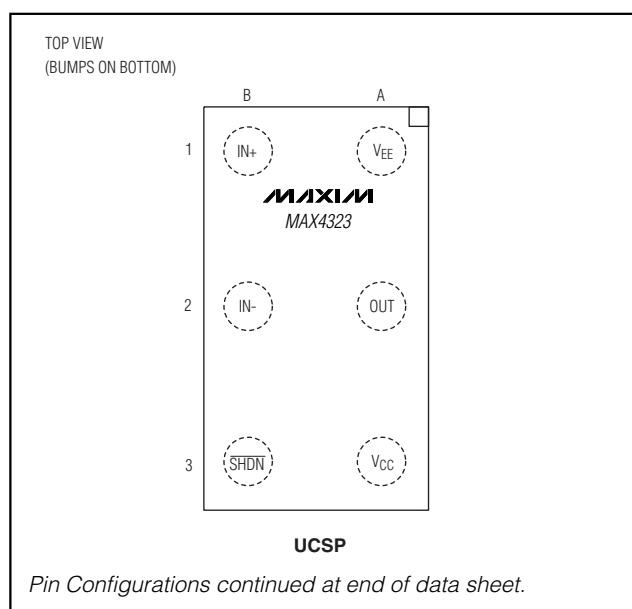
- ◆ 6-Bump UCSP Package (MAX4323)
- ◆ 2.4V to 6.5V Single-Supply Operation
- ◆ Rail-to-Rail Input Common-Mode Voltage Range
- ◆ Rail-to-Rail Output Voltage Swing
- ◆ 5MHz Gain-Bandwidth Product
- ◆ 650µA Quiescent Current per Amplifier
- ◆ 700µV Offset Voltage
- ◆ No Phase Reversal for Overdriven Inputs
- ◆ Drive 250Ω Loads
- ◆ 25µA Shutdown Mode (MAX4323/MAX4327)
- ◆ Unity-Gain Stable for Capacitive Loads Up to 500pF

Ordering Information

PART	TEMP RANGE	PIN/BUMP-PACKAGE	TOP MARK
MAX4322EUK-T	-40°C to +85°C	5 SOT23-5	ACGE
MAX4322EUA	-40°C to +85°C	8 µMAX	—
MAX4322ESA	-40°C to +85°C	8 SO	—

Ordering Information continued at end of data sheet.

Pin Configurations



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ABSOLUTE MAXIMUM RATINGS

Supply Voltage ($V_{CC} - V_{EE}$) 7.5V
 All Other Pins ($V_{CC} + 0.3V$) to ($V_{EE} - 0.3V$)
 Output Short-Circuit Duration Continuous
 (Short to Either Supply)
 Continuous Power Dissipation ($T_A = +70^\circ\text{C}$)
 5-Pin SOT23 (derate 7.1mW/ $^\circ\text{C}$ above $+70^\circ\text{C}$) 571mW
 6-Bump UCSP (derate 3.9mW/ $^\circ\text{C}$ above $+70^\circ\text{C}$) 308mW
 6-Pin SOT23 (derate 7.1mW/ $^\circ\text{C}$ Above $+70^\circ\text{C}$) 571mW
 8-Pin SO (derate 5.88mW/ $^\circ\text{C}$ above $+70^\circ\text{C}$) 471mW

8-Pin μMAX (derate 4.10mW/ $^\circ\text{C}$ above $+70^\circ\text{C}$) 330mW
 10-Pin μMAX (derate 5.6mW/ $^\circ\text{C}$ above $+70^\circ\text{C}$) 444mW
 14-Pin SO (derate 8.00mW/ $^\circ\text{C}$ above $+70^\circ\text{C}$) 640mW
 Operating Temperature Range
 MAX432_E__ -40°C to $+85^\circ\text{C}$
 Maximum Junction Temperature $+150^\circ\text{C}$
 Storage Temperature Range -65°C to $+160^\circ\text{C}$
 Bump Reflow Temperature $+235^\circ\text{C}$
 Lead Temperature (soldering, 10s) $+300^\circ\text{C}$

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC ELECTRICAL CHARACTERISTICS— $T_A = +25^\circ\text{C}$

($V_{CC} = 5.0V$, $V_{EE} = 0V$, $V_{CM} = 0V$, $V_{OUT} = V_{CC}/2$, $\overline{\text{SHDN}} = V_{CC}$, R_L connected to $V_{CC}/2$, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Input Offset Voltage	V_{OS}	$V_{CM} = V_{EE}$ or V_{CC}	MAX432_ESA/ MAX4327ESD	± 0.7	± 2.0		mV
			All other packages	± 1.2	± 2.50		
Input Bias Current	I_B	$V_{CM} = V_{EE}$ or V_{CC}		± 50	± 150		nA
Input Offset Current	I_{OS}	$V_{CM} = V_{EE}$ or V_{CC}		± 1	± 12		nA
Differential Input Resistance	R_{IN}	$-1.5V < V_{DIFF} < +1.5V$		500			k Ω
Common-Mode Input Voltage Range	CMVR	Inferred from CMRR test		V_{EE}		V_{CC}	V
Common-Mode Rejection Ratio	CMRR	$V_{EE} \leq V_{CM} \leq V_{CC}$	MAX432_ESA/ MAX4327ESD	62	94		dB
			All other packages	60	91		
Power-Supply Rejection Ratio	PSRR	$V_{CC} = 2.4V$ to $6.5V$		66	100		dB
Output Resistance	R_{OUT}	$A_V = +1V/V$		0.1			Ω
Large-Signal Voltage Gain	A_V	$V_{OUT} = 0.25V$ to $4.75V$, $R_L = 100k\Omega$		106			dB
		$V_{OUT} = 0.4V$ to $4.6V$, $R_L = 250\Omega$		70	86		
Output Voltage Swing	V_O	MAX4322/ MAX4323	$R_L = 100k\Omega$	$V_{CC} - V_{OH}$	12		mV
				$V_{OL} - V_{EE}$	20		
			$R_L = 250\Omega$	$V_{CC} - V_{OH}$	200	300	
				$V_{OL} - V_{EE}$	100	200	
		MAX4326/ MAX4327/ MAX4329	$R_L = 100k\Omega$	$V_{CC} - V_{OH}$	15		
				$V_{OL} - V_{EE}$	25		
			$R_L = 250\Omega$	$V_{CC} - V_{OH}$	220	350	
				$V_{OL} - V_{EE}$	120	250	
Output Short-Circuit Current	I_{SC}			50			mA
$\overline{\text{SHDN}}$ Logic Threshold	V_{IL}	MAX4323/MAX4327	Low		0.8		V
	V_{IH}		High	2.0			
$\overline{\text{SHDN}}$ Input Current		MAX4323/MAX4327		± 1	± 4		μA

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DC ELECTRICAL CHARACTERISTICS— $T_A = +25^\circ\text{C}$ (continued)

($V_{CC} = 5\text{V}$, $V_{EE} = 0\text{V}$, $V_{CM} = 0\text{V}$, $V_{OUT} = V_{CC}/2$, $\overline{\text{SHDN}} = V_{CC}$, R_L connected to $V_{CC}/2$, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Operating Supply Voltage Range	V_{CC}	Inferred from PSRR test		2.4		6.5	V
Supply Current per Amplifier	I_{CC}	$V_{CM} = V_{OUT} = V_{CC}/2$	$V_{CC} = 2.4\text{V}$		650		μA
			$V_{CC} = 5\text{V}$		725	1100	
Shutdown Supply Current per Amplifier	$I_{\overline{\text{SHDN}}}$	$V_{\overline{\text{SHDN}}} \leq 0.8\text{V}$, MAX4323/MAX4327	$V_{CC} = 2.4\text{V}$		25		μA
			$V_{CC} = 5\text{V}$		40	60	

DC ELECTRICAL CHARACTERISTICS— $T_A = -40^\circ\text{C}$ to $+85^\circ\text{C}$

($V_{CC} = 5\text{V}$, $V_{EE} = 0\text{V}$, $V_{CM} = 0\text{V}$, $V_{OUT} = V_{CC}/2$, $\overline{\text{SHDN}} = V_{CC}$, R_L connected to $V_{CC}/2$, unless otherwise noted.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Input Offset Voltage	V _{OS}	V _{CM} = V _{EE} or V _{CC}	MAX432_ESA/ MAX4327ESD			±3.0	mV
			All other packages			±6.0	
Input Offset Voltage Tempco	TCV _{OS}				±2		μV/°C
Input Bias Current	I _B	V _{CM} = V _{EE} or V _{CC}				±180	nA
Input Offset Current	I _{OS}	V _{CM} = V _{EE} or V _{CC}				±20	nA
Common-Mode Input Voltage Range	CMVR	Inferred from CMRR test		V _{EE}		V _{CC}	V
Common-Mode Rejection Ratio	CMRR	V _{EE} ≤ V _{CM} ≤ V _{CC}	MAX432_ESA/ MAX4327ESD	59			dB
			All other packages	54			
Power-Supply Rejection Ratio	PSRR	V _{CC} = 2.4V to 6.5V		62			dB
Large-Signal Voltage Gain	A _V	V _{OUT} = 0.4V to 4.6V, R _L = 250Ω		66			dB
Output Voltage Swing	V _O	MAX4322/ MAX4323	R _L = 250Ω	V _{CC} - V _{OH}		350	mV
				V _{OL} - V _{EE}		250	
		MAX4326/ MAX4327/ MAX4329	R _L = 250Ω	V _{CC} - V _{OH}		400	
				V _{OL} - V _{EE}		300	
SHDN Logic Threshold	V _{IL}	MAX4323/MAX4327		Low		0.8	V
	V _{IH}			High	2.0		
SHDN Input Current		MAX4323/MAX4327				±5	μA
Operating Supply Voltage Range	V _{CC}			2.4		6.5	V
Supply Current per Amplifier	I _{CC}	V _{CM} = V _{OUT} = V _{CC} /2				1200	μA
Shutdown Supply Current per Amplifier	I _{SHDN}	V _{SHDN} ≤ 0.8V, MAX4323/MAX4327				70	μA

MAX4322/MAX4323/MAX4326/MAX4327/MAX4329

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AC ELECTRICAL CHARACTERISTICS

($V_{CC} = 5V$, $V_{EE} = 0V$, $V_{CM} = V_{OUT} = V_{CC}/2$, $\overline{SHDN} = V_{CC}$, $T_A = +25^\circ C$, unless otherwise noted.)

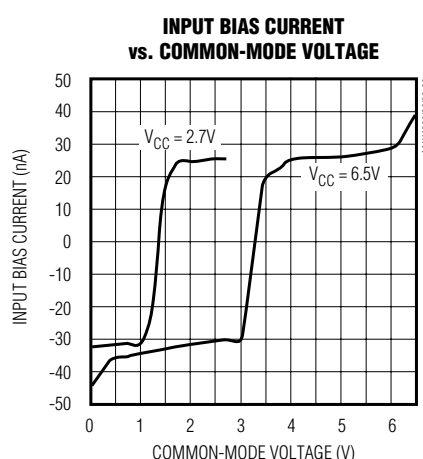
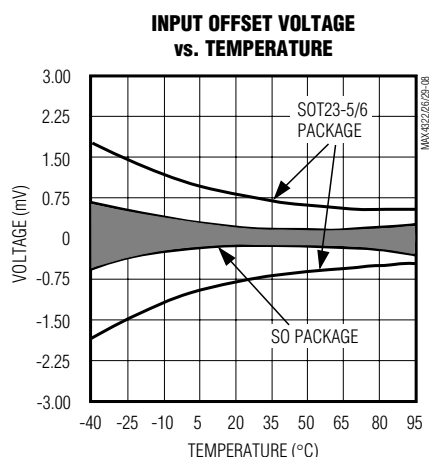
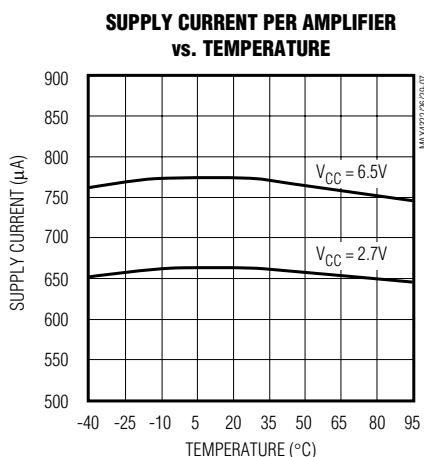
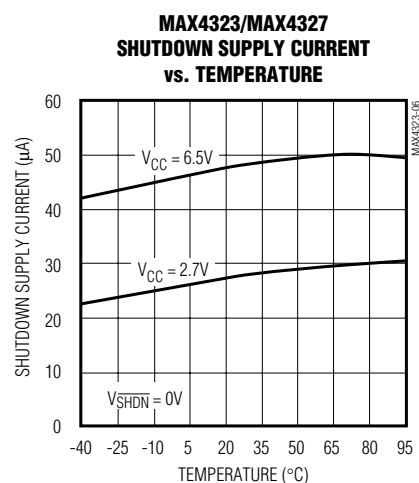
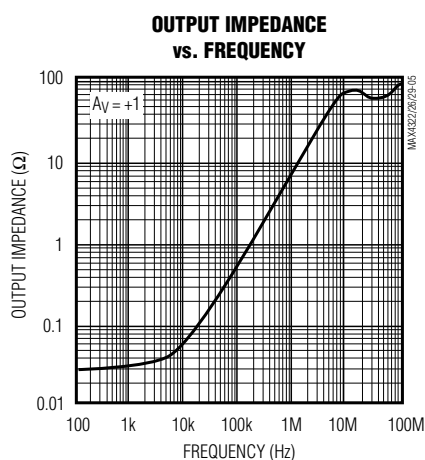
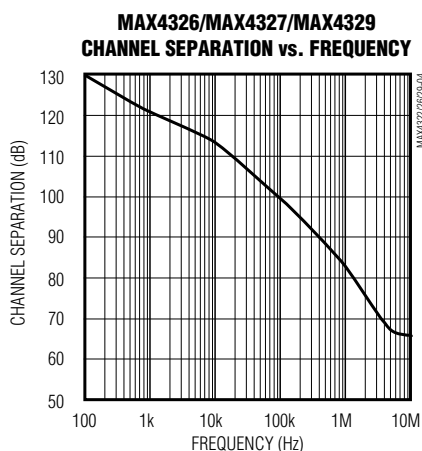
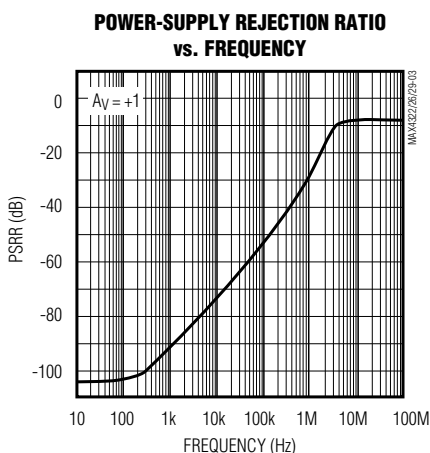
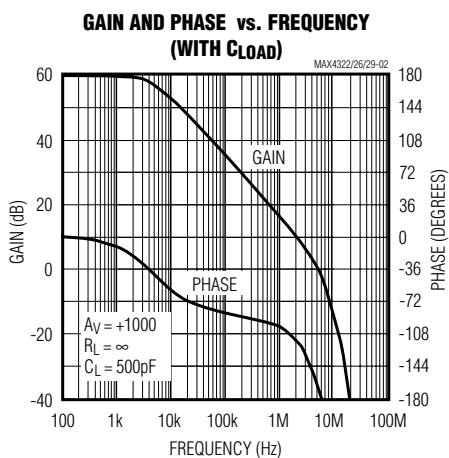
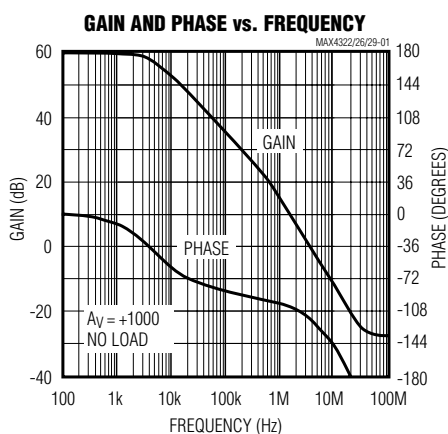
PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Gain-Bandwidth Product	GBWP			5		MHz
Phase Margin	ϕ_M			64		Degrees
Gain Margin	GM			12		dB
Total Harmonic Distortion	THD	$f = 10kHz$, $V_{OUT} = 2V_{P-P}$, $A_V = +1V/V$		0.003		%
Slew Rate	SR			2		V/ μs
Settling Time to 0.01%	t_S	$A_V = +1V/V$, $V_{OUT} = 2V$ step		2.0		μs
Turn-On Time	t_{ON}	$V_{CC} = 0$ to 3V step		1		μs
$\overline{SHDN}$ Delay		MAX4323/MAX4327	Enable	1		μs
			Disable	0.2		
Input Capacitance	C_{IN}			3		pF
Input Noise-Voltage Density	e_n	$f = 1kHz$		22		nV/ $\sqrt{Hz}$
Input Noise-Current Density	i_n	$f = 1kHz$		0.4		pA/ $\sqrt{Hz}$
Amp-Amp Isolation				135		dB
Capacitive-Load Stability	C_L	$A_V = +1V/V$		250		pF

Note 1: All devices are 100% tested at $T_A = +25^\circ C$. All temperature limits are guaranteed by design.

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Typical Operating Characteristics

($V_{CC} = 5V$, $V_{EE} = 0V$, $V_{CM} = V_{CC}/2$, $\overline{SHDN} = V_{CC}$, $T_A = +25^\circ C$, unless otherwise noted.)

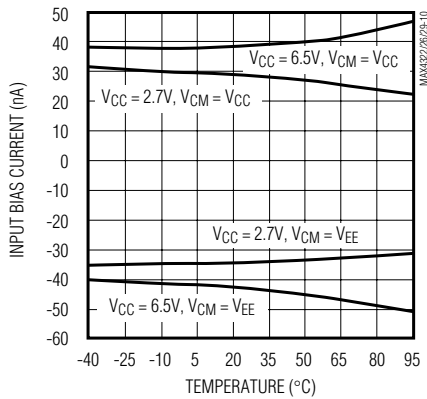


Single/Dual/Quad, Low-Cost, UCSP/SOT23, Low-Power, Rail-to-Rail I/O Op Amps

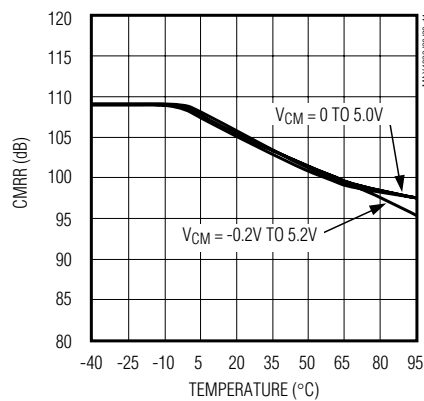
Typical Operating Characteristics (continued)

($V_{CC} = 5V$, $V_{EE} = 0V$, $V_{CM} = V_{CC}/2$, $\overline{SHDN} = V_{CC}$, $T_A = +25^\circ C$, unless otherwise noted.)

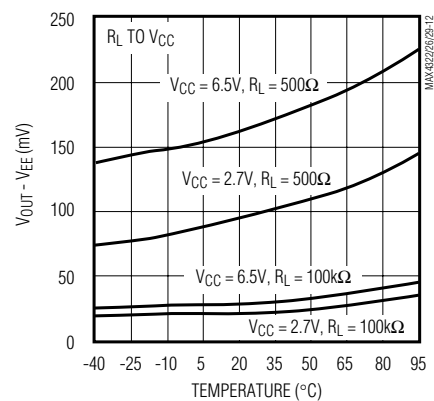
**INPUT BIAS CURRENT
vs. TEMPERATURE**



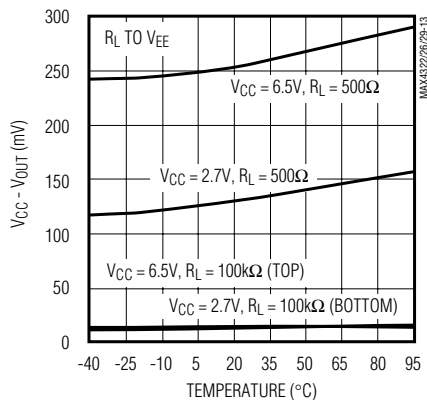
**COMMON-MODE REJECTION RATIO
vs. TEMPERATURE**



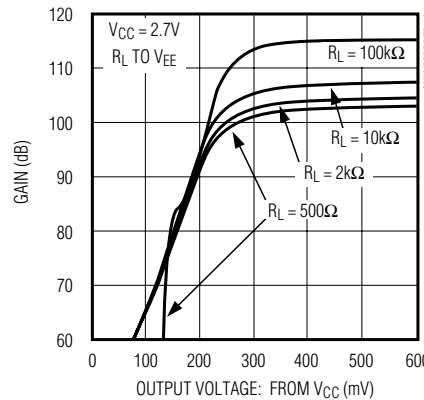
**MINIMUM OUTPUT VOLTAGE
vs. TEMPERATURE**



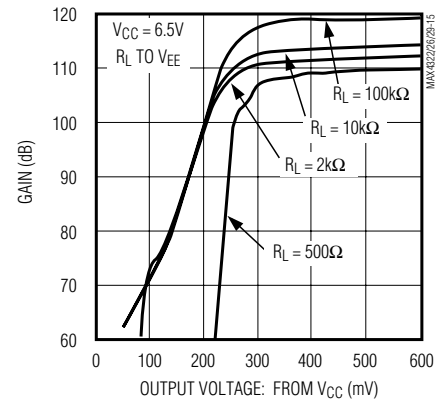
**MAXIMUM OUTPUT VOLTAGE
vs. TEMPERATURE**



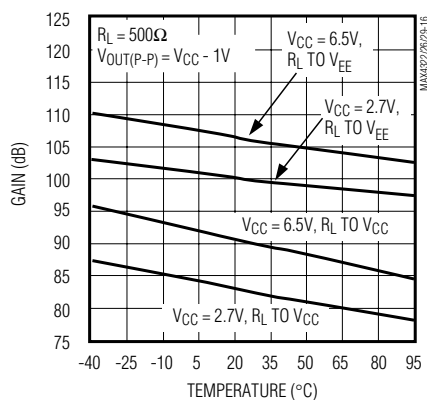
**LARGE-SIGNAL GAIN
vs. OUTPUT VOLTAGE**



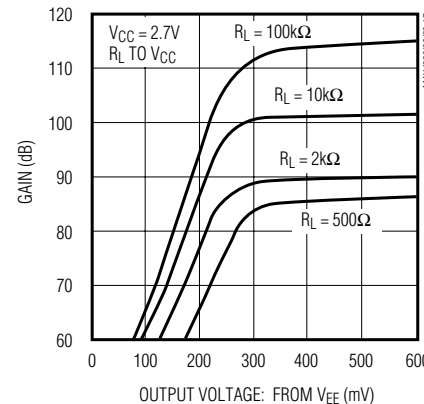
**LARGE-SIGNAL GAIN
vs. OUTPUT VOLTAGE**



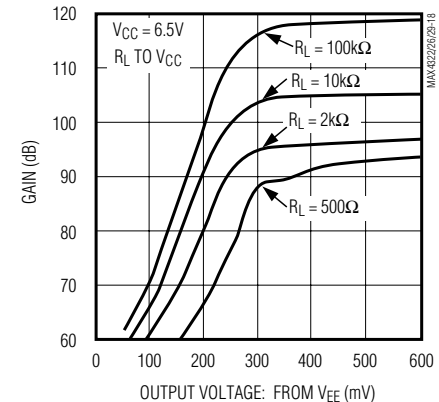
**LARGE-SIGNAL GAIN
vs. TEMPERATURE**



**LARGE-SIGNAL GAIN
vs. OUTPUT VOLTAGE**



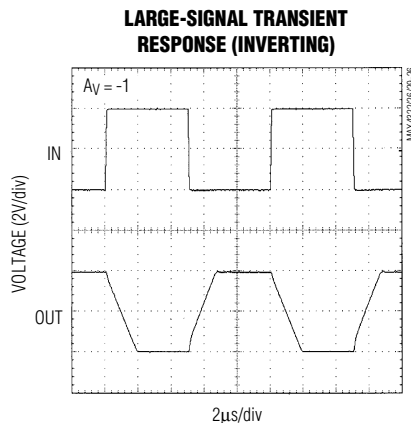
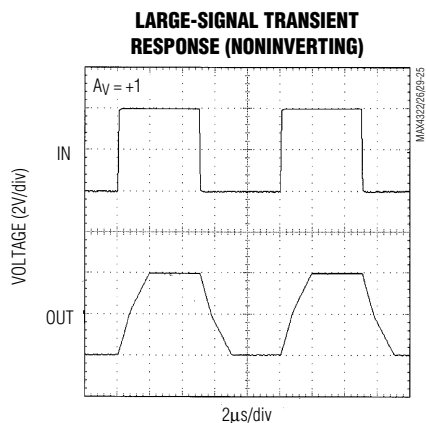
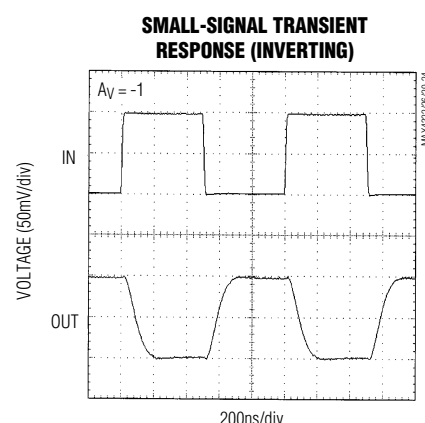
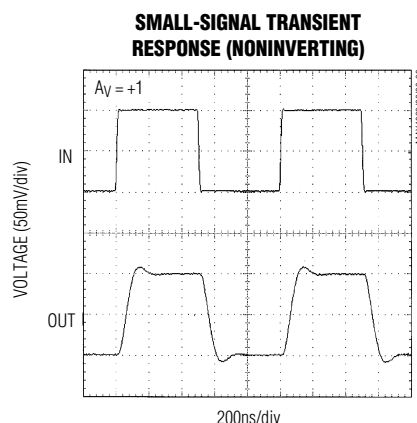
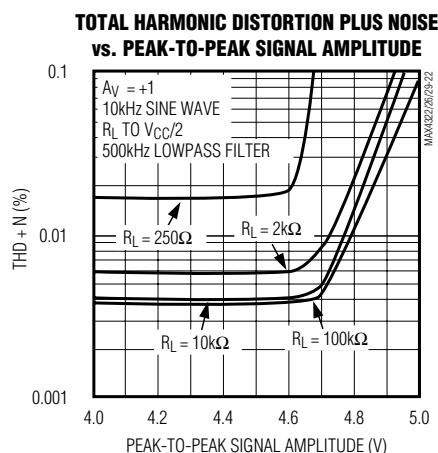
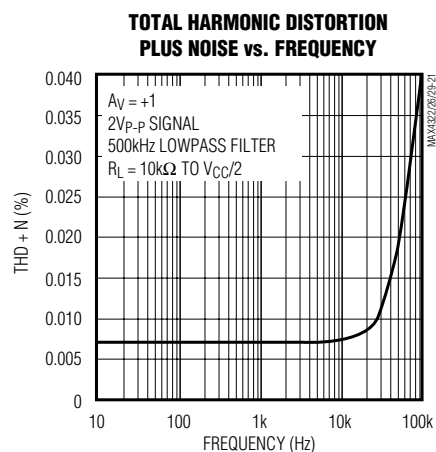
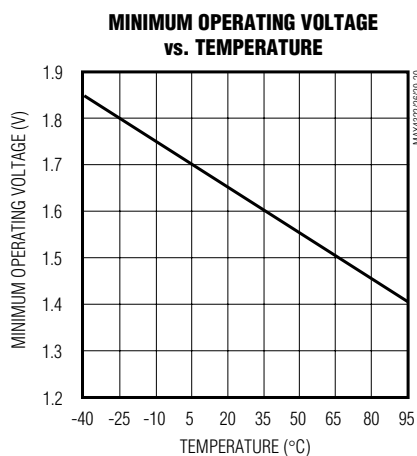
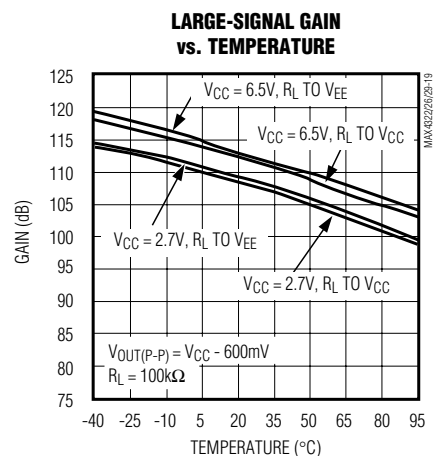
**LARGE-SIGNAL GAIN
vs. OUTPUT VOLTAGE**



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Typical Operating Characteristics (continued)

($V_{CC} = 5V$, $V_{EE} = 0V$, $V_{CM} = V_{CC}/2$, $\overline{SHDN} = V_{CC}$, $T_A = +25^\circ C$, unless otherwise noted.)



Single/Dual/Quad, Low-Cost, UCSP/SOT23, Low-Power, Rail-to-Rail I/O Op Amps

Pin Description

PIN									NAME	FUNCTION
MAX4322		MAX4323			MAX4326	MAX4327		MAX4329		
SOT23	SO/μMAX	SOT23	SO/μMAX	UCSP		μMAX	SO			
1	6	1	6	A2	—	—	—	—	OUT	Output
2	4	2	4	A1	4	4	4	11	V _{EE}	Negative Supply. Ground for single-supply operation.
3	—	3	3	B1	—	—	—	—	IN+	Noninverting Input
4	—	4	2	B2	—	—	—	—	IN-	Inverting Input
5	7	6	7	A3	8	10	14	4	V _{CC}	Positive Supply
—	1, 5, 8	—	1, 5	—	—	—	5, 7, 8, 10	—	N.C.	No Connection. Not internally connected.
—	—	5	8	B3	—			—	$\overline{\text{SHDN}}$	Shutdown Control. Connected high or leave floating to enable amplifier.
—	—	—	—	—	1, 7	1, 9	1, 13	1, 7	OUT1, OUT2	Outputs for Amps 1 and 2
—	2	—	—	—	2, 6	2, 8	2, 12	2, 6	IN1-, IN2-	Inverting Inputs for Amps 1 and 2
—	3	—	—	—	3, 5	3, 7	3, 11	3, 5	IN1+, IN2+	Noninverting Inputs for Amps 1 and 2
—	—	—	—	—	—	5, 6	5, 9	—	$\overline{\text{SHDN1}}$, $\overline{\text{SHDN2}}$	Shutdown Control for Amps 1 and 2. Connected high or leave floating to enable amplifier.
—	—	—	—	—	—	—	—	8, 14	OUT3, OUT4	Outputs for Amps 3 and 4
—	—	—	—	—	—	—	—	9, 13	IN3-, IN4-	Inverting Inputs for Amps 3 and 4
—	—	—	—	—	—	—	—	10, 12	IN3+, IN4+	Noninverting Inputs for Amps 3 and 4

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Applications Information

Rail-to-Rail Input Stage

Devices in the MAX4322/MAX4323/MAX4326/MAX4327/MAX4329 family of high-speed amplifiers have rail-to-rail input and output stages designed for low-voltage, single-supply operation. The input stage consists of separate NPN and PNP differential stages, which combine to provide an input common-mode range extending to the supply rails. The PNP stage is active for input voltages close to the negative rail, and the NPN stage is active for input voltages near the positive rail. The input offset voltage is typically below 250 μ V. The switchover transition region, which occurs near $V_{CC}/2$, has been extended to minimize the slight degradation in CMRR caused by the mismatch of the input pairs. Their low offset voltage, high bandwidth, and rail-to-rail common-mode range make these op amps excellent choices for precision, low-voltage, data-acquisition systems.

Since the input stage switches between the NPN and PNP pairs, the input bias current changes polarity as the input voltage passes through the transition region. To reduce the offset error caused by input bias currents flowing through external source impedances, match the effective impedance seen by each input (Figures 1a, 1b). High-source impedances, together with the input capacitance, can create a parasitic pole that produces an underdamped signal response. Reducing the input impedance or placing a small (2pF to 10pF) capacitor across the feedback resistor improves the response.

The MAX4322/MAX4323/MAX4326/MAX4327/MAX4329s' inputs are protected from large differential input voltages by 1k Ω series resistors and back-to-back triple diodes across the inputs (Figure 2). For differential input voltages less than 1.8V, the input resistance is typically 500k Ω . For differential input voltages greater than 1.8V, the input resistance is approximately 2k Ω , and the input bias current is determined by the following equation:

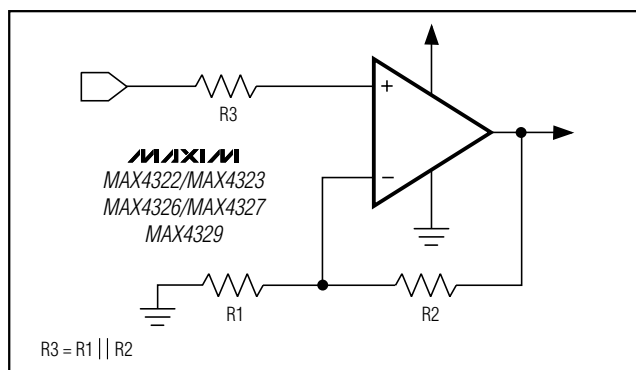


Figure 1a. Reducing Offset Error Due to Bias Current (Noninverting)

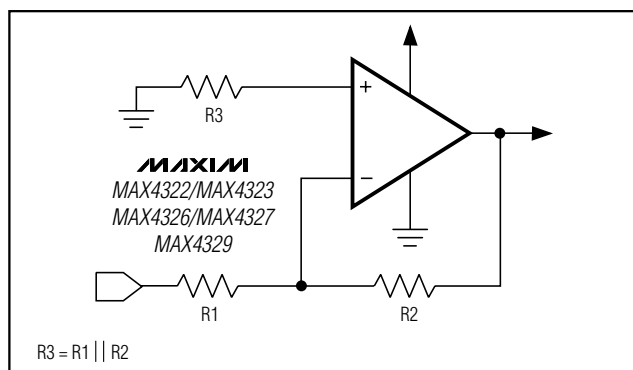


Figure 1b. Reducing Offset Error Due to Bias Current (Inverting)

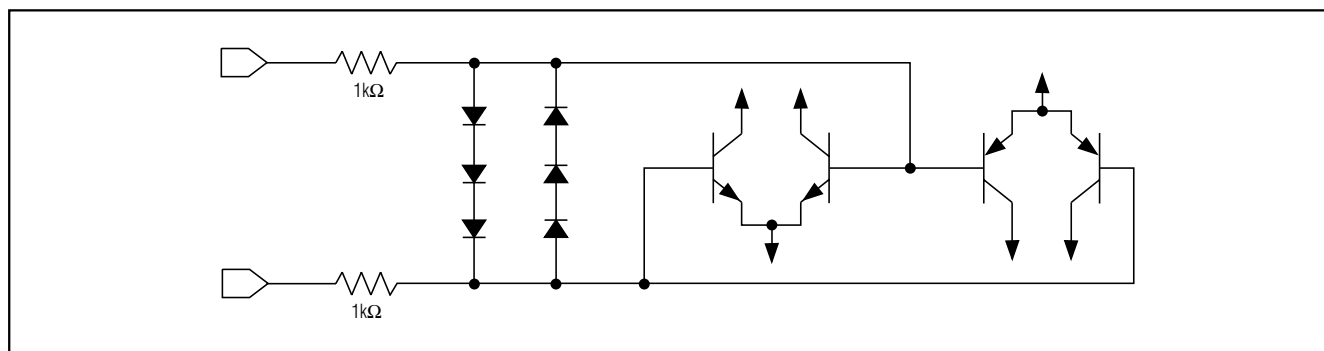


Figure 2. Input Protection Circuit

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$$I_{BIAS} = \frac{V_{DIFF} - 1.8V}{2k\Omega}$$

Rail-to-Rail Output Stage

The minimum output voltage is within millivolts of ground for single-supply operation where the load is referenced to ground (V_{EE}). Figure 3 shows the input voltage range and output voltage swing of a MAX4322 connected as a voltage follower. With a 3V supply and the load tied to ground, the output swings from 0 to 2.90V. The maximum output voltage swing depends on the load, but is within 350mV of a 5V supply, even with the maximum load (500Ω to ground).

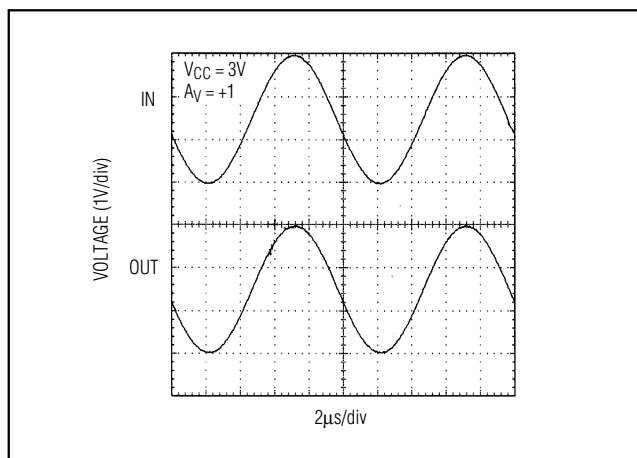


Figure 3. Rail-to-Rail Input/Output Voltage Range

Driving a capacitive load can cause instability in most high-speed op amps, especially those with low quiescent current. The MAX4322/MAX4323/MAX4326/MAX4327/MAX4329 have a high tolerance for capacitive loads. They are stable with capacitive loads up to 500pF. Figure 4 gives the stable operating region for capacitive loads. Figures 5 and 6 show the response with capacitive loads and the results of adding an isolation resistor in series with the output (Figure 7). The resistor improves the circuit's phase margin by isolating the load capacitor from the op amp's output.

Power-Up and Shutdown Mode

The MAX4322/MAX4323/MAX4326/MAX4327/MAX4329 amplifiers typically settle within $1\mu s$ after power-up.

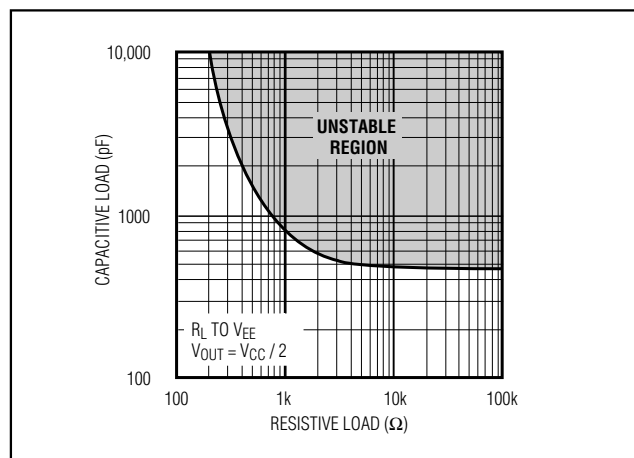


Figure 4. Capacitive-Load Stability

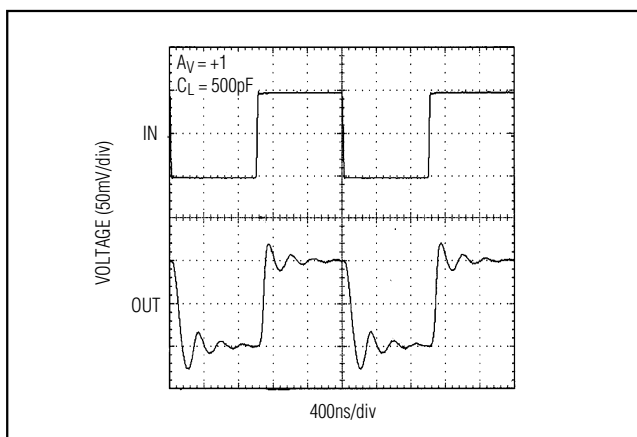


Figure 5. Small-Signal Transient Response with Capacitive Load

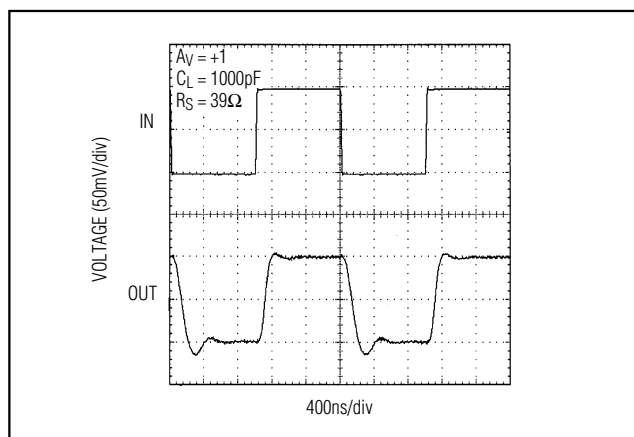


Figure 6. Transient Response to Capacitive Load with Isolation Resistor

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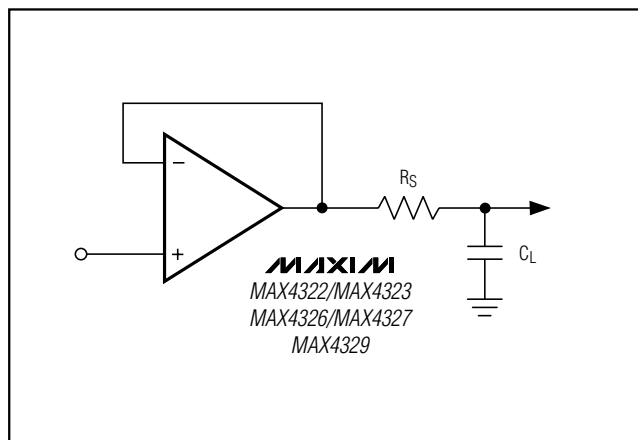


Figure 7. Capacitive-Load-Driving Circuit

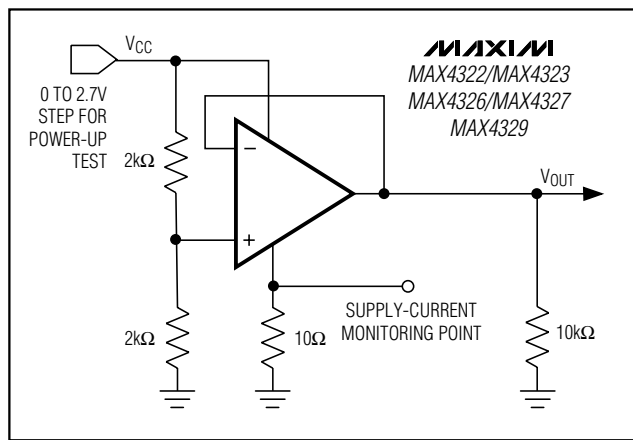


Figure 8. Power-Up Test Circuit

Figures 9 and 10 show the output voltage and supply current on power-up of the test circuit in Figure 8.

The MAX4323 and MAX4327 have a shutdown option. When shutdown (SHDN) is pulled low, the supply current drops to 25μA per amplifier and the amplifiers are disabled with the outputs in a high-impedance state. Pulling SHDN high or leaving it floating (1μA internal pullup) enables the amplifier. In the dual-amplifier MAX4327, the shutdown functions operate independently. Figures 11 and 12 show the output voltage and supply current responses of the MAX4323 to a shutdown pulse.

Power Supplies and Layout

The MAX4322/MAX4323/MAX4326/MAX4327/MAX4329 operate from a single 2.4V to 6.5V power supply, or from dual supplies of ±1.2V to ±3.25V. For single-supply operation, bypass the power supply with a 0.1μF ceramic capacitor in parallel with at least 1μF. For dual supplies, bypass each supply to ground.

Good layout improves performance by decreasing the amount of stray capacitance at the op amp's inputs and outputs. To decrease stray capacitance, minimize trace lengths and resistor leads by placing external components close to the op amp.

UCSP Information

Layout Issues

Design the layout for the device to be as compact as possible to minimize parasitics. The UCSP uses a bump pitch of 0.5mm (19.7mil) and a bump diameter of 0.33mm (~12mil). Therefore, lay out the solder-pad spacing on 0.5mm (19.7mil) centers, using a pad size of 0.25mm (~10mil) and a solder mask opening of

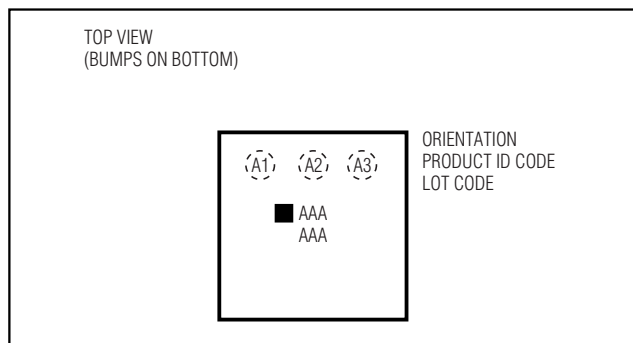
0.33mm (13mil). Round or square pads are permissible. Connect multiple vias from the ground plane as close to the ground connections as possible.

Install capacitors as close as possible to the device supply voltage input. Place the ground end of these capacitors near the ground plane to provide a low-impedance return path for the signal current.

Prototype Chip Installation

Alignment keys on the PC board, around the area where the chip is located, are helpful in the prototype assembly process. It is better to align the chip on the board before any other components are placed, and then place the board on a hot plate or hot surface until the solder starts melting. Remove the board from the hot plate without disturbing the position of the chip and let it cool down to room temperature before processing the board further.

MAX4323EBT (UCSP) Marking Information



MAX4322/MAX4323/MAX4326/MAX4327/MAX4329

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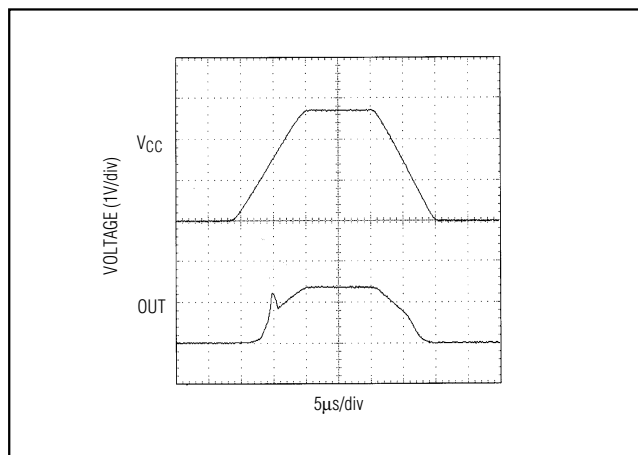


Figure 9. Power-Up Output Voltage

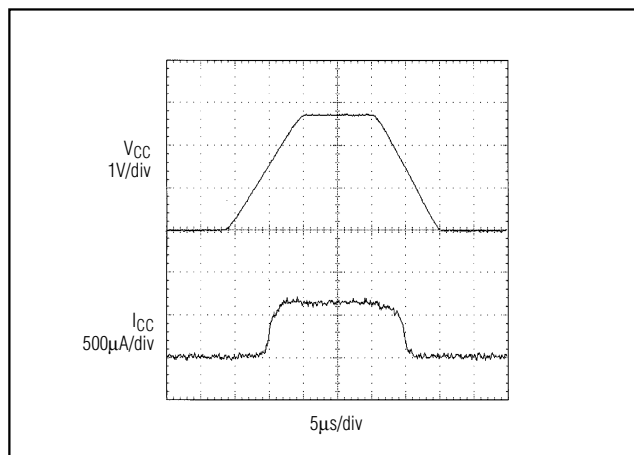


Figure 10. Power-Up Supply Current

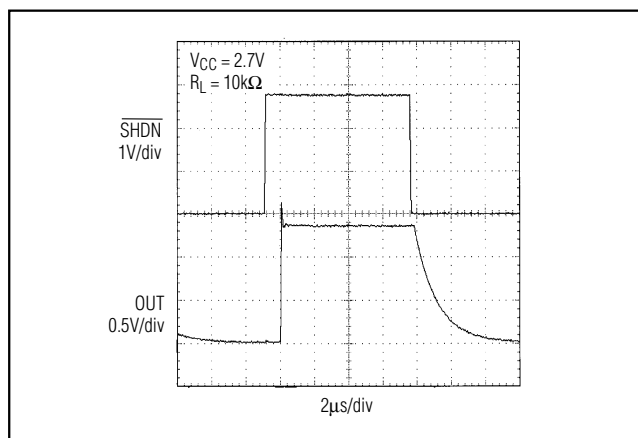


Figure 11. Shutdown Output Voltage

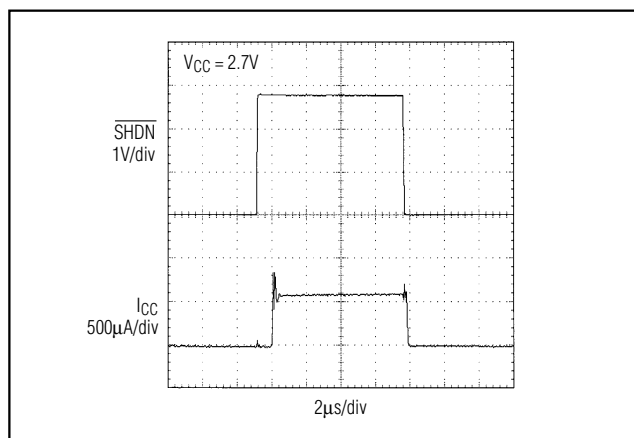
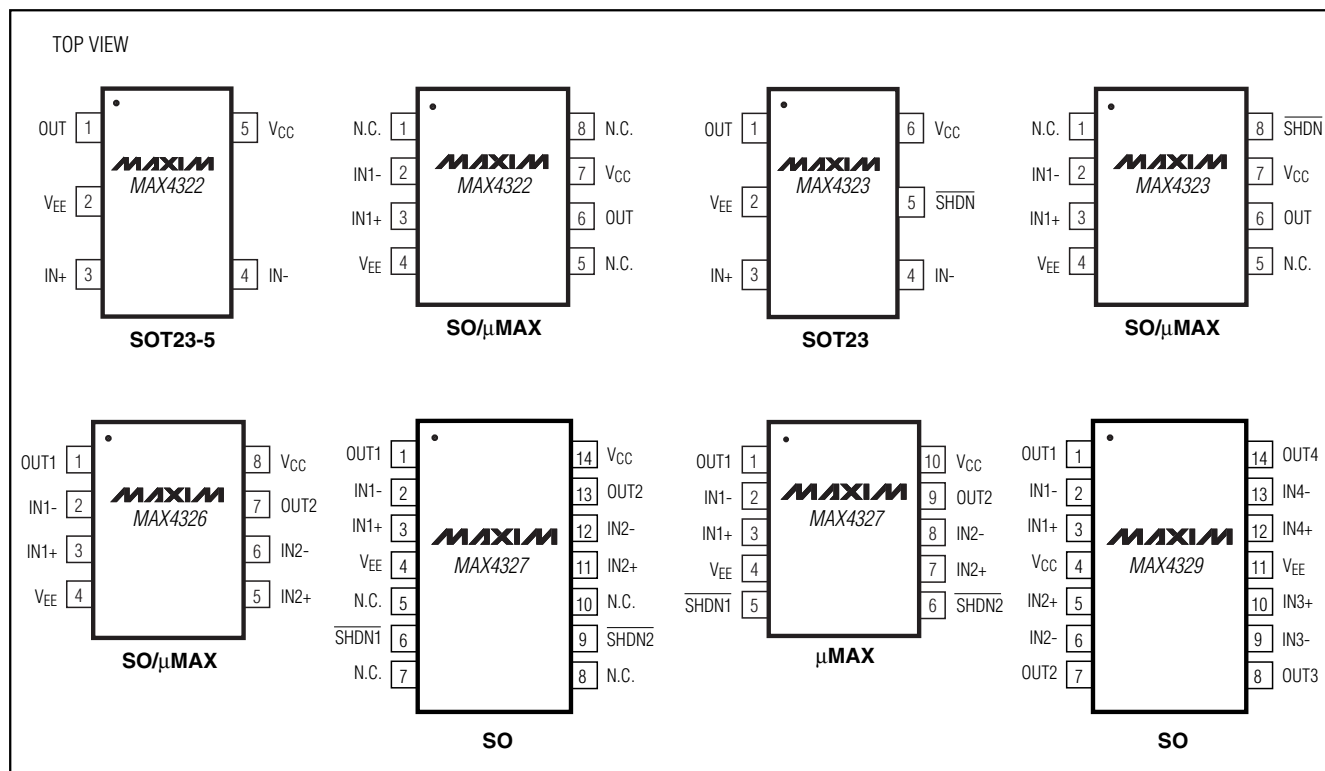


Figure 12. Shutdown Enable/Disable Supply Current

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Pin Configurations (continued)



UCSP Reliability

The UCSP represents a unique packaging form factor that may not perform as well as a packaged product through traditional mechanical reliability tests. UCSP reliability is integrally linked to the user's assembly methods, circuit board material, and usage environment. The user should closely review these areas when considering use of a UCSP.

Performance through operating-life test and moisture resistance remains uncompromised. The wafer-fabrication process primarily determines the performance. Mechanical stress performance is a greater consideration for UCSPs. UCSPs are attached through direct solder contact to the user's PC board, foregoing the inherent stress relief of a packaged product lead frame. Solder-joint contact integrity must be considered. Comprehensive reliability tests have been performed and are available upon request. In conclusion, the UCSP performs reliably through environmental stresses.

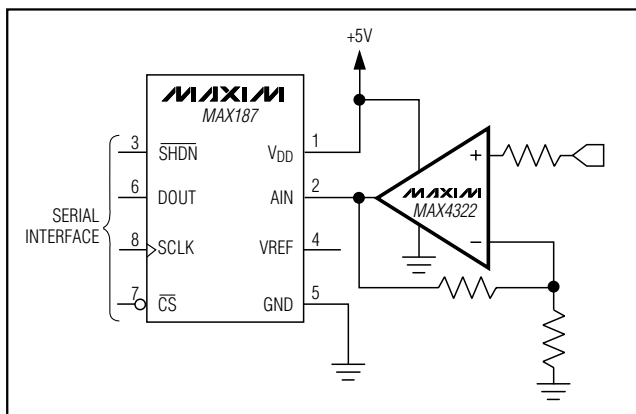
Ordering Information (continued)

PART	TEMP RANGE	PIN/BUMP-PACKAGE	TOP MARK
MAX4323EBT-T*	-40°C to +85°C	6 UCSP-6	AAW
MAX4323EUT-T	-40°C to +85°C	6 SOT23-6	AAEC
MAX4323EUA	-40°C to +85°C	8 μMAX	—
MAX4323ESA	-40°C to +85°C	8 SO	—
MAX4326EUA	-40°C to +85°C	8 μMAX	—
MAX4326ESA	-40°C to +85°C	8 SO	—
MAX4327EUB	-40°C to +85°C	10 μMAX	—
MAX4327ESD	-40°C to +85°C	14 SO	—
MAX4329ESD	-40°C to +85°C	14 SO	—

*UCSP reliability is integrally linked to the user's assembly methods, circuit board material, and environment. See the UCSP Reliability Notice in the UCSP Reliability section of this data sheet for more information.

Single/Dual/Quad, Low-Cost, UCSP/SOT23, Low-Power, Rail-to-Rail I/O Op Amps

Typical Operating Circuit

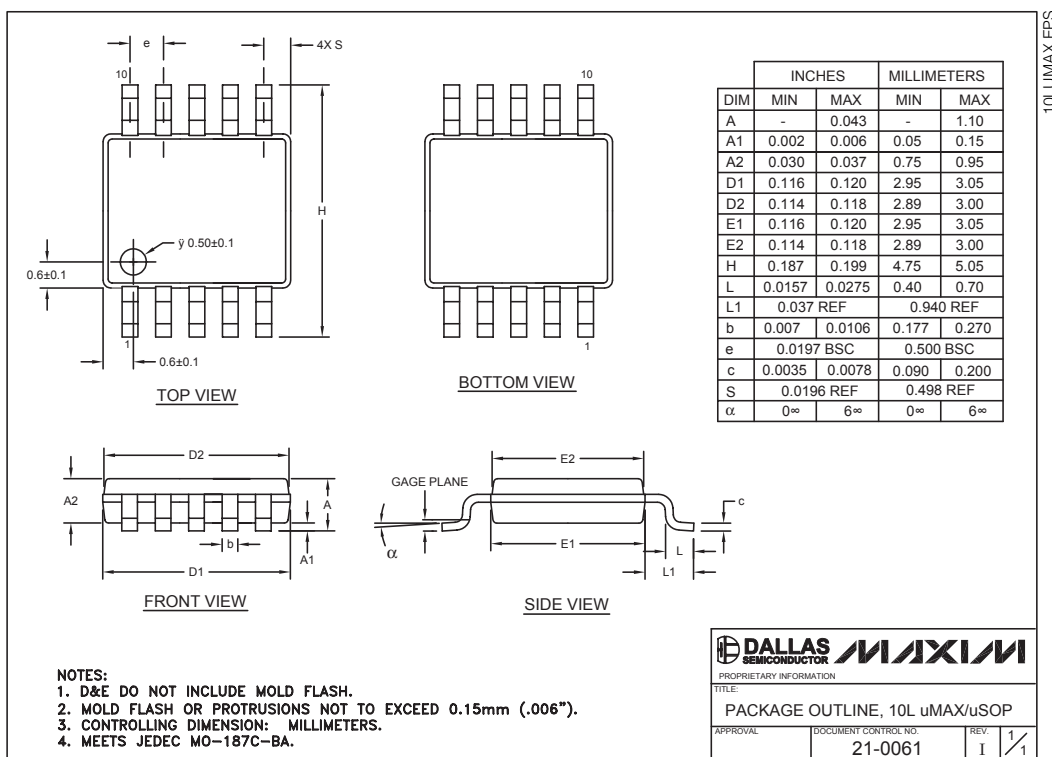


Chip Information

MAX4322 TRANSISTOR COUNT: 170
 MAX4323 TRANSISTOR COUNT: 170
 MAX4326 TRANSISTOR COUNT: 340
 MAX4327 TRANSISTOR COUNT: 340
 MAX4329 TRANSISTOR COUNT: 680
 PROCESS: Bipolar
 SUBSTRATE CONNECTED TO VEE

Package Information

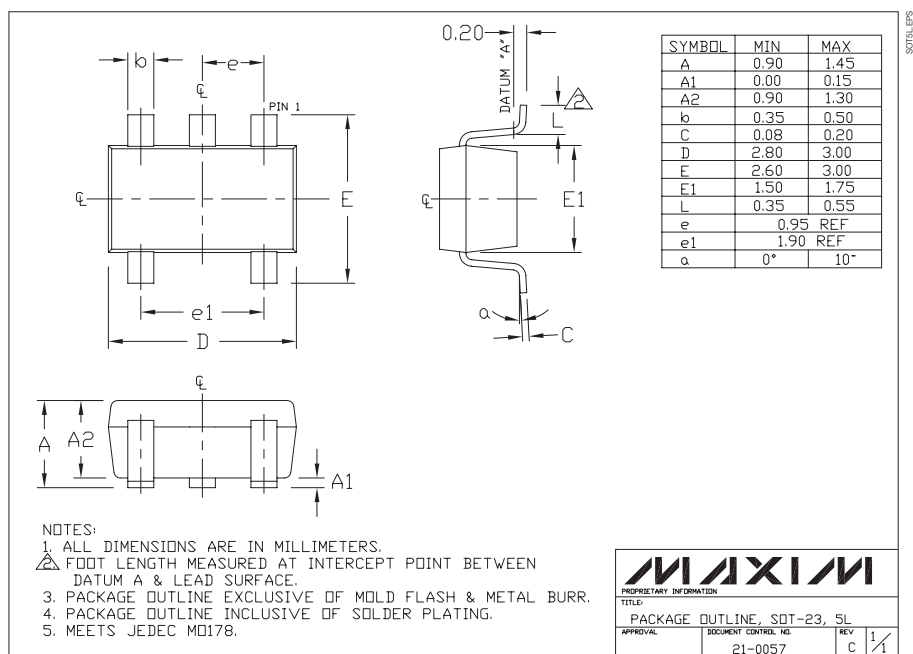
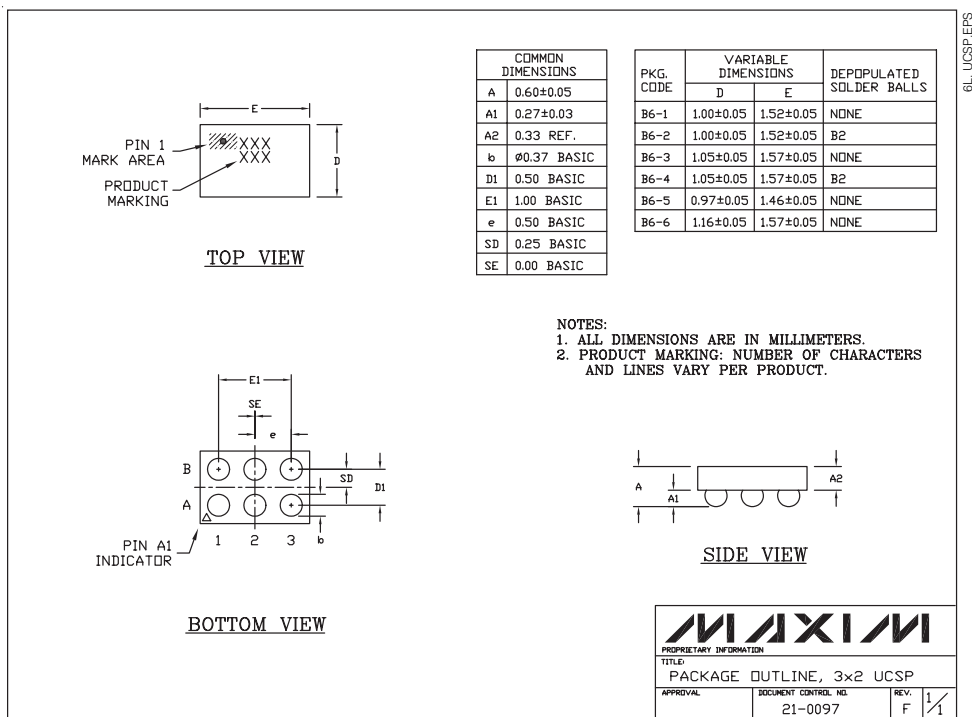
(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information, go to www.maxim-ic.com/packages.)



Single/Dual/Quad, Low-Cost, UCSP/SOT23, Low-Power, Rail-to-Rail I/O Op Amps

Package Information (continued)

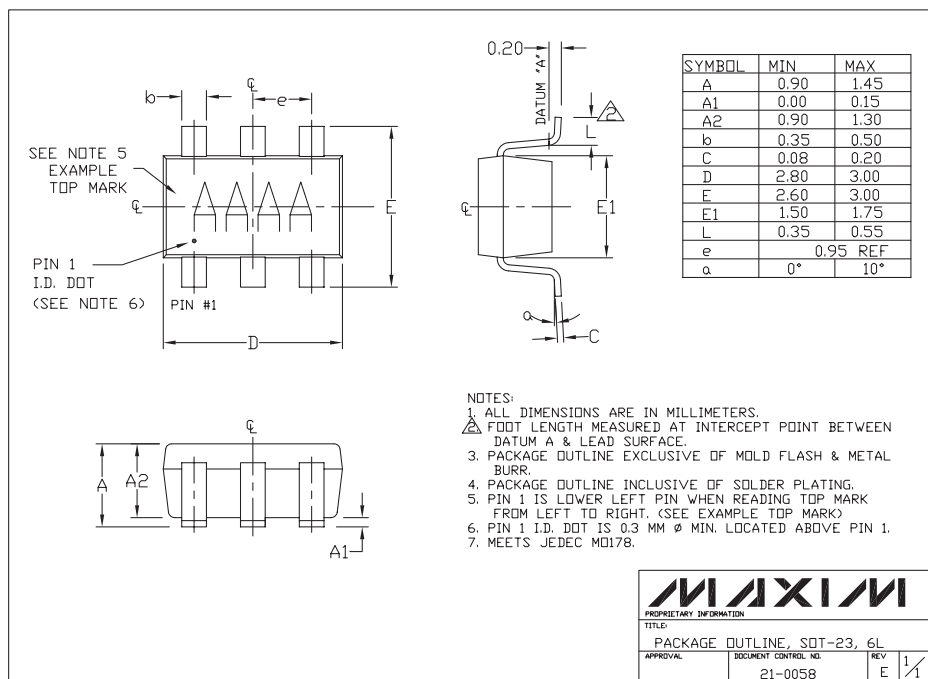
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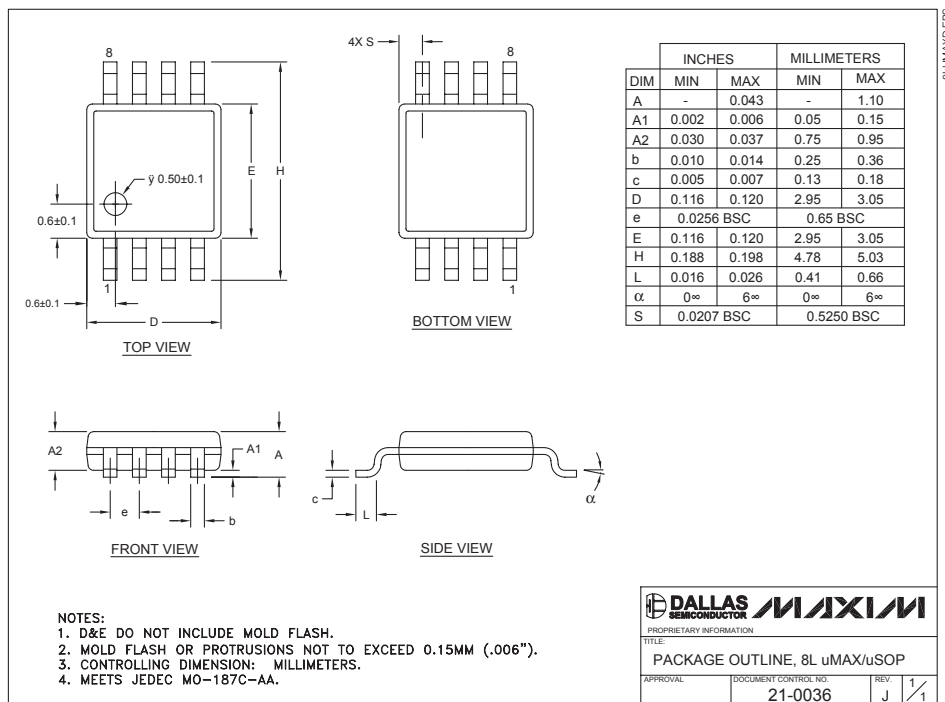
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Package Information (continued)

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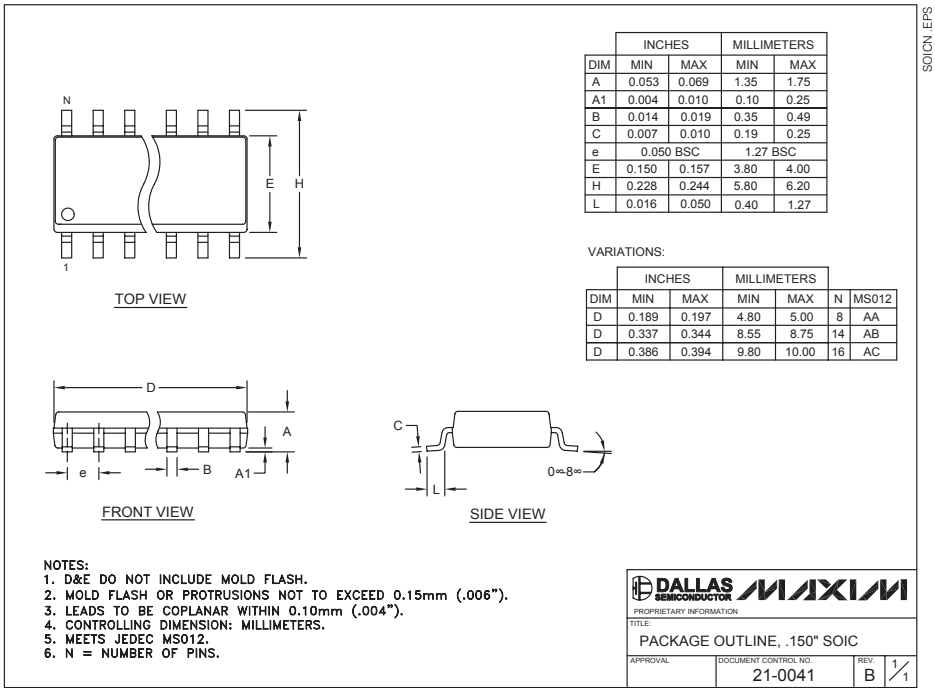


8LUMXD.EPS

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Package Information (continued)

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MAX4322/MAX4323/MAX4326/MAX4327/MAX4329

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