EVALUATION KIT AVAILABLE

*Click **here** to ask an associate for production status of specific part numbers.*

MAX40263

1.8V, 15MHz, Low-Offset, Low-Power, Rail-to-Rail Dual Op-Amp with Individual Shutdown

General Description

The MAX40263 is a dual-channel operational amplifier with two channels that can be disabled separately with two individual pins.

The MAX40263 offers a unique combination of high-speed, precision, and low-voltage operation, making it ideally suited for a large number of signal-processing functions such as filtering and amplification of signals in portable and industrial equipment.

The MAX40263's rail-to-rail input/outputs and low noise guarantee maximum dynamic range in demanding applications such as 12- to 14-bit SAR ADC drivers. Unlike traditional rail-to-rail input structures, input crossover distortion is absent due to an optimized input stage with an ultra-quiet charge pump. The input offset voltage is as low as 50µV due to the autocalibration performed during power-up. The device also includes a fast-power-on shutdown mode for further power savings.

The MAX40263 operates from a wide supply range of 1.8V to 5.5V over the -40°C to +125°C temperature range and consumes only 750µA (typ) supply current per channel. It is available in a tiny, 10-pin QFN package.

The MAX40263 is an extension of the MAX44259/60/61/63 and MAX40110/11 families with individual shutdown pins for separate channels.

Applications

- Notebooks
- 3G/4G Handsets
- Portable Medical Instruments
- Battery-Operated Devices
- Analog-to-Digital Converter Buffers
- Transimpedance Amplifiers
- General-Purpose Signal Processing

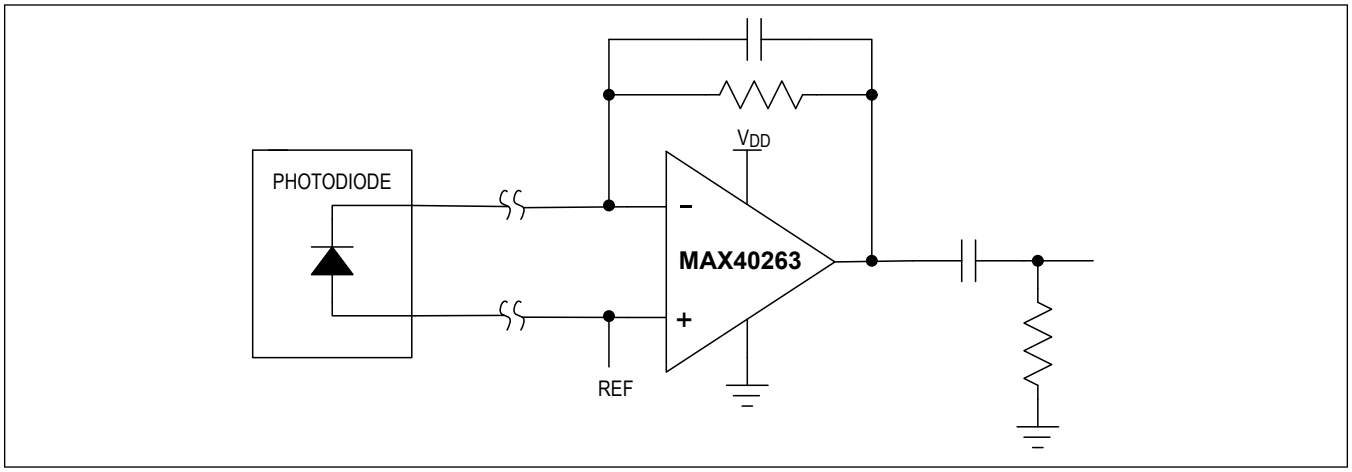
Benefits and Features

- Wide Supply Range from 1.8V to 5.5V over the -40°C to +125°C Range
- Low 50µV (Max) Input Offset Voltage with Power-On Autocalibration at +25°C
- 15 MHz Unity-Gain Bandwidth
- Low 12.7nV/√Hz Input Voltage-Noise Density
- 750µA Quiescent Current per Channel
- Rail-to-Rail Inputs and Outputs
- <1.5pA Low Input Bias Current at +25°C
- Power-Saving Shutdown Mode
- Separate Shutdown for Each Channel
- Low 105dB Total Harmonic Distortion
- No Phase Reversal in Overdrive Conditions

Ordering Information appears at end of data sheet.

19-101307, Rev 1, 4/22

Typical Application Circuits



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LIST OF FIGURES

Absolute Maximum Ratings

Supply Voltage (V_{DD} to V_{SS}) ..... -0.3V to +6V
SHDNA, SHDNB to V_{SS} ..... -0.3V to +6V
INA+, INA-, INB+, INB- to V_{SS} ..... -0.3V to V_{DD} + 0.3V
OUTA, OUTB to V_{SS} ..... -0.3V to V_{DD} + 0.3V
Output Short-Circuit Duration to V_{DD} or V_{SS} ..... Continuous
Continuous Input Current (any pins) ..... ±20mA
Differential Input Voltage ..... ±6V

Continuous Power Dissipation (T_A = +70°C)
(derate 9mW/°C above +70°C) .....722 mW
Operating Temperature Range .....-40°C to +125°C
Junction Temperature .....+150°C
Storage Temperature Range .....-65°C to +150°C
Soldering Temperature (reflow) .....+300°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

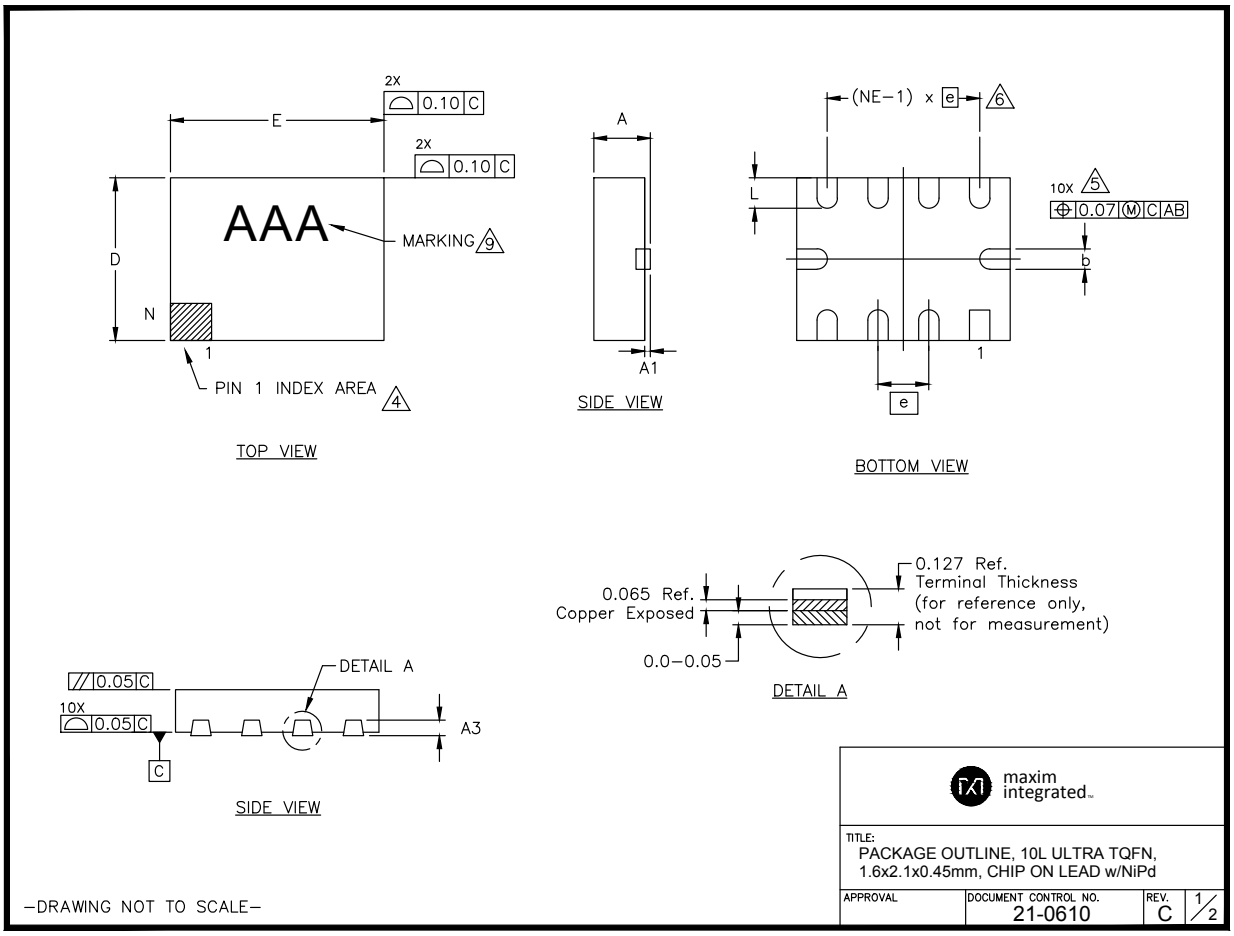
Package Information

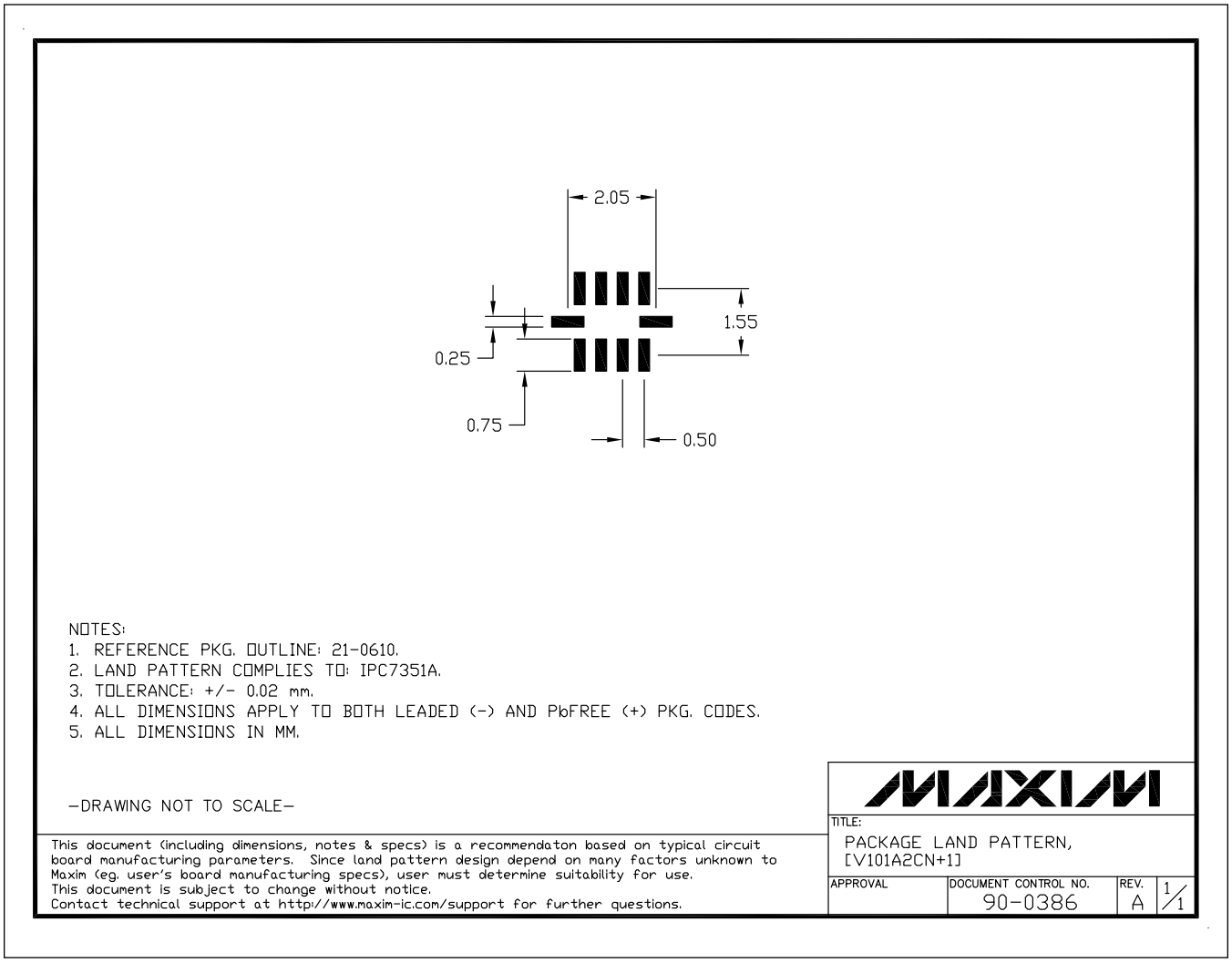
10-Ultra TQFN

Package Code	V101A2CN+1
Outline Number	21-0610
Land Pattern Number	90-0386
Thermal Resistance, Four-Layer Board:	
Junction to Ambient (θ_{JA})	110.8°C/W
Junction to Case (θ_{JC})	62.1°C/W

For the latest package outline information and land patterns (footprints), go to *www.maximintegrated.com/packages*. Note that a "+", "#", or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

Package thermal resistances were obtained using the method described in JEDEC specification JESD51-7, using a four-layer board. For detailed information on package thermal considerations, refer to *www.maximintegrated.com/thermal-tutorial*.


2X 0.10 C
E
2X 0.10 C
AAA
MARKING 9
D
N
1
PIN 1 INDEX AREA 4
TOP VIEW
A
A1
SIDE VIEW
(NE−1) x e 6
L
10X 5
0.07 M C AB
b
1
e
BOTTOM VIEW
0.065 Ref.
Copper Exposed
0.127 Ref.
Terminal Thickness
(for reference only,
not for measurement)
0.0−0.05
DETAIL A
0.05 C
10X 0.05 C
C
DETAIL A
A3
SIDE VIEW
maxim integrated
TITLE:
PACKAGE OUTLINE, 10L ULTRA TQFN,
1.6x2.1x0.45mm, CHIP ON LEAD w/NiPd
APPROVAL
DOCUMENT CONTROL NO.
21-0610
REV.
C
1/2
−DRAWING NOT TO SCALE−



Electrical Characteristics

(V_{DD} = 3.3V, V_{SS} = 0V, V_{IN+} = V_{IN-} = V_{DD}/2, R_{LOAD} = 10kΩ to V_{DD}/2, $V_{\overline{SHDN}}$ = V_{DD}, T_A = -40°C to +125°C, unless otherwise noted. Typical values are at +25°C.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
POWER SUPPLY							
Supply Voltage Range	V_{DD}	Guaranteed by PSRR		1.8		5.5	V
Power-Supply Rejection Ratio	PSRR	V_{CM} = V_{DD}/2		76	95		dB
Quiescent Current	I_{DD}	Only one op-amp channel enabled	R_{LOAD} = no load		750	1300	µA
		Both op-amp channels enabled	R_{LOAD} = no load		1300	2200	
Shutdown Supply Current	I_{SHDN}					1	µA

Electrical Characteristics (continued)

(V_{DD} = 3.3V, V_{SS} = 0V, V_{IN+} = V_{IN-} = V_{DD}/2, R_{LOAD} = 10kΩ to V_{DD}/2, $V_{\overline{SHDN}}$ = V_{DD}, T_A = -40°C to +125°C, unless otherwise noted. Typical values are at +25°C.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Shutdown Input Low	V_{IL}					0.5	V
Shutdown Input High	V_{IH}			1.3			V
Output Leakage Current in Shutdown					100		pA
Shutdown Input Bias Current	I_{IL}/I_{IH}					1	µA
Shutdown Turn-On Time	$t_{\overline{SHDN}}$	T_A = +25°C (Note 2)	One channel recovers after its own shutdown			9	µs
			Both recover after a complete shutdown		14.4	18.9	
		-40°C < T_A < +125°C (Note 2)	One channel recovers after its own shutdown			12	
			Both recover after a complete shutdown			26.7	
Power-Up Time	t_{ON}	Includes power-on VOS self-calibration	T_A = +25°C (Note 2)		9.7	15.2	ms
			-40°C < T_A < +125°C (Note 2)			18.4	
DC CHARACTERISTICS							
Input Common-Mode Range	V_{CM}	Guaranteed by CMRR test		V_{SS} - 0.1		V_{DD} + 0.1	V
Common-Mode Rejection Ratio	CMRR	V_{CM} = V_{SS} - 0.1V to V_{DD} + 0.1V		75	90		dB
Input Offset Voltage (Note 2)	V_{OS}	T_A = +25°C (Note 3)			10	50	µV
		-40°C ≤ T_A ≤ +125°C (Note 4)				100	
		-40°C ≤ T_A ≤ +125°C (Note 5)				600	
Input Offset Voltage Drift (Note 2)	TC V_{OS}				1	6	µV/°C
Input Bias Current (Note 2)	I_B	T_A = +25°C			0.01	1.5	pA
		-40°C < T_A < +85°C				10	
		-40°C < T_A < +125°C				200	
Input Resistance	R_{IN}	Common-Mode	V_{CM} = -0.1V to (V_{DD} + 0.1V)		10^{11}		Ω
		Differential			10^{12}		
Open-Loop Gain	A_{VOL}	400mV ≤ V_{OUT} ≤ V_{DD} - 400mV, R_{LOAD} = 10kΩ		97	115		dB
		400mV ≤ V_{OUT} ≤ V_{DD} - 400mV, R_{LOAD} = 600Ω		86	100		
Output Short-Circuit Current		To V_{DD} or V_{SS}			50		mA

Electrical Characteristics (continued)

(V_{DD} = 3.3V, V_{SS} = 0V, V_{IN+} = V_{IN-} = V_{DD}/2, R_{LOAD} = 10kΩ to V_{DD}/2, $V_{\overline{SHDN}}$ = V_{DD}, T_A = -40°C to +125°C, unless otherwise noted. Typical values are at +25°C.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Output Voltage Low	V_{OL}	V_{OUT} – V_{SS}	R_{LOAD} = 10kΩ to V_{DD}/2			20	mV
			R_{LOAD} = 600Ω to V_{DD}/2			50	
Output Voltage High	V_{OH}	V_{DD} – V_{OUT}	R_{LOAD} = 10kΩ to V_{DD}/2			10	mV
			R_{LOAD} = 600Ω to V_{DD}/2			50	
AC CHARACTERISTICS							
Input Voltage Noise Density	e_n	f = 10kHz			12.7		nV/√Hz
Input Voltage Noise		0.1Hz ≤ f ≤ 10Hz			10		μV_{P-P}
Input Capacitance	C_{IN}				2.5		pF
Gain-Bandwidth Product	GBW				15		MHz
Slew Rate	SR	A_V = 1V/V, V_{OUT} = $2V_{P-P}$, 10% to 90%			7		V/µs
Capacitive Loading	C_{LOAD}	No sustained oscillation, A_V = 1V/V			300		pF
Total Harmonic Distortion +Noise	THD+N	V_{OUT} = $2V_{P-P}$, AV = 1V/V, R_{LOAD} = 10kΩ	f = 10kHz		-105		dB
Settling Time		To 0.01%, V_{OUT} = $2V_{P-P}$, A_V = 1V/V, C_{LOAD} = 30pF			1.7		µs
Output Transient Recovery Time		ΔV_{OUT} = 0.2V, V_{DD} = 3.3V, A_V = 1V/V, R_S = 20Ω, C_{LOAD} = 1nF			1		µs

Note 1: All devices are 100% production tested at T_A = +25°C. Specifications over temperature are guaranteed by design.

Note 2: Guaranteed by design.

Note 3: At +25°C, upon power up and after calibration.

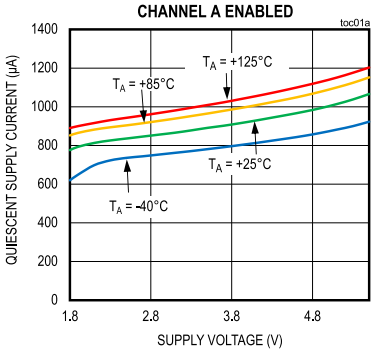
Note 4: For any temperature values between -40°C to +125°C, upon power up and after calibration.

Note 5: For any temperature values between -40°C and +125°C, it indicates the maximum drift from the power-up initial calibrated value.

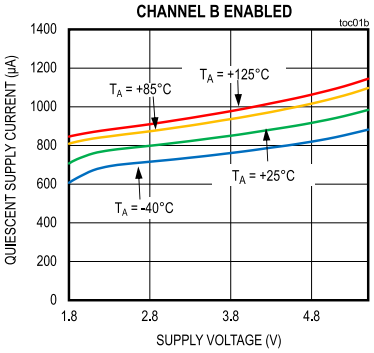
Typical Operating Characteristics

(T_A = +25°C, unless otherwise noted.)

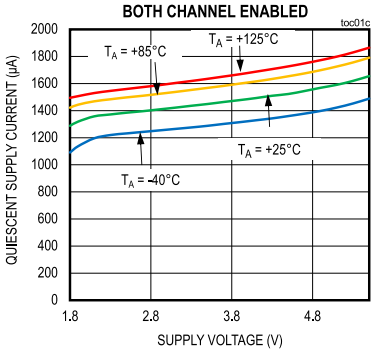
QUIESCENT SUPPLY CURRENT vs. SUPPLY VOLTAGE CHANNEL A ENABLED



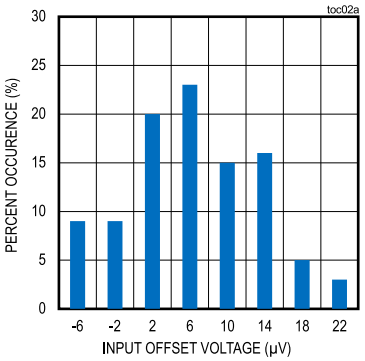
QUIESCENT SUPPLY CURRENT vs. SUPPLY VOLTAGE CHANNEL B ENABLED



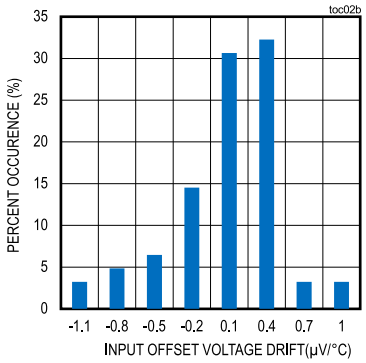
QUIESCENT SUPPLY CURRENT vs. SUPPLY VOLTAGE BOTH CHANNEL ENABLED



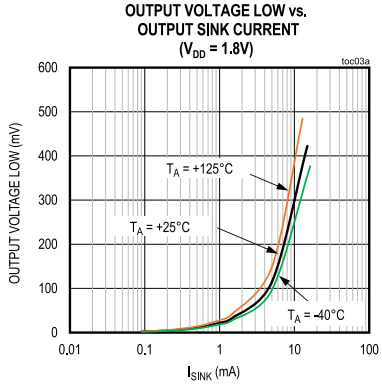
INPUT OFFSET VOLTAGE HISTOGRAM



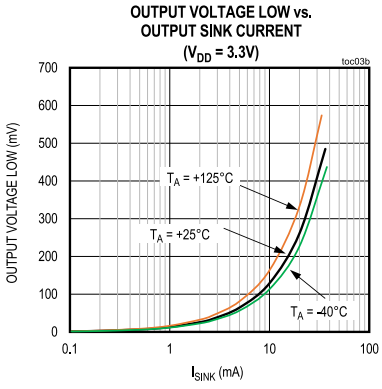
INPUT OFFSET VOLTAGE DRIFT HISTOGRAM



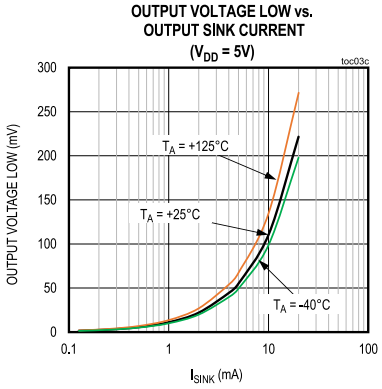
OUTPUT VOLTAGE LOW vs. OUTPUT SINK CURRENT (V_{DD} = 1.8V)



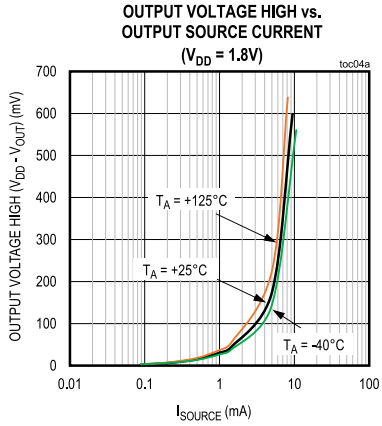
OUTPUT VOLTAGE LOW vs. OUTPUT SINK CURRENT (V_{DD} = 3.3V)



OUTPUT VOLTAGE LOW vs. OUTPUT SINK CURRENT (V_{DD} = 5V)



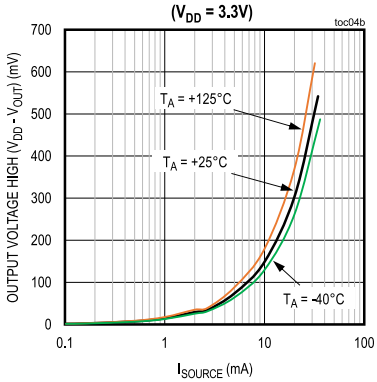
OUTPUT VOLTAGE HIGH vs. OUTPUT SOURCE CURRENT (V_{DD} = 1.8V)



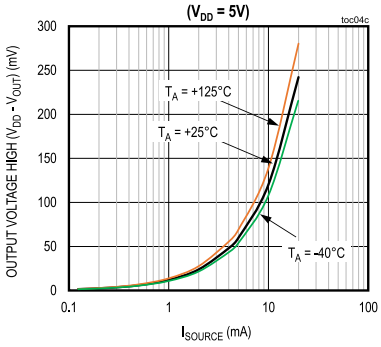
Typical Operating Characteristics (continued)

(T_A = +25°C, unless otherwise noted.)

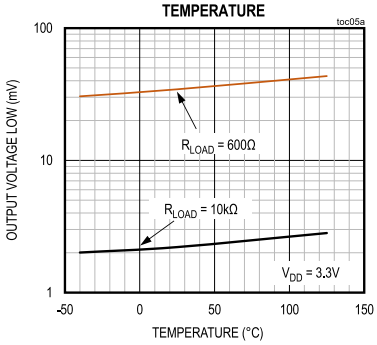
OUTPUT VOLTAGE HIGH vs. OUTPUT SOURCE CURRENT (V_{DD} = 3.3V)



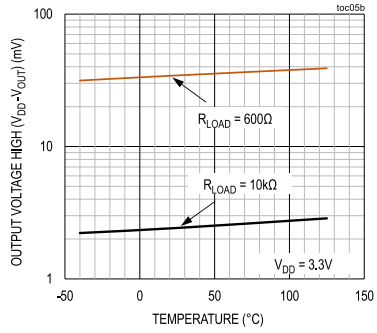
OUTPUT VOLTAGE HIGH vs. OUTPUT SOURCE CURRENT (V_{DD} = 5V)



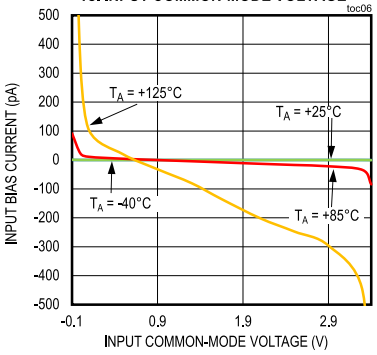
OUTPUT VOLTAGE LOW vs. TEMPERATURE



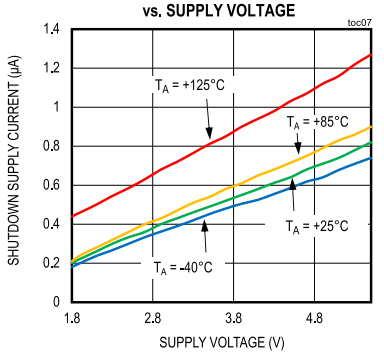
OUTPUT VOLTAGE HIGH vs. TEMPERATURE



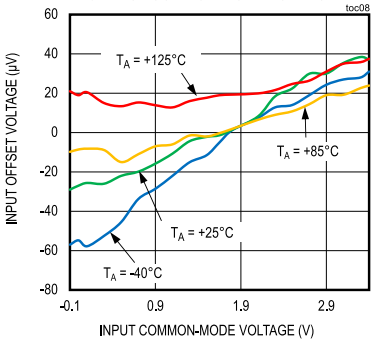
INPUT BIAS CURRENT vs. INPUT COMMON-MODE VOLTAGE



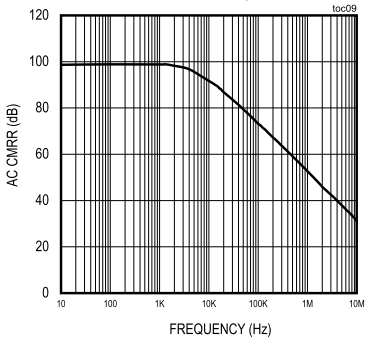
SHUTDOWN SUPPLY CURRENT vs. SUPPLY VOLTAGE



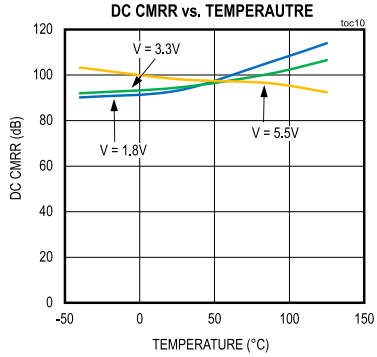
INPUT OFFSET VOLTAGE vs. INPUT COMMON-MODE VOLTAGE



AC CMRR vs. FREQUENCY



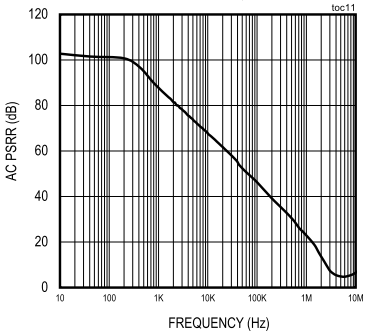
DC CMRR vs. TEMPERAUTRE



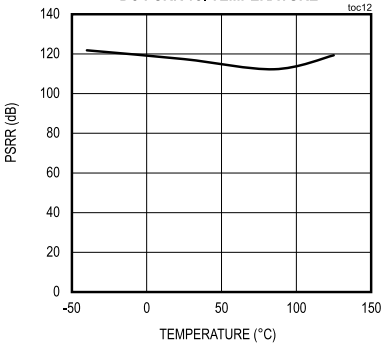
Typical Operating Characteristics (continued)

(T_A = +25°C, unless otherwise noted.)

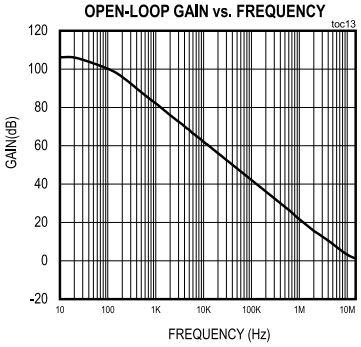
AC PSRR vs. FREQUENCY



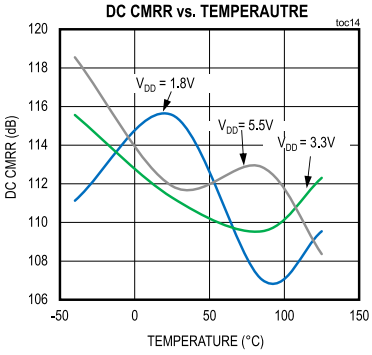
DC PSRR vs. TEMPERATURE



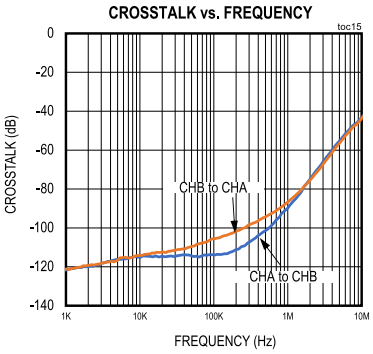
OPEN-LOOP GAIN vs. FREQUENCY



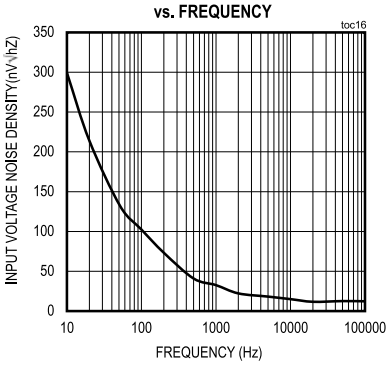
DC CMRR vs. TEMPERAUTRE



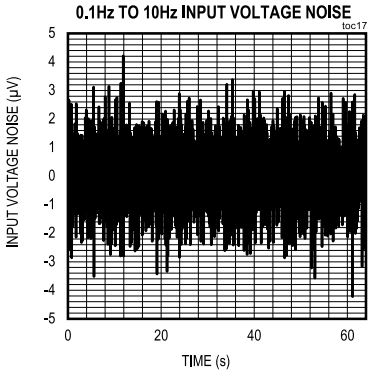
CROSSTALK vs. FREQUENCY



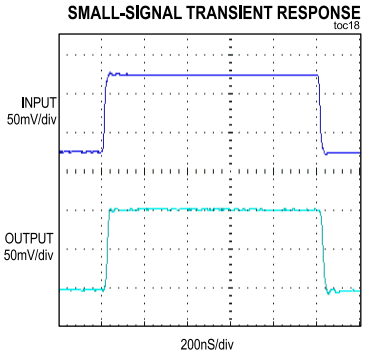
INPUT VOLTAGE NOISE DENSITY vs. FREQUENCY



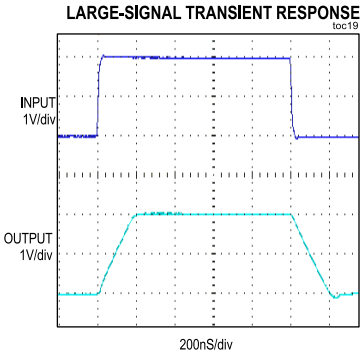
0.1Hz TO 10Hz INPUT VOLTAGE NOISE



SMALL-SIGNAL TRANSIENT RESPONSE

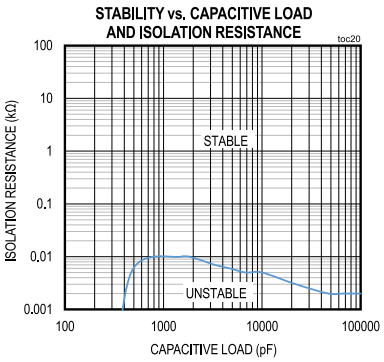


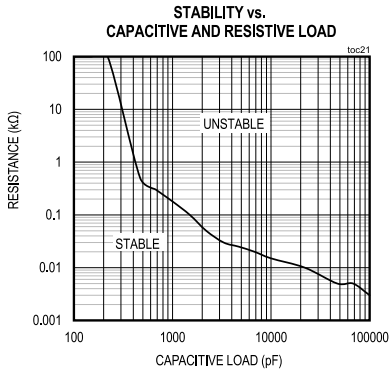
LARGE-SIGNAL TRANSIENT RESPONSE

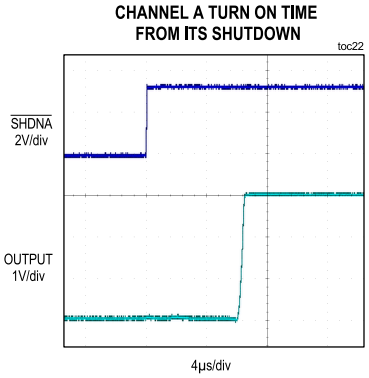


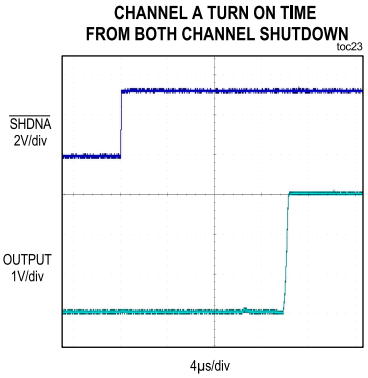
Typical Operating Characteristics (continued)

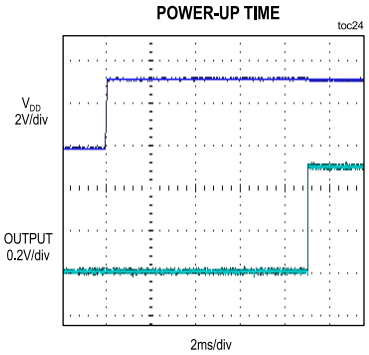
(T_A = +25°C, unless otherwise noted.)





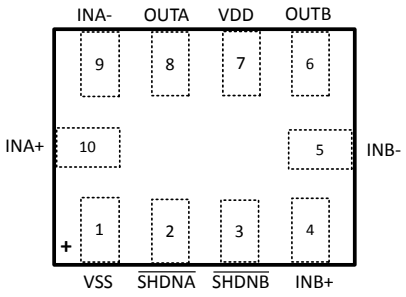






Pin Configuration

TOP VIEW – PINS AT THE BOTTOM



ULTRA TQFN, 2.1mm x 1.6mm

Pin Description

PIN	NAME	FUNCTION	TYPE
1	VSS	Negative Supply Voltage. Connect to the ground return of the V_{DD} supply.	Power
7	VDD	Positive Supply Voltage	Power
2	$\overline{SHDNA}$	Active-Low Shutdown Input for Channel A. Connect to V_{DD} for normal operation.	Analog Input
8	OUTA	Output for Channel A	Analog Output
10	INA+	Positive Input for Channel A	Analog Input
9	INA-	Negative Input for Channel A	Analog Input
3	$\overline{SHDNB}$	Active-Low Shutdown Input for Channel B. Connect to V_{DD} for normal operation.	Analog Input
6	OUTB	Output for Channel B	Analog Output
4	INB+	Positive Input for Channel B	Analog Input
5	INB-	Negative Input for Channel B	Analog Input

Detailed Description

The MAX40263 is a high-speed, low-power dual-channel op-amp ideal for signal processing applications due to the device's high precision and low-noise CMOS inputs. The device self-calibrates on power-up to eliminate the effects of temperature and power supply variation. Each channel of MAX40263 can enter into low-power shutdown mode separately and recover in 30µs.

Crossover Distortion

The device features a low-noise integrated charge pump that creates an internal voltage rail 1V above V_{DD}, which powers the input differential pair of PMOS transistors as shown in Figure 1. This unique architecture eliminates crossover distortion common in traditional CMOS input architecture (Figure 2), especially when used in a noninverting configuration such as Sallen-Key filters.

The charge pump operating frequency lies well above the unity-gain frequency of the amplifier. Because of its high-frequency operation and ultra-quiet circuitry, the charge pump generates little noise, does not require external components, and is entirely transparent to the user.

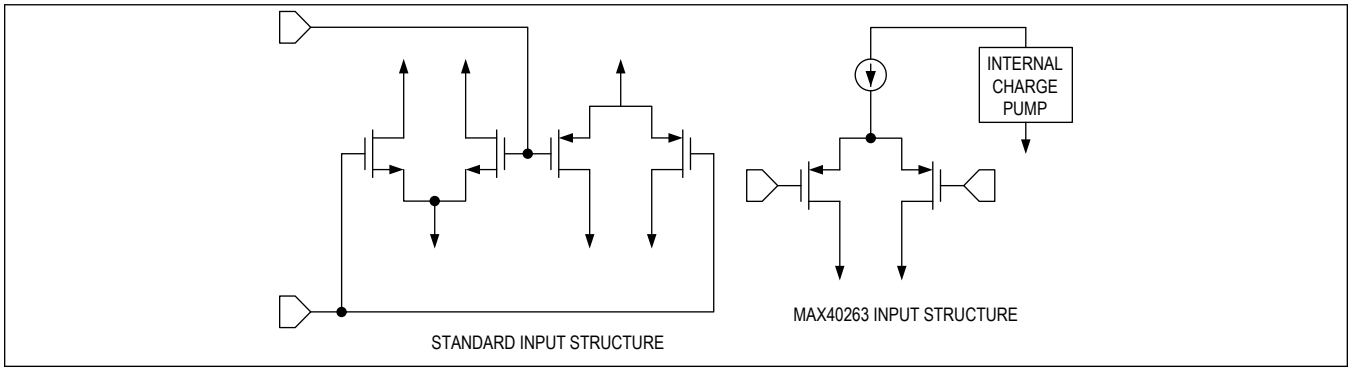


Figure 1. Comparing the Input Structure of the MAX40263 to Standard Op Amps

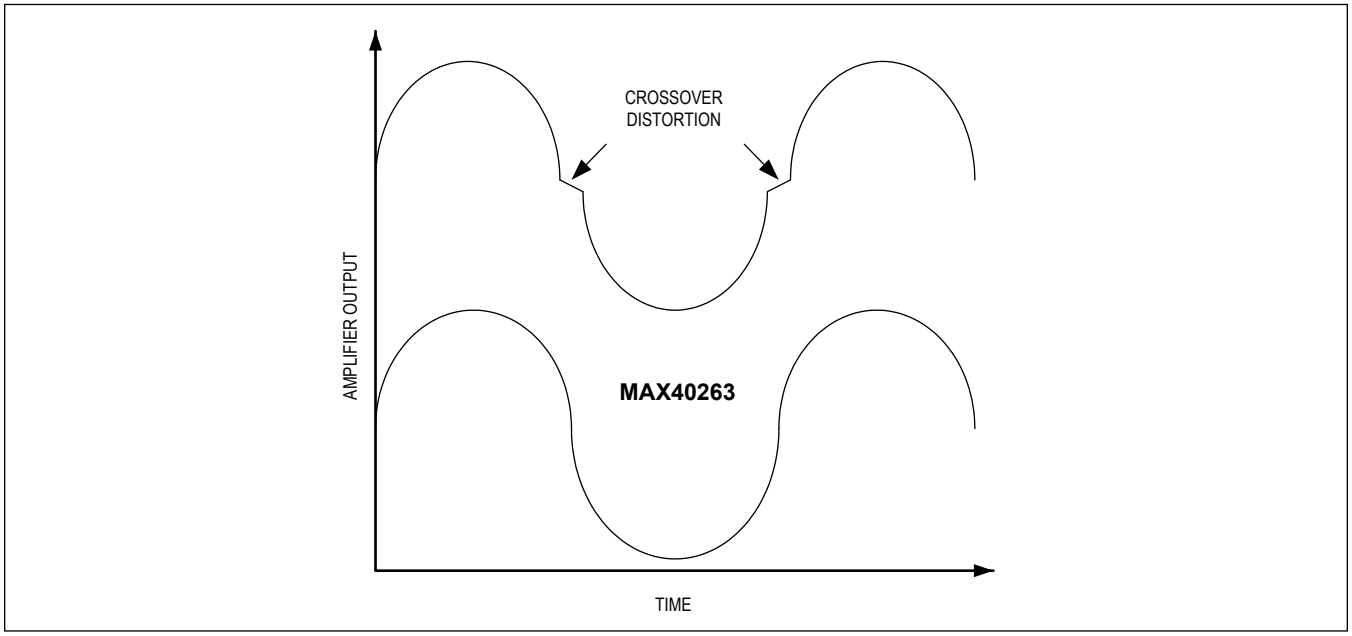


Figure 2. Crossover Distortion of Typical Amplifiers

Applications Information

Power-Up Autotrim

The MAX40263 features an automatic trim that self-calibrates the input offset voltage (V_{OS}) to less than 50µV on power-up. This self-calibration feature allows the device to eliminate input offset voltage effects due to power supply and operating temperature variation simply by cycling its power.

The device power-up speed should be fast to avoid the case when the self-calibration is triggered before the supply settles. Such a wrong condition would give an undesired large offset. To achieve targeted low V_{OS} values, it is recommended to either (a) use a power supply with a fast slew rate (power supply settles in <10ms), or (b) power up the chip in the shutdown mode ($\overline{SHDNA}$ = $\overline{SHDNB}$ = low) and enable the chip ($\overline{SHDNA}$ = $\overline{SHDNB}$ = high) after the supply settles.

Shutdown Operation

The MAX40263 is a dual channel op-amp, and each channel of MAX40263 can enter into low-power shutdown mode separately by pulling down $\overline{SHDNA}$ or $\overline{SHDNB}$.

Shutdown mode puts both inputs and outputs into high impedance and substantially lowers the quiescent current. Putting the output into high impedance allows multiple outputs to be multiplexed onto a single output line without the additional external buffers. The device does not self-calibrate when exiting shutdown mode and retains its power-up trim settings. Figure 3 shows how the device recovers from shutdown in less than 30µs.

The shutdown logic levels of the device are independent of supply, allowing the shutdown feature of the device to operate off a 1.8V or 3.3V microcontroller, regardless of supply voltage.

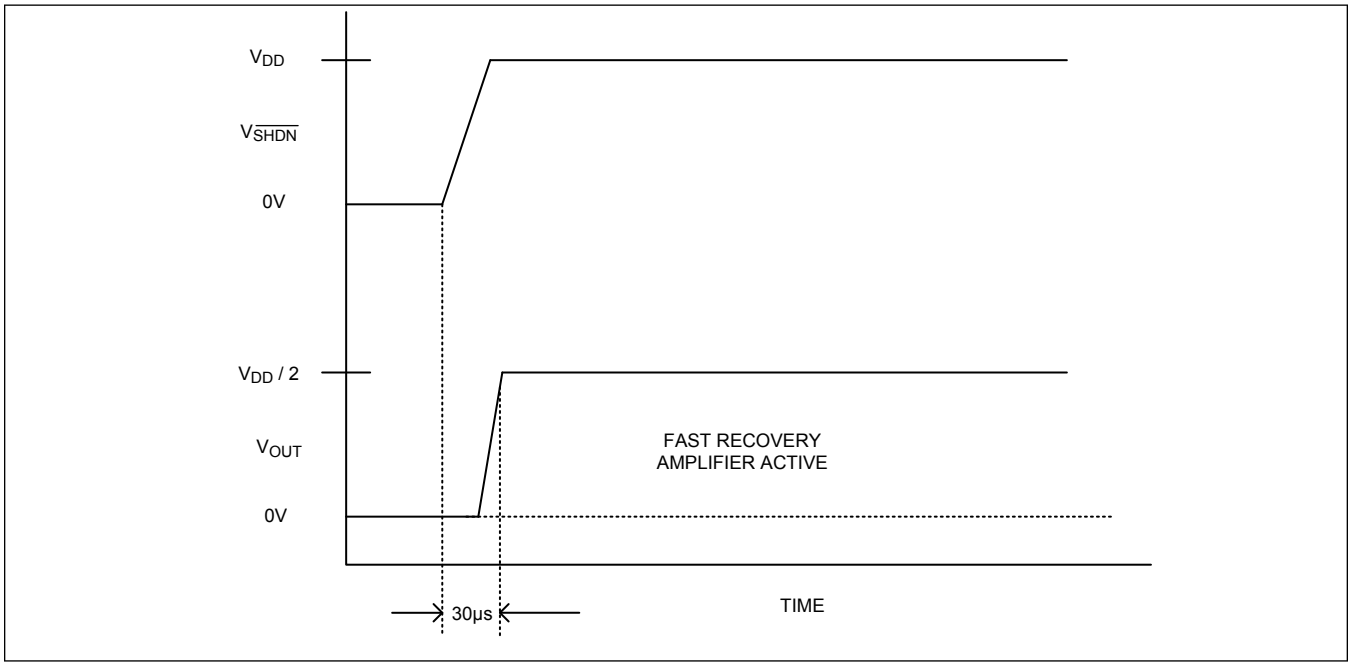


Figure 3. Shutdown Input Operation

Rail-to-Rail Input/Output

The input voltage range of the device extends 100mV above V_{DD} and below V_{SS}. The wide input common mode voltage range allows the op amp to be used as a buffer and as a differential amplifier in a variety of signal processing applications. Output voltage high/low is only 50mV above V_{SS} and below V_{DD}, allowing maximum dynamic range in single-supply

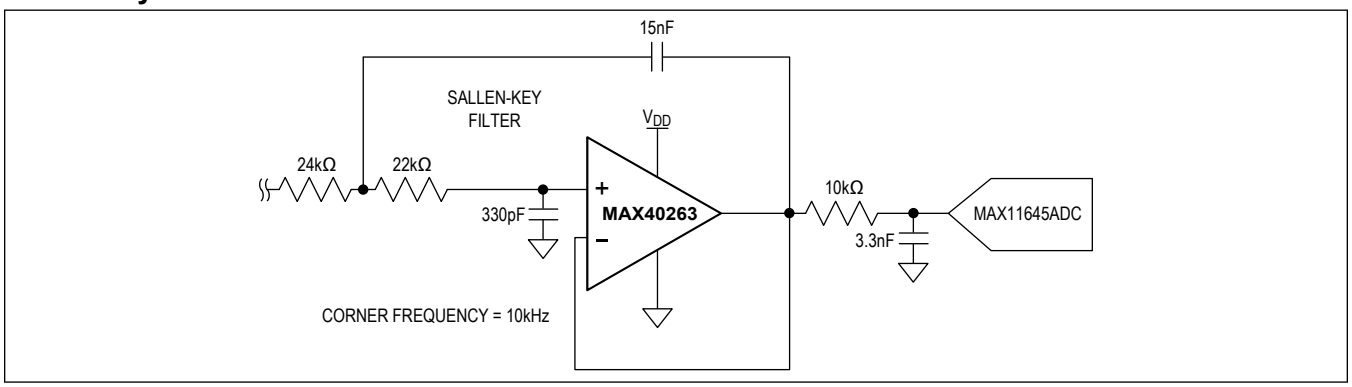
applications. The high output current and capacitance drive capability of the device make it ideal as an ADC driver and a line driver.

Input Bias Current

The MAX40263 features a high-impedance CMOS input stage and a specialized ESD structure that allows low input bias current operation at low-input, common-mode voltages. Low-input bias current is useful when interfacing with high-impedance sensors. It is also beneficial for designing transimpedance amplifiers for photodiode sensors. This makes the device ideal for ground referenced medical and industrial sensor applications.

Typical Application Circuits

Sallen-Key Filter



Ordering Information

PART NUMBER	TEMP RANGE	PIN-PACKAGE	TOP MARK
MAX40263AVB+T	-40°C to +125°C	10-UTQFN	+ABI

+Denotes a lead(Pb)-free/RoHS-compliant package.

Revision History

REVISION NUMBER	REVISION DATE	DESCRIPTION	PAGES CHANGED
0	3/22	Release for Market Intro	—
1	4/22	Updated *Benefits and Features* section	1

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Analog Devices Inc.:

MAX40263AVB+ MAX40263AVB+T