maxim integrated™

MAX3747A/MAX3747B

155Mbps to 3.2Gbps, Low-Power SFP Limiting Amplifiers

General Description

The MAX3747A/MAX3747B multirate limiting amplifiers function as data quantizers for OC-3 through OC-48 synchronous optical network (SONET), Fibre-Channel, and Gigabit Ethernet optical receivers. They are pin-for-pin compatible with the SY88993V from Micrel Semiconductor, Inc. The amplifiers accept a wide range of input voltages and provide constant-level, current-mode logic (CML) output voltages with controlled edge speeds. The MAX3747A/MAX3747B output voltages are 800mV$_{P-P}$. The MAX3747B has enhanced LOS operation under overload conditions.

The MAX3747A/MAX3747B limiting amplifiers feature a programmable loss-of-signal detect (LOS) and an optional disable function (DISABLE) that can be combined to implement squelch.

The MAX3747A/MAX3747B are available in a 3mm, 10-pin µMAX® package ideal for small form-factor receivers.

Applications

Gigabit Ethernet SFP/SFF Optical Transceiver Modules

1G/2G Fibre-Channel SFP/SFF Optical Transceiver Modules

Multirate OC-3 to OC-48 FEC SFP/SFF Optical Transceiver Modules

10G LX4 Transceiver Modules

Features

- **Pin Compatible with Micrel SY88993V**
- **155Mbps to 3.2Gbps Operation**
- **> 57dB of Gain**
- **< 10^{-12} BER with 2mV$_{P-P}$ Input Amplitude**
- **18mA Supply Current**
- **Chatter-Free LOS with Programmable Threshold**
- **Output DISABLE Function**
- **PECL-Compatible Inputs**

Ordering Information

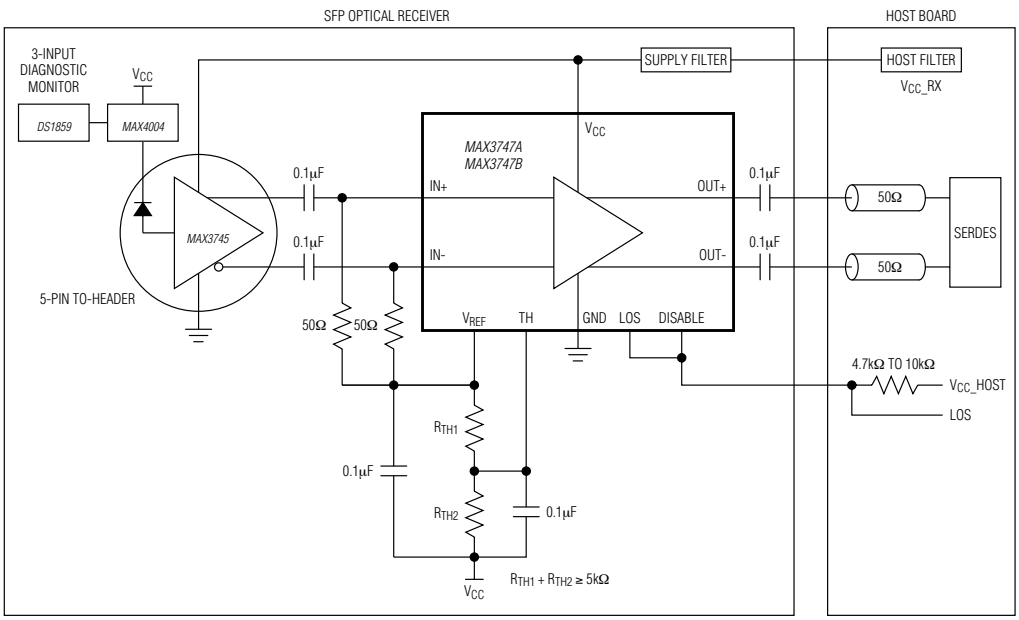
PART	TEMP RANGE	PIN-PACKAGE
MAX3747AEUB+	-40°C to +85°C	10 µMAX
MAX3747BEUB+	-40°C to +85°C	10 µMAX

+Denotes a lead(Pb)-free/RoHS-compliant package.

µMAX is a registered trademark of Maxim Integrated Products, Inc.

Pin Configuration appears at end of data sheet.

Typical Application Circuit



For pricing, delivery, and ordering information, please contact Maxim Direct at 1-888-629-4642, or visit Maxim's website at www.maximintegrated.com.

19-0281; Rev 2; 8/12

ABSOLUTE MAXIMUM RATINGS

Power-Supply Voltage (V_{CC}) .....-0.5V to +4.5V
Voltage at IN+, IN- .....(V_{CC} - 2.4V) to (V_{CC} + 0.5V)
Voltage at DISABLE, LOS, TH, V_{REF} .....-0.5V to (V_{CC} + 0.5V)
Current into LOS .....-1mA to +9mA
Current into V_{REF} 2mA
Differential Input Voltage (IN+ - IN-) 2.5V
Continuous Current at CML Outputs
(OUT+, OUT-) .....-25mA to +25mA

Continuous Power Dissipation (T_A = +70°C)
10-Pin µMAX (derate 6.9mW/°C above +70°C) 552mW
Operating Junction Temperature Range (T_J) .....-55°C to +150°C
Storage Ambient Temperature Range (T_S) .....-55°C to +150°C
Lead Temperature (soldering, 10s) .....+300°C
Soldering Temperature (reflow) .....+260°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(V_{CC} = +2.97V to +3.63V, CML output load is 50Ω to V_{CC}, T_A = -40°C to +85°C. Typical values are at V_{CC} = +3.3V and T_A = +25°C, unless otherwise specified.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
POWER SUPPLY						
Supply Current (Note 2)	I_{CC}	MAX3747A including the CML output current		36	41	mA
		MAX3747B including the CML output current		38	43	
		MAX3747A excluding the CML output current		18	24	
		MAX3747B excluding the CML output current		20	26	
Power-Supply Noise Rejection	PSNR	f < 2MHz		30		dB
INPUT SPECIFICATION						
Input Sensitivity	V_{IN-MIN}	(Note 3)			4	mV_{P-P}
Input Overload	V_{IN-MAX}	(Note 3)	1200			mV_{P-P}
OUTPUT SPECIFICATION						
Output Resistance	R_{OUT}	(Note 4)	42	50	58	Ω
Differential Output Return Loss		DUT is powered on, f < 3GHz		15		dB
CML Differential Output Voltage		MAX3747A/MAX3747B $4mV_{P-P} \le V_{IN} \le 1200mV_{P-P}$	600	800	1000	mV_{P-P}
Differential Output Signal When Disabled		AC-coupled outputs, V_{IN-MAX} applied to the input (Note 4)			15	mV_{P-P}
Data-Output Transition Time		20% to 80% (Note 4)		70	120	ps
TRANSFER CHARACTERISTIC						
Deterministic Jitter (Notes 4, 5)	DJ	K28.5 pattern at 3.2Gbps		13.2	19	ps_{P-P}
		PRBS 2^{23} - 1 equivalent pattern at 2.7Gbps (Note 6)		14	25	
		K28.5 pattern at 2.1Gbps		12	17	
		PRBS 2^{23} - 1 equivalent pattern at 155Mbps (Note 6)		85	150	
Random Jitter		V_{IN} = $4mV_{P-P}$ (Notes 4, 7)		3.5	5	ps_{RMS}

ELECTRICAL CHARACTERISTICS (continued)

(V_{CC} = +2.97V to +3.63V, CML output load is 50Ω to V_{CC}, T_A = -40°C to +85°C. Typical values are at V_{CC} = +3.3V and T_A = +25°C, unless otherwise specified.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Input-Referred Noise		V_{IN} = 4mV_{P-P} (Note 4)		120	150	μV_{RMS}
Low-Frequency Cutoff				6.4		kHz
LOS Hysteresis		10log($V_{DEASSERT}$ / V_{ASSERT}) (Note 4)	1.25			dB
LOS Assert/Deassert Time		MAX3747A (Notes 4, 8)	2.3		40.0	μs
		MAX3747B (Notes 4, 8, 9)				
Low LOS Assert Level		V_{TH} = -1.3V (Notes 4, 10)	2.5	4.1	5.9	mV_{P-P}
Low LOS Deassert Level		V_{TH} = -1.3V (Notes 4, 10)		6.2	9.3	mV_{P-P}
Medium LOS Assert Level		V_{TH} = -0.68V (Notes 4, 10)	22.0	29.0	36.0	mV_{P-P}
Medium LOS Deassert Level		V_{TH} = -0.68V (Notes 4, 10)		44.8	62.0	mV_{P-P}
High LOS Assert Level		V_{TH} = -0.114V (Notes 4, 10)	36.0	53.7	63.6	mV_{P-P}
High LOS Deassert Level		V_{TH} = -0.114V (Notes 4, 10)		86.0	115	mV_{P-P}
TTL/CMOS I/O						
V_{REF} Voltage	V_{REF}		V_{CC} - 1.35	V_{CC} - 1.3V	V_{CC} - 1.19	V
LOS Output High Voltage	V_{OH}	R_{LOS} = 4.7kΩ to 10kΩ to V_{CC_HOST} (3V)	2.4			V
LOS Output Low Voltage	V_{OL}	R_{LOS} = 4.7kΩ to 10kΩ to V_{CC_HOST} (3.6V)			0.4	V
DISABLE Input High	V_{IH}		2.0			V
DISABLE Input Low	V_{IL}				0.8	V
DISABLE Input Current		R_{LOS} = 4.7kΩ to 10kΩ to V_{CC_HOST}			10	μA

Note 1: The data-input transition time is controlled by a 4th-order Bessel filter with f_{-3dB} = 0.75 x 2.667GHz for all data rates of 2.667Gbps and below. The f_{-3db} = 0.75 x 3.2GHz for a data rate of 3.2Gbps.

Note 2: Supply current is measured with unterminated outputs or with AC-coupled output termination (see Figure 1).

Note 3: Between sensitivity and overload, all AC specifications are met and the output is 0.95 x limited output amplitude.

Note 4: Guaranteed by design and characterization.

Note 5: The deterministic jitter (DJ) caused by the input filter is not included in the DJ generation specification.

Note 6: The PRBS 2^{23} - 1 equivalent pattern consists of a K28.5 pattern plus 240 ones plus K28.5 pattern plus 240 zeros.

Note 7: Random jitter was measured without using a filter at the input.

Note 8: The signal at the input is switched between two amplitudes, Signal_ON and Signal_OFF, as shown in Figure 2A.

Note 9: The signal at the input is switched between 1.2V_{P-P} and Signal_OFF as shown in Figure 2B.

Note 10: V_{TH} is the voltage at pin 5 referenced to V_{CC} (see Figure 5).

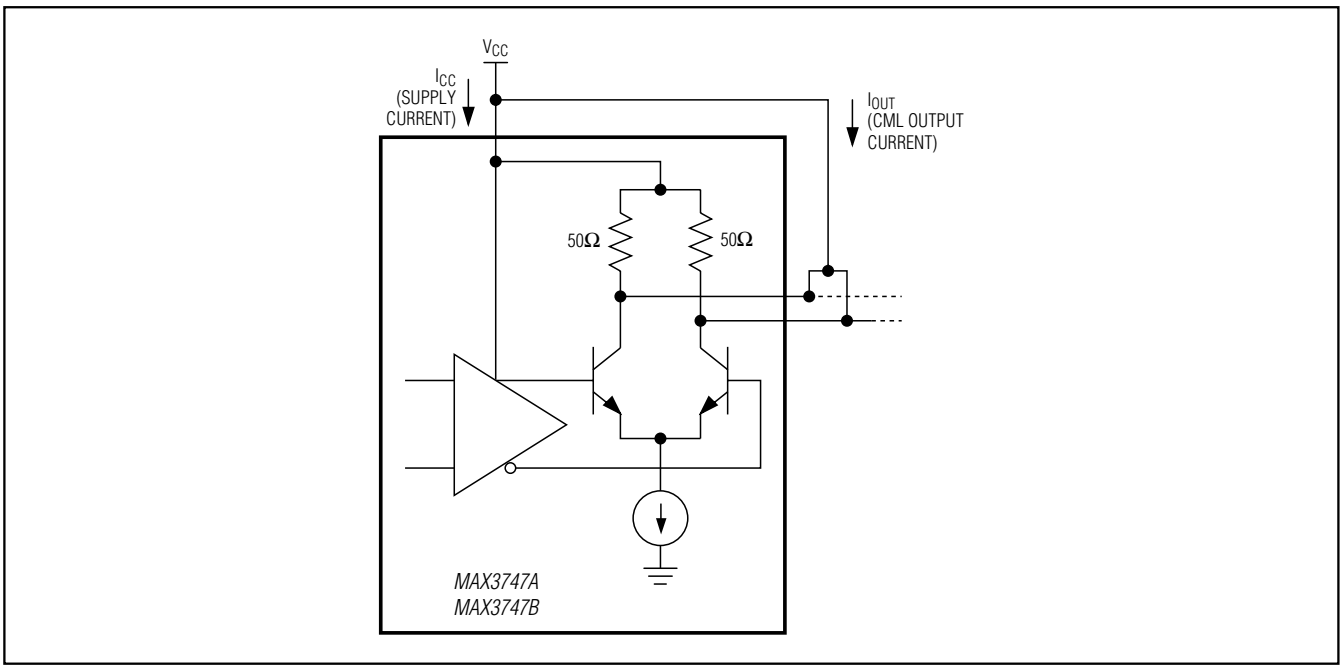


Figure 1. Power-Supply Current Measurement

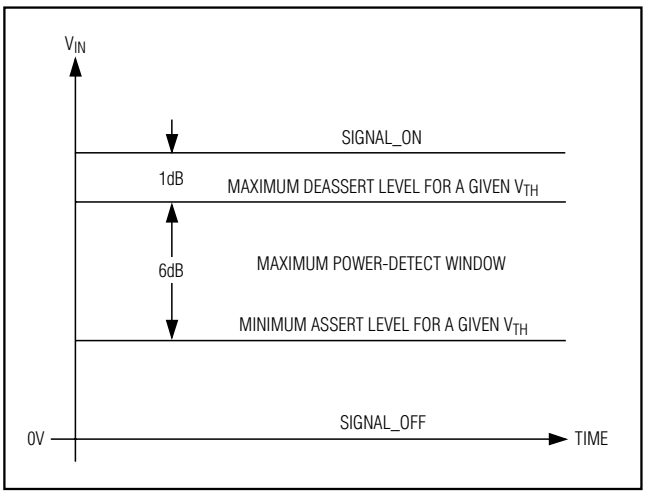


Figure 2A. LOS Deassert Threshold—Set 1dB Below Receiver Sensitivity

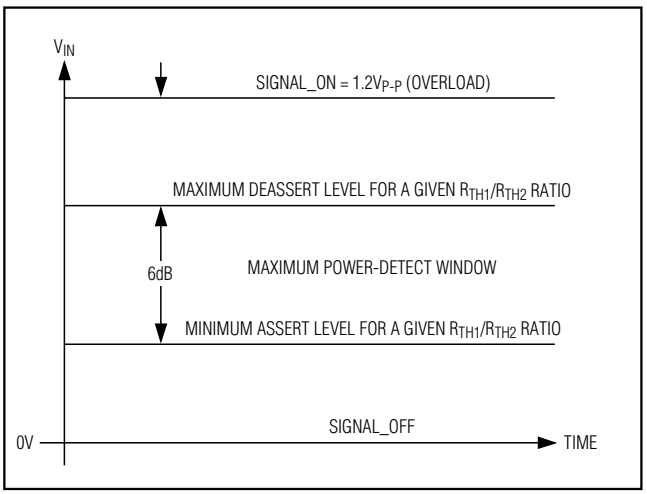
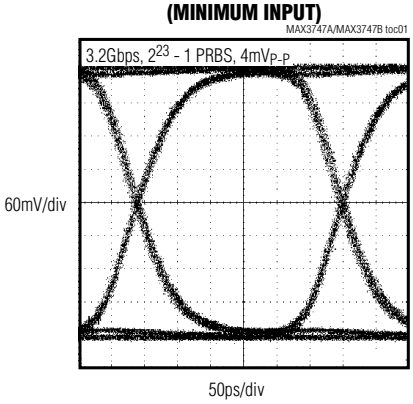


Figure 2B. LOS Deassert Threshold—Operating at Input Overload

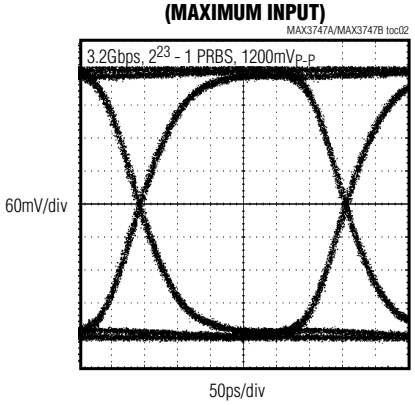
Typical Operating Characteristics

(V_{CC} = +3.3V, T_A = +25°C, unless otherwise noted.)

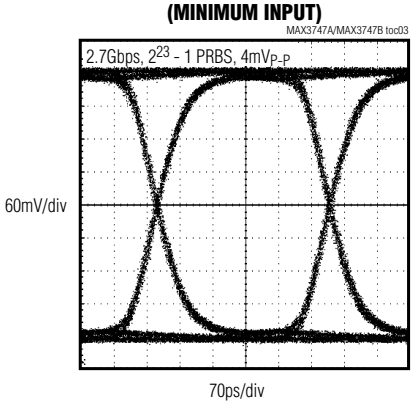
OUTPUT EYE DIAGRAM (MINIMUM INPUT)



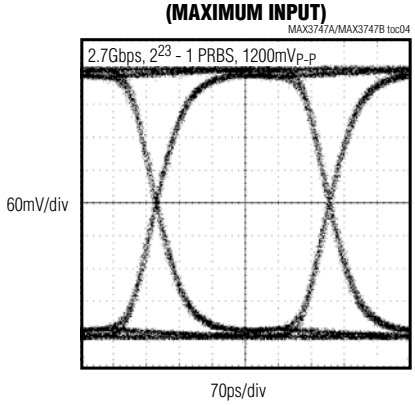
OUTPUT EYE DIAGRAM (MAXIMUM INPUT)



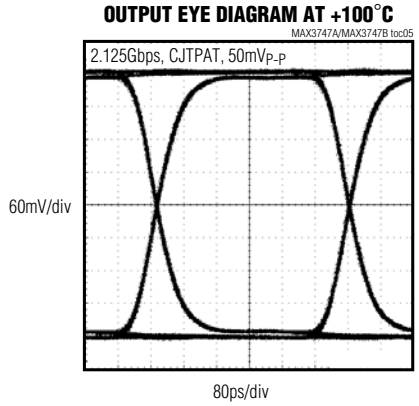
OUTPUT EYE DIAGRAM (MINIMUM INPUT)



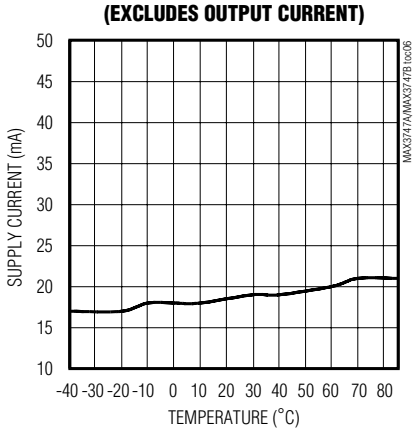
OUTPUT EYE DIAGRAM (MAXIMUM INPUT)



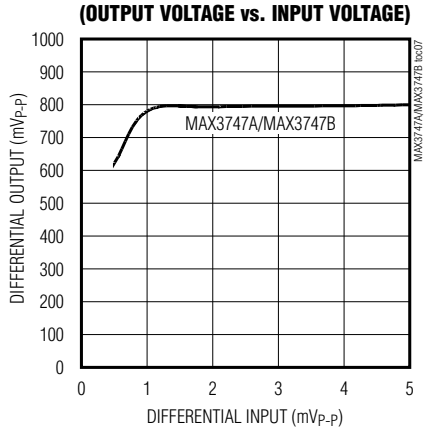
OUTPUT EYE DIAGRAM AT +100°C



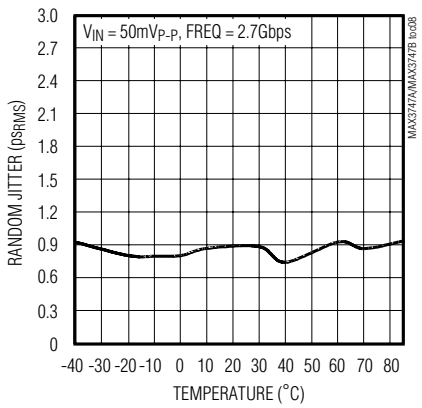
SUPPLY CURRENT vs. TEMPERATURE (EXCLUDES OUTPUT CURRENT)



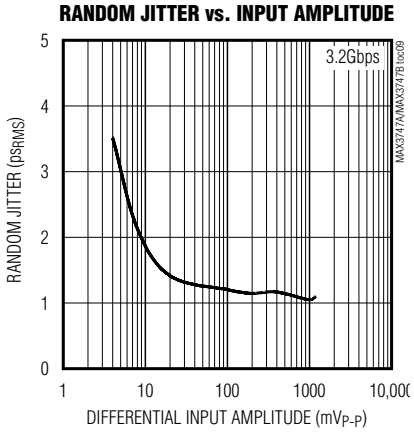
TRANSFER FUNCTION (OUTPUT VOLTAGE vs. INPUT VOLTAGE)



RANDOM JITTER vs. TEMPERATURE



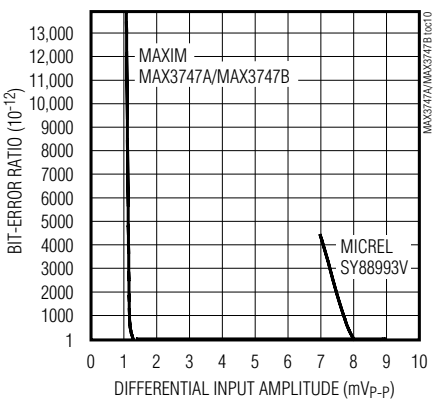
RANDOM JITTER vs. INPUT AMPLITUDE



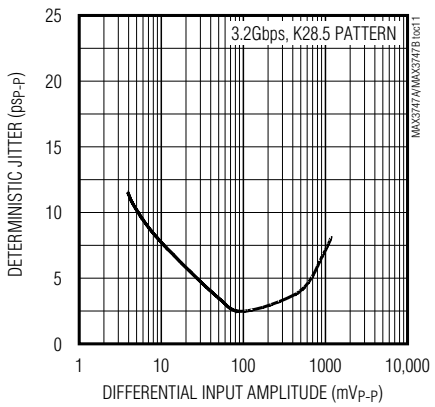
Typical Operating Characteristics (continued)

(V_{CC} = +3.3V, T_A = +25°C, unless otherwise noted.)

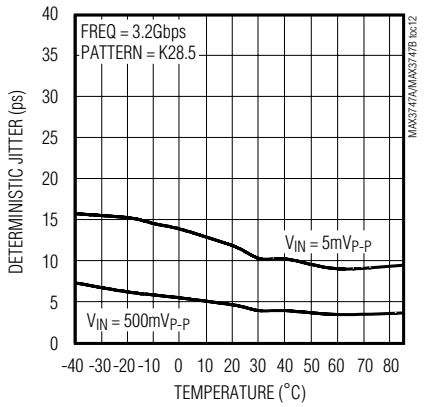
BIT-ERROR RATIO vs. INPUT VOLTAGE



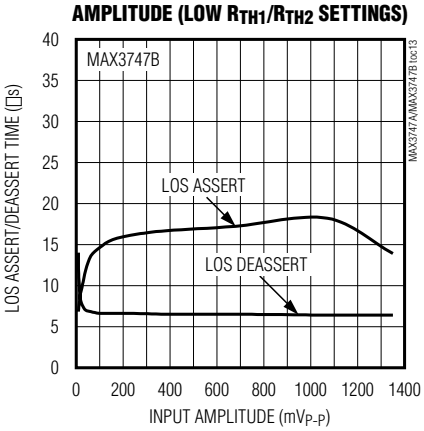
DETERMINISTIC JITTER vs. INPUT AMPLITUDE



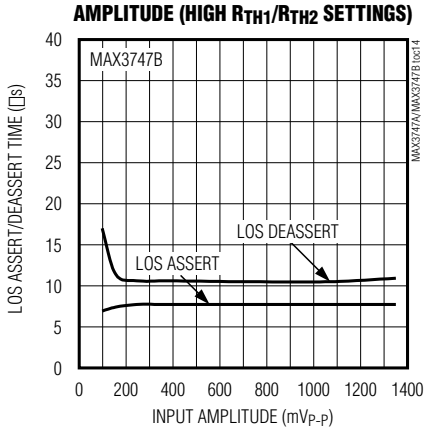
DETERMINISTIC JITTER vs. TEMPERATURE



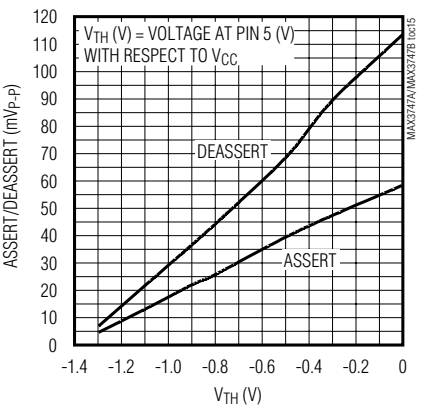
LOS ASSERT/DEASSERT TIMES vs. INPUT AMPLITUDE (LOW R_{TH1}/R_{TH2} SETTINGS)



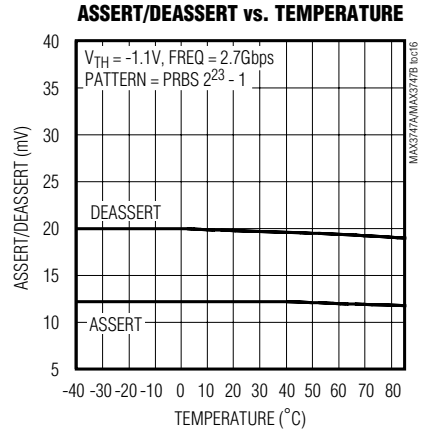
LOS ASSERT/DEASSERT TIMES vs. INPUT AMPLITUDE (HIGH R_{TH1}/R_{TH2} SETTINGS)



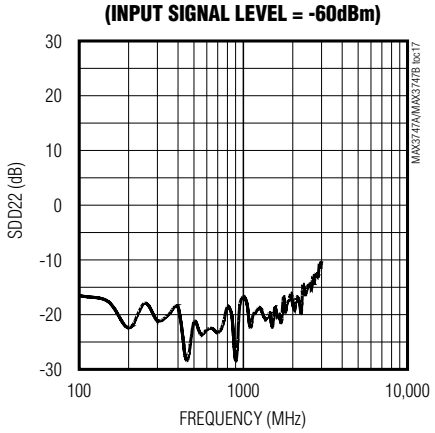
ASSERT/DEASSERT vs. V_{TH}



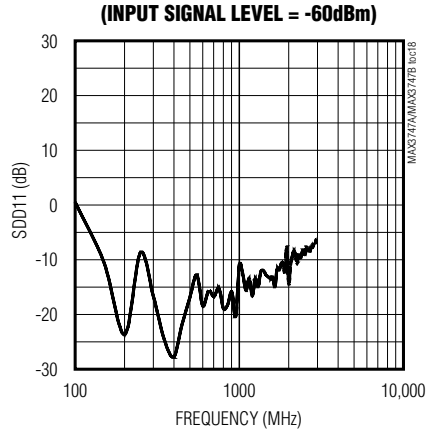
ASSERT/DEASSERT vs. TEMPERATURE



OUTPUT RETURN vs. FREQUENCY (SDD22) (INPUT SIGNAL LEVEL = -60dBm)



INPUT RETURN vs. FREQUENCY (SDD11) (INPUT SIGNAL LEVEL = -60dBm)



Pin Description

PIN	NAME		FUNCTION
	MAX3747A/ MAX3747B	MICREL SY8893V	
1	DISABLE	$\overline{EN}$	Disable Function Pin. The data outputs are held static when this pin is asserted high, transistor-to-transistor logic (TTL). The data outputs are enabled when this pin is held low. LOS functions remain active when outputs are disabled. For normal operation connect to GND.
2	IN+	DIN	Noninverted Input Signal
3	IN-	$\overline{DIN}$	Inverted Input Signal
4	V_{REF}	V_{REF}	Reference Voltage for LOS Threshold Setting
5	TH	LOSLVL	Loss-of-Signal Level Set. A voltage on this pin created by a two-resistor divider sets the threshold level. Connect one resistor from this pin to V_{CC} and another from this pin to V_{REF} (see Figure 5).
6	GND	GND	Ground
7	LOS	LOS	Loss of Signal. Open collector for the MAX3747A; internal 100kΩ pullup to V_{CC} for the MAX3747B. LOS is high when the level of the input signal drops below the preset threshold set by the TH input. LOS is deasserted low when the signal level is above the threshold.
8	OUT-	$\overline{DOUT}$	Inverted Data Output, CML
9	OUT+	DOUT	Noninverted Data Output, CML
10	V_{CC}	V_{CC}	Positive Power Supply

Detailed Description

The limiting amplifiers consist of a multistage amplifier, offset-correction circuitry, an output buffer, and loss-of-signal detect circuitry (see the *Functional Diagram*).

Input Stage

The input stage is shown in Figure 3. It provides 50Ω termination to V_{REF} for each input signal, IN+ and IN-. The MAX3747A/MAX3747B should be AC-coupled.

Multistage Amplifier

The high-bandwidth multistage amplifier provides approximately 61dB of gain for the MAX3747A/MAX3747B.

Offset Correction Loop

The MAX3747A/MAX3747B are susceptible to DC offsets in the signal path because they have high gain. In communication systems using NRZ data with a 50% duty cycle, pulse-width distortion present in the signal or generated in the transimpedance amplifier appears as an input offset and is reduced by the offset correction loop.

The offset correction loop sets a low-frequency cutoff of 3.2kHz.

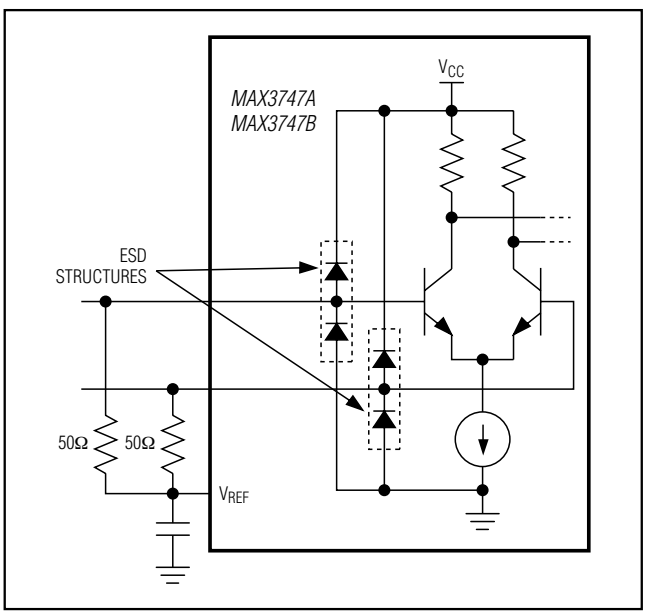
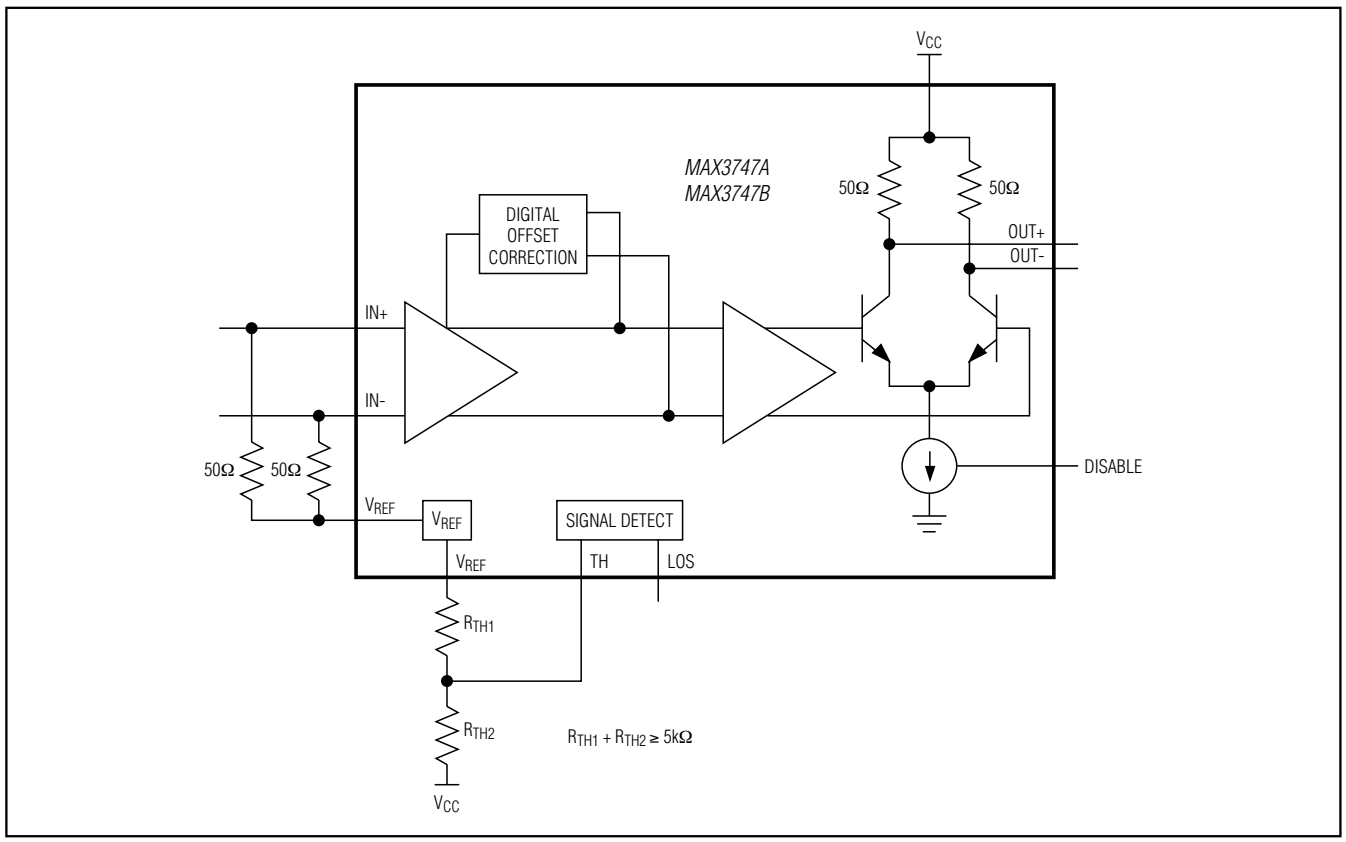


Figure 3. Differential Input Stage

Functional Diagram



CML Output Buffer

The CML outputs of the MAX3747A/MAX3747B limiting amplifiers provide high tolerance to impedance mismatches and inductive connectors. The output current is approximately 16mA for the MAX3747A/MAX3747B. Connecting the DISABLE pin to V_{CC} disables the output. If the LOS pin is connected to the DISABLE pin, the outputs OUT+ and OUT- are at a static voltage (squelch) whenever the input signal level drops below the LOS threshold. The output buffer can be AC- or DC-coupled to the load (Figure 4).

The MAX3747A/MAX3747B output is 800mV_{P-P}.

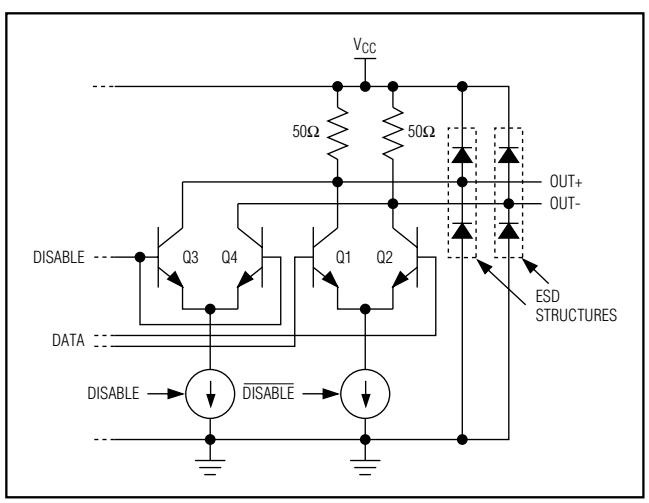


Figure 4. CML Output Buffer

Loss-of-Signal Indicator

The MAX3747A/MAX3747B are equipped with LOS circuitry that indicates when the input signal is below a programmable threshold, set by a voltage on the TH pin (see the *Typical Operating Characteristics*). The voltage on the TH pin is set by two resistors, one connecting from the TH pin to V_{CC} and the other connecting from TH to V_{REF} (Figure 5). An RMS power detector compares the input signal amplitude with this threshold and feeds the signal-detect information to the LOS output, which is open collector. To prevent LOS chatter in the region of the programmed threshold, approximately 2dB of hysteresis is built into the LOS assert/deassert function. Once asserted, LOS is not deasserted until the input amplitude rises to the required level. Figure 6 shows the LOS output circuit.

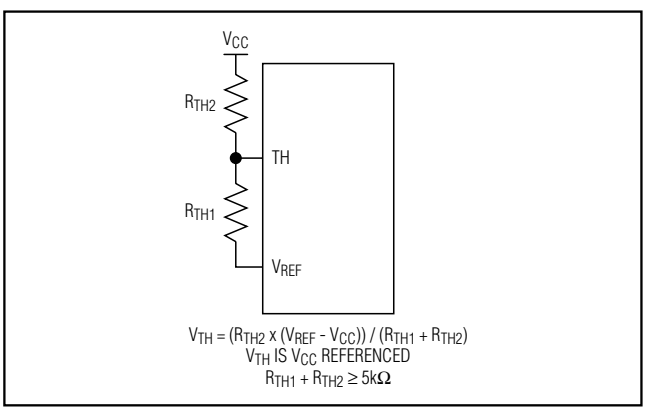


Figure 5. MAX3747A/MAX3747B LOS Threshold Circuit

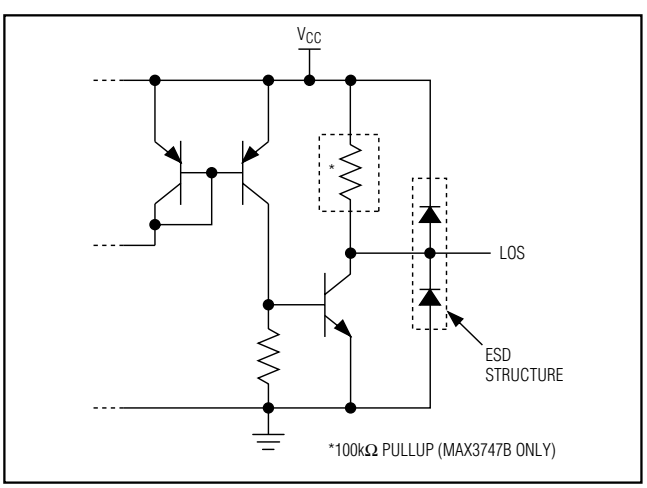


Figure 6. MAX3747A/MAX3747B LOS Output Circuit

Applications Information

Program the LOS Assert Threshold

Program the LOS assert threshold according to Figure 5. The combination of R_{TH1} and R_{TH2} should be greater than or equal to 5kΩ, see the Assert/Deassert vs. V_{TH} graph in the *Typical Operating Characteristics*.

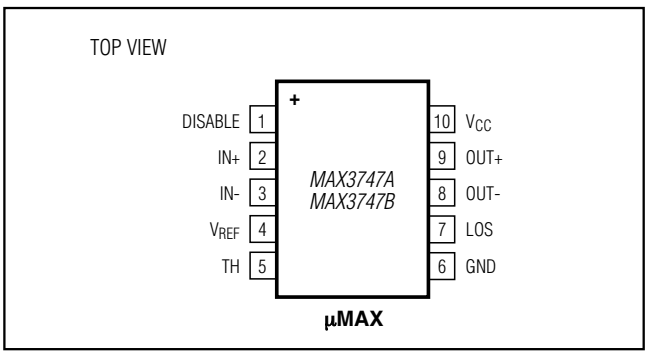
Select the Coupling Capacitor

When AC-coupling is desired, coupling capacitors C_{IN} and C_{OUT} should be selected to minimize the receiver's deterministic jitter. Jitter is decreased as the input low-frequency cutoff (f_{IN}) is decreased:

$$f_{IN} = 1/[2\pi(50)(C_{IN})]$$

For all applications, the recommended value for C_{IN} and C_{OUT} is 0.1µF, which provides f_{IN} equal to 32kHz. Refer to Application Note HFAN-1.1: *Choosing AC-Coupling Capacitors* on the Maxim website (www.maximintegrated.com).

Pin Configuration



Chip Information

PROCESS: SiGe Bipolar

Package Information

For the latest package outline information and land patterns (footprints), go to **www.maximintegrated.com/packages**. Note that a "+", "#", or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

PACKAGE TYPE	PACKAGE CODE	OUTLINE NO.	LAND PATTERN NO.
10 µMAX	U10CN+1	21-0061	90-0330

Revision History

REVISION NUMBER	REVISION DATE	DESCRIPTION	PAGES CHANGED
0	5/05	Initial release	—
1	10/07	Release of the MAX3747B.	1–10
2	8/12	Removed MAX3747 from data sheet, updated *Electrical Characteristics*.	1–10

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