MAX32625/MAX32626

Ultra-Low-Power Arm Cortex-M4 with FPU-Based Microcontroller (MCU) with 512KB Flash and 160KB SRAM

General Description

DARWIN is a new breed of low-power microcontrollers built to thrive in the rapidly evolving Internet of Things (IoT). They are smart, with the biggest memories in their class and a massively scalable memory architecture. They run forever, thanks to wearable-grade power technology. They are also tough enough to withstand the most advanced cyberattacks. DARWIN microcontrollers are designed to run any application imaginable—in places where you wouldn't dream of sending other microcontrollers.

Generation U microcontrollers are perfect for wearables and IoT applications that cannot afford to compromise power or performance. The MAX32625/MAX32626 feature an Arm® Cortex®-M4 with FPU CPU that delivers high-efficiency signal processing, ultra-low power consumption and ease of use.

Flexible power modes, an intelligent PMU, and dynamic clock and power gating optimize performance and power consumption for each application. Internal oscillators run at 96MHz for high-performance or 4MHz to maximize battery life in applications requiring always-on monitoring.

Multiple SPI, UART, I²C, 1-Wire® master, and USB interfaces are provided. The four-input, 10-bit ADC with selectable references can monitor external sensors.

All versions provide a hardware AES engine. The MAX32626 provides a secure trust protection unit (TPU) with a modular arithmetic accelerator (MAA) for fast ECDSA, a hardware PRNG entropy generator, and a secure boot loader. The MAX32625L provides a reduced 256KB of flash memory and 128KB of SRAM.

Applications

- Sports Watches
- Fitness Monitors
- Wearable Medical Patches
- Portable Medical Devices
- Sensor Hubs

***Ordering Information* appears at end of data sheet.**

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1-Wire is a registered trademark of Maxim Integrated Products, Inc.

Benefits and Features

- High-Efficiency Microcontroller for Wearable Devices
  - Internal Oscillator Operates Up to 96MHz
  - Low Power 4MHz Oscillator System Clock Option for Always-On Monitoring Applications
  - 512KB Flash Memory (256KB "L" Version)
  - 160KB SRAM (128KB "L" Version)
  - 8KB Instruction Cache
  - 1.2V Core Supply Voltage
  - 1.8V to 3.3V I/O
  - Optional 3.3V ±5% USB Supply Voltage
  - Wide Operating Temperature: -30°C to +85°C
- Power Management Maximizes Uptime for Battery Applications
  - 106µA/MHz Active Current Executing from Cache
  - 49µA/MHz Active Current Executing from Flash
  - Wake-Up to 96MHz Clock or 4MHz Clock
  - 600nA Low Power Mode (LP0) Current with RTC Enabled
  - 2.56µW Ultra-Low Power Data Retention Sleep Mode (LP1) with Fast 5µs Wake-Up on 96MHz Clock Source
  - 27µA/MHz Low Power Mode (LP2) Current
- Optimal Peripheral Mix Provides Platform Scalability
  - SPI Execute in Place (SPIX) Engine for Memory Expansion with Minimal Footprint
  - Three SPI Masters, One SPI Slave
  - Three UARTs
  - Up to Two I²C Masters, One I²C Slave
  - 1-Wire Master
  - Full-Speed USB 2.0 Device with Internal Transceiver
  - Sixteen Pulse Train (PWM) Engines
  - Six 32-Bit Timers and 3 Watchdog Timers
  - Up to 40 General-Purpose I/O Pins
  - 10-Bit Delta-Sigma ADC Operating at 7.8ksps
  - AES -128, -192, -256
  - RTC Calibration Output
- Secure Valuable IP and Data with Robust Internal Hardware Security (MAX32626 Only)
  - Trust Protection Unit (TPU) Provides ECDSA and Modular Arithmetic Acceleration Support
  - True Random Number Generator
  - Secure Boot Loader

19-8596; Rev 6; 2/20

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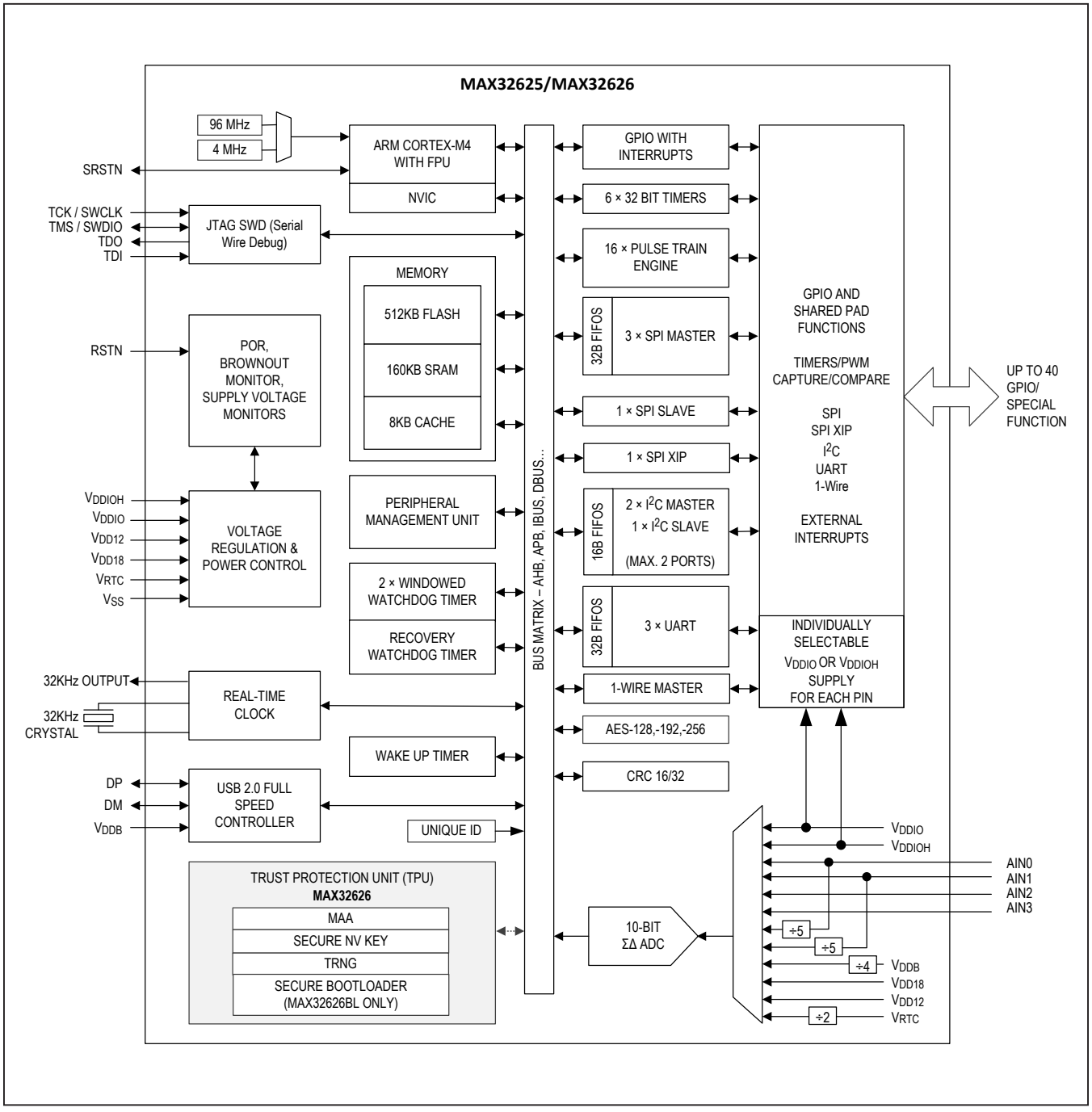
Simplified Block Diagram



Absolute Maximum Ratings

V_{DD18} .....-0.3V to +1.89V
V_{DD12} .....-0.3V to +1.32V
V_{RTC} .....-0.3V to +1.89V
V_{DDB} .....-0.3V to +3.6V
V_{DDIO} .....-0.3V to +3.6V
V_{DDIOH} .....-0.3V to +3.6V
32KIN, 32KOUT.....-0.3V to +3.6V
RSTN, SRSTN, DP, DM, GPIO, JTAG .....-0.3V to +3.6V
AIN[1:0].....-0.3V to +5.5V
AIN[3:2].....-0.3V to +3.6V

(All voltages with respect to V_{SS}, unless otherwise noted.)

Total Current into All V_{DDIO} and V_{DDIOH} Power Pins Combined (Sink) 100mA
Total Current into V_{SS} 100mA
Output Current (Sink) by Any I/O Pin 25mA
Output Current (Source) by Any I/O Pin.....-25mA
Continuous Package Power Dissipation TQFN (multilayer board) T_A = +70°C (derate 49.5mW/°C above +70°C).....3960.4mW
Operating Temperature Range..... -30°C to +85°C
Storage Temperature Range ..... -65°C to +150°C
Soldering Temperature (reflow) .....+260°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Package Information

63 WLP

PACKAGE CODE	W6333B+1
Outline Number	21-100084
Land Pattern Number	Refer to Application Note 1891
Thermal Resistance, Single Layer Board:	
Junction-to-Ambient (θ_{JA})	N/A
Junction-to-Case Thermal Resistance (θ_{JC})	N/A
Thermal Resistance, Four Layer Board:	
Junction-to-Ambient (θ_{JA})	35.87ºC/W
Junction-to-Case Thermal Resistance (θ_{JC})	N/A

68 TQFN-EP

PACKAGE CODE	T6888+1
Outline Number	21-0510
Land Pattern Number	90-0354
Thermal Resistance, Single Layer Board:	
Junction-to-Ambient (θ_{JA})	N/A
Junction-to-Case Thermal Resistance (θ_{JC})	N/A
Thermal Resistance, Four Layer Board:	
Junction-to-Ambient (θ_{JA})	20.20ºC/W
Junction-to-Case Thermal Resistance (θ_{JC})	1ºC/W

For the latest package outline information and land patterns (footprints), go to **www.maximintegrated.com/packaging**. Note that a "+", "#", or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

Package thermal resistances were obtained using the method described in JEDEC specification JESD51-7, using a four-layer board. For detailed information on package thermal considerations, refer to **www.maximintegrated.com/thermal-tutorial**.

Electrical Characteristics

(Limits are 100% tested at T_A = +25ºC and T_A = +85ºC. Limits over the operating temperature range and relevant supply voltage range are guaranteed by design and characterization. Specifications marked GBD are guaranteed by design and not production tested. Specifications to -30°C are guaranteed by design and are not production tested.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
POWER SUPPLIES						
Supply Voltage	V_{DD18}		1.71	1.8	1.89	V
	V_{DD12}		1.14	1.2	1.26	
	V_{RTC}		1.75	1.8	1.89	
	V_{DDIO}		1.71	1.8	3.6	
	V_{DDIOH}	V_{DDIOH} must be ≥ V_{DDIO}	1.71	1.8	3.6	
1.2V Internal Regulator	V_{REG12}		1.14	1.2	1.26	V
Power-Fail Reset Voltage	V_{RST}	Monitors V_{DD18}	1.61		1.7	V
Power-On Reset Voltage	V_{POR}	Monitors V_{DD18}		1.5		V
RAM Data Retention Voltage	V_{DRV}	V_{DD12} supply, retention in LP1		0.930		mV
V_{DD12} Dynamic Current, LP3 Mode	I_{DD12_DLP3}	Measured on the V_{DD12} pin and executing code from cache memory, all inputs are tied to V_{SS} or V_{DD18}, outputs do not source/sink any current, PMU disabled		106		µA/MHz
V_{DD12} Fixed Current, LP3 Mode	I_{DD12_FLP3}	96MHz oscillator selected as system clock, measured on the V_{DD12} pin and executing code from cache memory, all inputs are tied to V_{SS} or V_{DD18}, outputs do not source/sink any current		87		µA
		4MHz oscillator selected as system clock, measured on the V_{DD12} pin and executing code from cache memory, all inputs are tied to V_{SS} or V_{DD18}, outputs do not source/sink any current		39		
V_{DD18} Fixed Current, LP3 Mode	I_{DD18_FLP3}	96MHz oscillator selected as system clock, measured on the V_{DD18} pin and executing code from cache memory, all inputs are tied to V_{SS} or V_{DD18}, outputs do not source/sink any current		366		µA
		4MHz oscillator selected as system clock, measured on the V_{DD18} pin and executing code from cache memory, all inputs are tied to V_{SS} or V_{DD18}, outputs do not source/sink any current		33		
V_{DD12} Dynamic Current, LP2 Mode	I_{DD12_DLP2}	Measured on the V_{DD12} pin, ARM in sleep mode, PMU with two channels active		27		µA/MHz

Electrical Characteristics (continued)

(Limits are 100% tested at T_A = +25ºC and T_A = +85ºC. Limits over the operating temperature range and relevant supply voltage range are guaranteed by design and characterization. Specifications marked GBD are guaranteed by design and not production tested. Specifications to -30°C are guaranteed by design and are not production tested.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
V_{DD12} Fixed Current, LP2 Mode	I_{DD12_FLP2}	96MHz oscillator selected as system clock, measured on the V_{DD12} pin, ARM in sleep mode, PMU with two channels active		87		µA
		4MHz oscillator selected as system clock, measured on the V_{DD12} pin, ARM in sleep mode, PMU with two channels active		39		
V_{DD18} Fixed Current, LP2 Mode	I_{DD18_FLP2}	96MHz oscillator selected as system clock, measured on the V_{DD18} pin, ARM in sleep mode, PMU with two channels active		366		µA
		4MHz oscillator selected as system clock, measured on the V_{DD18} pin, ARM in sleep mode, PMU with two channels active		33		
V_{DD12} Fixed Current, LP1 Mode	I_{DD12_FLP1}	Standby state with full data retention		1.06		µA
V_{DD18} Fixed Current, LP1 Mode	I_{DD18_FLP1}	Standby state with full data retention		120		nA
V_{RTC} Fixed Current, LP1 Mode	I_{DDRTC_FLP1}	RTC enabled, retention regulator powered by V_{DD12}		594		nA
V_{DD12} Fixed Current, LP0 Mode	I_{DD12_FLP0}			14		nA
V_{DD18} Fixed Current, LP0 Mode	I_{DD18_FLP0}			120		nA
V_{RTC} Fixed Current, LP0 Mode	I_{DDRTC_FLP0}	RTC enabled		505		nA
		RTC disabled		105		
LP2 Mode Resume Time	t_{LP2_ON}			0		µs
LP1 Mode Resume Time	t_{LP1_ON}			5		µs
LP0 Mode Resume Time	t_{LP0_ON}	Polling flash ready		11		µs
GENERAL-PURPOSE I/O						
Input Low Voltage for All GPIO	V_{IL_GPIO}	V_{DDIO} selected as I/O supply, pin configured as GPIO			0.3 × V_{DDIO}	V
		V_{DDIOH} selected as I/O supply, pin configured as GPIO			0.3 × V_{DDIOH}	
Input Low Voltage for RSTN	V_{IL_RSTN}				0.3 x V_{RTC}	V
Input Low Voltage for SRSTN	V_{IL_SRSTN}				0.3 x V_{DDIO}	
Input High Voltage for All GPIO	V_{IH_GPIO}	V_{DDIO} selected as I/O supply, pin configured as GPIO	0.7 × V_{DDIO}			V
	V_{IH_GPIOH}	V_{DDIOH} selected as I/O supply, pin configured as GPIO	0.7 × V_{DDIOH}			

Electrical Characteristics (continued)

(Limits are 100% tested at T_A = +25ºC and T_A = +85ºC. Limits over the operating temperature range and relevant supply voltage range are guaranteed by design and characterization. Specifications marked GBD are guaranteed by design and not production tested. Specifications to -30°C are guaranteed by design and are not production tested.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Input High Voltage for RSTN	V_{IH_RSTN}		0.7 x V_{RTC}			V
Input High Voltage for SRSTN	V_{IH_SRSTN}		0.7 x V_{DDIO}			V
Output Low Voltage for All GPIO	V_{OL_GPIO}	I_{OL} = 4mA, V_{DDIO} = V_{DDIOH} = 1.71V, V_{DDIO} selected as I/O supply, normal drive configuration, pin configured as GPIO		0.2	0.4	V
		I_{OL} = 24mA, V_{DDIO} = V_{DDIOH} = 1.71V, V_{DDIO} selected as I/O supply, fast drive configuration, pin configured as GPIO		0.2	0.4	
		I_{OL} = 900µA, V_{DDIO} = 1.71V, V_{DDIOH} = 2.97V, V_{DDIOH} selected as I/O supply, pin configured as GPIO		0.2	0.4	
Output High Voltage for All GPIO	V_{OH_GPIO}	I_{OH} = -2mA, V_{DDIO} = V_{DDIOH} = 1.71V, V_{DDIO} selected as I/O supply, normal drive configuration, pin configured as GPIO	V_{DDIO} - 0.4			V
		I_{OH} = -8mA, V_{DDIO} = V_{DDIOH} = 1.71V, V_{DDIO} selected as I/O supply, fast drive configuration, pin configured as GPIO	V_{DDIO} - 0.4			
		I_{OH} = -900µA, V_{DDIOH} = 3.6V, V_{DDIOH} selected as I/O supply, pin configured as GPIO	V_{DDIOH} - 0.4			
		I_{OH} = -2mA, V_{DDIO} = 1.71V, V_{DDIOH} = 3.6V, V_{DDIO} selected as I/O supply, pin configured as GPIO	V_{DDIO} - 0.50			
Combined I_{OL}, All GPIO	I_{OL_TOTAL}				48	mA
Combined I_{OH}, All GPIO	I_{OH_TOTAL}				-48	mA
Input Hysteresis (Schmitt)	V_{IHYS}			300		mV
Input/Output Pin Capacitance for All Pins	C_{IO}			3		pF
Input Leakage Current Low	I_{IL}	V_{DDIO} = 1.89V, V_{DDIOH} = 3.6V, V_{DDIOH} selected as I/O supply, V_{IN} = 0V, internal pullup disabled	-100		+100	nA
Input Leakage Current High	I_{IH}	V_{DDIO} = 1.89V, V_{DDIOH} = 3.6V, V_{DDIOH} selected as I/O supply, V_{IN} = 3.6V, internal pulldown disabled	-100		+100	nA
	I_{OFF}	V_{DDIO} = 0V, V_{DDIOH} = 0V, V_{DDIO} selected as I/O supply, V_{IN} < 1.89V	-1		+1	µA
	I_{IH3V}	V_{DDIO} = V_{DDIOH} = 1.71V, V_{DDIO} selected as I/O supply, V_{IN} = 3.6V	-2		+2	

Electrical Characteristics (continued)

(Limits are 100% tested at T_A = +25ºC and T_A = +85ºC. Limits over the operating temperature range and relevant supply voltage range are guaranteed by design and characterization. Specifications marked GBD are guaranteed by design and not production tested. Specifications to -30°C are guaranteed by design and are not production tested.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Input Pullup Resistor to SRSTN, TMS, TCK, TDI	R_{PU_VDDIO}	Pullup to V_{DDIO}		25		kΩ
Input Pullup Resistor to RSTN	R_{PU_VRTC}	Pullup to V_{RTC}		25		kΩ
Input Pullup/Pulldown Resistor for All GPIO	R_{PU_NORM}	Normal resistance, pin configured as GPIO		25		kΩ
	R_{PU_HIGH}	Highest resistance, pin configured as GPIO		1		MΩ
JTAG						
Input Low Voltage for TCK, TMS, TDI	V_{IL}				0.3 x V_{DDIO}	V
Input High Voltage for TCK, TMS, TDI	V_{IH}		0.7 x V_{DDIO}			V
Output Low Voltage for TDO	V_{OL}			0.2	0.4	V
Output High Voltage for TDO	V_{OH}		V_{DDIO} - 0.4			V
CLOCKS						
System Clock Frequency	f_{SYS_CLK}		0.001		98	MHz
System Clock Period	t_{SYS_CLK}			$1/f_{SYS_CLK}$		ns
Internal Relaxation Oscillator Frequency	f_{INTCLK}	Factory default	94	96	98	MHz
		Firmware trimmed, required for USB compliance	95.76	96	96.24	
Internal RC Oscillator Frequency	f_{RCCLK}		3.9	4	4.1	MHz
RTC Input Frequency	f_{32KIN}	32kHz watch crystal, 6pF, ESR < 70kΩ		32.768		kHz
RTC Operating Current	I_{RTC_LP23}	LP2 or LP3 mode		0.7		µA
	I_{RTC_LP01}	LP0 or LP1 mode		0.35		
RTC Power-Up Time	t_{RTC_ON}			250		ms
FLASH MEMORY						
Page Size				8		KB
Flash Erase Time	t_{M_ERASE}	Mass erase		30		ms
	t_{P_ERASE}	Page erase		30		
Flash Programming Time Per Word	t_{PROG}			60		µs
Flash Endurance			10			kcycles
Data Retention	t_{RET}	T_A = +25°C	10			years

Electrical Characteristics—ADC

(Internal bandgap reference selected and ADC_SCALE = ADC_REFSCL = 1 unless otherwise specified. Specifications marked GBD are guaranteed by design and not production tested.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Resolution				10		Bits
ADC Clock Rate	f_{ADC_CLK}		0.1		8	MHz
ADC Clock Period	t_{ADC_CLK}			$1/f_{ADC_CLK}$		µs
Input Voltage Range	V_{AIN}	AIN0-AIN3, ADC_CHSEL = 0–3, BUF_BYPASS = 0	0.05		V_{DD18}	V
		AIN0–AIN1, ADC_CHSEL = 4–5, BUF_BYPASS = 0	0.05		5.5	
		AIN0–AIN3, ADC_CHSEL = 0–3, BUF_BYPASS = 1	V_{SS}		V_{DD18}	
		AIN0-AIN1, ADC_CHSEL = 4–5, BUF_BYPASS = 1	V_{SS}		5.5	
Input Dynamic Current, Switched Capacitance	I_{AIN}	ADC active, ADC buffer bypassed		4.5		µA
		ADC active, ADC buffer enabled		50		nA
Analog Input Capacitance	C_{AIN}	Fixed capacitance to V_{SS}		1		pF
		Dynamically switched capacitance		250		nF
Integral Nonlinearity	INL				±2	LSB
Differential Nonlinearity	DNL				±1	LSB
Offset Error	V_{OS}			±1		LSB
Gain Error	GE			±2		LSB
Signal-to-Noise Ratio	SNR			58.5		dB
Signal-to-Noise and Distortion	SINAD			58.5		dB
Total Harmonic Distortion	THD			-68.5		dB
Spurious Free Dynamic Range	SFDR			74		dB
ADC Active Current	I_{ADC}	ADC active, reference buffer enabled, input buffer disabled		240		µA
Input Buffer Active Current	I_{INBUF}			53		µA
ADC Setup Time	t_{ADC_SU}	Any power-up of ADC clock, ADC bias, reference buffer or input buffer, to CpuAdcStart			10	µs
		Any power-up of ADC clock or ADC bias to CpuAdcStart			48	tACLK
ADC Output Latency	t_{ADC}			1025		tACLK
ADC Sample Rate	f_{ADC}				7.8	ksps
ADC Input Leakage	I_{ADC_LEAK}	AIN0 or AIN1, ADC inactive or channel not selected		0.12	4	nA
		AIN2 or AIN3, ADC inactive or channel not selected		0.02	1	

Electrical Characteristics—ADC (continued)

(Internal bandgap reference selected and ADC_SCALE = ADC_REFSCL = 1 unless otherwise specified. Specifications marked GBD are guaranteed by design and not production tested.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
AIN0/AIN1 Resistor Divider Error		ADC_CHSEL = 4 or 5, not including ADC offset/gain error		±2		LSB
Full-Scale Voltage	V_{FS}	ADC code = 0x3FF		1.2		V
Bandgap Temperature Coefficient	V_{TEMPCO}	Box method		30		ppm/°C

Electrical Characteristics—USB

(V_{DD18} = V_{RST} to 1.89V, T_A = -30°C to +85°C.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
USB PHY Supply Voltage	V_{DDB}			3.3		V
Single-Ended Input High Voltage DP, DM	V_{IHD}		2			V
Single-Ended Input Low Voltage DP, DM	V_{ILD}				0.8	V
Output Low Voltage DP, DM	V_{OLD}	R_L = 1.5kΩ from DP to 3.6V			0.3	V
Output High Voltage DP, DM	V_{OHD}	R_L = 15kΩ from DP and DM to V_{SS}	2.8			V
Differential Input Sensitivity DP, DM	V_{DI}	DP to DM	0.2			V
Common-Mode Voltage Range	V_{CM}	Includes V_{DI} range	0.8		2.5	V
Single-Ended Receiver Threshold	V_{SE}		0.8		2	V
Single-Ended Receiver Hysteresis	V_{SEH}			200		mV
Differential Output Signal Cross-Point Voltage	V_{CRS}	C_L = 50pF, GBD	1.3		2	V
DP, DM Off-State Input Impedance	R_{LZ}		300			kΩ
Driver Output Impedance	R_{DRV}	Steady-state drive	28		44	Ω
DP Pullup Resistor	R_{PU}	Idle	0.9		1.575	kΩ
DP Pullup Resistor	R_{PU}	Receiving	1.425		3.09	kΩ
USB TIMING						
DP, DM Rise Time (Transmit)	t_R	C_L = 50pF, GBD	4		20	ns
DP, DM Fall Time (Transmit)	t_F	C_L = 50pF, GBD	4		20	ns
Rise/Fall Time Matching (Transmit)	t_R, t_F	C_L = 50pF, GBD	90		110	%

Electrical Characteristics—SPI Master/SPIX Master

(Timing specifications are guaranteed by design and are not production tested.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Master Operating Frequency	f_{MCK}				48	MHz
Master SCLK Period	t_{MCK}			$1/f_{MCK}$		ns
SCLK Output Pulse-Width High	t_{MCH}		$t_{MCK}/2$			ns
SCLK Output Pulse-Width Low	t_{MCL}		$(t_{MCK}/2) - 4$			ns
MOSI Output Hold Time After SCLK Sample Edge	t_{MOH}		$(t_{MCK}/2) - 4$			ns
MOSI Output Valid to Sample Edge	t_{MOV}		$(t_{MCK}/2) - 4$			ns
MISO Input Valid to SCLK Sample Edge Setup	t_{MIS}		1			ns
MISO Input to SCLK Sample Edge	t_{MIH}				1	ns

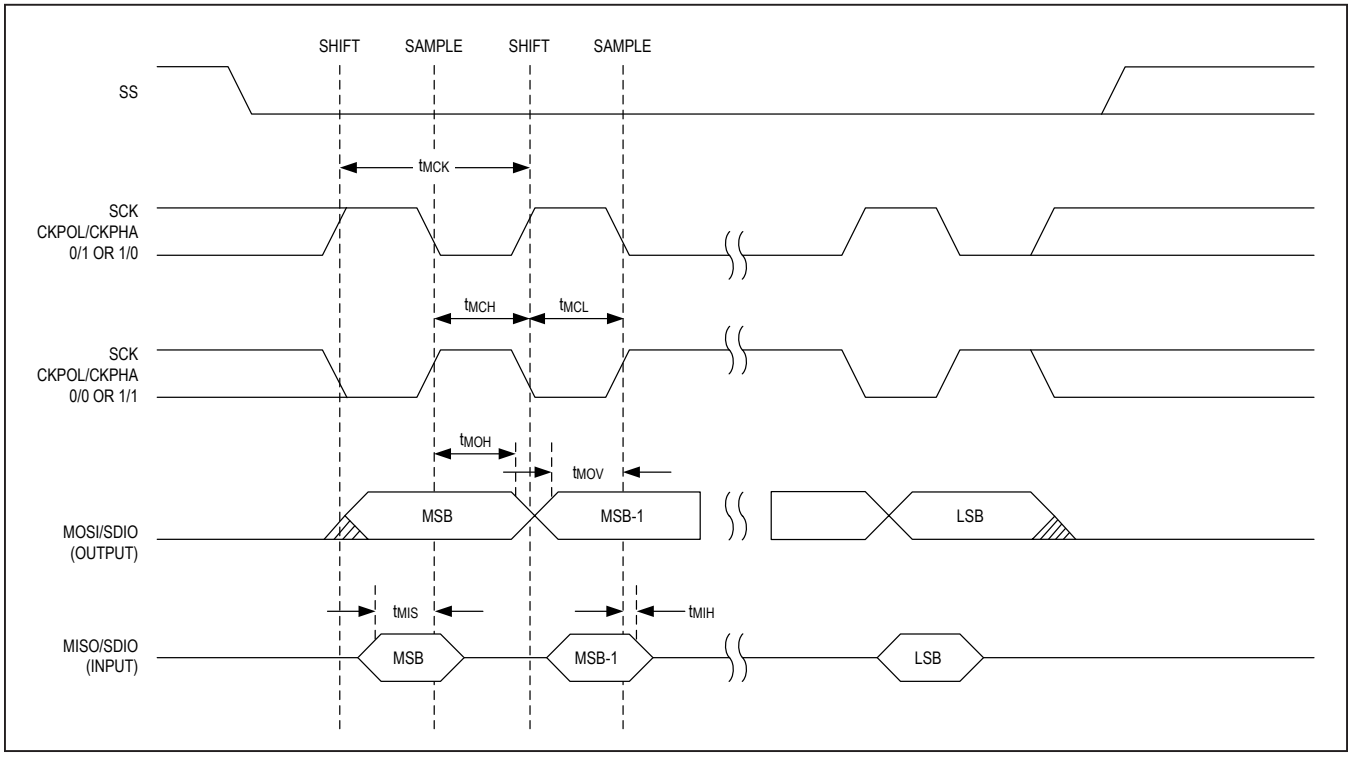


Figure 1. SPI Master and SPI XIP Master Timing

Electrical Characteristics—SPI Slave

(AC Electrical Specifications are guaranteed by design and are not production tested, V_{DD18} = V_{RST} to 1.89V, T_A = -30°C to +85°C.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Slave Operating Frequency	f_{SCK}	Standard SPI mode			22.7	MHz
		Fast SPI mode			45.5	
SCLK Period	t_{SCK}			$1/f_{SCK}$		ns

Electrical Characteristics—I²C Bus

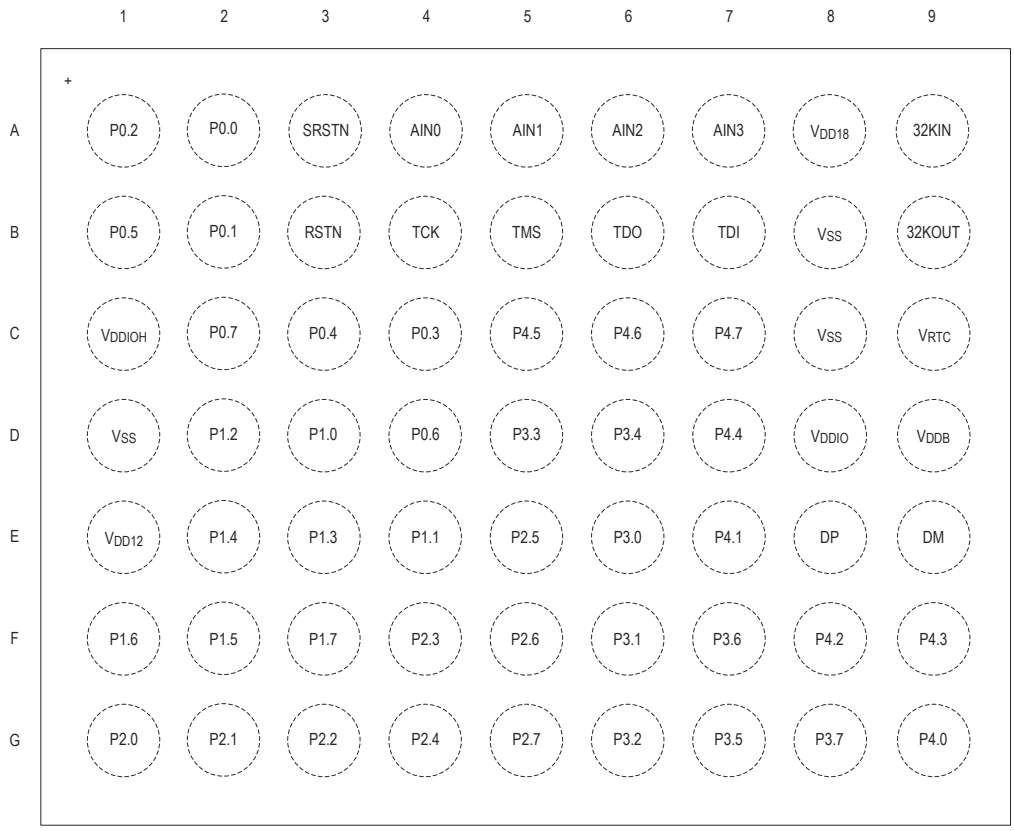
(Limits are 100% tested at T_A = +25°C and T_A = +85°C. Limits over the operating temperature range and relevant supply voltage range are guaranteed by design and characterization. Specifications marked "GBD" are guaranteed by design and not production tested.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
I²C BUS						
Input High Voltage	V_{IH_I2C}	Standard mode, V_{DDIO} selected as I/O supply	0.7 × V_{DDIO}			V
		Standard mode, V_{DDIOH} selected as I/O supply	0.7 × V_{DDIOH}			
		Fast mode, V_{DDIO} selected as I/O supply	0.7 × V_{DDIO}		V_{DDIO} + 0.5	
		Fast mode, V_{DDIOH} selected as I/O supply	0.7 × V_{DDIOH}		V_{DDIOH} + 0.5	
Input Low Voltage	V_{IL_I2C}	Standard mode, V_{DDIO} selected as I/O supply	-0.5		0.3 × V_{DDIO}	V
		Standard mode, V_{DDIOH} selected as I/O supply	-0.5		0.3 × V_{DDIOH}	
		Fast mode, V_{DDIO} selected as I/O supply	-0.5		0.3 × V_{DDIO}	
		Fast mode, V_{DDIOH} selected as I/O supply	-0.5		0.3 × V_{DDIOH}	
Input Hysteresis (Schmitt)	V_{IHYS_I2C}	Fast mode, V_{DDIO} selected as I/O supply	0.05 x V_{DDIO}			V
		Fast mode, V_{DDIOH} selected as I/O supply	0.05 x V_{DDIOH}			
Output Logic-Low (Open Drain or Open Collector)	V_{OL_I2C}	Standard mode, I_{IL} = 3mA	0		0.4	V
		Fast mode, I_{IL} = 3mA	0		0.4	
		Fast mode, I_{IL} = 2mA, V_{DDIO} selected as I/O supply	0		0.2 x V_{DDIO}	
		Fast mode, I_{IL} = 2mA, V_{DDIOH} selected as I/O supply	0		0.2 x V_{DDIOH}	
I²C TIMING						
SCL Clock Frequency	f_{SCL}	Standard mode	0		100	kHz
		Fast mode	0		400	

Pin Configurations

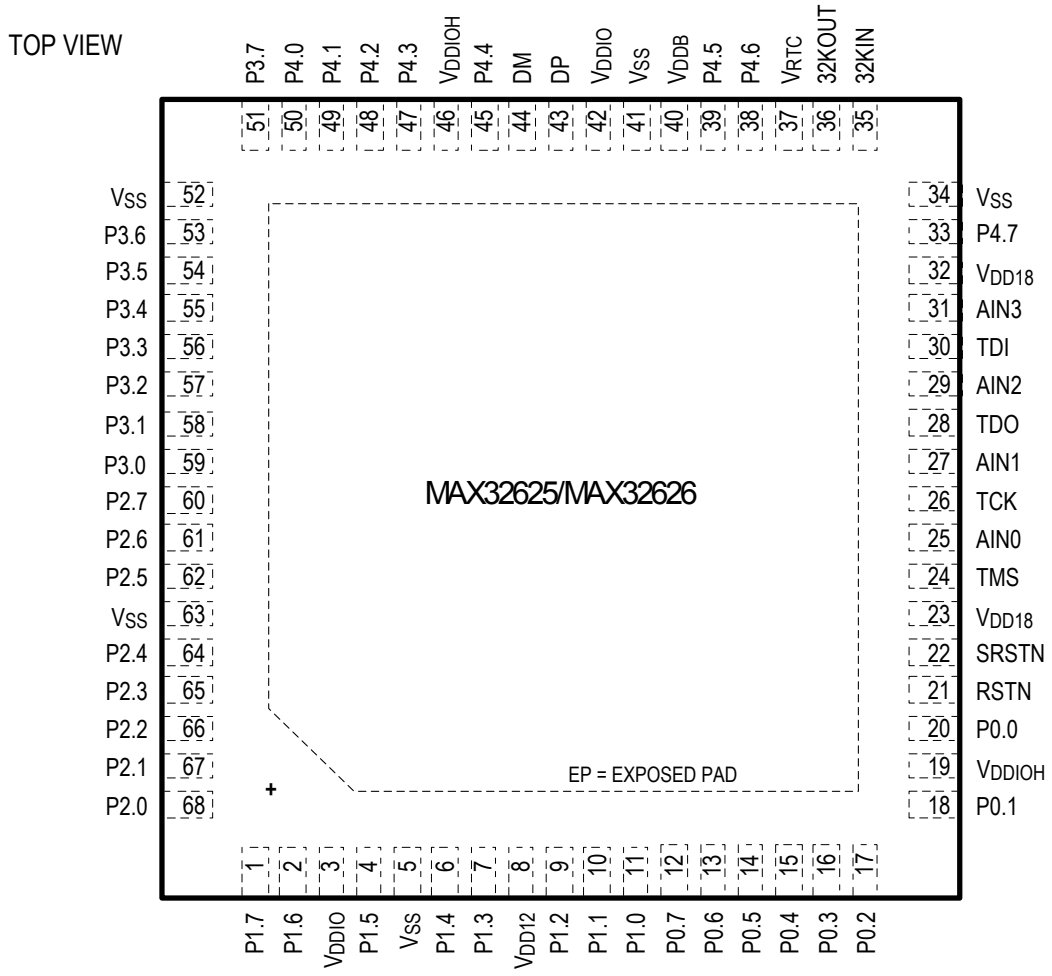
MAX32625/MAX32626

TOP VIEW (BUMP SIDE DOWN)



63 WLP

Pin Configurations (continued)



68 TQFN-EP

Pin Description

PIN		NAME	FUNCTION
63 WLP	68 TQFN-EP		
POWER PINS			
A8	23, 32	V_{DD18}	1.8V Supply Voltage. This pin must be bypassed to V_{SS} with a 1.0µF capacitor as close as possible to the package.
B8, C8, D1	5, 34, 41, 52, 63	V_{SS}	Digital Ground
C1	19, 46	V_{DDIOH}	I/O Supply Voltage, High. 1.8V ≤ V_{DDIOH} ≤ 3.6V, always with V_{DDIOH} ≥ V_{DDIO}. See EC table for V_{DDIOH} specification. This pin must be bypassed to V_{SS} with a 1.0µF capacitor as close as possible to the package.
C9	37	V_{RTC}	RTC Supply Voltage. This pin must be bypassed to V_{SS} with a 1.0µF capacitor as close as possible to the package.
D8	3, 42	V_{DDIO}	I/O Supply Voltage. 1.8V ≤ V_{DDIO} ≤ 3.6V. See EC table for V_{DDIO} specification. This pin must be bypassed to V_{SS} with a 1.0µF capacitor as close as possible to the package.
D9	40	V_{DDB}	USB Transceiver Supply Voltage. This pin must be bypassed to V_{SS} with a 1.0µF capacitor as close as possible to the package.
E1	8	V_{DD12}	1.2V Nominal Supply Voltage. This pin must be bypassed to V_{SS} with a 1.0µF capacitor as close as possible to the package.
—	—	EP	Exposed Pad (TQFN-EP Only). This pad must be connected to V_{SS}. Refer to Application Note 3273: *Exposed Pads: A Brief Introduction* for additional information.
CLOCK PINS			
A9	35	32KIN	32kHz Crystal Oscillator Input. Connect a 6pF 32kHz crystal between 32KIN and 32KOUT for RTC operation. Optionally, an external clock source can be driven on 32KIN if the 32KOUT pin is left unconnected. A 32kHz crystal or external clock source is required for proper USB operation.
B9	36	32KOUT	32kHz Crystal Oscillator Output
USB PINS			
E8	43	DP	USB DP Signal. This bidirectional pin carries the positive differential data or single-ended data. This pin is weakly pulled high internally when the USB is disabled.
E9	44	DM	USB DM Signal. This bidirectional pin carries the negative differential data or single-ended data. This pin is weakly pulled high internally when the USB is disabled.
JTAG PINS			
B4	26	TCK/SWCLK	JTAG Clock Serial Wire Debug Clock This pin has an internal 25kΩ pullup to V_{DDIO}.
B5	24	TMS/SWDIO	JTAG Test Mode Select Serial Wire Debug I/O This pin has an internal 25kΩ pullup to V_{DDIO}.

Pin Description (continued)

PIN		NAME	FUNCTION
63 WLP	68 TQFN-EP		
B6	28	TDO	JTAG Test Data Output
B7	30	TDI	JTAG Test Data Inputt. This pin has an internal 25kΩ pullup to V_{DDIO}.
RESET PINS			
A3	22	SRSTN	Software Reset, Active-Low Input/Output. The device remains in software reset while this pin is in its active state. When the pin transitions to its inactive state, the device performs a reset to the ARM core, digital registers and peripherals (resetting most of the core logic on the V_{DD12} supply). This reset does not affect the POR only registers, RTC logic, ARM debug engine or JTAG debugger allowing for a soft reset without having to reconfigure all registers. After the device senses SRSTN as a logic 0, the pin automatically reconfigures as an output sourcing a logic 0. The device continues to output for 6 system clock cycles and then repeats the input sensing/output driving until SRSTN is sensed inactive. This pin is internally connected with an internal 25kΩ pullup to the V_{DDIO} supply. This pin should be left unconnected if the system design does not provide a reset signal to the device.
B3	21	RSTN	Hardware Power Reset (Active-Low) Input. The device remains in reset while this pin is in its active state. When the pin transitions to its inactive state, the device performs a POR reset (resetting all logic on all supplies except for real-time clock circuitry) and begins execution. This pin is internally connected with an internal 25kΩ pullup to the V_{RTC} supply. This pin should be left unconnected if the system design does not provide a reset signal to the device.
GENERAL-PURPOSE I/O AND SPECIAL FUNCTIONS (See Table 1. General-Purpose I/O Matrix)			
A2	20	P0.0	GPIO Port 0.0
B2	18	P0.1	GPIO Port 0.1
A1	17	P0.2	GPIO Port 0.2
C4	16	P0.3	GPIO Port 0.3
C3	15	P0.4	GPIO Port 0.4
B1	14	P0.5	GPIO Port 0.5
D4	13	P0.6	GPIO Port 0.6
C2	12	P0.7	GPIO Port 0.7
D3	11	P1.0	GPIO Port 1.0
E4	10	P1.1	GPIO Port 1.1
D2	9	P1.2	GPIO Port 1.2
E3	7	P1.3	GPIO Port 1.3
E2	6	P1.4	GPIO Port 1.4
F2	4	P1.5	GPIO Port 1.5
F1	2	P1.6	GPIO Port 1.6
F3	1	P1.7	GPIO Port 1.7
G2	67	P2.1	GPIO Port 2.1
G3	66	P2.2	GPIO Port 2.2

Pin Description (continued)

PIN		NAME	FUNCTION
63 WLP	68 TQFN-EP		
F4	65	P2.3	GPIO Port 2.3
G4	64	P2.4	GPIO Port 2.4
E5	62	P2.5	GPIO Port 2.5
F5	61	P2.6	GPIO Port 2.6
G5	60	P2.7	GPIO Port 2.7
E6	59	P3.0	GPIO Port 3.0
F6	58	P3.1	GPIO Port 3.1
G6	57	P3.2	GPIO Port 3.2
D5	56	P3.3	GPIO Port 3.3
D6	55	P3.4	GPIO Port 3.4
G7	54	P3.5	GPIO Port 3.5
F7	53	P3.6	GPIO Port 3.6
G8	51	P3.7	GPIO Port 3.7
G9	50	P4.0	GPIO Port 4.0
E7	49	P4.1	GPIO Port 4.1
F8	48	P4.2	GPIO Port 4.2
F9	47	P4.3	GPIO Port 4.3
D7	45	P4.4	GPIO Port 4.4
C5	39	P4.5	GPIO Port 4.5
C6	38	P4.6	GPIO Port 4.6
C7	33	P4.7	GPIO Port 4.7
ANALOG INPUT PINS			
A4	25	AIN0	ADC Input 0. 5V Tolerant Input
A5	27	AIN1	ADC Input 1. 5V Tolerant Input
A6	29	AIN2	ADC Input 2
A7	31	AIN3	ADC Input 3

Detailed Description

MAX32625/MAX32626

The MAX32625/MAX32626 is an ultra-low power, high-efficiency, mixed-signal microcontroller based on the ARM Cortex-M4 with FPU with a maximum operating frequency of 96MHz with a hardware AES engine. An internal 4MHz oscillator supports minimal power consumption for applications requiring always-on monitoring. The MAX32626 is a secure version of the MAX32625, incorporating a trust protection unit (TPU) with advanced security features.

Application code executes from an internal 512KB program flash memory with up to 160KB SRAM available for general-application use. An 8KB instruction cache improves execution throughput, and a transparent code scrambling scheme is used to protect customer intellectual property residing in the internal program flash memory. Additionally, a SPI execute in place (SPIX) external memory interface allows application code and data (up to 16MB) to be accessed from an external SPI memory device.

The MAX32625L is a lower-cost version of the MAX32625, providing 256KB of flash and 128KB of SRAM.

A 10-bit delta-sigma ADC is provided with a multiplexer front end for four external input channels (two of which are 5.5V tolerant) and internal channels to monitor internal voltages. Built-in limit monitors allow converted input samples to be compared against user-configurable high and low limits with an option to trigger an interrupt and wake the CPU from a low power mode if attention is required.

A wide variety of communications and interface peripherals are provided. Other communications peripherals include a USB 2.0 slave interface, three master SPI interfaces, one slave SPI interface, three UART interfaces with multidrop support, up to two master I^2C interfaces, and one slave I^2C interface.

ARM Cortex-M4 with FPU Processor

The ARM Cortex-M4 with FPU processor is ideal for the emerging category of wearable medical and wellness applications. The architecture combines high-efficiency signal processing functionality with the low power, low cost, and ease-of-use benefits.

The ARM Cortex-M4 with FPU DSP supports single instruction multiple data (SIMD) path DSP extensions, providing:

- 4 parallel 8-bit add/sub
- 2 parallel 16-bit add/sub
- 2 parallel MACs
- 32- or 64-bit accumulate
- Signed, unsigned data with or without saturation

Power Operating Modes

Low Power Mode 0 (LP0)

This mode places the core and peripheral logic in a static, low-power state. All features of the device are disabled except:

- Power sequencer
- RTC clock (if enabled)
- Key data retention registers
- Power-on reset
- Voltage supply monitoring

Data retention in this mode can be maintained using only the V_{RTC} supply with all other voltage supplies disabled.

Low Power Mode 1 (LP1)

This mode places the core logic in a static, low-power state that supports a fast wake-up feature. Data retention in this mode can be maintained using only the V_{RTC} supply with all other voltage supplies disabled.

Low Power Mode 2 (LP2)

This configuration allows the ADC and some peripherals to operate while the ARM core is in sleep mode. The peripheral management unit provides intelligent, dynamic clocking of any enabled peripherals, ensuring the lowest possible power consumption.

Low Power Mode 3 (LP3)

During this state, the CPU is executing application code and all digital and analog peripherals are fully powered and awake. Dynamic clocking disables peripherals not in use, providing the optimal mix of high performance and low power consumption.

Analog-to-Digital Converter

The 10-bit delta-sigma ADC provides 4 external inputs and can also measure all internal power supplies. It operates at a maximum of 7.8ksps. AIN0 and AIN1 are 5V tolerant, making them suitable for monitoring batteries.

An optional feature allows samples captured by the ADC to be automatically compared against user-programmable high and low limits. Up to four channel limit pairs can be configured in this way. The comparison allows the ADC to trigger an interrupt (and potentially wake the CPU from a low power sleep mode) when a captured sample goes outside the preprogrammed limit range. Since this comparison is performed directly by the sample limit monitors, it can be performed even while the main CPU is suspended in a low power mode.

The ADC measures:

- AIN[3:2] (up to 3.3V)
- AIN[1:0] (up to 5.5V)
- V_{DD12}
- V_{DD18}
- V_{DDB}
- V_{RTC}
- V_{DDIO}
- V_{DDIOH}

Pulse Train Engine

16 independent pulse train generators can provide either a square wave or a repeating pattern from 2 bits to 32 bits in length. Any single pulse train generator or any desired group of pulse train generators can be synchronized at the bit level allowing for multibit patterns

Each pulse train generator is independently configurable.

The pulse train generators provide the following features:

- Independently enabled
- Multiple pin configurations allow for flexible layout
- Pulse trains can be started/synchronized independently or as a group
- Frequency of each enabled pulse train generator is also set separately, based on a divide down (divide by 2, divide by 4, divide by 8, and so on) of the input pulse train module clock
- Multiple repetition options for pulse train mode
  - Single shot (nonrepeating pattern of 2–32 bits)
  - Pattern repeats user-configurable number of times or indefinitely
  - End of one pulse train's loop count can restart one or more other pulse trains

Clocking Scheme

The high-frequency internal relaxation oscillator operates at a nominal frequency of 96MHz. It is the primary clock source for the digital logic and peripherals. Select the 4MHz internal oscillator to optimize active power consumption. Wake-up is possible from either the 4MHz or the 96MHz internal oscillator.

An external 32.766kHz time base is required when using the RTC or USB features of the device.

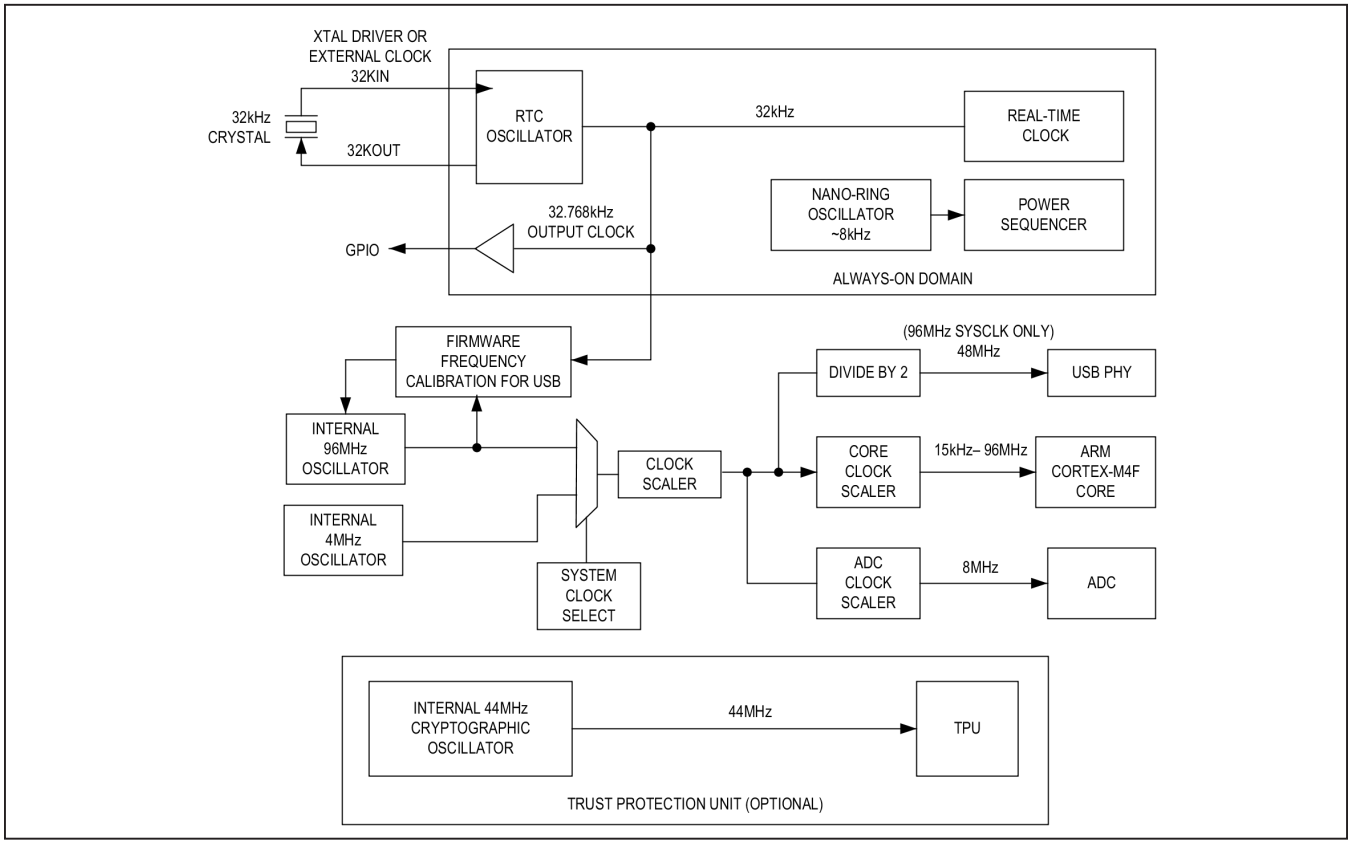


Figure 2. MAX32625/MAX32626 Clock Scheme

Interrupt Sources

The ARM nested vector interrupt controller (NVIC) provides high speed, deterministic interrupt response, interrupt masking, and multiple interrupt sources. Each peripheral is connected to the NVIC and can have multiple interrupt flags indicating the specific source of the interrupt within the peripheral. The NVIC provides:

- Up to 43 distinct interrupt sources (including internal and external interrupts)
- 8 priority levels
- A dedicated interrupt for each port

Real-Time Clock and Wake-Up Timer

A real-time clock (RTC) keeps the time of day in absolute seconds. The time base can be generated by connecting a 32kHz crystal between 32KIN and 32KOUT or an external clock source can be applied to the 32KIN pin. The external clock source must meet the electrical/timing requirements in the Electrical Characteristics table. The 32kHz output can be directed on a GPIO for observation and use.

The 32-bit seconds register can count up to approximately 136 years and be translated to calendar format by application software. A time-of-day alarm and independent subsecond alarm can cause an interrupt or wake the device from stop mode.

The wake-up timer allows the device to remain in low power mode for extended periods of time. The minimum wake-up interval is 244µs.

The V_{RTC} supply supports SRAM retention in power mode LP0.

General-Purpose I/O and Special Function Pins

General-purpose I/O (GPIO) pins are controlled directly by firmware or one or more peripheral modules connected to that pin. GPIO are logically divided into 8-pin ports. Each 8-bit port provides a dedicated interrupt.

The alternate functions for each pin are shown in Table 1.

The following features are independently configurable for each GPIO pin:

- GPIO or special function mode operation
- V_{DDIO} or V_{DDIOH} supply voltage
- Normal and fast output drive strength
- Open-drain output or high impedance input
- Configurable strong or weak internal pullup/pulldown resistors
- Simple output-only functions
  - Output from pulse trains (0 through 15)
  - Output from timers running in 32-bit mode

Some peripherals have optional pin assignments, allowing for greater flexibility during PCB layout. These optional pin assignments are identified with the letter "B," "C," or "D" after the peripheral name. For example, if the "A" configuration is chosen for UART0, the UART0_RX signal is mapped to the P0.0 pin. If the "B" configuration is chosen, the UART0_RX signal is mapped to the P0.1 pin.

CRC Module

A CRC hardware module provides fast calculations and data integrity checks by application software. The CRC module supports both the CRC-16-CCITT and CRC-32 ($X^{32} + X^{26} + X^{23} + X^{22} + X^{16} + X^{12} + X^{11} + X^{10} + X^8 + X^7 + X^5 + X^4 + X^2 + X + 1$) polynomials.

Watchdog Timers

Two independent watchdog timers (WDT0 and WDT1) with window support are provided. The watchdog timers are independent and have multiple clock source options to ensure system security. The watchdog uses a 32-bit timer with prescaler to generate the watchdog reset. When enabled, the watchdog timers must be fed prior to timeout or within a window of time if window mode is enabled. Failure to reset the watchdog timer during the programmed timing window results in a watchdog timeout. The WDT0 or WDT1 flags are set on reset if a watchdog expiration caused the system reset. The clock source options for the watchdog timers include:

- Scaled-system clock
- Real-time clock
- Power-management clock

A third watchdog timer (WDT2) is provided for recovery from runaway code or system unresponsiveness. When enabled, this watchdog must be reset prior to timeout, resulting in a watchdog timeout. The WDT2 flag is set on reset if a watchdog expiration caused the system reset.

WDT2 is unique in that is in the always-on domain, and continues to run even in LP1 or LP0. The timeout period for WDT2 can be programmed as long as 8 seconds. The granularity of the timeout period is intended only for system recovery.

Programmable Timers

Six 32-bit timers provide timing, capture/compare, or generation of pulse-width modulated (PWM) signals. Each of the 32-bit timers can also be split into two 16-bit timers, enabling 12 standard 16-bit timers.

The 32-bit timer provide a number of features:

- 32-bit up/down autoreload
- Programmable prescaler
- PWM output generation
- Capture, compare, and capture/compare capability
- External input pin for timer input, clock gating or capture, limited to an input frequency of 1/4 of the peripheral clock frequency
- Timer output pin
- Configurable as 2x 16-bit general-purpose timers
- Timer interrupt

Serial Peripherals

USB

The integrated USB slave controller is compliant with the full-speed (12Mb/s) USB 2.0 specification. The integrated USB physical interface (PHY) reduces board space and system cost. The USB is powered by the V_{DDB} supply.

The USB controller supports DMA for the endpoint buffers. A total of 7 endpoint buffers are supported with configurable selection of IN or OUT in addition to endpoint 0.

An external 32kHz crystal or clock source is required for USB operation, even if the RTC function is not used. Although the USB timing is derived from the internal 96MHz oscillator, the default accuracy is not sufficient for USB operation. Periodic firmware adjustments of the 96MHz oscillator, using the 32kHz timebase as a reference, are necessary to comply with the USB timing requirements.

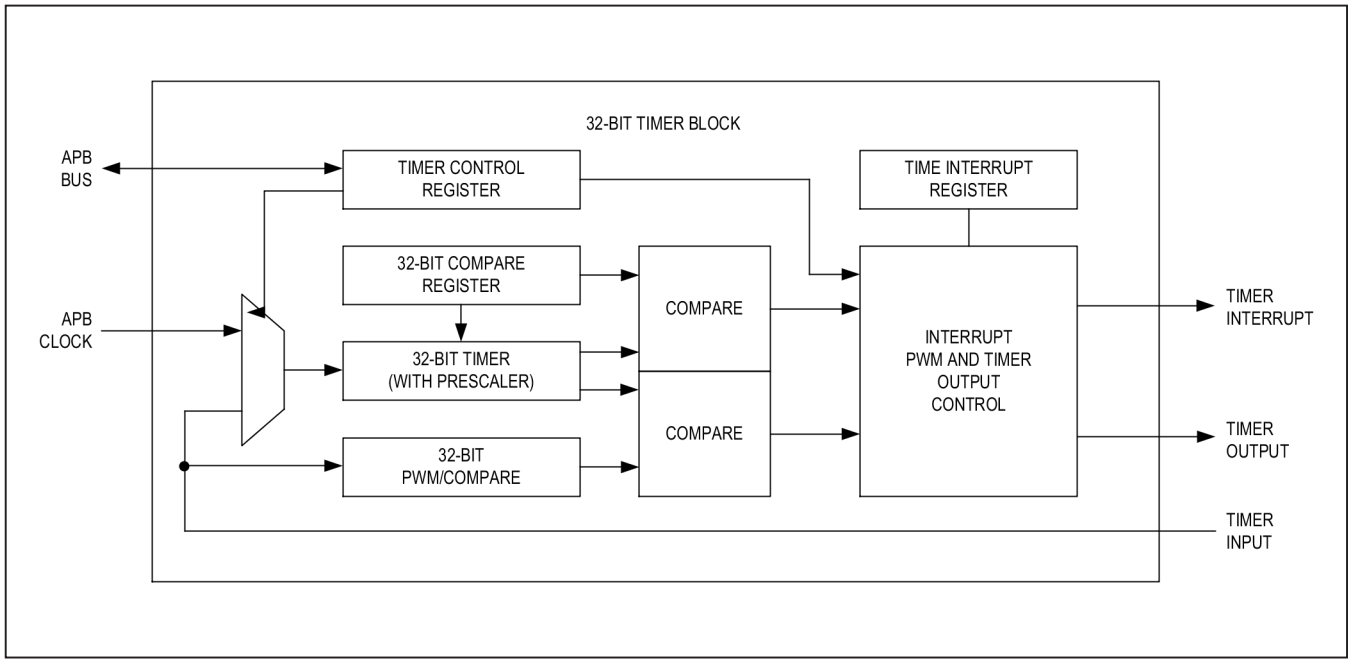


Figure 3. 32-Bit Timer

I2C Master and Slave

The I2C interface is a bidirectional, two-wire serial bus that provides a medium-speed communications network. It can operate as a one-to-one, one-to-many, or many-to-many communications medium.

Two I2C interfaces allow combinations of up to two I2C master engines and/or one I2C-selectable slave engine to connect to a wide variety of I2C-compatible peripherals. These engines support both standard-mode and fast-mode I2C standards. The slave engine shares the same I/O port as the master engines and is selected through the I/O configuration settings. It provides the following features:

- Master or slave mode operation
- Supports standard (7-bit) addressing or 10-bit addressing
- Support for clock stretching to allow slower slave devices to operate on higher speed busses
- Multiple transfer rates
  - Standard mode: 100KBps
  - Fast mode: 400KBps
- Internal filter to reject noise spikes
- Receiver FIFO depth of 16 bytes
- Transmitter FIFO depth of 16 bytes

SPI (Master)

The SPI master-mode-only (SPIM) interface operates independently in a single or multiple slave system and is fully accessible to the user application.

The SPI ports provide a highly configurable, flexible, and efficient interface to communicate with a wide variety of SPI slave devices. The three SPI master ports (SPI0, SPI1, SPI2) support the following features:

- Supports all four SPI modes (0, 1, 2, 3) for single-bit communication
- High-speed AHB access to transmit and receive using 32-byte Rx FIFO and 16-byte Tx FIFO
- 3- or 4-wire mode for single-bit slave device communication
- Full-duplex operation in single-bit, 4-wire mode
- Dual and quad I/O supported
- Up to 5 slave select lines per port
- Up to 2 slave ready lines
- Programmable interface timing
- Programmable SCK frequency and duty cycle
- Programmable SCK alternate timing
- SS assertion and deassertion timing with respect to leading/trailing SCK edge

SPI (Slave)

The SPI slave (SPIS) port provides a highly configurable, flexible, and efficient interface to communicate with a wide variety of SPI master devices. The SPI slave interface provides the following features:

- Supports SPI modes 0 and 3
- Full-duplex operation in single-bit, 4-wire mode
- Slave select polarity fixed (active low)
- Dual and quad I/O supported
- High-speed AHB access to transmit and receive using 32-byte FIFOs
- Four interrupts to monitor FIFO levels

SPI (Execute in Place (SPIX) Master)

The SPI execute in place (SPIX) master allows the CPU to transparently execute instructions stored in an external SPI flash. Instructions fetched through the SPIX master are cached just like instructions fetched from internal program memory. The SPIX master can also be used to access large amounts of external static data that would otherwise reside in internal data memory.

UART

All three universal asynchronous receiver-transmitter (UART) interfaces support full-duplex asynchronous communication with optional hardware flow control (HFC) modes to prevent data overruns. If HFC mode is enabled on a given port, the system uses two extra pins to implement the industry standard request to send (RTS) and clear to send (CTS) methodology. Each UART is individually programmable.

- 2-wire interface or 4-wire interface with flow control
- 32-byte send/receive FIFO
- Full-duplex operation for asynchronous data transfers
- Programmable interrupt for receive and transmit
- Independent baud-rate generator
- Programmable 9th bit supports even/odd parity or multi-drop mode
- User-selectable UART slave address
- Start/stop bit support
- Hardware flow control using RTS/CTS
- Maximum baud rate: 1843.2KB

1-Wire Master

Maxim's DeepCover® 1-Wire security solutions provide a cost-effective solution to authenticate medical sensors and peripherals, preventing counterfeit products. The integrated 1-Wire master communicates with slave devices through the bidirectional, multidrop 1-Wire bus. All of the devices on the 1-Wire bus share one signal that carries data communication and also supplies power to the slave devices. The single contact serial interface is ideal for communication networks requiring minimal interconnect. Features of the 1-Wire bus include:

- Single contact for control and operation
- Unique factory identifier for any 1-Wire device
- Power is distributed to all slave device (parasitic power)
- Multiple device capability on a single line
- Supports 1-Wire standard (15.6KBps) and overdrive (110KBps) speeds

The incorporation of the 1-Wire master enables the creation of 1-Wire enhanced consumable and reusable accessories. The following benefits can be added to products by the addition of only one contact:

- OEM authenticity is verifiable with SHA-256 and ECDSA
- External tracking is eliminated because calibration data can be securely stored within an accessory
- Reuse of single-use accessories can be prevented
- Counterfeit products can be identified and use denied using the unique, factory identifier
- Environmental temperature and humidity sensing

Peripheral Management Unit (PMU)

The PMU is a DMA-based link list processing engine that performs operations and data transfers involving memory and/or peripherals in the advanced peripheral bus (APB) and advanced high-performance bus (AHB) peripheral memory space while the main CPU is in a sleep state. This allows low-overhead peripheral operations to be performed without the CPU, significantly reducing overall power consumption. Using the PMU with the CPU in a sleep state provides a lower-noise environment critical for obtaining optimum ADC performance.

Key features of the PMU engine include:

- Six independent channels with round-robin scheduling allows for multiple parallel operations
- Programmed using PMU opcodes stored in SRAM
- PMU action can be initiated from interrupt conditions from peripherals without CPU
- Integrated AHB bus master
- Coprocessor-like state machine

Additional Documentation

Engineers must have the following documents to fully use this device:

- This data sheet, containing pin descriptions, feature overviews, and electrical specifications
- The device-appropriate user guide, containing detailed information and programming guidelines for core features and peripherals
- Errata sheets for specific revisions noting deviations from published specifications

Development and Technical Support

Contact technical support for information about highly versatile, affordable development tools, available from Maxim Integrated and third-party vendors.

- Evaluation kits
- Software development kit
- Compilers
- Integrated development environments (IDEs)
- USB interface modules for programming and debugging

Trust Protection Unit (TPU) (MAX32626 Only)

The TPU enhances cryptographic data security for valuable intellectual property (IP) and data. High-speed, hardware-based cryptographic accelerators perform mathematical computations that support cryptographic algorithms, including:

- AES-128
- AES-192
- AES-256
- 1024-bit DSA
- 2048-bit (CRT)

The device provides a true random number generator (TRNG) that can be used to create cryptographic keys for any application. A user-selectable entropy source further increases the randomness and key strength.

The secure bootloader protects against unauthorized access to program memory.

DeepCover is a registered trademark of Maxim Integrated Products, Inc.

Applications Information

General-Purpose I/O Matrix

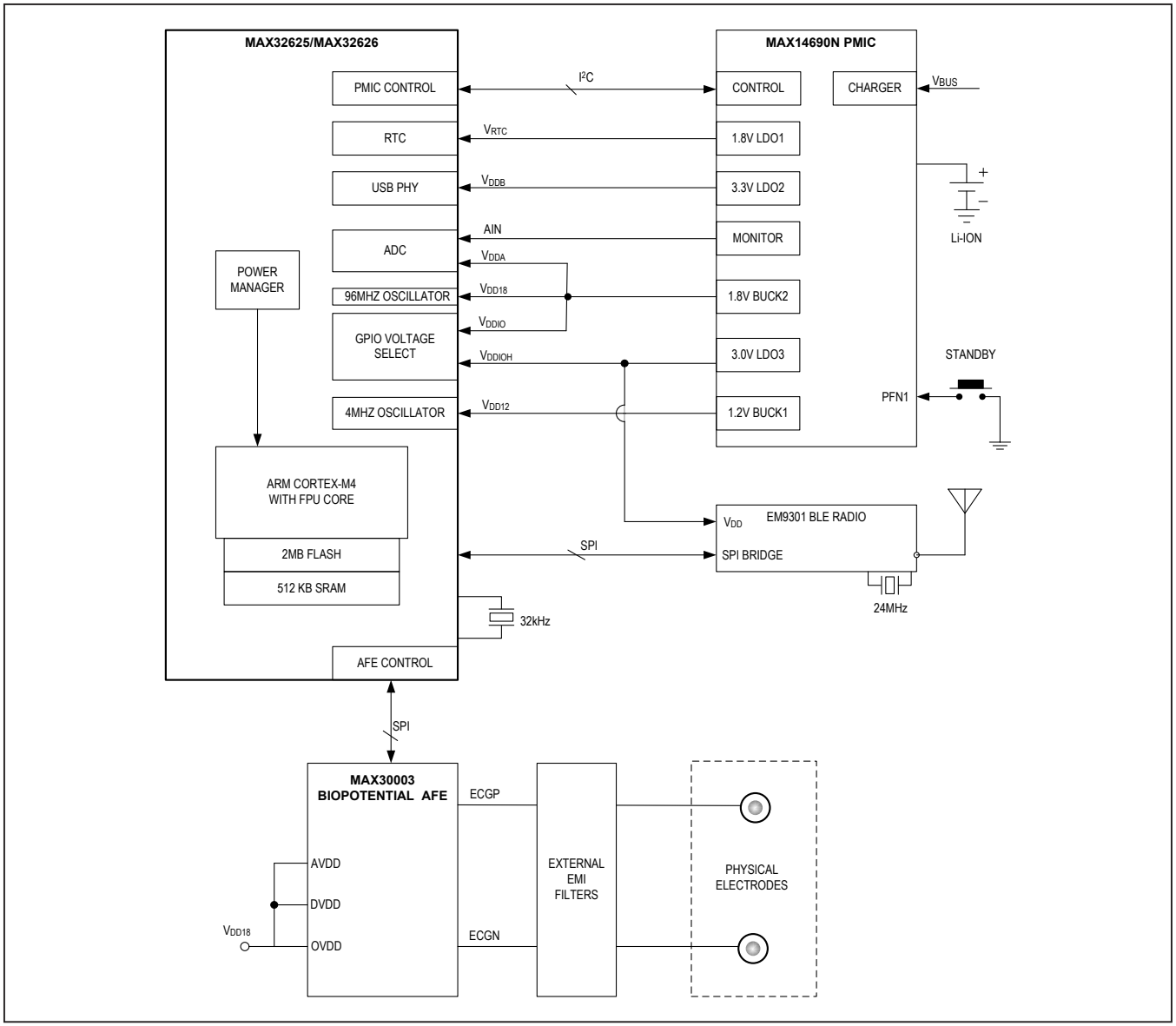
Table 1. General-Purpose I/O Matrix

GPIO	PRIMARY FUNCTION	SECONDARY FUNCTION	PULSE TRAIN OUTPUT	TIMER INPUT	GPIO INTERRUPT
P0.0	UART0A_RX	UART0B_TX	PT_PT0	TIMER_TMR0	GPIO_INT(P0)
P0.1	UART0A_TX	UART0B_RX	PT_PT1	TIMER_TMR1	GPIO_INT(P0)
P0.2	UART0A_CTS	UART0B_RTS	PT_PT2	TIMER_TMR2	GPIO_INT(P0)
P0.3	UART0A_RTS	UART0B_CTS	PT_PT3	TIMER_TMR3	GPIO_INT(P0)
P0.4	SPIM0A_SCK		PT_PT4	TIMER_TMR4	GPIO_INT(P0)
P0.5	SPIM0A_MOSI/SDIO0		PT_PT5	TIMER_TMR5	GPIO_INT(P0)
P0.6	SPIM0A_MISO/SDIO1		PT_PT6	TIMER_TMR0	GPIO_INT(P0)
P0.7	SPIM0A_SS0		PT_PT7	TIMER_TMR1	GPIO_INT(P0)
P1.0	SPIM1A_SCK	SPIX0A_SCK	PT_PT8	TIMER_TMR2	GPIO_INT(P1)
P1.1	SPIM1A_MOSI/SDIO0	SPIX0A_SDIO0	PT_PT9	TIMER_TMR3	GPIO_INT(P1)
P1.2	SPIM1A_MISO/SDIO1	SPIX0A_SDIO1	PT_PT10	TIMER_TMR4	GPIO_INT(P1)
P1.3	SPIM1A_SS0	SPIX0A_SS0	PT_PT11	TIMER_TMR5	GPIO_INT(P1)
P1.4	SPIM1A_SDIO2	SPIX0A_SDIO2	PT_PT12	TIMER_TMR0	GPIO_INT(P1)
P1.5	SPIM1A_SDIO3	SPIX0A_SDIO3	PT_PT13	TIMER_TMR1	GPIO_INT(P1)
P1.6	I2CM0A_SDA / I2CS0A_SDA		PT_PT14	TIMER_TMR2	GPIO_INT(P1)
P1.7	I2CM0A_SCL / I2CS0A_SCL		PT_PT15	TIMER_TMR3	GPIO_INT(P1)
P2.0	UART1A_RX	UART1B_TX	PT_PT0	TIMER_TMR4	GPIO_INT(P2)
P2.1	UART1A_TX	UART1B_RX	PT_PT1	TIMER_TMR5	GPIO_INT(P2)
P2.2	UART1A_CTS	UART1B_RTS	PT_PT2	TIMER_TMR0	GPIO_INT(P2)
P2.3	UART1A_RTS	UART1B_CTS	PT_PT3	TIMER_TMR1	GPIO_INT(P2)
P2.4	SPIM2A_SCK		PT_PT4	TIMER_TMR2	GPIO_INT(P2)
P2.5	SPIM2A_MOSI/SDIO0		PT_PT5	TIMER_TMR3	GPIO_INT(P2)
P2.6	SPIM2A_MISO/SDIO1		PT_PT6	TIMER_TMR4	GPIO_INT(P2)
P2.7	SPIM2A_SS0		PT_PT7	TIMER_TMR5	GPIO_INT(P2)
P3.0	UART2A_RX	UART2B_TX	PT_PT8	TIMER_TMR0	GPIO_INT(P3)
P3.1	UART2A_TX	UART2B_RX	PT_PT9	TIMER_TMR1	GPIO_INT(P3)
P3.2	UART2A_CTS	UART2B_RTS	PT_PT10	TIMER_TMR2	GPIO_INT(P3)
P3.3	UART2A_RTS	UART2B_CTS	PT_PT11	TIMER_TMR3	GPIO_INT(P3)
P3.4	I2CM1A_SDA / I2CS0B_SDA	SPIM2A_SS1	PT_PT12	TIMER_TMR4	GPIO_INT(P3)
P3.5	I2CM1A_SCL / I2CS0B_SCL	SPIM2A_SS2	PT_PT13	TIMER_TMR5	GPIO_INT(P3)
P3.6	SPIM1A_SS1	SPIX_SS1	PT_PT14	TIMER_TMR0	GPIO_INT(P3)
P3.7	SPIM1A_SS2	SPIX_SS2	PT_PT15	TIMER_TMR1	GPIO_INT(P3)
P4.0	OWM_I/O	SPIM2A_SR0	PT_PT0	TIMER_TMR2	GPIO_INT(P4)
P4.1	OWM_PUPEN	SPIM2A_SR1	PT_PT1	TIMER_TMR3	GPIO_INT(P4)
P4.2	SPIM0A_SDIO2	SPIS0A_SDIO2	PT_PT2	TIMER_TMR4	GPIO_INT(P4)

Table 1. General-Purpose I/O Matrix (continued)

GPIO	PRIMARY FUNCTION	SECONDARY FUNCTION	PULSE TRAIN OUTPUT	TIMER INPUT	GPIO INTERRUPT
P4.3	SPIM0A_SDIO3	SPIS0A_SDIO3	PT_PT3	TIMER_TMR5	GPIO_INT(P4)
P4.4	SPIM0A_SS1	SPIS0A_SCLK	PT_PT4	TIMER_TMR0	GPIO_INT(P4)
P4.5	SPIM0A_SS2	SPIS0A_MOSI/SDIO0	PT_PT5	TIMER_TMR1	GPIO_INT(P4)
P4.6	SPIM0A_SS3	SPIS0A_MISO/SDIO1	PT_PT6	TIMER_TMR2	GPIO_INT(P4)
P4.7	SPIM0A_SS4	SPIS0A_SS0	PT_PT7	TIMER_TMR3	GPIO_INT(P4)

Typical Application Circuit



Ordering Information

PART	FLASH (KB)	SRAM (KB)	TRUST PROTECTION UNIT (TPU)	PIN-PACKAGE
MAX32625IWY+	512	160	No	63 WLP
MAX32625IWY+T	512	160	No	63 WLP
MAX32625ITK+	512	160	No	68 TQFN-EP
MAX32625ITK+T	512	160	No	68 TQFN-EP
MAX32625IWYL+	256	128	No	63 WLP
MAX32625IWYL+T	256	128	No	63 WLP
MAX32625ITKL+	256	128	No	68 TQFN-EP
MAX32625ITKL+T	256	128	No	68 TQFN-EP
MAX32626IWY+	512	160	Yes	63 WLP
MAX32626IWY+T	512	160	Yes	63 WLP
MAX32626ITK+	512	160	Yes	68 TQFN-EP
MAX32626ITK+T	512	160	Yes	68 TQFN-EP
MAX32626ITKBL+	512	160	Yes (includes secure boot)	68 TQFN-EP
MAX32626ITKBL+T	512	160	Yes (includes secure boot)	68 TQFN-EP
MAX32626IWYBL+*	512	160	Yes (includes secure boot)	63 WLP
MAX32626IWYBL+T*	512	160	Yes (includes secure boot)	63 WLP

+Denotes a lead(Pb)-free/RoHS-compliant package.
T = Tape and reel.
**Future product—contact factory for availability.*

Revision History

REVISION NUMBER	REVISION DATE	DESCRIPTION	PAGES CHANGED
0	8/16	Initial release	—
1	6/17	Corrected ARM trademarks, clarified 1-Wire master functions are listed in GPIO matrix table, added *Typical Application Circuit* diagram, corrected *Figure 1*. SPI Master and SPI XIP Master Timing, explained V_{RTC} supply supports SRAM retention in LP0, corrected pin 46 from V_{DDIO} to V_{DDIOH} on 68 TQFN-EP *Pin Configuration* drawing to match *Pin Description* table (no change to fit or function), added EP to *Pin Description*, changed PRNG to TRNG	1, 15, 16, 19, 24, 26
2	8/17	Updated *Simplified Block Diagram*, removed future product references	4, 27
3	10/17	Removed future product references	27
4	3/18	Updated *General Description*, updated Arm trademarks, corrected TQFN instances to TQFN-EP	1–28
4.1		Corrected typo in *General Description*	1
5	10/18	Updated title, *General Description*, *Benefits and Features*, *Additional Documentation*, *Development and Technical Support*, and *Trust Protection Unit (TPU) (MAX32626 Only)* sections	1–28
6	2/20	Updated *Simplified Block Diagram* and *Ordering Information*	4, 27

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