Reinforced, Ultra-Low-Power, Two-Channel Digital Isolators

MAX22420, MAX22421
MAX22820, MAX22821

Product Highlights

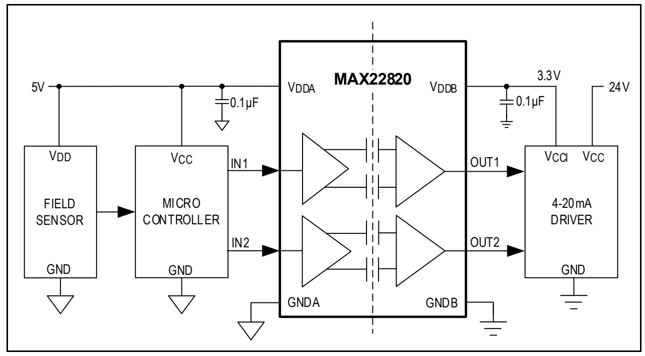
- Ultra-Low Power Consumption
  - 11.4µA per Channel at DC with VDD = 3.3V
  - 15.4µA per Channel at 100kbps with VDD = 3.3V
  - 54.7µA per Channel at 1Mbps with V_{DD} = 3.3V
- Wide Supply Range Supports from 1.71V to 5.5V
- Reinforced Galvanic Isolation for Digital Signals
  - 8-NSOIC with 4mm Creepage and Clearance Withstands 3kVRMS for 60s (VISO) and Continuously Withstands 445VRMS (VIOWM)
  - 8-WSOIC with 8mm Creepage and Clearance Withstands 5kVRMS for 60s (VISO) and Continuously Withstands 848VRMS (VIOWM)
  - Withstands ±10kV Surge Between GNDA and GNDB with 1.2/50µs Waveform
  - High CMTI (200kV/µs, min)
- Low Propagation Delay and Low Jitter
  - Maximum Data Rate Up to 10Mbps
  - Low Propagation Delay 51ns (typ) at VDD = 3.3V
  - Clock Jitter RMS 15.4ps (typ)
- Safety Regulatory Approvals
  - UL According to UL1577
  - cUL According to CSA Bulletin 5A
  - VDE 0884-11 Reinforced Insulation (Pending)
  - IECEx and ATEX Intrinsic Safety (IS): Sira 0518 II 1G Ex ia IIC Ga (Pending)

Key Applications

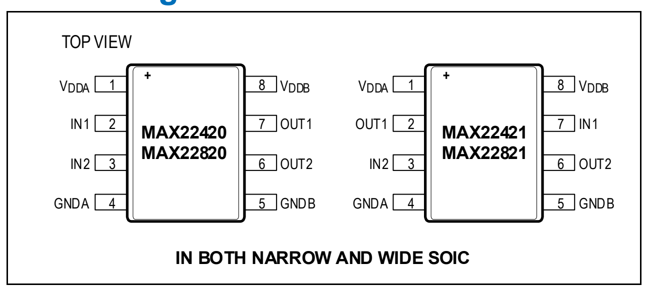
- 4-20mA Loop Process Control
- Battery Management
- Compact Micro PLC
- Parasitically Powered Applications

The MAX22420/1, MAX22820/1 are a family of 2-channel, reinforced, ultra-low-power digital galvanic isolators using Analog Devices' proprietary process technology. The MAX22420/1 feature reinforced isolation with a withstand voltage rating of $3kV_{RMS}$ for 60 seconds. The MAX22820/1 feature reinforced isolation with a withstand voltage rating of $5kV_{RMS}$ for 60 seconds. Devices are rated for operation at ambient temperature from -40°C to +125°C.

Simplified Application Diagram



Pin Configurations



These devices transfer digital signals between circuits with different power domains, using as little as 90.7µW per channel at 1Mbps (1.8V supply). The ultra-low-power feature reduces system dissipation, increases reliability, and enables compact designs.

Devices are available with a glitch rejection filter of either 29ns or 70ns (typ) and with default-high or default-low outputs. The devices feature low propagation delay and low clock jitter, which reduces system latency.

Independent 1.71V to 5.5V supplies on each side also make the devices suitable for use as level translators.

The MAX22420/MAX22820 feature two channels transferring data in the same direction. The two channels of the MAX22421/MAX22821 transfer data in opposite directions.

***Ordering Information* appears at end of data sheet.**

19-101281; Rev 3; 11/23

Absolute Maximum Ratings

V_{DDA} to GNDA .... -0.3V to +6V

V_{DDB} to GNDB .... -0.3V to +6V

IN_ on Side A to GNDA .... -0.3V to +6V

IN_ on Side B to GNDB .... -0.3V to +6V

OUT_ on Side A to GNDA ....-0.3V to (V_{DDA} + 0.3)V

OUT_ on Side B to GNDB ....-0.3V to (V_{DDB} + 0.3)V

Short-Circuit Continuous Current

OUT_ on Side A to GNDA .... ±30mA

OUT_ on Side B to GNDB .... ±30mA

Continuous Power Dissipation (T_A = +70°C)

Narrow SOIC (derate 5.79mW/°C above +70°C) 462.96mW

Wide SOIC (derate 11.35mW/°C above +70°C) . 908.06mW

Temperature Ratings

Operating Temperature Range.................. -40°C to +125°C

Maximum Junction Temperature ....+150°C

Storage Temperature Range..................... -60°C to +150°C

Lead Temperature (soldering, 10s) ....+300°C

Soldering Temperature (reflow)................................+260°C

Stresses beyond those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Package Information

8 Narrow SOIC

Package Code	S8MS+24
Outline Number	21-0041
Land Pattern Number	90-0096
Thermal Resistance, Four Layer Board:	
Junction-to-Ambient (θ_{JA})	172.80ºC/W
Junction-to-Case Thermal Resistance (θ_{JC})	67.60ºC/W

8 Wide SOIC

Package Code	W8MS+7
Outline Number	21-100415
Land Pattern Number	90-100146
Thermal Resistance, Four Layer Board:	
Junction-to-Ambient (θ_{JA})	88.10ºC/W
Junction-to-Case Thermal Resistance (θ_{JC})	42.40ºC/W

Package thermal resistances were obtained using the method described in JEDEC specification JESD51-7, using a four-layer board. For detailed information on package thermal considerations, refer to www.maximintegrated.com/thermal-tutorial.

For the latest package outline information and land patterns (footprints), go to www.maximintegrated.com/packages. Note that a “+”, “#”, or “-” in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

DC Electrical Characteristics

(V_{DDA} - V_{GNDA} = 1.71V to 5.5V, V_{DDB} - V_{GNDB} = 1.71V to 5.5V, C_L = 15pF, T_A = -40°C to +125°C, unless otherwise noted. Typical values are at V_{DDA} - V_{GNDA} = 3.3V, V_{DDB} - V_{GNDB} = 3.3V, V_{GNDA} = V_{GNDB}, T_A = +25°C, unless otherwise noted.) (Notes 1, 3)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
SUPPLY VOLTAGE							
Supply Voltage	V_{DDA}	Relative to GNDA		1.71		5.5	V
	V_{DDB}	Relative to GNDB		1.71		5.5	
Undervoltage-Lockout Threshold	$V_{UVLO\_}$	$V_{DD\_}$ rising		1.5	1.59	1.69	V
Undervoltage-Lockout Threshold Hysteresis	V_{UVLO_HYST}				30		mV
MAX22420, MAX22820 SUPPLY CURRENT (Note 2)							
Side A Supply Current	I_{DDA}	DC, C_L = 0pF	V_{DDA} = 5V		6.9	21.6	µA
			V_{DDA} = 3.3V		6.7	20.8	
			V_{DDA} = 2.5V		6.6	20.6	
			V_{DDA} = 1.8V		6.6	20.0	
		5kHz square wave, C_L = 0pF	V_{DDA} = 5V		7.6	21.6	
			V_{DDA} = 3.3V		7.4	21.8	
			V_{DDA} = 2.5V		7.3	20.6	
			V_{DDA} = 1.8V		6.6	20.0	
		50kHz square wave, C_L = 0pF	V_{DDA} = 5V		13.4	31.5	
			V_{DDA} = 3.3V		12.9	30.3	
			V_{DDA} = 2.5V		12.7	29.9	
			V_{DDA} = 1.8V		12.5	29.0	
		500kHz square wave, C_L = 0pF	V_{DDA} = 5V		75.1	129.5	
			V_{DDA} = 3.3V		72.1	126.1	
			V_{DDA} = 2.5V		70.6	124.1	
			V_{DDA} = 1.8V		70.3	117.3	
Side B Supply Current	I_{DDB}	DC, C_L = 0pF	V_{DDB} = 5V		16.1	31.4	µA
			V_{DDB} = 3.3V		16.0	30.6	
			V_{DDB} = 2.5V		15.9	30.3	
			V_{DDB} = 1.8V		15.9	29.7	
		5kHz square wave, C_L = 0pF	V_{DDB} = 5V		16.4	31.6	
			V_{DDB} = 3.3V		16.2	30.7	
			V_{DDB} = 2.5V		16.1	30.4	
			V_{DDB} = 1.8V		15.9	29.8	
		50kHz square wave, C_L = 0pF	V_{DDB} = 5V		18.9	34.7	
			V_{DDB} = 3.3V		17.9	32.9	
			V_{DDB} = 2.5V		17.6	32.3	
			V_{DDB} = 1.8V		17.3	31.3	
		500kHz square wave, C_L = 0pF	V_{DDB} = 5V		44.7	65.5	
			V_{DDB} = 3.3V		37.2	56.4	

(V_{DDA} - V_{GNDA} = 1.71V to 5.5V, V_{DDB} - V_{GNDB} = 1.71V to 5.5V, C_L = 15pF, T_A = -40°C to +125°C, unless otherwise noted. Typical values are at V_{DDA} - V_{GNDA} = 3.3V, V_{DDB} - V_{GNDB} = 3.3V, V_{GNDA} = V_{GNDB}, T_A = +25°C, unless otherwise noted.) (Notes 1, 3)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
			V_{DDB} = 2.5V		33.9	52.3	
			V_{DDB} = 1.8V		30.5	46.8	
MAX22421, MAX22821 SUPPLY CURRENT (Note 2)							
Side A Supply Current	I_{DDA}	DC, C_L = 0pF	V_{DDA} = 5V		11.4	26.5	µA
			V_{DDA} = 3.3V		11.3	25.7	
			V_{DDA} = 2.5V		11.2	25.4	
			V_{DDA} = 1.8V		11.1	24.9	
		5kHz square wave, C_L = 0pF	V_{DDA} = 5V		12.0	26.6	
			V_{DDA} = 3.3V		11.8	25.8	
			V_{DDA} = 2.5V		11.7	25.5	
			V_{DDA} = 1.8V		11.3	24.9	
		50kHz square wave, C_L = 0pF	V_{DDA} = 5V		16.1	33.1	
			V_{DDA} = 3.3V		15.4	31.6	
			V_{DDA} = 2.5V		15.1	31.1	
			V_{DDA} = 1.8V		14.9	30.1	
		500kHz square wave, C_L = 0pF	V_{DDA} = 5V		60.1	97.2	
			V_{DDA} = 3.3V		55.3	91.1	
			V_{DDA} = 2.5V		53.0	88.1	
			V_{DDA} = 1.8V		50.4	81.9	
Side B Supply Current	I_{DDB}	DC, C_L = 0pF	V_{DDB} = 5V		11.4	26.5	µA
			V_{DDB} = 3.3V		11.3	25.7	
			V_{DDB} = 2.5V		11.2	25.4	
			V_{DDB} = 1.8V		11.1	24.9	
		5kHz square wave, C_L = 0pF	V_{DDB} = 5V		12.0	26.6	
			V_{DDB} = 3.3V		11.8	25.8	
			V_{DDB} = 2.5V		11.7	25.5	
			V_{DDB} = 1.8V		11.3	24.9	
		50kHz square wave, C_L = 0pF	V_{DDB} = 5V		16.1	33.1	
			V_{DDB} = 3.3V		15.4	31.6	
			V_{DDB} = 2.5V		15.1	31.1	
			V_{DDB} = 1.8V		14.9	30.1	
		500kHz square wave, C_L = 0pF	V_{DDB} = 5V		60.1	97.2	
			V_{DDB} = 3.3V		55.3	91.1	
			V_{DDB} = 2.5V		53.0	88.1	
			V_{DDB} = 1.8V		50.4	81.9	
LOGIC INTERFACE (IN_, OUT_)							
Input High Voltage	V_{IH}	2.25V ≤ $V_{DD\_}$ ≤ 5.5V		0.7 x $V_{DD\_}$			V

(V_{DDA} - V_{GNDA} = 1.71V to 5.5V, V_{DDB} - V_{GNDB} = 1.71V to 5.5V, C_L = 15pF, T_A = -40°C to +125°C, unless otherwise noted. Typical values are at V_{DDA} - V_{GNDA} = 3.3V, V_{DDB} - V_{GNDB} = 3.3V, V_{GNDA} = V_{GNDB}, T_A = +25°C, unless otherwise noted.) (Notes 1, 3)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
		1.71V ≤ $V_{DD\_}$ < 2.25V		0.76 x $V_{DD\_}$			
Input Low Voltage	V_{IL}	2.25V ≤ $V_{DD\_}$ ≤ 5.5V				0.8	V
		1.71V ≤ $V_{DD\_}$ < 2.25V				0.7	
Input Hysteresis	V_{HYS}				410		mV
Input Leakage Current	I_{LEAK}			-1		+1	µA
Input Capacitance	C_{IN}	f_{SW} = 1MHz			2		pF
Output Voltage High	V_{OH}	I_{OUT} = -4mA source	4.5V ≤ $V_{DD\_}$ ≤ 5.5V	$V_{DD\_}$ - 0.4			V
		I_{OUT} = -2mA source	3.0V ≤ $V_{DD\_}$ ≤ 3.6V	$V_{DD\_}$ - 0.3			
		I_{OUT} = -1mA source	2.25V ≤ $V_{DD\_}$ ≤ 2.75V	$V_{DD\_}$ - 0.2			
			1.71V ≤ $V_{DD\_}$ ≤ 1.89V	$V_{DD\_}$ - 0.2			
Output Voltage Low	V_{OL}	I_{OUT} = 4mA sink	4.5V ≤ $V_{DD\_}$ ≤ 5.5V			0.4	V
		I_{OUT} = 2mA sink	3.0V ≤ $V_{DD\_}$ ≤ 3.6V			0.3	
		I_{OUT} = 1mA sink	2.25V ≤ $V_{DD\_}$ ≤ 2.75V			0.2	
			1.71V ≤ $V_{DD\_}$ ≤ 1.89V			0.2	

Dynamic Characteristics—MAX22_2_C/F

(V_{DDA} - V_{GNDA} = 1.71V to 5.5V, V_{DDB} - V_{GNDB} = 1.71V to 5.5V, C_L = 15pF, T_A = -40°C to +125°C, unless otherwise noted. Typical values are at V_{DDA} - V_{GNDA} = 3.3V, V_{DDB} - V_{GNDB} = 3.3V, V_{GNDA} = V_{GNDB}, T_A = +25°C, unless otherwise noted.) (Notes 2, 4)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Common-Mode Transient Immunity	CMTI	(Note 5)		200			kV/µs
Maximum Data Rate	DR_{MAX}			10			Mbps
Minimum Pulse Width	PW_{MIN}					100	ns
Glitch Rejection				24	29	37	ns
Propagation Delay (Figure 1)	t_{PLH}	IN_ to OUT_, C_L = 15pF	4.5V ≤ $V_{DD\_}$ ≤ 5.5V	45	51	61	ns
			3.0V ≤ $V_{DD\_}$ ≤ 3.6V	46	52	63	
			2.25V ≤ $V_{DD\_}$ ≤ 2.75V	47	53	65	
			1.71V ≤ $V_{DD\_}$ ≤ 1.89V	50	58	72	
	t_{PHL}	IN_ to OUT_, C_L = 15pF	4.5V ≤ $V_{DD\_}$ ≤ 5.5V	45	50	61	
			3.0V ≤ $V_{DD\_}$ ≤ 3.6V	46	51	63	
			2.25V ≤ $V_{DD\_}$ ≤ 2.75V	47	52	65	
			1.71V ≤ $V_{DD\_}$ ≤ 1.89V	50	56	72	
Pulse Width Distortion	PWD	$\|t_{PLH} - t_{PHL}\|$	4.5V ≤ $V_{DD\_}$ ≤ 5.5V			6	ns
			3.0V ≤ $V_{DD\_}$ ≤ 3.6V			6	
			2.25V ≤ $V_{DD\_}$ ≤ 2.75V			6	
			1.71V ≤ $V_{DD\_}$ ≤ 1.89V			6.5	
Propagation Delay Skew Part-to-Part (Same Channel)	t_{SPLH}	4.5V ≤ $V_{DD\_}$ ≤ 5.5V				16	ns
		3.0V ≤ $V_{DD\_}$ ≤ 3.6V				17	
		2.25V ≤ $V_{DD\_}$ ≤ 2.75V				18	
		1.71V ≤ $V_{DD\_}$ ≤ 1.89V				22	
	t_{SPHL}	4.5V ≤ $V_{DD\_}$ ≤ 5.5V				16	
		3.0V ≤ $V_{DD\_}$ ≤ 3.6V				17	
		2.25V ≤ $V_{DD\_}$ ≤ 2.75V				18	
		1.71V ≤ $V_{DD\_}$ ≤ 1.89V				22	
Propagation Delay Skew Channel-to-Channel (Same Direction) (Figure 1)	t_{SCSLH}	1.71V ≤ $V_{DD\_}$ ≤ 5.5V				6	ns
	t_{SCSHL}	1.71V ≤ $V_{DD\_}$ ≤ 5.5V				6	
Propagation Delay Skew Channel-to-Channel (Opposite Direction)	t_{SCOLH}	1.71V ≤ $V_{DD\_}$ ≤ 5.5V				6	ns
	t_{SCOHL}	1.71V ≤ $V_{DD\_}$ ≤ 5.5V				6	
Peak Eye Diagram Jitter	$t_{JIT(PK)}$	1Mbps			130		ps
Clock Jitter RMS	$t_{JCLK(RMS)}$	500kHz clock input, rising/falling edges			15.4		ps

(V_{DDA} - V_{GNDA} = 1.71V to 5.5V, V_{DDB} - V_{GNDB} = 1.71V to 5.5V, C_L = 15pF, T_A = -40°C to +125°C, unless otherwise noted. Typical values are at V_{DDA} - V_{GNDA} = 3.3V, V_{DDB} - V_{GNDB} = 3.3V, V_{GNDA} = V_{GNDB}, T_A = +25°C, unless otherwise noted.) (Notes 2, 4)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Rise Time (Figure 1)	t_R	C_L = 15pF	4.5V ≤ $V_{DD\_}$ ≤ 5.5V			5	ns
			3.0V ≤ $V_{DD\_}$ ≤ 3.6V			5	
			2.25V ≤ $V_{DD\_}$ ≤ 2.75V			5	
			1.71V ≤ $V_{DD\_}$ ≤ 1.89V			8	
Fall Time (Figure 1)	t_F	C_L = 15pF	4.5V ≤ $V_{DD\_}$ ≤ 5.5V			5	ns
			3.0V ≤ $V_{DD\_}$ ≤ 3.6V			5	
			2.25V ≤ $V_{DD\_}$ ≤ 2.75V			5	
			1.71V ≤ $V_{DD\_}$ ≤ 1.89V			8	
Output UVLO to Output Data Valid (Figure 2)	t_{UVLO_EN}	C_L = 15pF, $V_{DD\_}$ rising			1.1	1.7	ms
Input UVLO to Output Default (Figure 2)	t_{UVLO_DE}	C_L = 15pF, $V_{DD\_}$ falling				0.5	ms
Refresh Rate	F_R				10		kHz

Dynamic Characteristics—MAX22_2_B/E

(V_{DDA} - V_{GNDA} = 1.71V to 5.5V, V_{DDB} - V_{GNDB} = 1.71V to 5.5V, C_L = 15pF, T_A = -40°C to +125°C, unless otherwise noted. Typical values are at V_{DDA} - V_{GNDA} = 3.3V, V_{DDB} - V_{GNDB} = 3.3V, V_{GNDA} = V_{GNDB}, T_A = +25°C, unless otherwise noted.) (Notes 2, 4)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Common-Mode Transient Immunity	CMTI	(Note 5)		200			kV/µs
Maximum Data Rate	DR_{MAX}			10			Mbps
Minimum Pulse Width	PW_{MIN}					100	ns
Glitch Rejection				60	70	80	ns
Propagation Delay (Figure 1)	t_{PLH}	IN_ to OUT_, C_L = 15pF	4.5V ≤ $V_{DD\_}$ ≤ 5.5V	109	122	136	ns
			3.0V ≤ $V_{DD\_}$ ≤ 3.6V	110	123	138	
			2.25V ≤ $V_{DD\_}$ ≤ 2.75V	110	124	140	
			1.71V ≤ $V_{DD\_}$ ≤ 1.89V	115	129	145	
	t_{PHL}	IN_ to OUT_, C_L = 15pF	4.5V ≤ $V_{DD\_}$ ≤ 5.5V	109	120	136	
			3.0V ≤ $V_{DD\_}$ ≤ 3.6V	110	121	138	
			2.25V ≤ $V_{DD\_}$ ≤ 2.75V	110	122	140	
			1.71V ≤ $V_{DD\_}$ ≤ 1.89V	115	126	145	
Pulse Width Distortion	PWD	$\|t_{PLH} - t_{PHL}\|$	1.71V ≤ $V_{DD\_}$ ≤ 5.5V			15	ns
	t_{SPLH}	4.5V ≤ $V_{DD\_}$ ≤ 5.5V				27	ns

(V_{DDA} - V_{GNDA} = 1.71V to 5.5V, V_{DDB} - V_{GNDB} = 1.71V to 5.5V, C_L = 15pF, T_A = -40°C to +125°C, unless otherwise noted. Typical values are at V_{DDA} - V_{GNDA} = 3.3V, V_{DDB} - V_{GNDB} = 3.3V, V_{GNDA} = V_{GNDB}, T_A = +25°C, unless otherwise noted.) (Notes 2, 4)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Propagation Delay Skew Part-to-Part (Same Channel)		3.0V ≤ $V_{DD\_}$ ≤ 3.6V			28	
		2.25V ≤ $V_{DD\_}$ ≤ 2.75V			30	
		1.71V ≤ $V_{DD\_}$ ≤ 1.89V			30	
	t_{SPHL}	4.5V ≤ $V_{DD\_}$ ≤ 5.5V			27	
		3.0V ≤ $V_{DD\_}$ ≤ 3.6V			28	
		2.25V ≤ $V_{DD\_}$ ≤ 2.75V			30	
		1.71V ≤ $V_{DD\_}$ ≤ 1.89V			30	
Propagation Delay Skew Channel-to-Channel (Same Direction) (*Figure 1*)	t_{SCSLH}	1.71V ≤ $V_{DD\_}$ ≤ 5.5V			10	ns
	t_{SCSHL}	1.71V ≤ $V_{DD\_}$ ≤ 5.5V			10	
Propagation Delay Skew Channel-to-Channel (Opposite Direction)	t_{SCOLH}	1.71V ≤ $V_{DD\_}$ ≤ 5.5V			10	ns
	t_{SCOHL}	1.71V ≤ $V_{DD\_}$ ≤ 5.5V			10	
Peak Eye Diagram Jitter	$t_{JIT(PK)}$	1Mbps		220		ps
Clock Jitter RMS	$t_{JCLK(RMS)}$	500kHz clock input, rising/falling edges		26.5		ps
Rise Time (*Figure 1*)	t_R	C_L = 15pF, 4.5V ≤ $V_{DD\_}$ ≤ 5.5V			5	ns
		C_L = 15pF, 3.0V ≤ $V_{DD\_}$ ≤ 3.6V			5	
		C_L = 15pF, 2.25V ≤ $V_{DD\_}$ ≤ 2.75V			5	
		C_L = 15pF, 1.71V ≤ $V_{DD\_}$ ≤ 1.89V			8	
Fall Time (*Figure 1*)	t_F	C_L = 15pF, 4.5V ≤ $V_{DD\_}$ ≤ 5.5V			5	ns
		C_L = 15pF, 3.0V ≤ $V_{DD\_}$ ≤ 3.6V			5	
		C_L = 15pF, 2.25V ≤ $V_{DD\_}$ ≤ 2.75V			5	
		C_L = 15pF, 1.71V ≤ $V_{DD\_}$ ≤ 1.89V			8	
Output UVLO to Output Data Valid (*Figure 2*)	t_{UVLO_EN}	C_L = 15pF, $V_{DD\_}$ rising		1.1	1.7	ms
Input UVLO to Output Default (*Figure 2*)	t_{UVLO_DE}	C_L = 15pF, $V_{DD\_}$ falling			0.5	ms
Refresh Rate	F_R			10		kHz

Note 1: All devices are 100% production tested at T_A = +25°C. Specifications over temperature are guaranteed by design and characterization.

Note 2: Not production tested. Guaranteed by design and characterization.

Note 3: All currents into the device are positive. All currents out of the device are negative. All voltages are referenced to their respective ground (GNDA or GNDB), unless otherwise noted.

Note 4: All measurements taken with V_{DDA} = V_{DDB}, unless otherwise noted.

Note 5: CMTI is the maximum sustainable common-mode voltage slew rate while maintaining the correct output. CMTI applies to both rising and falling common-mode voltage edges. Tested with the transient generator connected between GNDA and GNDB (V_{CM} = 1000V).

ESD Protection

PARAMETER	SYMBOL	CONDITIONS	VALUE	UNITS
ESD		Human Body Model, All Pins	±4	kV
		IEC 61000-4-2 Contact, GNDB to GNDA	±6	kV

Safety Regulatory Approvals

UL
The devices are certified under UL1577. For more details, refer to File E351759.
The MAX22420/MAX22421 are rated up to 3000V_{RMS} isolation voltage for single protection.
The MAX22820/MAX22821 are rated up to 5000V_{RMS} isolation voltage for single protection.
cUL (Equivalent to CSA notice 5A)
The MAX22420/MAX22421 are certified up to 3000V_{RMS} for single protection. For more details, refer to File E351759.
The MAX22820/MAX22821 are certified up to 5000V_{RMS} for single protection. For more details, refer to File E351759.
VDE (Pending)
The MAX22420/MAX22421 are certified to DIN VDE V 0884-11: 2017-1. Reinforced Insulation, Maximum Transient Isolation Voltage 4242V_{PK}, Maximum Repetitive Peak Isolation Voltage 630V_{PK}.
The MAX22820/MAX22821 are certified to DIN VDE V 0884-11: 2017-1. Reinforced Insulation, Maximum Transient Isolation Voltage 7070V_{PK}, Maximum Repetitive Peak Isolation Voltage 1200V_{PK}.
CSA/Sira (Pending)
The devices are certified for use in intrinsic safety (IS) to IS applications under ATEX and IECEx.
ATEX: EN 60079-0:2012+A11:2013 and EN 60079-11:2012
IECEx: IEC 60079-0:2011 Edition 6 and IEC 60079-11:2011 Edition 6
II 1G Ex ia IIC Ga

These couplers are suitable for safe electrical insulation only within the safety ratings. Compliance with the safety ratings shall be ensured by means of suitable protective circuits.

Test Circuits and Timing Diagrams

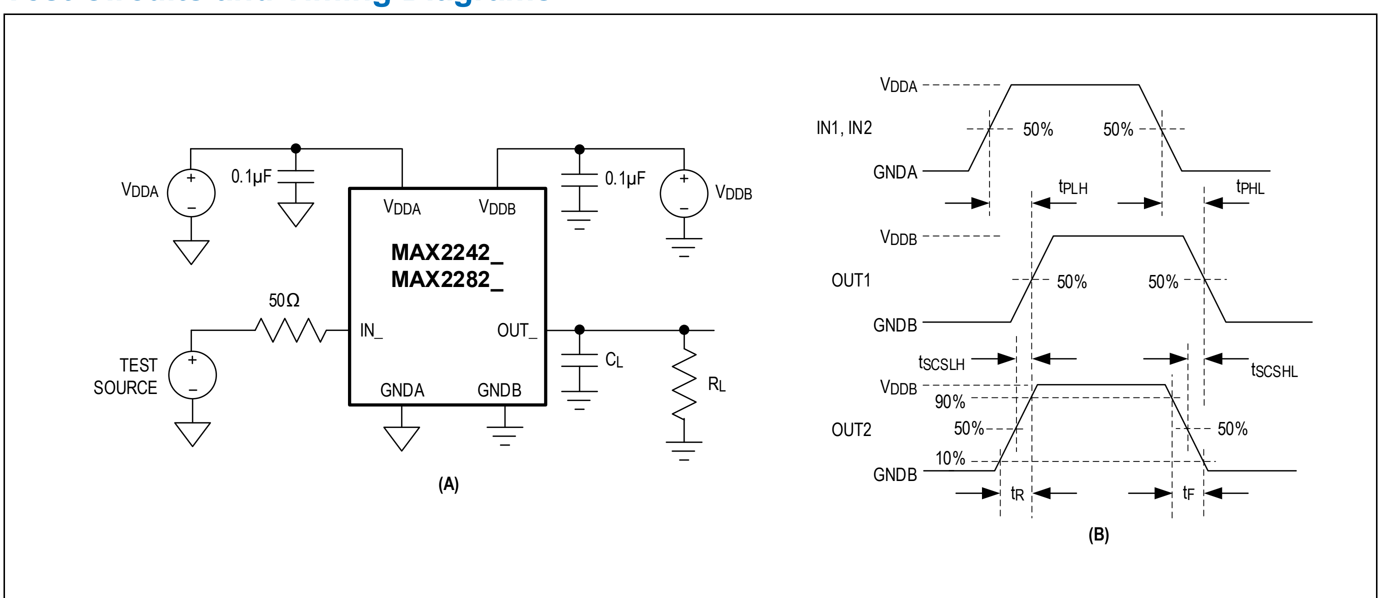


Figure 1. Test Circuit (A) and Timing Diagram (B)

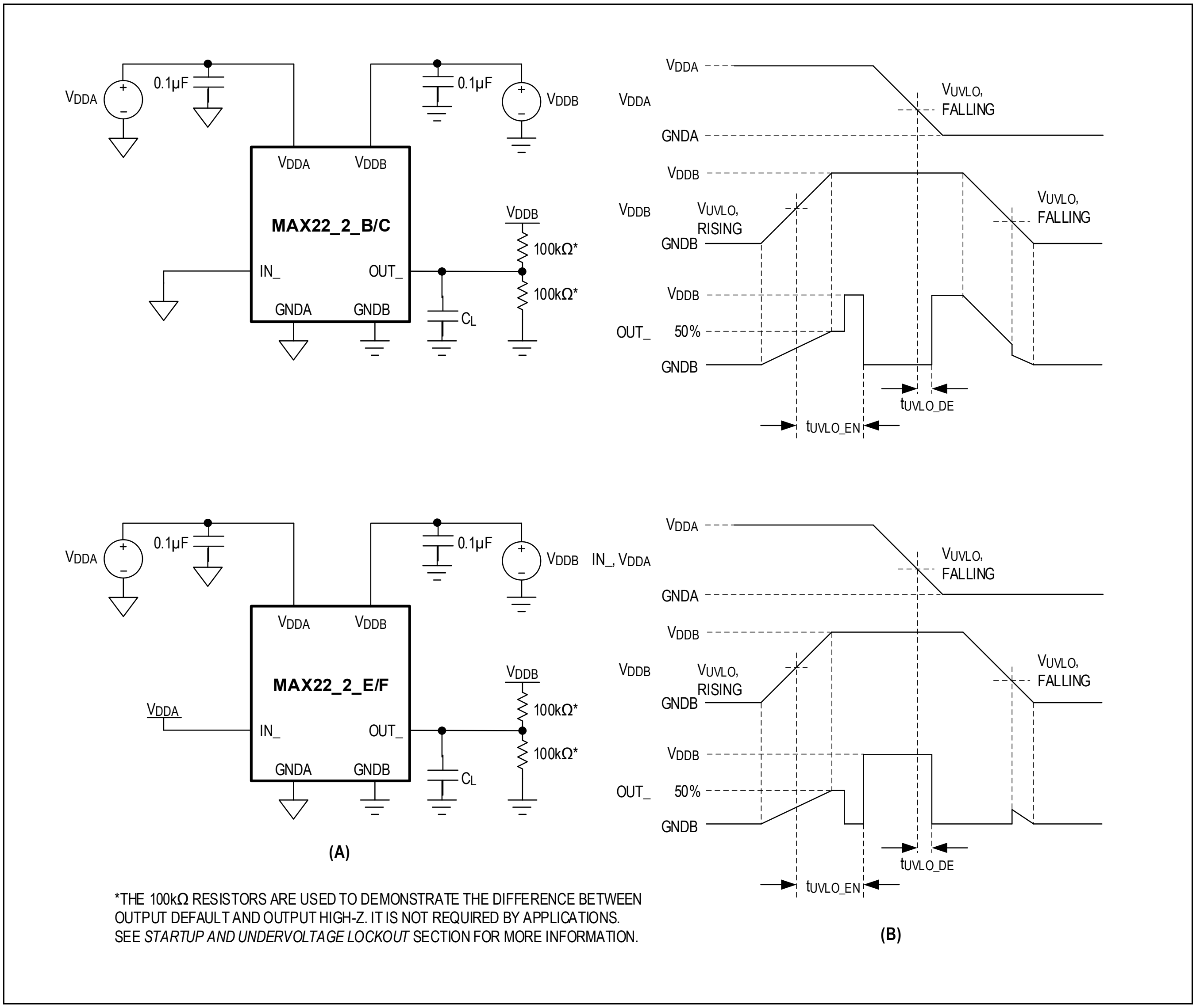


Figure 2. Enable to Output Timing Diagrams (t_{UVLO_EN}, t_{UVLO_DE})

Table 1. Insulation Characteristics (Narrow SOIC)

PARAMETER	SYMBOL	CONDITIONS	VALUE	UNITS
Partial Discharge Test Voltage	V_{PR}	Method B1 = V_{IORM} x 1.875 (t = 1s, partial discharge < 5pC)	1182	V_P
Maximum Repetitive Peak Isolation Voltage	V_{IORM}	(Note 6)	630	V_P
Maximum Working Isolation Voltage	V_{IOWM}	Continuous RMS voltage (Note 6)	445	V_{RMS}
Maximum Transient Isolation Voltage	V_{IOTM}	t = 1s (Note 6)	4242	V_P
Maximum Withstanding Isolation Voltage	V_{ISO}	f_{SW} = 60Hz, duration = 60s (Notes 6, 7)	3000	V_{RMS}
Maximum Surge Isolation Voltage	V_{IOSM}	Reinforced Insulation, test method per IEC 60065, V_{TEST} = 1.6 x V_{IOSM} = 10000V_{PEAK} (Notes 6, 9)	6250	V_P
Isolation Resistance	R_{IO}	V_{IO} = 500V, T_A = 25°C	> 10^{12}	Ω
		V_{IO} = 500V, 100°C ≤ T_A ≤ 125°C	> 10^{11}	
		V_{IO} = 500V, T_S = 150°C	> 10^{9}	
Barrier Capacitance Side A to Side B	C_{IO}	f_{SW} = 1MHz (Note 8)	1.5	pF
Minimum Creepage Distance	CPG		4	mm
Minimum Clearance Distance	CLR		4	mm
Internal Clearance		Distance through insulation	0.021	mm
Comparative Tracking Index	CTI	Material Group I (IEC 60112)	> 600	
Climate Category			40/125/21	
Pollution Degree (DIN VDE 0110, Table 1)			2	

Table 2. Insulation Characteristics (Wide SOIC)

PARAMETER	SYMBOL	CONDITIONS	VALUE	UNITS
Partial Discharge Test Voltage	V_{PR}	Method B1 = V_{IORM} x 1.875 (t = 1s, partial discharge < 5pC)	2250	V_P
Maximum Repetitive Peak Isolation Voltage	V_{IORM}	(Note 6)	1200	V_P
Maximum Working Isolation Voltage	V_{IOWM}	Continuous RMS voltage (Note 6)	848	V_{RMS}
Maximum Transient Isolation Voltage	V_{IOTM}	t = 1s (Note 6)	7070	V_P
Maximum Withstanding Isolation Voltage	V_{ISO}	f_{SW} = 60Hz, duration = 60s (Notes 6, 7)	5000	V_{RMS}
Maximum Surge Isolation Voltage	V_{IOSM}	Reinforced Insulation, test method per IEC 60065, V_{TEST} = 1.6 x V_{IOSM} = 12800V_{PEAK} (Notes 6, 9)	8000	V_P
	R_{IO}	V_{IO} = 500V, T_A = 25°C	> 10^{12}	Ω

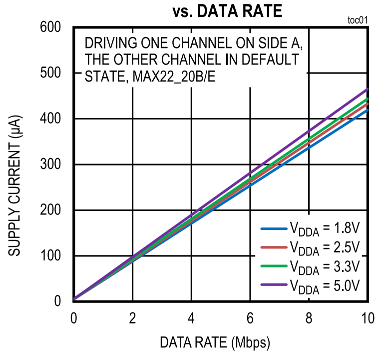
Isolation Resistance		V_{IO} = 500V, 100°C ≤ T_A ≤ 125°C	> 10^{11}	
		V_{IO} = 500V, T_S = 150°C	> 10^{9}	
Barrier Capacitance Side A to Side B	C_{IO}	f_{SW} = 1MHz (Note 8)	1.5	pF
Minimum Creepage Distance	CPG		8	mm
Minimum Clearance Distance	CLR		8	mm
Internal Clearance		Distance through insulation	0.021	mm
Comparative Tracking Index	CTI	Material Group I (IEC 60112)	> 600	
Climate Category			40/125/21	
Pollution Degree (DIN VDE 0110, Table 1)			2	

Note 6: V_{ISO}, V_{IOTM}, V_{IOWM}, V_{IORM}, and V_{IOSM} are defined by the IEC 60747-5-5 standard.
Note 7: Product is qualified at V_{ISO} for 60s and 100% production tested at 120% of V_{ISO} for 1s.
Note 8: Capacitance is measured with all pins on field-side and logic-side tied together.
Note 9: Devices are immersed in oil during surge characterization.

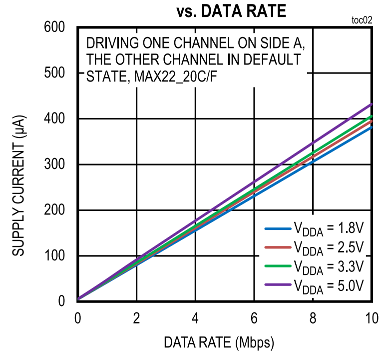
Typical Operating Characteristics

(V_{DDA} - V_{GNDA} = +3.3V, V_{DDB} - V_{GNDB} = +3.3V, V_{GNDA} = V_{GNDB}, T_A = +25°C, unless otherwise noted.)

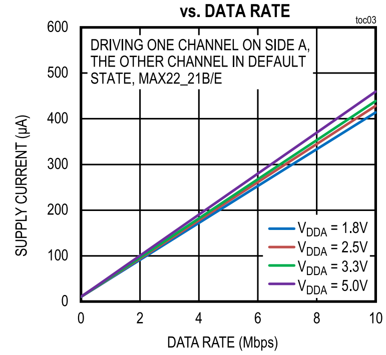
SIDE A SUPPLY CURRENT vs. DATA RATE



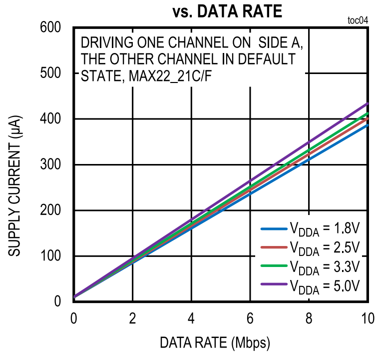
SIDE A SUPPLY CURRENT vs. DATA RATE



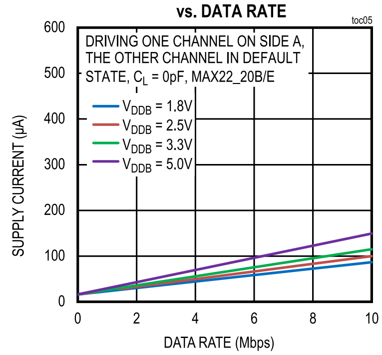
SIDE A SUPPLY CURRENT vs. DATA RATE



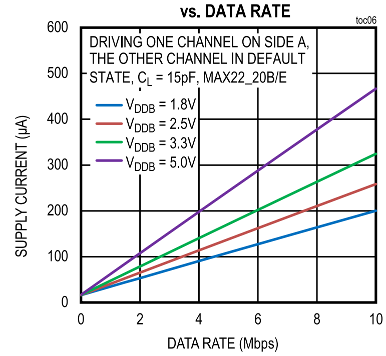
SIDE A SUPPLY CURRENT vs. DATA RATE



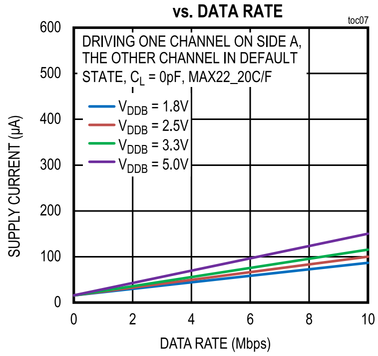
SIDE B SUPPLY CURRENT vs. DATA RATE



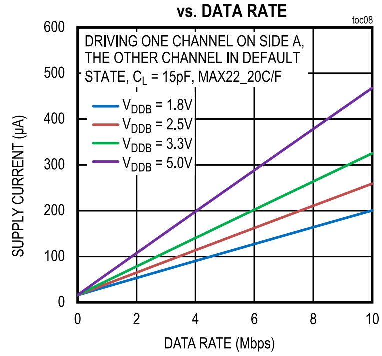
SIDE B SUPPLY CURRENT vs. DATA RATE



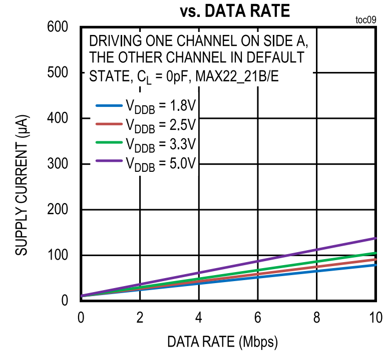
SIDE B SUPPLY CURRENT vs. DATA RATE



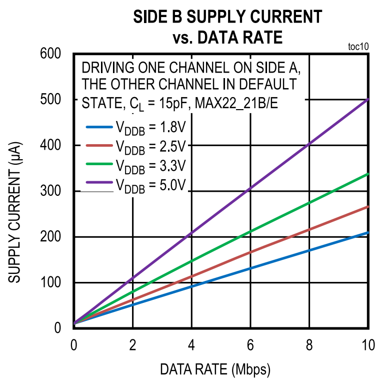
SIDE B SUPPLY CURRENT vs. DATA RATE

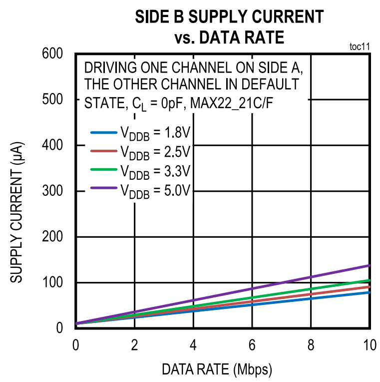


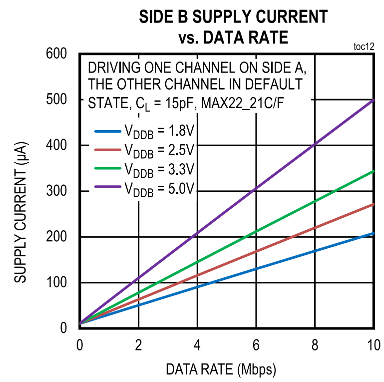
SIDE B SUPPLY CURRENT vs. DATA RATE

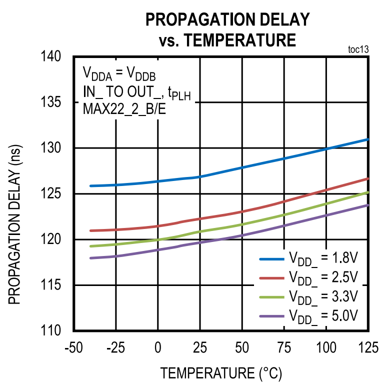


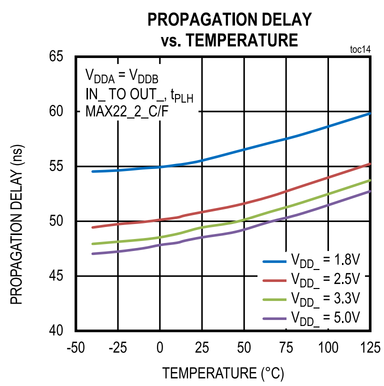
(V_{DDA} - V_{GNDA} = +3.3V, V_{DDB} - V_{GNDB} = +3.3V, V_{GNDA} = V_{GNDB}, T_A = +25°C, unless otherwise noted.)

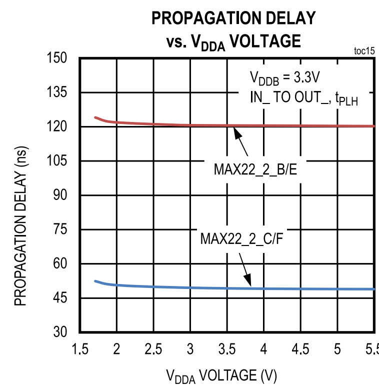


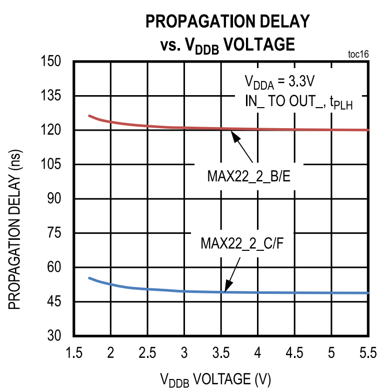


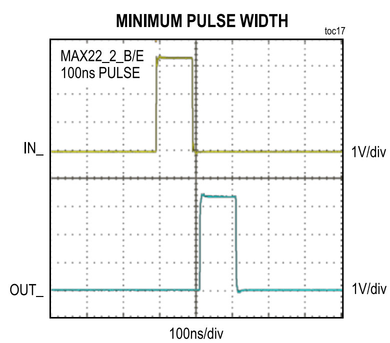


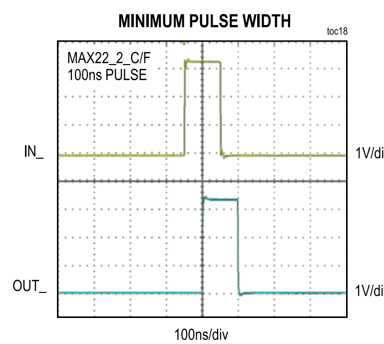




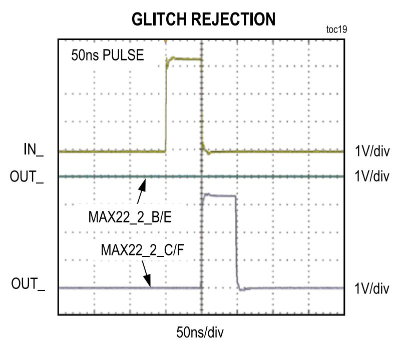


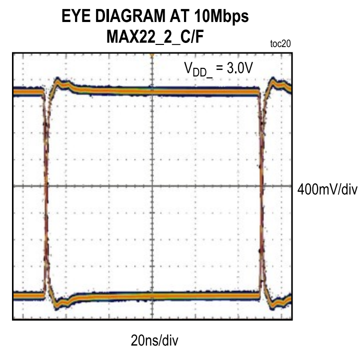


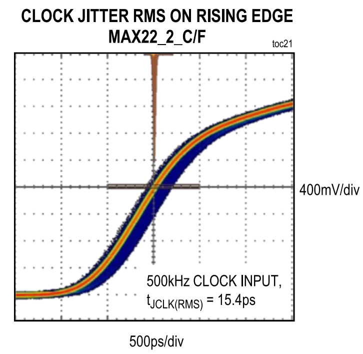


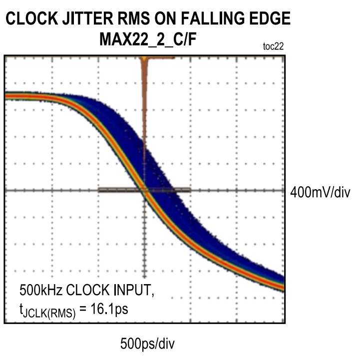


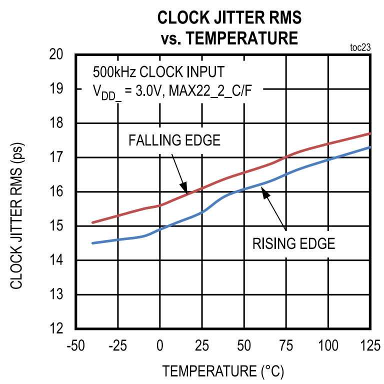
(V_{DDA} - V_{GNDA} = +3.3V, V_{DDB} - V_{GNDB} = +3.3V, V_{GNDA} = V_{GNDB}, T_A = +25°C, unless otherwise noted.)



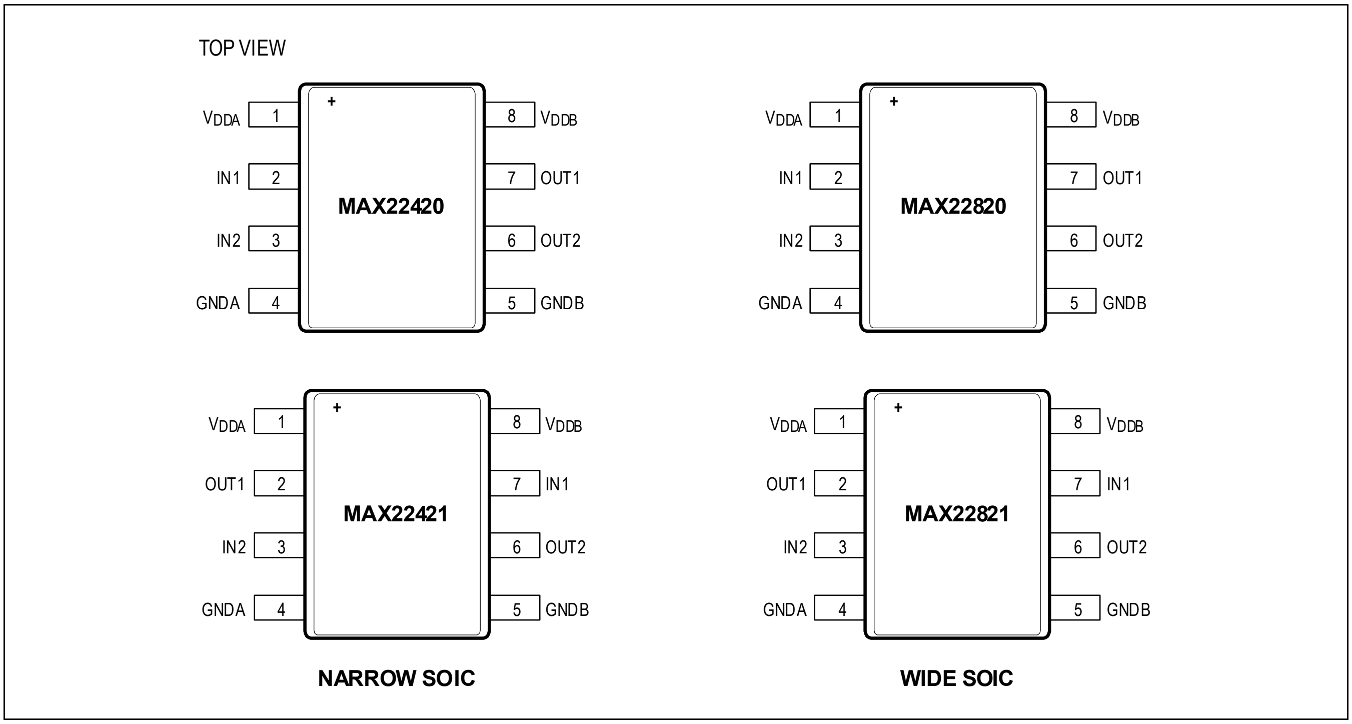








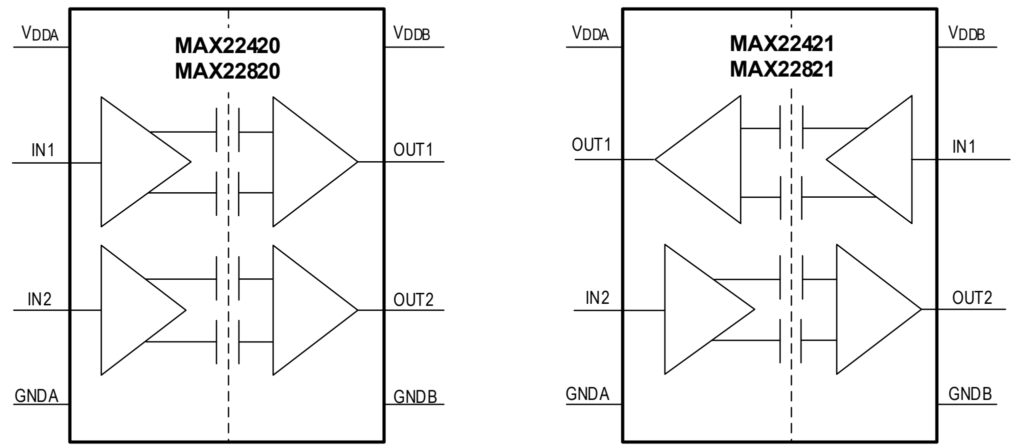
Pin Configurations



Pin Descriptions

PIN		NAME	FUNCTION
MAX22420/ MAX22820	MAX22421/ MAX22821		
1	1	V_{DDA}	Power Supply Input for Side A. Bypass V_{DDA} to GNDA with a 0.1μF ceramic capacitor as close as possible to the pin.
2	—	IN1	Logic Input 1 on Side A.
—	2	OUT1	Logic Output 1 on Side A.
3	3	IN2	Logic Input 2 on Side A.
4	4	GNDA	Ground Reference for Side A.
5	5	GNDB	Ground Reference for Side B.
6	6	OUT2	Logic Output 2 on Side B.
7	—	OUT1	Logic Output 1 on Side B.
—	7	IN1	Logic Input 1 on Side B.
8	8	V_{DDB}	Power Supply Input for Side B. Bypass V_{DDB} to GNDB with a 0.1μF ceramic capacitor as close as possible to the pin.

Functional Diagrams



Detailed Description

The MAX22_2_ are a family of 2-channel reinforced ultra-low-power digital isolators. The MAX22_2_ consume ultra-low power not only in DC but also across the entire operating speed range up to 10Mbps. The family offers two unidirectional channel configurations to accommodate any 2-channel design.

The MAX22_20 feature two channels transferring digital signals in one direction. The MAX22_21 have one channel to transmit data in one direction and the other channel to transmit in the opposite direction.

The MAX22420/1 are available in an 8-pin narrow-body SOIC package with 4mm creepage and clearance and are rated up to $3kV_{RMS}$. The MAX22820/1 are available in an 8-pin wide-body SOIC package with 8mm creepage and clearance and are rated up to $5kV_{RMS}$. This family of digital isolators offers ultra-low-power operation, high electromagnetic interference (EMI) immunity, and stable temperature performance through Analog Devices' proprietary process technology. The devices isolate different ground domains and block high-voltage/high-current transients from sensitive or human interface circuitry.

The family of devices has a maximum data rate of 10Mbps and can be ordered with two glitch filter options and default-high or default-low outputs. The default is the state the output assumes when the input is open circuit. The B/E versions have 70ns (typ) glitch filter and C/F versions have 29ns (typ) glitch filter. The devices have two supply inputs (V_{DDA} and V_{DDB}) that independently set the logic levels on either side of device. V_{DDA} and V_{DDB} are referenced to GNDA and GNDB, respectively. The family also features a refresh circuit to ensure output accuracy when an input remains in the same state indefinitely.

Digital Isolation

The MAX22_2_ provide reinforced galvanic isolation for digital signals that are transmitted between two ground domains. The MAX22420/1 withstand differences of up to $3kV_{RMS}$ for up to 60 seconds, and up to $630V_{PEAK}$ of continuous isolation. The MAX22820/1 withstand differences of up to $5kV_{RMS}$ for up to 60 seconds, and up to $1200kV_{PEAK}$ of continuous isolation.

Level Shifting

The wide supply voltage range of both V_{DDA} and V_{DDB} allows the family of devices to be used for level translation in addition to isolation. V_{DDA} and V_{DDB} can be independently set to any voltage from 1.71V to 5.5V. The supply voltage sets the logic level on the corresponding side of the isolator.

Unidirectional Channels

Each channel of the devices is unidirectional; it only passes data in one direction, as indicated in the *Functional Diagrams*. Each device features two unidirectional channels that operate independently with guaranteed data rates from DC up to 10Mbps. The output driver of each channel is push-pull, eliminating the need for pullup resistors. The outputs are able to drive both TTL and CMOS logic inputs.

Startup and Undervoltage Lockout

The V_{DDA} and V_{DDB} supplies are both internally monitored for undervoltage conditions. Undervoltage events can occur during power-up, power-down, or during normal operation due to a sagging supply voltage. When an undervoltage condition is detected on the output supply, the outputs go to high-Z regardless of the state of the inputs. When an undervoltage condition is detected on the input supply, the outputs go to default regardless of the state of the inputs as seen in *Table 3*. During the output supply rises above the UVLO (Powered), the output transitions from high-Z to default state for a short period of time before becoming valid. During the output supply drops below the UVLO (Undervoltage), the output transitions to high-Z immediately. *Figure 2* shows the output UVLO to output valid and input UVLO to output default timing diagrams. *Figure 3* through *Figure 6* show the behavior of the outputs during power-up and power-down.

Table 3. Output Behavior During Undervoltage Condition

$V_{IN\_}$	V_{DDA}	V_{DDB}	V_{OUTA}	V_{OUTB}
1	Powered	Powered	High	High
0	Powered	Powered	Low	Low
X	Undervoltage	Powered	High-Z	Default
X	Powered	Undervoltage	Default	High-Z

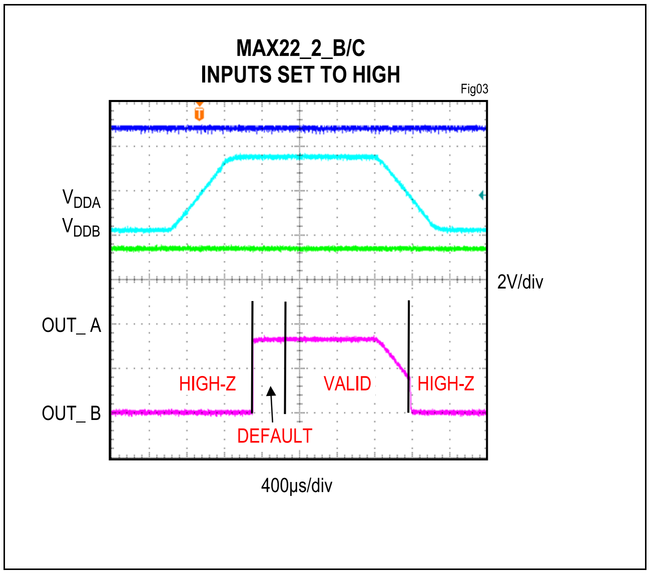


Figure 3. Undervoltage Lockout Behavior MAX22_2_B/C, Input High, Weak Outputs Pulldown to Ground

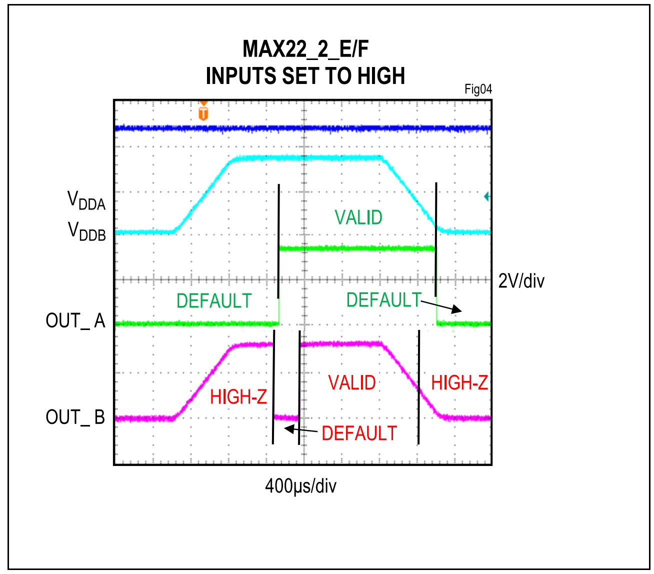


Figure 4. Undervoltage Lockout Behavior MAX22_2_E/F, Input High, Weak Outputs Pullup to Supply

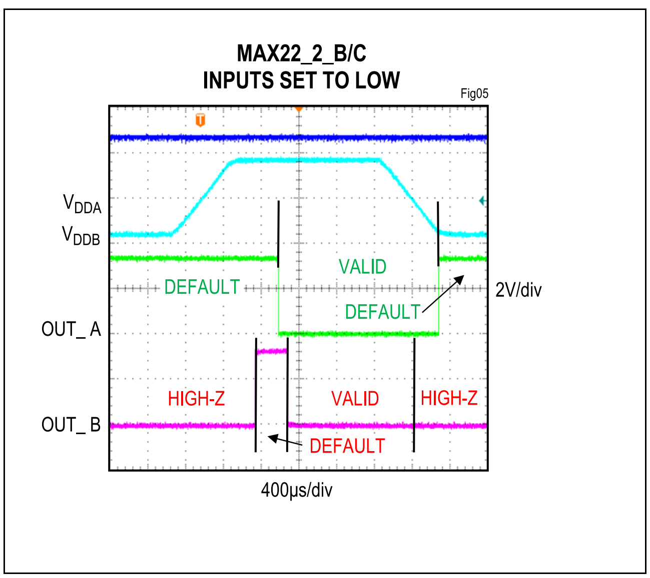


Figure 5. Undervoltage Lockout Behavior MAX22_2_B/C, Input Low, Weak Outputs Pulldown to Ground

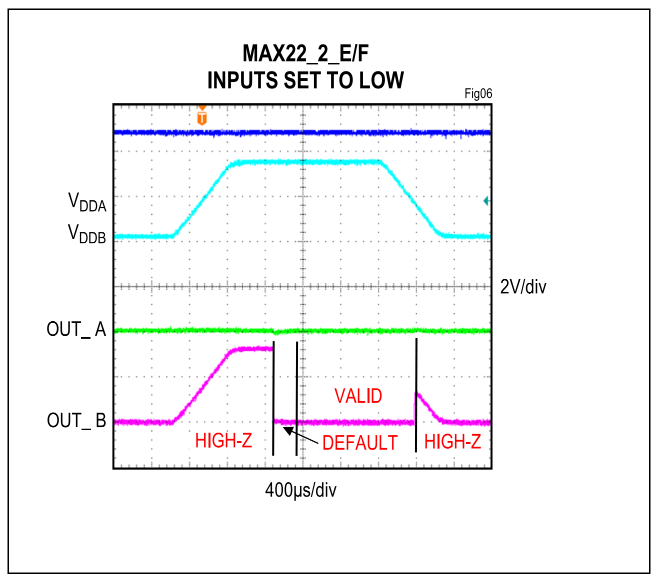


Figure 6. Undervoltage Lockout Behavior MAX22_2_E/F, Input Low, Weak Outputs Pullup to Supply

Safety Limits

Damage to the IC can result in a low-resistance path to ground or to the supply and, without current limiting, the devices can dissipate excessive amounts of power. Excessive power dissipation can damage the die and result in damage to the isolation barrier, potentially causing downstream issues. *Table 4* shows the safety limits for the MAX22_2_.

The maximum safety temperature (T_S) for the device is the 150°C maximum junction temperature specified in the *Absolute Maximum Ratings*. The power dissipation (P_D) and junction-to-ambient thermal impedance (θ_{JA}) determine the junction temperature. Thermal impedance values (θ_{JA} and θ_{JC}) are available in the *Package Information* section and power dissipation calculations are discussed in the *Calculating Power Dissipation* section. Calculate the junction temperature (T_J) as:

$$T_J = T_A + (P_D \times \theta_{JA})$$

Figure 7 shows the thermal derating curves for safety limiting the power of the device. *Figure 8* shows the thermal derating curve for safety limiting the current of the device. Ensure that the junction temperature does not exceed 150°C.

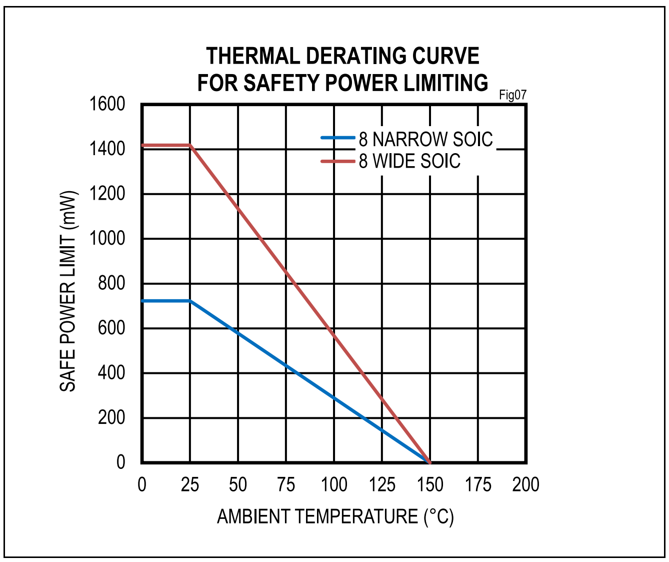


Figure 7. Thermal Derating Curve for Safety Power Limiting

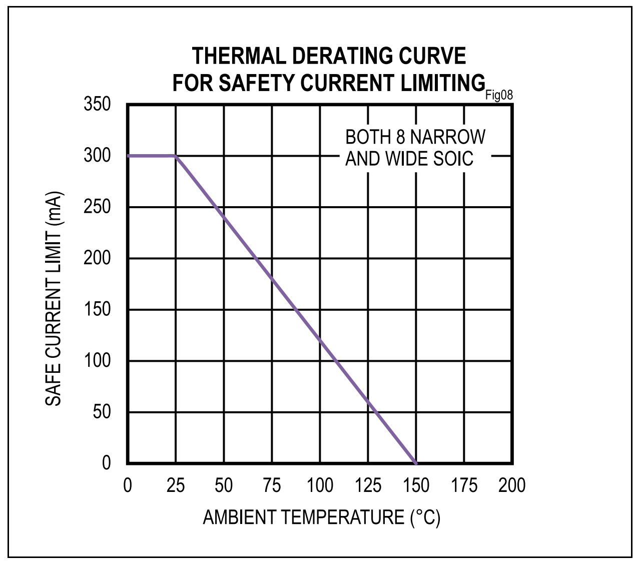


Figure 8. Thermal Derating Curve for Safety Current Limiting

Table 4. Safety Limiting Values

PARAMETER	SYMBOL	TEST CONDITIONS		MAX	UNIT
Safety Current on Any Pin (No Damage to Isolation Barrier)	I_S	T_J = 150°C, T_A = 25°C		300	mA
Total Safety Power Dissipation	P_S	T_J = 150°C, T_A = 25°C	8 Narrow SOIC	723	mW
			8 Wide SOIC	1418	
Maximum Safety Temperature	T_S			150	°C

Applications Information

Power-Supply Sequencing

The family of devices does not require special power-supply sequencing. The logic levels are set independently on either side by V_{DDA} and V_{DDB}. Each supply can be present over the entire specified range regardless of the level or presence of the other supply.

Power-Supply Decoupling

To reduce ripple and the chance of introducing data errors, bypass V_{DDA} and V_{DDB} with 0.1µF low-ESR ceramic capacitors to GNDA and GNDB, respectively. Place the bypass capacitors as close to the power supply input pins as possible.

Layout Considerations

The PCB designer should follow some critical recommendation in order to get the best performance from the design.

- Keep the input/output traces as short as possible. To keep signal paths low inductance, avoid using vias.
- Have a solid ground plane underneath the high-speed signal layer.
- Keep the area underneath the devices free from ground and signal planes. Any galvanic or metallic connection between the field-side and logic-side defeats the isolation.

Calculating Power Dissipation

The required current for a given supply (V_{DDA} or V_{DDB}) can be estimated by summing the current required for each channel. The supply current for a channel depends on whether the channel is an input or an output, the channel's data rate, and the capacitive or resistive load if it is an output. The typical current for an input or output at any data rate can be estimated from the graphs in Figure 9 and Figure 10. Note that the data in Figure 9 and Figure 10 are extrapolated from the supply current measurements in a typical operating condition.

The total current for a single channel is the sum of the no load current (shown in Figure 9 and Figure 10), which is a function of voltage and data rate, and the load current, which depends on the type of load. Current into a capacitive load is a function of the load capacitance, the switching frequency, and the supply voltage.

$$I_{CL} = C_L \times f_{SW} \times V_{DD}$$

where:

I_{CL} is the current required to drive the capacitive load.

C_L is the load capacitance on the isolator's output pin.

f_{SW} is the switching frequency (bits per second/2).

V_{DD} is the supply voltage on the output side of the isolator.

Current into a resistive load depends on the load resistance, the supply voltage and the average duty cycle of the data waveform. The DC load current can be conservatively estimated by assuming the output is always high.

$$I_{RL} = V_{DD} \div R_L$$

where:

I_{RL} is the current required to drive the resistive load.

V_{DD} is the supply voltage on the output side of the isolator.

R_L is the load resistance on the isolator's output pin.

Example (shown in Figure 11): A MAX22421C is operating with V_{DDA} = 2.5V, V_{DDB} = 3.3V, channel 1 operating at 2Mbps with a 15pF capacitive load, and channel 2 operating at 10Mbps with a 10kΩ resistive load. See Table 5 and Table 6 for V_{DDA} and V_{DDB} supply-current calculation worksheets.

V_{DDA} must supply:

Channel 1 is an output channel operating at 2.5V and 2Mbps, consuming 23.93µA, estimated from Figure 10.
Channel 2 is an input channel operating at 2.5V and 10Mbps, consuming 393.35µA, estimated from Figure 9.
I_{CL} on Channel 1 for 15pF capacitor at 2.5V and 2Mbps is 37.5µA.

Total current for side A = 454.8µA (typ)

V_{DDB} must supply:

Channel 1 is an input channel operating at 3.3V and 2Mbps, consuming 82.92μA, estimated from *Figure 9*.
Channel 2 is an output channel operating at 3.3V and 10Mbps, consuming 102.49μA, estimated from *Figure 10*.
I_{RL} on Channel 2 for 10kΩ resistor switching at 50% duty cycle and at 3.3V is 165μA.

Total current for side B = 350.4μA (typ)

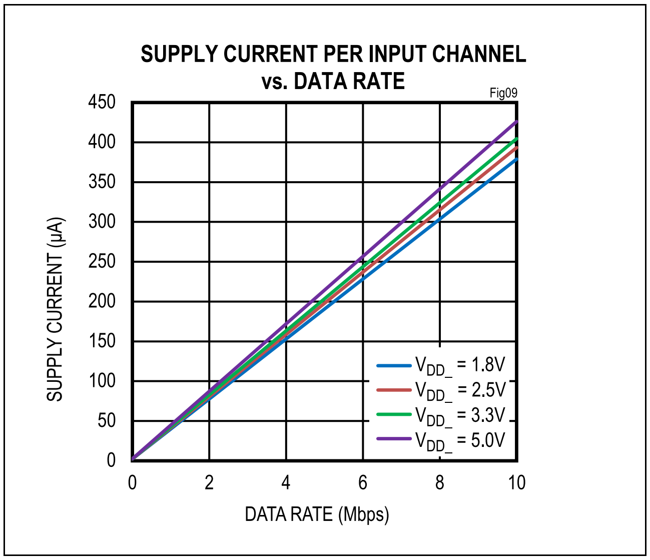


Figure 9. Supply Current per Input Channel (Estimated)

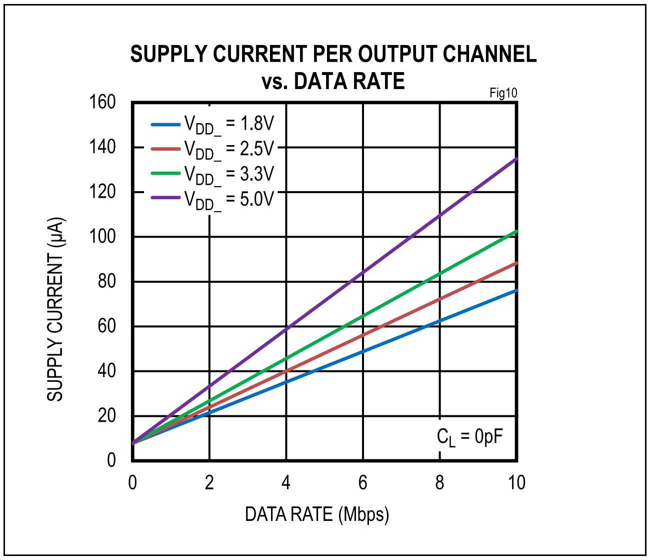


Figure 10. Supply Current per Output Channel (Estimated)

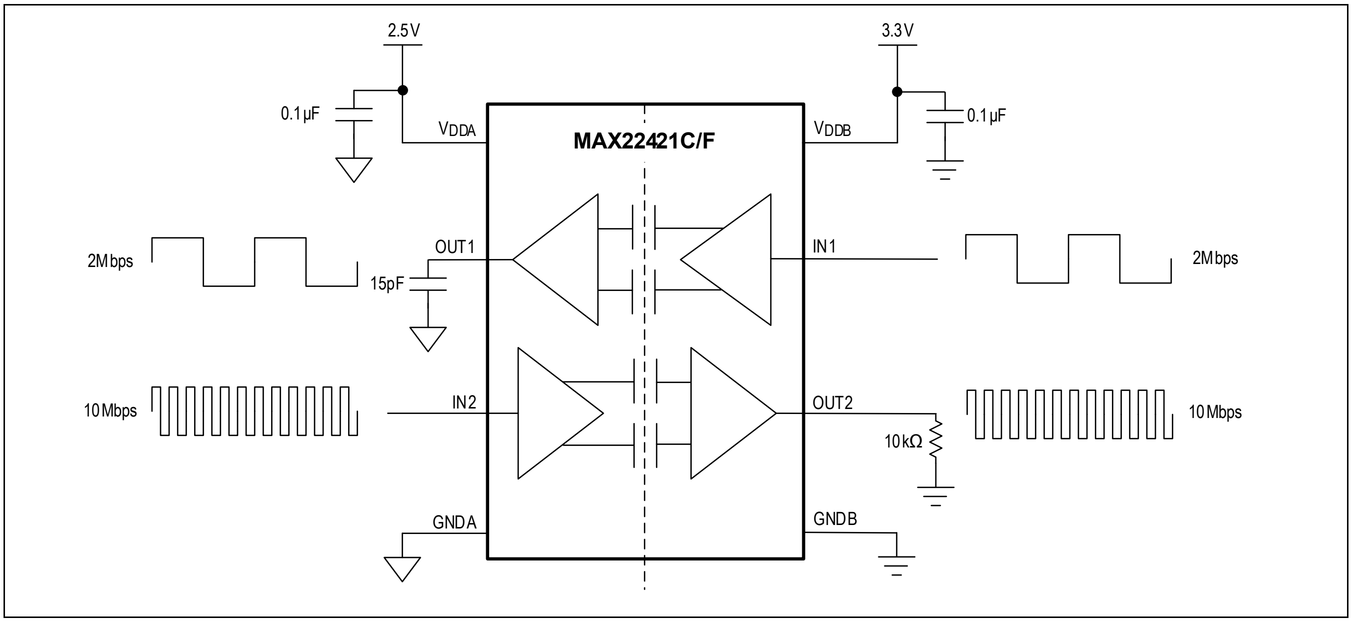


Figure 11. Example Circuit for Supply Current Calculation

Table 5. Side A Supply Current Calculation Worksheet

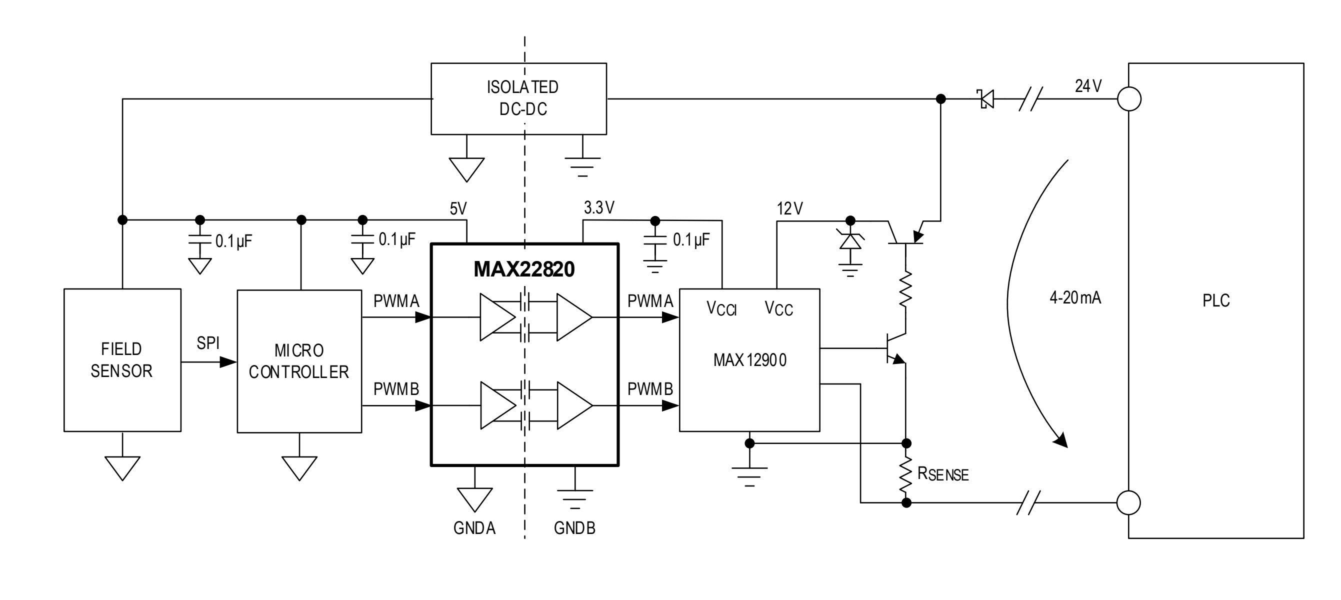
SIDE A	V_{DDA} = 2.5V					
CHANNEL	IN/OUT	DATA RATE (Mbps)	LOAD TYPE	LOAD	NO LOAD CURRENT (µA)	LOAD CURRENT (µA)
1	OUT	2	Capacitive	15pF	23.93	2.5V x 1MHz x 15pF = 37.5µA
2	IN	10			393.35	
Total: 454.8µA						

Table 6. Side B Supply Current Calculation Worksheet

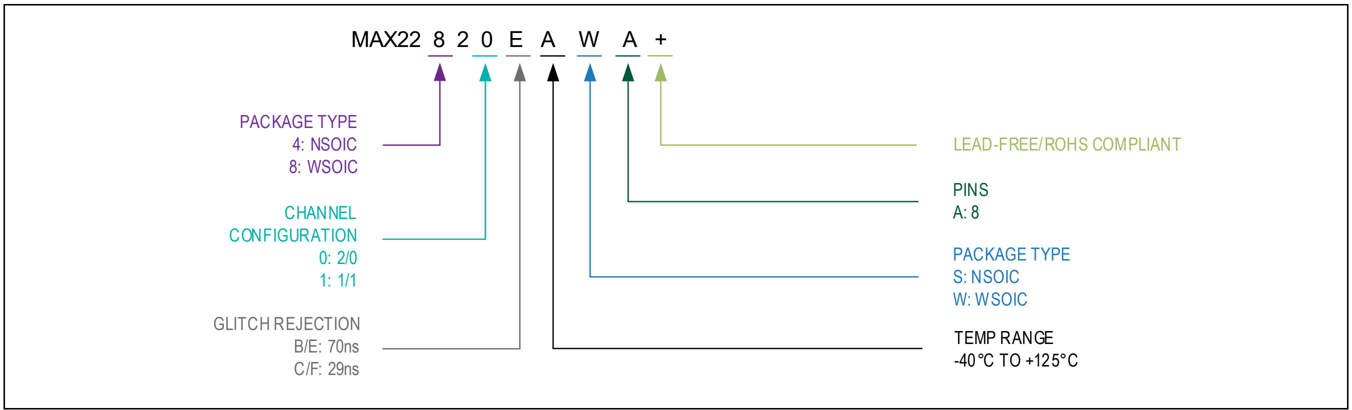
SIDE B	V_{DDB} = 3.3V					
CHANNEL	IN/OUT	DATA RATE (Mbps)	LOAD TYPE	LOAD	NO LOAD CURRENT (µA)	LOAD CURRENT (µA)
1	IN	2			82.92	
2	OUT	10	Resistive	10kΩ	102.49	3.3V/10kΩ x 0.5 = 165µA
Total: 350.4µA						

Typical Application Circuits

4-20mA Loop Powered Control



Product Selector Guide



Ordering Information

PART NUMBER	CHANNEL CONFIGURATION	GLITCH REJECTION (ns)	DEFAULT OUTPUT	PIN-PACKAGE	TEMPERATURE RANGE (°C)
MAX22420BASA+*	2/0	70	High	8 Narrow SOIC	-40 to +125
MAX22420CASA+*	2/0	29	High	8 Narrow SOIC	-40 to +125
MAX22420EASA+*	2/0	70	Low	8 Narrow SOIC	-40 to +125
MAX22420FASA+	2/0	29	Low	8 Narrow SOIC	-40 to +125
MAX22421BASA+	1/1	70	High	8 Narrow SOIC	-40 to +125
MAX22421CASA+	1/1	29	High	8 Narrow SOIC	-40 to +125
MAX22421EASA+	1/1	70	Low	8 Narrow SOIC	-40 to +125
MAX22421FASA+	1/1	29	Low	8 Narrow SOIC	-40 to +125
MAX22820BAWA+*	2/0	70	High	8 Wide SOIC	-40 to +125
MAX22820CAWA+*	2/0	29	High	8 Wide SOIC	-40 to +125
MAX22820EAWA+	2/0	70	Low	8 Wide SOIC	-40 to +125
MAX22820FAWA+*	2/0	29	Low	8 Wide SOIC	-40 to +125
MAX22821BAWA+*	1/1	70	High	8 Wide SOIC	-40 to +125
MAX22821CAWA+*	1/1	29	High	8 Wide SOIC	-40 to +125
MAX22821EAWA+*	1/1	70	Low	8 Wide SOIC	-40 to +125
MAX22821FAWA+*	1/1	29	Low	8 Wide SOIC	-40 to +125

**Future product—contact Analog Devices for availability.*

+Denotes a lead(Pb)-free/RoHS-compliant package.

Chip Information

PROCESS: BiCMOS

Revision History

REVISION NUMBER	REVISION DATE	DESCRIPTION	PAGES CHANGED
0	2/22	Release for Market Intro	—
1	3/22	Remove future product asterisks in the *Ordering Information* table	26
2	8/22	Remove future product asterisks in the Ordering Information table	26
3	11/23	Remove future product asterisks in the *Ordering Information* table	26