EVALUATION KIT AVAILABLE

*Click **here** to ask an associate for production status of specific part numbers.*

MAX20463/MAX20463A

USB Type-A to Type-C Port Converter with Protection

General Description

The MAX20463 is a small, integrated USB Type-C® Downstream-Facing Port (DFP) solution used to convert an existing USB-A head-unit captive-cable port to a head-unit USB Type-C captive-cable port. When the MAX20463 is designed into an automotive module at the end of the cable, then the existing upstream head-unit USB-A solution and the existing USB-A captive-cable housing can be reused.

The device protection features include ±15kV/±8kV IEC 61000-4-2 ESD on CC1/CC2, and IEC ESD with short-to-battery (18V) on SENSE/HVBUS. The MAX20463A senses a short of the passenger cable shield to car battery, preventing damage to the port. Short-to-ground and short-to-battery survival are also provided on the HVBUS signal and defined to operate in concert with the existing head-unit USB-A charger/protector, allowing coordinated fault detection and reporting to the head-unit USB host.

The MAX20463 is available in a small, 3mm x 3mm, 12-pin TDFN package, using very few external components.

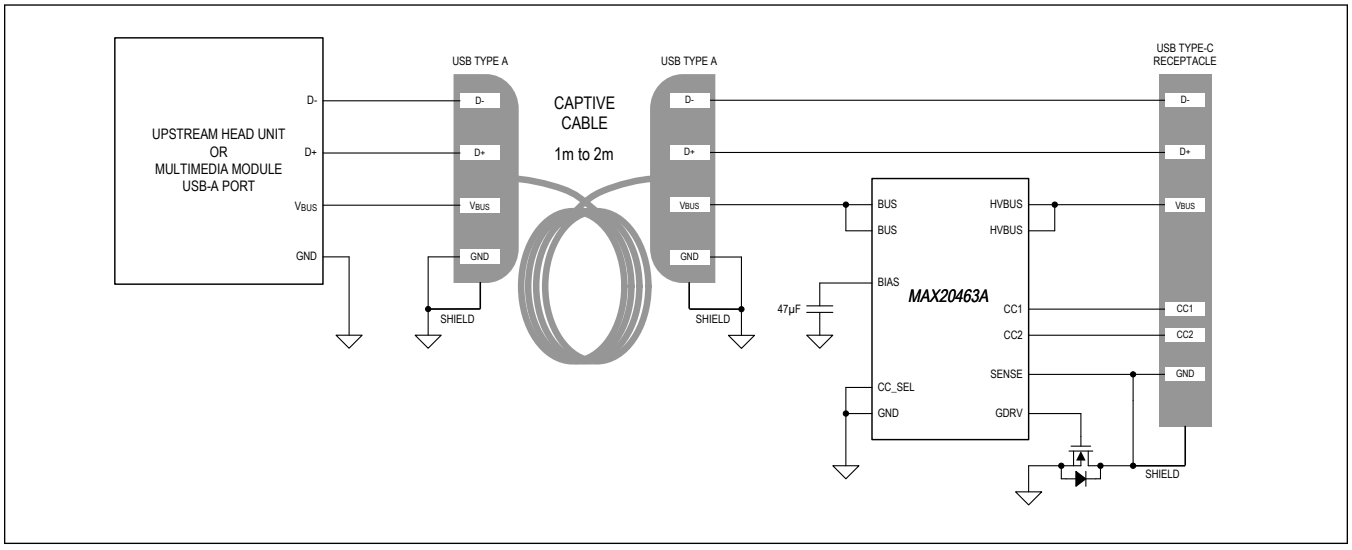
Applications

- Automotive USB Captive-Cable Housing
- Automotive Downstream USB Modules

Benefits and Features

- Designed to USB Type-C R1.3 Specification with Integrated V_{BUS} Discharge
  - USB Type-C 1.5A, 3.0A DFP Controller
  - Type-C Current Limit Reduction with V_{BUS} Dropout
- Designed for Cooperative Protection with Head-Unit Protector
  - Short-to-Battery and Short-to-Ground Survival on HVBUS for Upstream Protector to Handle
  - Accurate USB Bus Forward Current Threshold
  - Low R_{ON} 28mΩ (typ) USB Power Switch
- Robust Design Keeps Vehicle System and Portable Devices Safe in Automotive Environment
  - Optional Shield Short-to-Battery Detection and External FET Control
  - Short-to-BUS Protection on Protected CC1 and CC2 Outputs
  - IEC 61000-4-2 Level-4 ESD Protection (HVBUS, CC1, CC2, SENSE)
- 3mm x 3mm 12-Pin TDFN Package
- -40°C to +105°C Operating Temperature Range
- AEC-Q100 Qualified

Simplified Block Diagram



USB Type-C is a registered certification mark of the USB Implementers Forum, Inc.

***Ordering Information** appears at end of data sheet.*

19-100441; Rev 4; 5/22

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Absolute Maximum Ratings

BIAS, CC1, CC2, CC_SEL, GDRV ..... -0.3V to +6V
BUS, HVBUS, SENSE to GND ..... -0.3V to +18V
BUS to HVBUS..... -0.3V to +9V
Short-Circuit Between HVBUS and GND 3.5A

Continuous Power Dissipation (Multilayer Board) (T_A = +70°C, derate 41mW/°C above +70°C.) 1951mW
Operating Temperature Range .....-40°C to +105°C
Storage Temperature Range .....-65°C to +150°C
Lead Temperature Range..... +300°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Package Information

TDFN

Package Code	TD1233+1C
Outline Number	21-0664
Land Pattern Number	90-0397
Thermal Resistance, Four-Layer Board:	
Junction to Ambient (θ_{JA})	41°C/W
Junction to Case (θ_{JC})	8.5°C/W

For the latest package outline information and land patterns (footprints), go to *www.maximintegrated.com/packages*. Note that a "+", "#", or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

Package thermal resistances were obtained using the method described in JEDEC specification JESD51-7, using a four-layer board. For detailed information on package thermal considerations, refer to *www.maximintegrated.com/thermal-tutorial*.

Electrical Characteristics

(V_{CC_SEL} = 0V, V_{BUS} = 5V, V_{SENSE} = 0V, All Other Pins = Floating, T_A = T_J = -40°C to +105°C. Typical values are at T_A = +25°C under normal conditions unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
BUS POWER SUPPLY						
BUS Supply Voltage Range	V_{BUS}	V_{BUS} supplied by upstream facing supply. V_{BUS} can be overdriven with short-to-battery.	4.75		6.0	V
BUS Supply Current	I_{BUS3P0}	FSM state = Attached.SRC_CCx, DFP 3.0, CCx = 5.1kΩ to ground			1.8	mA
	I_{BUS1P5}	FSM state = Attached.SRC_CCx, DFP 1.5, CCx = 5.1kΩ to ground			1.6	
	I_{BUS}	FSM state = Unattached.SRC			1	
BIAS REGULATOR						
BIAS Regulator Output Voltage	V_{BIAS}	V_{BUS} = 4.75V to 7V	3.85		5.5	V
BIAS Undervoltage Lockout Rising Threshold	$V_{UVBIAS, RISE}$	V_{BIAS} rising	3.34	3.5	3.66	V
Falling Threshold to Force DFP1.5	$V_{DFPP, FALL}$	V_{BIAS} falling	3.32	3.43	3.54	V
BIAS Power-On Reset Rising Threshold	$V_{BIAS\_POR, RISE}$	V_{BIAS} rising	2.4	2.5	2.6	V
BIAS Undervoltage Lockout Falling Threshold	$V_{UVBIAS, FALL}$	V_{BIAS} falling	2.3	2.4	2.5	V
BIAS Supply Current (Current Supplied by the Bias Capacitor)	$I_{BIAS\_DFP1.5}$	BUS = 0V, BIAS from 2.55V to 5.5, FSM state = Attached.SRC_CCx, DFP 1.5, CCx = 5.1kΩ to ground		810		μA
BIAS Supply Current (Current Supplied by the Bias Capacitor)	$I_{BIAS\_DFP3.0}$	BUS = 0V, BIAS from 3.37V to 5.5, FSM state = Attached.SRC_CCx, DFP 3.0, CCx = 5.1kΩ to ground		960		μA
HVBUS USB POWER FET						
On-Resistance	R_{ON_BUS}	V_{BUS} = 5.0V, I_{BUS} = 500mA		28		mΩ
HVBUS Off-Leakage Current	$I_{LKG\_HVBUS, L}$	V_{BUS} = 5.0V, V_{HVBUS} = 0V			10	μA
	$I_{LKG\_HVBUS, H}$	V_{BUS} = 18V, V_{HVBUS} = 18V			100	
HVBUS Off Voltage	$V_{HVBUS, O}$	HVBUS = Open			0.2	V
HVBUS Short-to-GND Circuit Breaker Threshold	I_{SHRT}	V_{BUS} = 5.0V		11.5		A
HVBUS Short-to-GND Circuit Breaker Response Time (Deglitch)	t_{SHRT}			0.25		ms
Circuit Breaker Forward Current Threshold	I_{FWD}	Maximum Input Current to BUS is externally limited per USB spec (< 3.5A)	3.8	4.4	5	A

Electrical Characteristics (continued)

(V_{CC_SEL} = 0V, V_{BUS} = 5V, V_{SENSE} = 0V, All Other Pins = Floating, T_A = T_J = -40°C to +105°C. Typical values are at T_A = +25°C under normal conditions unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Circuit Breaker Response Time (Deglitch)	t_{FWD}			50		ms
HVBUS Overvoltage Threshold Rising	V_{OV}		7	7.5	8	V
HVBUS Overvoltage Threshold Hysteresis	$V_{OV, HYST}$			0.1		V
HVBUS Overvoltage Deglitch Time	t_{OV}			1		ms
HVBUS Discharge Current	I_{DISCHG}	HVBUS = 5V	10		35	mA
Thermal Shutdown Assertion Threshold	$T_{OVT, RISE}$			150		°C
Thermal Shutdown Threshold Hysteresis	$T_{OVT, HYST}$			15		°C
Fault Recovery Auto-Retry Time	t_{RETRY}		2	2.3	2.6	s
GROUND SWITCH CONTROL (MAX20463A)						
GDRV Unloaded Output Voltage High	$V_{GDRV, H}$		4.5		5.5	V
GDRV Output Voltage High	$V_{GDRV, LOAD}$	I_{GDRV} = 10µA (sink)	4			V
GDRV Output Resistance	R_{GDRV}	I_{GDRV} = 10µA and 20µA (sink), GDRV set high.		21	50	kΩ
GDRV Output Voltage Low	$V_{GDRV, L}$	I_{SINK} = 1mA (pullup)			0.4	V
SENSE Pin Trip Voltage Rising Threhsold	$V_{SENSE, RISE}$		130	150	175	mV
SENSE Pin Trip Voltage Threshold Hysteresis	$V_{SENSE, HYST}$			40		mV
SENSE Pin Blanking Time	$t_{SENSE, BLNK}$			4		µs
SENSE Pin Leakage	$I_{LKG\_SENSE, H}$	V_{SENSE} = 16V			20	µA
SENSE Pin Pulldown Current	$I_{PULLDOWN}$	V_{SENSE} = 0.25V	7	10	11	µA
USB TYPE-C						
CC Pin Operational Voltage	V_{CC_OP}				5.5	V
CC RA RD Detect Threshold	$V_{RA\_RD1.5}$	Rising, DFP 1.5A mode	0.36	0.4	0.45	V
		Falling, DFP 1.5A mode	0.35			
	$V_{RA\_RD3.0}$	Rising, DFP 3.0A mode	0.76	0.8	0.85	
		Falling, DFP 3.0A mode	0.75			

Electrical Characteristics (continued)

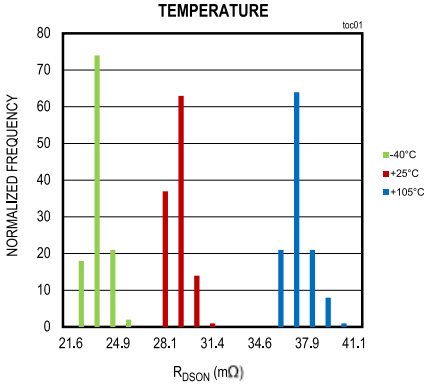
(V_{CC_SEL} = 0V, V_{BUS} = 5V, V_{SENSE} = 0V, All Other Pins = Floating, T_A = T_J = -40°C to +105°C. Typical values are at T_A = +25°C under normal conditions unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
CC DFP V_{OPEN} Detect Threshold	V_{DFP_OPEN}	1.5A DFP modes, rising	1.51	1.575	1.65	V
		1.5A DFP modes, falling	1.5			
	$V_{DFP\_OPEN\_3A}$	3.0A DFP modes, rising	2.46	2.6	2.75	
		3.0A DFP modes, falling	2.45			
V_{BUS} Removal Detect Threshold	V_{SAFE_0V}		0.6	0.68	0.8	V
V_{BUS} Removal Detect Hysteresis	$V_{SAFE\_0V\_HYST}$	Rising hysteresis		0.1		V
CC DFP 1.5A Current Source	$I_{DFP1.5\_CCx}$		166	180	194	µA
CC DFP 3.0A Current Source	$I_{DFP3.0\_CCx}$		304	330	356	µA
CC Open Termination Impedance	Z_{OPEN}		126			kΩ
Type-C Quick Debounce	$t_{Q\_DEBOUNCE}$	Transitions to/from Unattached states	0.9	1.05	1.2	ms
Type-C CC Pin Detection Debounce	$t_{CC\_DEBOUNCE}$	Final transitions to Attached states	100		200	ms
Type-C Error Recovery Delay	$t_{ERROR\_RECOVERY}$	Recovery time from Error state	25			ms
Type-C V_{BUS} Debounce	$t_{VBUS\_DEBOUNCE}$	V_{BDET} and V_{SAFE0V} debounce	8.4	10	11.6	ms
V_{BUS} On-Time	t_{VBUS_ON}	Time from UFP attached until DFP turns V_{BUS} on and reaches V_{BDET} (for reference only)	0		275	ms
V_{BUS} Off-Time	t_{VBUS_OFF}	Time from UFP detached until DFP turns V_{BUS} off and reaches V_{SAFE0V} (for reference only)	0		650	ms
DIGITAL INPUT (CC_SEL)						
Input Leakage Current	I_{LKG}	V_{CC_SEL} = 5.5V, 0V	-5		5	µA
Logic-High	V_{IH}		0.7 x V_{BIAS}			V
Logic-Low	V_{IL}				0.2 x V_{BIAS}	V
Hysteresis	V_{TH_HYST}			100		mV
ESD PROTECTION (ALL PINS)						
ESD Protection Level	V_{ESD}	Human Body Model		±2		kV
ESD PROTECTION (CC1, CC2, HVBUS with 2 x 1µF CAPACITOR, SENSE WITH 2 x 0.22µF)						
ESD Protection Level	V_{ESD}	ISO 10605 (330pF, 2kΩ) Air Gap		±25		kV
		ISO 10605 (150pF, 330Ω) Air Gap		±25		
		ISO 10605 (330pF, 330Ω) Air Gap		±15		
		ISO 10605 (330pF, 330Ω) Contact		±8		
		IEC 61000-4-2 Air Gap		±15		
		IEC 61000-4-2 Contact		±8		

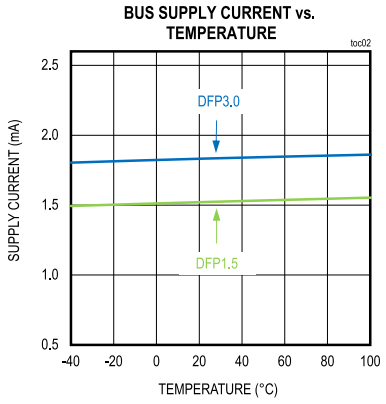
Typical Operating Characteristics

(T_A = +25°C, unless otherwise noted.)

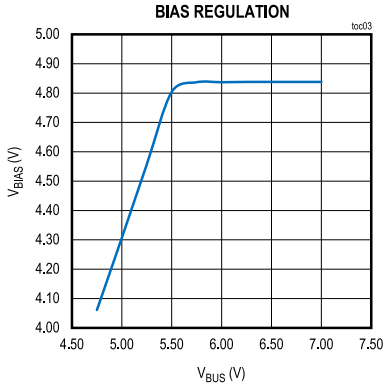
HVBUS POWER SWITCH ON-RESISTANCE vs. TEMPERATURE



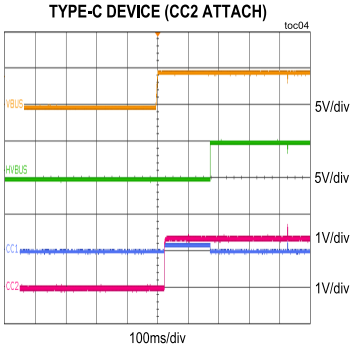
BUS SUPPLY CURRENT vs. TEMPERATURE



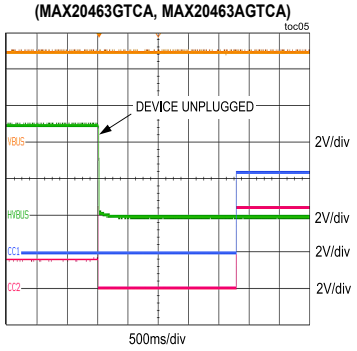
BIAS REGULATION



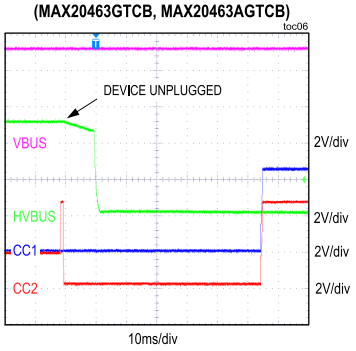
START UP INTO TYPE-C DEVICE (CC2 ATTACH)



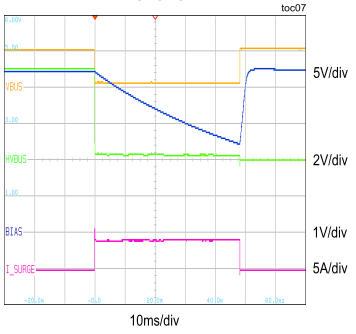
HVBUS SHUTDOWN AFTER TYPE-C DEVICE UNPLUGGED (MAX20463GTCA, MAX20463AGTCA)



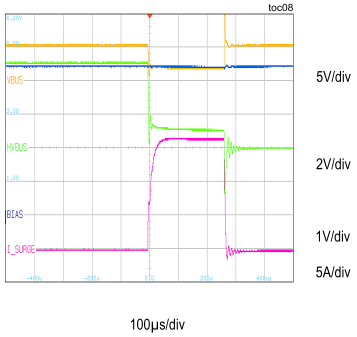
HVBUS SHUTDOWN AFTER TYPE-C DEVICE UNPLUGGED (MAX20463GTCB, MAX20463AGTCB)



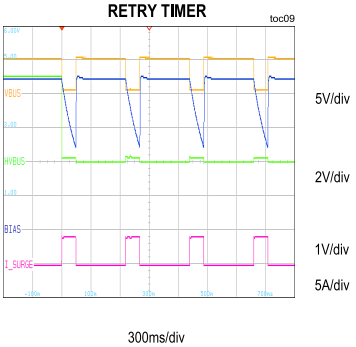
HVBUS SHORT-TO-GROUND RESPONSE



HVBUS SHORT-TO-GROUND RESPONSE WITH BENCH SUPPLY



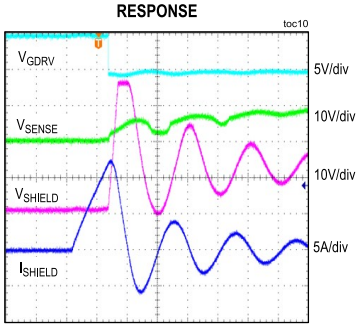
HVBUS SHORT-TO-GROUND RETRY TIMER



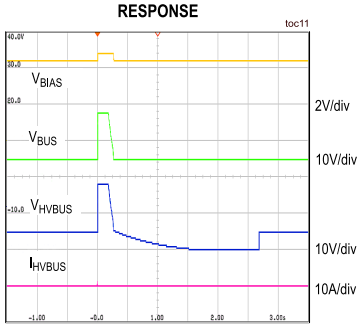
Typical Operating Characteristics (continued)

(T_A = +25°C, unless otherwise noted.)

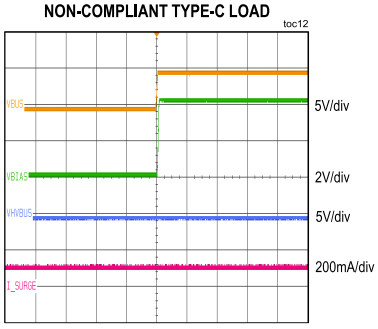
SHIELD SHORT-TO-BATTERY RESPONSE



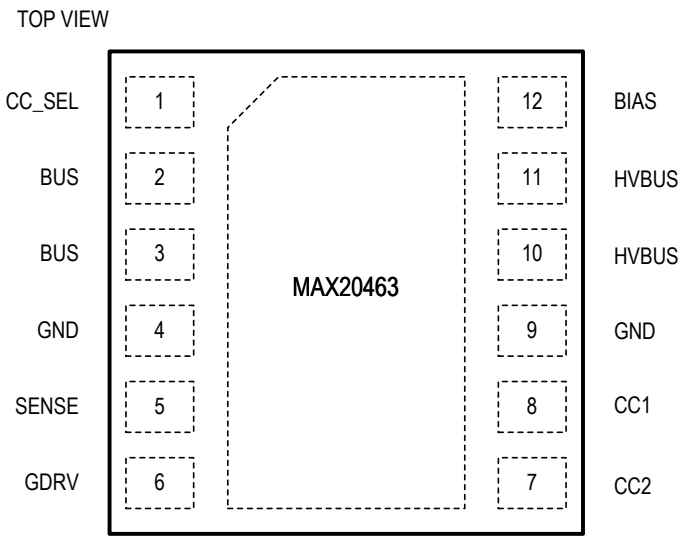
VBUS SHORT-TO-BATTERY RESPONSE



HVBUS TURN ON INTO NON-COMPLIANT TYPE-C LOAD



Pin Configuration

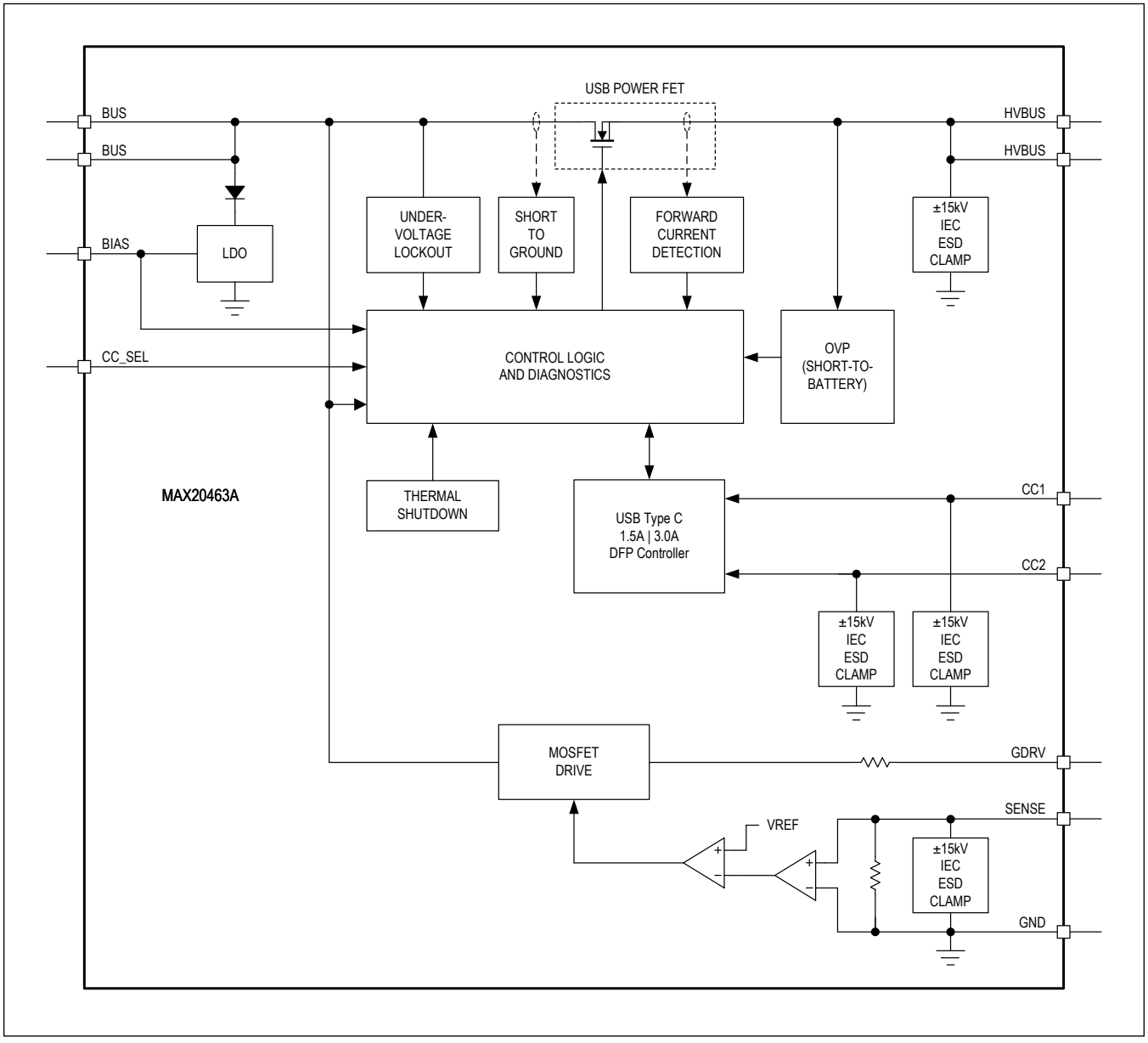


Pin Description

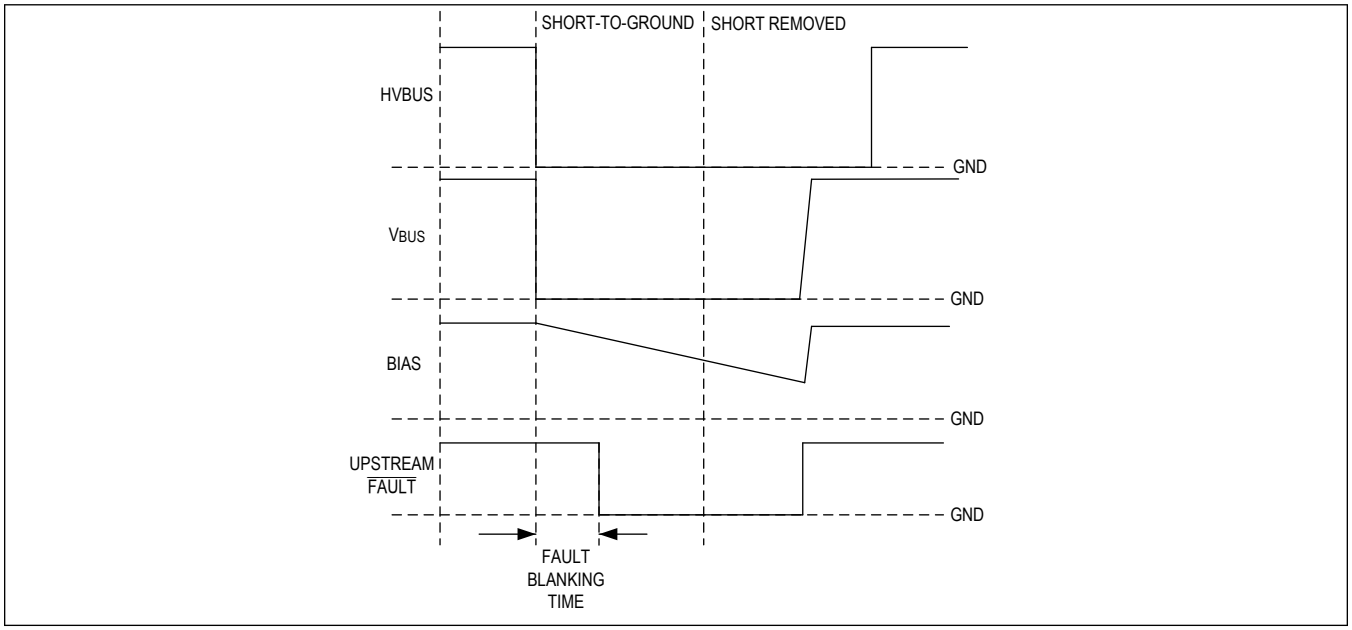
PIN	NAME	FUNCTION
1	CC_SEL	CC Mode Select. Changes advertised Type-C output current capability. High/low selection changes based on part number.
2	BUS	USB Power Supply. Connect BUS to upstream USB +5V supply. Both BUS inputs must be connected together. Connect a minimum of 0.1µF low-ESR ceramic capacitor from BUS to GND.
3		USB Power Supply Input. Connect BUS to upstream USB +5V supply. Both BUS inputs must be connected together. Connect a minimum of 0.1µF low-ESR ceramic capacitor from BUS to GND.
4	GND	Ground. Connect directly to GND. Tie to GND pour underneath IC. Tie GND directly to BUS and HVBUS capacitance.
5	SENSE	MAX20463A: GND Protection Sense Input. Only used for GND short to V_{BAT}. Connect to source (downstream Type-C connector side) of GND at NMOS drain. When using the MAX20463, connect to GND.
6	GDRV	MAX20463A: GND Protection FET Gate Drive Output. Connect to gate of ground-protection NMOS. When using the MAX20463, leave floating.
7	CC2	CC2 Signaling/Output. Connect to downstream Type-C port CC pin.
8	CC1	CC1 Signaling/Output. Connect to downstream Type-C port CC pin.
9	GND	GND. Connect directly to GND.
10, 11	HVBUS	USB Power Supply Output. Connect HVBUS to downstream Type-C port. Connect a 2.2µF ceramic capacitor to ground.
12	BIAS	Filtered Power Supply. Connect a ceramic capacitor to GND for proper operation. See *Detailed Description* and *Applications Information* for special requirements for sustained operation during long-term low-voltage transients

Functional Diagrams

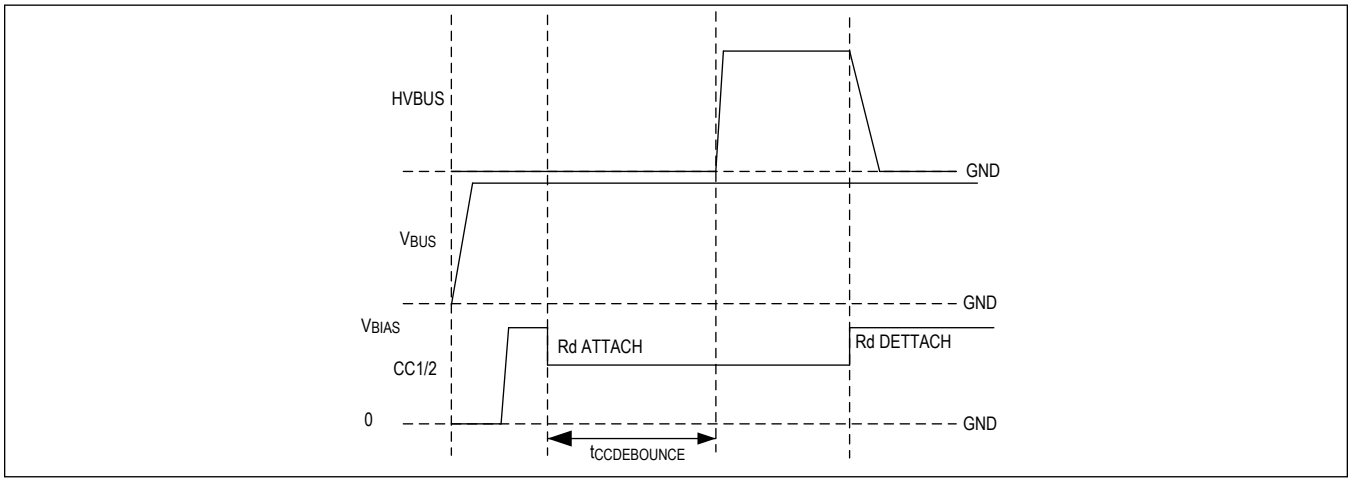
Block Diagram



Short-to-Ground Response



CC Attachment and HVBUS Discharge



Detailed Description

The MAX20463 combines a USB Type-C DFP host emulator with a specialized USB power control/protection switch and an industry-first integrated GND short to V_{BAT} protection circuitry. The IC is capable of DFP charge enumeration at 3.0A and 1.5A.

The device features high-ESD protection on the V_{BUS} and CC pin outputs, as well as high-voltage protection on the power switch output.

The MAX20463 is designed for installation at the end of automotive captive cables. Due to the challenging nature of the transients in this end-of-cable application, combined with the need to minimize end-of-cable capacitance in order to provide best-in-class transient response, the IC contains a unique control scheme and internal BIAS regulator with the ability to power from an external tank capacitor during extended low-voltage transients. During low-voltage excursions on the 5V USB bus input, the high-side USB power protection switch is designed to stay on continuously during CC attach for a duration of time defined by the size of the local tank capacitance on the BIAS pin. For this reason, the upstream USB power supply is always expected to perform USB current limiting as specified in USB-IF and other specifications. The MAX20463 power switch will only open on CC detach, and during extreme conditions when the MAX20463 determines that the upstream power supply is experiencing a failure to limit current according to USB specifications.

The MAX20463 FAULT debounce timer periods have been carefully chosen not to interfere with the fault detection/protection of the Upstream V_{BUS} power source. Therefore, the primary V_{BUS} fault detection/protection responsibility resides with the Upstream source, and the MAX20463 supplements this with its own fault protection.

Power-Up and Enabling

System Enable

Due to the intended end-of-cable application, the MAX20463 does not have a separate master enable pin. System enable/disable is achieved by means of voltage thresholds and hysteresis on the BIAS pin which allow for robust operation and precise calculation of the tank capacitance required in order to achieve the desired transient behavior.

BIAS Pin

All internal supply current is sourced off of the BIAS pin, and the USB power switch will not turn on until BIAS has risen above the BIAS lockout voltage. For more information about selecting the amount of capacitance to install on the BIAS pin, see the *Applications Information* section.

CC1 and CC2 Pins

The CC1 and CC2 pins connect directly to the USB Type-C DFP host emulator analog circuitry and provide the necessary information to detect and maintain a CC attach condition. No external circuitry is used on either CC pin, and both pins can be routed directly to the USB Type-C receptacle. Note that, due to the lack of a Type-C polarity indicator output, the CC1 and CC2 pins can be routed in either polarity (to either side) of the USB Type-C receptacle, allowing for layout optimization on 2-layer PCBs.

Upon attachment of a Type-C device to the USB receptacle, the USB Type-C DFP state machine will check for valid turn-on conditions, and if these are satisfied, will enable the USB 5V power switch between BUS and HVBUS pins according to the USB Type-C specification.

The device will only turn on with a valid Rd pulldown resistor on one of the CC pins. There is no V_{CONN} functionality present.

Control

CC_SEL Pin

The CC_SEL pin selects between two different levels of advertised charging current for the internal USB Type-C DFP emulator to address all options of the USB Type-C specification. This pin is designed to be tied directly to GND for DFP1.5 operation, or tied directly to BIAS for DFP3.0 operation.

Table 1. CC_SEL Configuration

CC_SEL STATE	DFP MODE	NOTE
Tied to GND	DFP_1.5	Remains in DFP_1.5 also during BIAS discharge
Tied to BIAS	DFP_3.0	Changes to DFP_1.5 during BIAS discharge to extend charge duration

Fault Detection and Protection

Overview

The MAX20463 incorporates a fault-detection and protection system designed to work in unison with an upstream protected HVBUS power source. The device's fault detection thresholds and timing parameters have been carefully selected to protect the attached Type-C device, while allowing the upstream HVBUS power source sufficient time to detect the fault condition and enable its protection mechanism.

HVBUS Shorts to GROUND

The HVBUS output is continuously monitored for shorts to ground. If a short persisting longer than 250µs is detected, the HVBUS power switch is opened, mitigating the short fault. The auto-retry logic will attempt to reconnect the power switch every 2 seconds until the short to ground is removed. Two seconds after the short is removed, the HVBUS power switch will be re-enabled, and HVBUS will be restored.

HVBUS Shorts to Battery

The HVBUS output is continuously monitored for shorts to battery, up to 18V. If the MAX20463 overvoltage detection circuit detects that the HVBUS output is greater than approximately 7.5V for a period longer than 1ms, the HVBUS power switch will open. The auto-retry logic will attempt to reconnect the power switch every 2s until the short to battery is removed. Two seconds after the short is removed, and the HVBUS power switch will be re-enabled, and HVBUS will be restored. This functionality is depicted by TOC10 in the Typical Operating Characteristics section.

SHIELD Shorts to Battery

The MAX20463 is the first automotive USB protector to integrate USB shield GND short to V_{BAT} conditions.

USB shield GND short to car battery can occur when a customer's portable device cable is connected to the downstream receptacle, and the far end of this cable falls in to the 12V cigarette lighter receptacle and contacts the 12V center terminal. This condition results in a damaging amount of current flow, with insufficient response time by the cigarette lighter fuse.

The MAX20463 is designed to sense this shield GND short to V_{BAT} condition with the SENSE pin and control an external nMOSFET with the GDRV pin. For more information on this feature, see *Applications Information*.

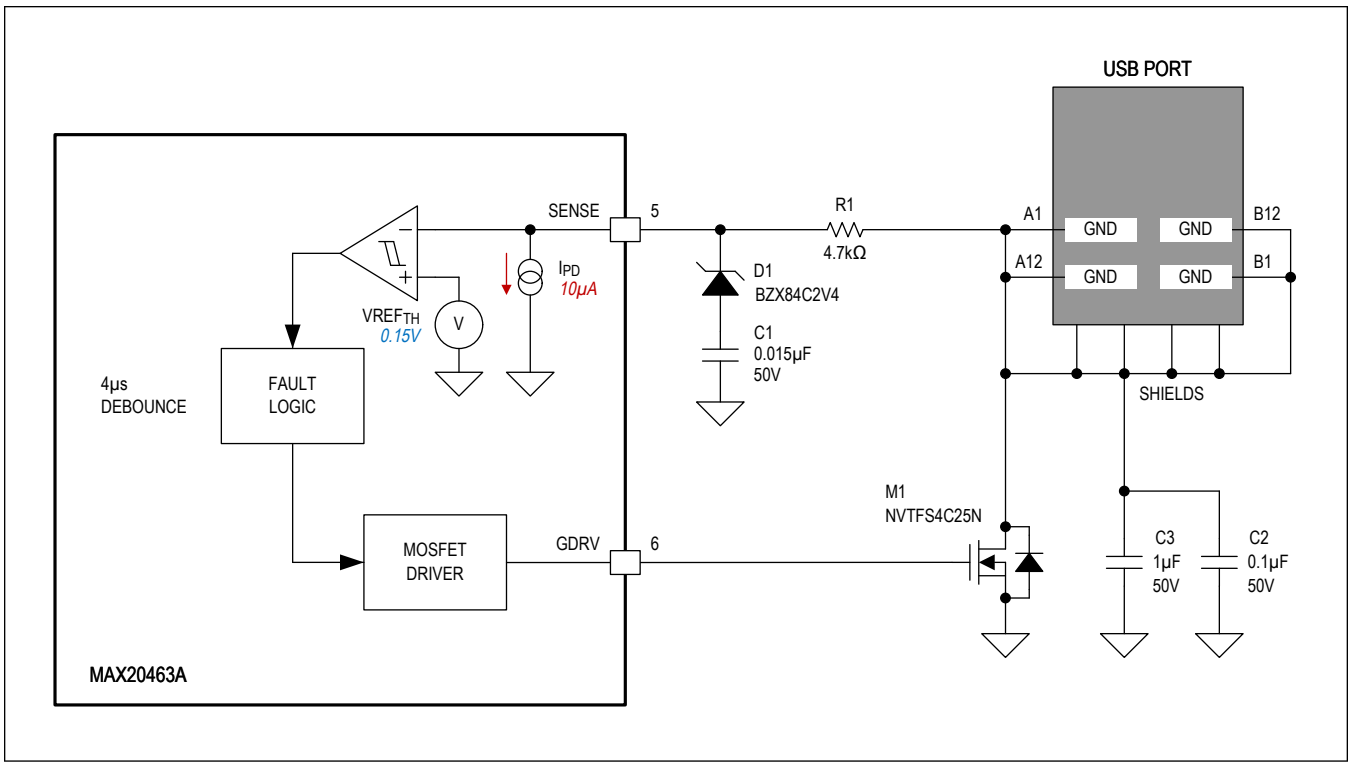


Figure 1. SHIELD Short-to-Battery Protection Circuitry

Figure 1 illustrates the protection circuit for SHIELD shorts-to-battery. The nMOSFET M1 serves to open the path to Ground for the USB cable shield during a short to battery (up to 18V). M1 $R_{DS(ON)}$ is used to develop a small sense voltage proportional to the short-circuit current incurred during the short to battery. Resistor R1 and diode D1 junction capacitance form a low-pass filter to suppress any voltage glitches that could falsely trigger the SHIELD short comparator threshold of 150mV. M1 has been chosen to have a low $R_{DS(ON)}$ and sufficient avalanche rating to limit any ringing that occurs on the SHIELD connection. Capacitor C1, R1, and D1 limit the maximum transient voltage on the SENSE pin to 18V.

See TOC09 in the Typical Operating Characteristics section as a reference for the following explanation of the SHIELD short-to-battery function. When the cable SHIELD contacts V_{BAT}, a large surge current flows through MOSFET M1 to ground. This surge current develops a voltage across M1 $R_{DS(ON)}$, and is sensed through the SENSE pin. When the sense voltage exceeds 150mV, the fault-detection comparator is triggered, reporting the fault condition to the fault logic. After a 4µs debounce period, the GDRV pin output goes low, causing MOSFET M1 to switch off. Because there is a large current flowing through the USB cable when M1 turns off, the cable inductance resonates with capacitor C3 and causes significant ringing on the SHIELD connection. M1 will avalanche to control this peak voltage, and will dissipate some of the energy as heat. When the short is removed, C3 slowly discharges at a constant 10µA, allowing M1 to remain off and cool for several seconds. The fault retry logic will switch MOSFET M1 back on after C3 is discharged to less than 150mV.

HVBUS Current Limit

The output current is normally controlled by the upstream supply. The device integrates two separate current limit thresholds to protect against extreme short to ground or upstream failure conditions. The first threshold is a short to ground protection threshold that will protect against a severe short to ground where the current exceeds approximately 11.5A for 250µs. The second turns the part off if a forward current greater than 4.4A is detected for 50ms in the event that the upstream supply fails to limit the output current. Exceeding either of these thresholds for the specified deglitch time will cause the device to turn off the BUS power switch and wait 2s before enabling again.

Thermal

The MAX20463 die temperature is continuously monitored. Should the die temperature rise above 150ºC for a period longer than 100µs, the MAX20463 will shutdown to protect the device from damage. Once the die temperature falls below 135ºC for a period longer than 100µs, the device will recover.

Table 2. Fault Conditions

MAX20463 FAULT	TRIGGERED BY	DEBOUNCE TIME PRIOR TO ACTION	ACTION	WAIT TIME TO RECOVER AFTER FAULT CONDITION REMOVED
Thermal Fault	Die temp exceeds threshold	100µs $t_{OVT, DEL}$	Reset Type-C state machine (Open HVBUS as a consequence)	t_{RETRY}
Forward Current	HVBUS current exceeds I_{FWD}	50ms t_{FWD}	Reset Type-C state machine (Open HVBUS as a consequence)	t_{RETRY}
HVBUS Short-to-GND	HVBUS current exceeds I_{SHRT}	0.25ms t_{SHRT}	Reset Type-C state machine (Open HVBUS as a consequence)	t_{RETRY}
Ground/ Shield Short-to-Battery	SENSE voltage exceeds $V_{SENSE, RISE}$	4µs t_{SENSE_BLNK}	Reset Type-C state machine (Open HVBUS as a consequence), wait 4µs, set GDRV to 0V	Immediate turn on of the ground switch. Wait t_{RETRY} to enable the Type-C state machine
HVBUS Overvoltage	HVBUS voltage exceeds V_{OV}	1ms t_{OV}	Reset Type-C state machine (Open HVBUS as a consequence)	t_{RETRY}

Applications Information

BIAS Pin Capacitance Selection

Selecting adequate capacitance for the BIAS pin is important for keeping the MAX20463 on during overload and short to ground conditions. In the event of a short to ground on the HVBUS connection at the Type-C connector, the BUS voltage drops as well and similarly affect the upstream supply. The MAX20463 has then lost its source of power and the BIAS voltage will begin to droop as the internal circuitry consumes power to stay on and keep the BUS power switch closed. If enough capacitance is present, then the power switch can stay closed long enough for the upstream power supply to report a FAULT. The amount of time required to stay on depends on the selected upstream supply. If a MAX20037/MAX20038 is the upstream supply, then the MAX20463 must stay on for greater than 16ms during a short to ground for a FAULT to be reported.

To calculate the hold-up time for a chosen BIAS pin capacitor, first determine the DFP current selection, and apply the appropriate formula.

For DFP1.5 (CC_SEL pin = GND):

$$t_{HOLD\_UP} = C_{BIAS} \times \left[\frac{\left[V_{BIAS} - V_{UVBIAS,\,FALL}\right]}{I_{BIAS\_DFP1.5}}\right]$$

For DFP3.0 (CC_SEL pin = BIAS):

$$t_{HOLD\_UP} = C_{BIAS} \times \left[\frac{V_{DFPP,\,FALL} - V_{UVBIAS,\,FALL}}{I_{BIAS\_DFP1.5}} + \frac{V_{BIAS} - V_{DFPP,\,FALL}}{I_{BIAS\_DFP3.0}}\right]$$

SENSE and GDRV Component Selection

If protection against shorting the USB shield to V_{BAT} is required, the external components shown in Figure 1 should be used.

To calculate the Battery to SHIELD short-circuit current that will disable the ground disconnect protection MOSFET, use the following formula:

$$I_{TRIP} = \frac{VREF_{TH} + (R1 x I_{PD})}{R_{M1}}$$

Where $VREF_{TH}$ is the SHIELD short comparator threshold 150mV, I_{PD} is the SENSE pin compensation current 10µA.

Design Example:

$VREF_{TH}$ = 0.15V

I_{PD} = 10µA

R1 = 4.7kΩ

M1_R_{DSON} = 21mΩ

$$I_{TRIP} = \frac{150mV + (4.7k\Omega x 10\,\mu\,A)}{21m\Omega} = \frac{0.197V}{0.021\Omega} = 9.38A$$

If this protection is not required, the SENSE pin can be shorted directly to ground, the GDRV pin can be left unconnected, and the USB shield ground is not isolated from the rest of the PCB ground. All other circuitry mentioned above can be removed.

ESD Protection

The MAX20463 state-of-the-art structures protect against ESD of ±15kV on HVBUS, SENSE, CC1, and CC2 pins. The ESD structures withstand high ESD in all states: normal operation, shutdown, and powered down. The devices are characterized for protection to the limits outline in [[HVBUS, SENSE, CC[1/2] ESD Protection]].

Table 3. HVBUS, SENSE, CC[1/2] ESD Protection

HVBUS, SENSE, CC1, CC2			TYP	UNIT
ESD Protection Level	V_{ESD}	Human Body Model	±2	kV
		IEC 61000-4-2 Air-Gap Discharge, device powered (PV = 5V)	±15	kV
		IEC 61000-4-2 Contact Discharge, device powered (PV = 5V)	±8	kV
		ISO 10605 Air Gap Discharge 330pF, 2kΩ, device powered (PV = 5V)	±25	kV
		ISO 10605 Air Gap Discharge 150pF, 330Ω, device powered (PV = 5V)	±25	kV
		ISO 10605 Air Gap Discharge 330pF, 330Ω, device powered (PV = 5V)	±15	kV
		ISO 10605 Contact Discharge 330pF, 330Ω, device powered (PV = 5V)	±8	kV

Figure 2 shows the Human Body Model, and Figure 3 shows the current waveform it generates when discharged into a low impedance. This model consists of a 100pF capacitor charged to the ESD voltage of interest, which is then discharged into the device through a 1.5kΩ resistor.

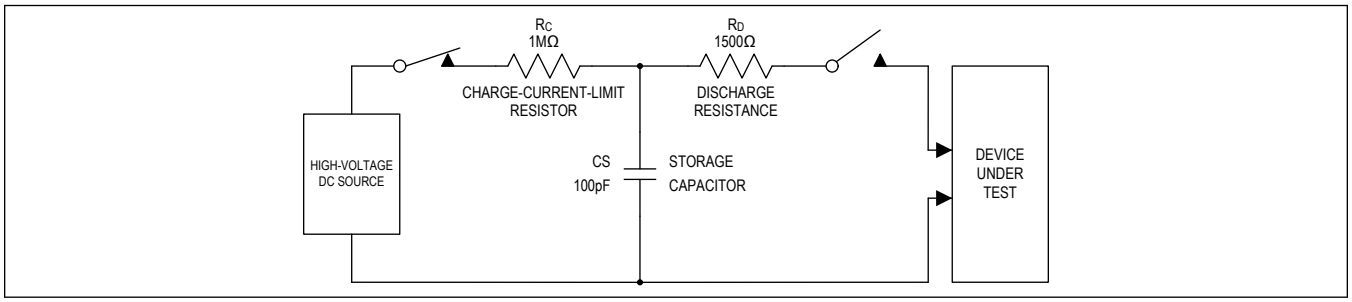


Figure 2. Human Body Test Model

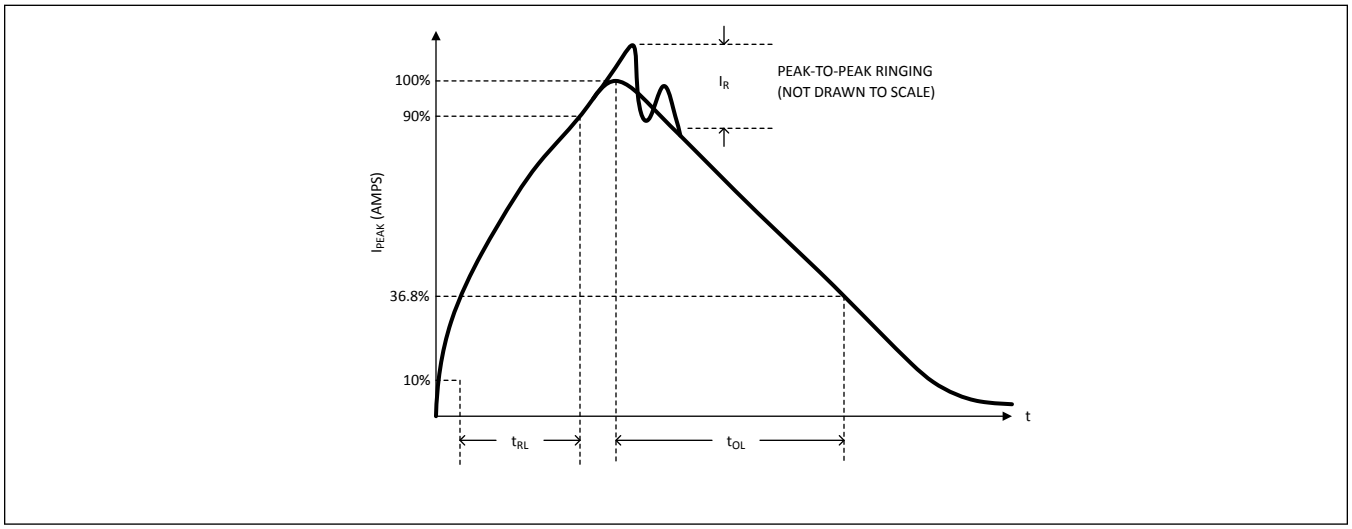


Figure 3. Human Body Current Waveform

The IEC 61000-4-2 standard covers ESD testing and performance of finished equipment. The devices help users design equipment that meet Level 4 of IEC 61000- 4-2. The Human Body Model testing is performed on unpowered devices, while IEC 61000-4-2 is performed while the device is powered. The main difference between tests performed using the Human Body Model and IEC 61000-4-2 is a higher peak current in IEC 61000-4-2. Because series resistance is lower in the IEC 61000-4-2 ESD test model (Figure 4), the ESD withstand voltage measured to this standard is generally lower than that measured using the Human Body Model. Figure 5 shows the current waveform for the ±8kV, IEC 61000-4-2

Level 4, ESD Contact Discharge test. The Air Gap Discharge test involves approaching the device with a charged probe. The Contact Discharge method connects the probe to the device before the probe is energized.

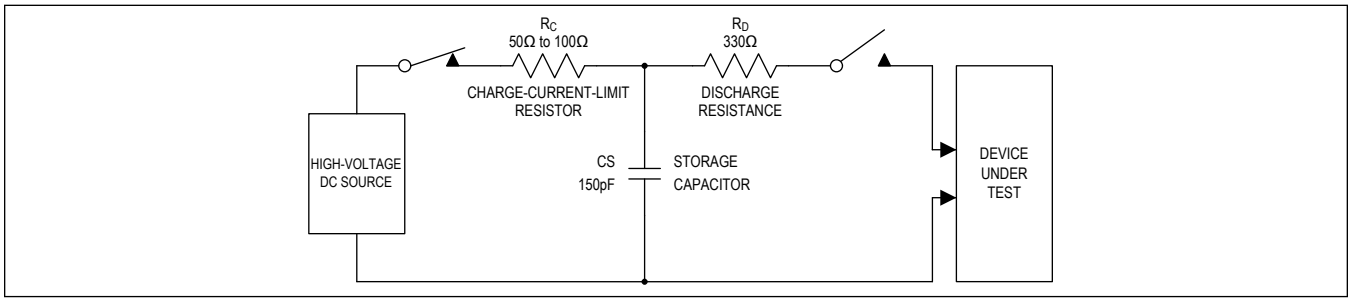


Figure 4. IEC 61000-4-2 ESD Test Model

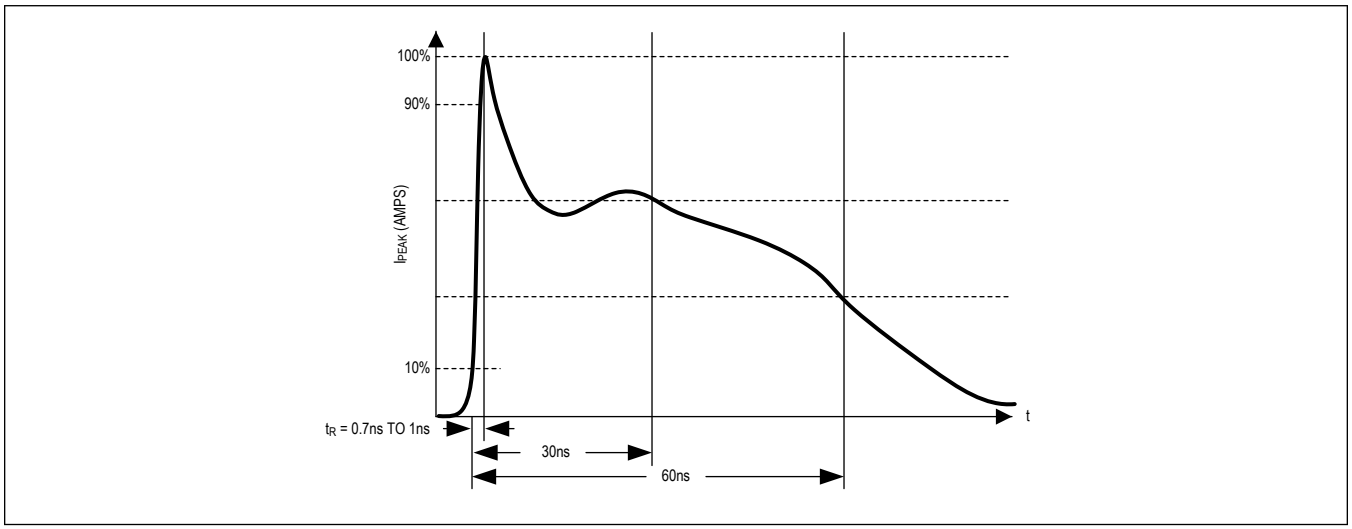
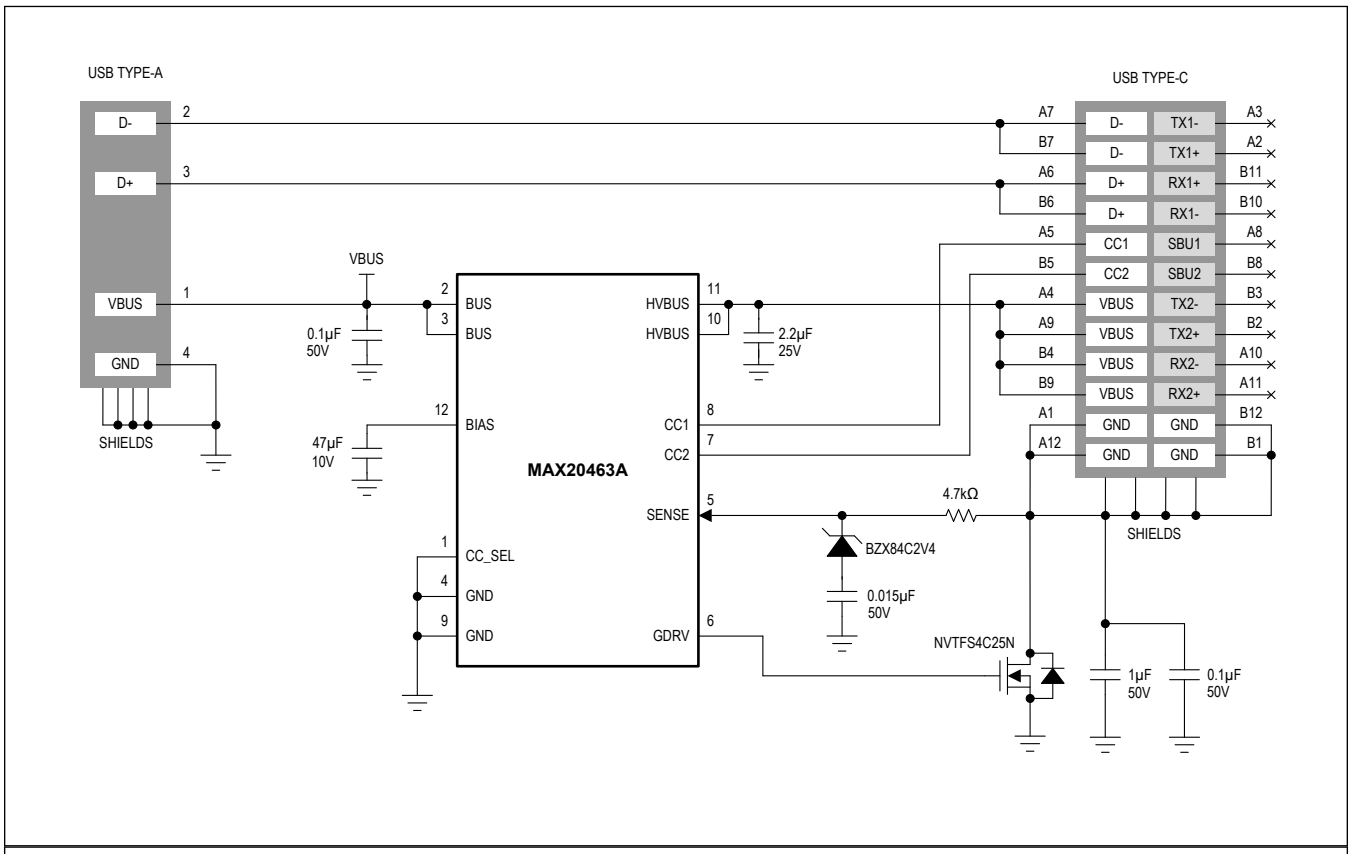
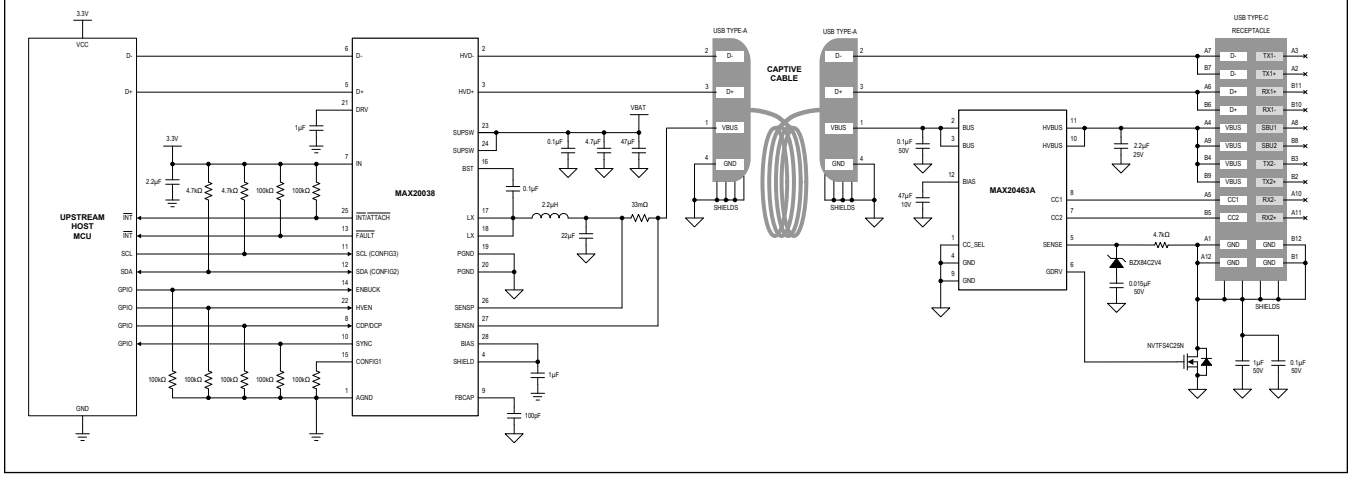


Figure 5. IEC 61000-4-2 ESD Generator Current Waveform

Typical Application Circuits





Ordering Information

PART NUMBER	TEMP RANGE	PIN-PACKAGE	R_P RESET TIMER	SHIELD PROTECTION
MAX20463GTCA/V+	-40°C to +105°C	TDFN-EP-12	2s	No
MAX20463AGTCA/V+				Yes
MAX20463GTCB/V+			50ms	No
MAX20463AGTCB/V+				Yes

/V denotes an automotive-qualified part.

+Denotes a lead(Pb)-free/RoHS-compliant package.

T = Tape and reel.

Revision History

REVISION NUMBER	REVISION DATE	DESCRIPTION	PAGES CHANGED
0	12/18	Initial release	—
1	4/19	Updated Absolute Maximum Ratings, Electrical Characteristics, Typical Operating Characteristics, Detailed Description, Applications Information and Typical Application Circuits.	2, 3–8, 13–15, 18
2	7/19	Updated General Description, Benefits and Features, Electrical Characteristics, Pin Description, Detailed Description and Applications Information.	1, 3, 6, 9, 12, 13, 15, 16
3	10/19	Updated General Description, Electrical Characteristics, Typical Operating Characteristics, Pin Description, Functional Diagrams, Detailed Description, Applications Information, Typical Application Circuits and Ordering Information.	1–19
4	5/22	Updated General Description, Benefits and Features, Typical Operating Characteristics, Fault Conditions, and Ordering Information.	1, 9–11, 15, 16, 21

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