

## MAX20010C/MAX20010D/ MAX20010E

## Automotive Single 6A Step-Down Converters

### General Description

The MAX20010C/MAX20010D/MAX20010E ICs are high-efficiency, synchronous step-down converters that operate with a 3.0V to 5.5V input voltage range and provide a 0.5V to 1.5875V output voltage range. The wide input/output voltage range and the ability to provide up to 6A load current make these ICs ideal for on-board point-of-load and post-regulation applications. The ICs achieve  $\pm 2\%$  output error over load, line, and temperature ranges. The MAX20010D/MAX20010E offers improved transient response.

The ICs feature a 2.2MHz fixed-frequency PWM mode for better noise immunity and load-transient response, and a pulse-frequency modulation mode (skip) for increased efficiency during light-load operation. The 2.2MHz frequency operation allows the use of all-ceramic capacitors and minimizes the solution footprint. The programmable spread-spectrum frequency modulation minimizes radiated electromagnetic emissions. Integrated low  $R_{DS(ON)}$  switches improve efficiency at heavy loads and make the layout a much simpler task with respect to discrete solutions.

The ICs are offered with factory-preset output voltages (see the [Ordering Information](#) for options). The I<sup>2</sup>C interface supports dynamic voltage adjustment with programmable slew rates. Other features include programmable soft-start, overcurrent, and overtemperature protections.

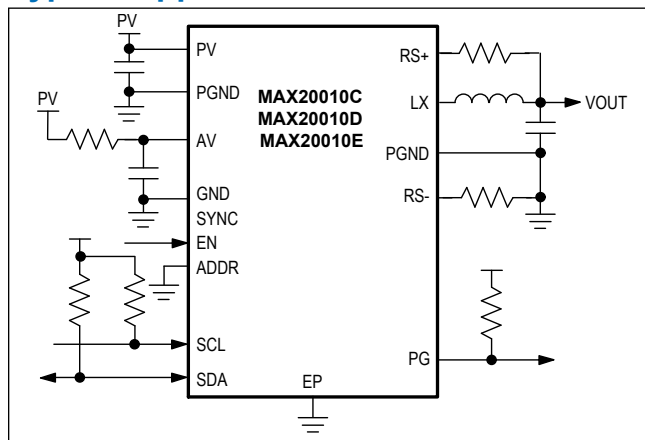
### Applications

- Automotive

### Benefits and Features

- Fully Integrated, Synchronous 6A DC-DC Converter Enables Small Solution Size
  - 3.0V to 5.5V Operating Supply Voltage
- High-Precision Voltage Regulator for Applications Processors
  - $\pm 2\%$  Output-Voltage Accuracy
  - Differential Remote Voltage Sensing
  - I<sup>2</sup>C-Controlled Output Voltage of 0.5V to 1.27V in 10mV Steps, or 0.625V to 1.5875V in 12.5mV Steps
  - Excellent Load-Transient Performance
- Low-Noise Feature Reduces EMI
  - 2.2MHz Operation
  - Spread-Spectrum Option
  - Frequency-Synchronization Input/Output
  - Current-Mode, Forced-PWM, and Skip Operation
- Robust for the Automotive Environment
  - PGOOD Output
  - Overtemperature and Short-Circuit Protection
  - 20-Pin (4mm x 4mm) TQFN with an Exposed Pad
  - 40°C to +125°C Operating Temperature Range
  - AECQ-100 Qualified

### Typical Application Circuits



## Absolute Maximum Ratings

PV, AV to GND ..... -0.3V to +6V  
 ADDR, EN, PG, RS+, RS-, SYNC to GND ..... -0.3V to  $V_{AV} + 0.3V$   
 SDA, SCL to GND ..... -0.3V to +6V  
 GND to PGND ..... -0.3V to +0.3V  
 LX to PGND (*Note 1*) ..... -0.3V to  $V_{PV} + 0.3V$   
 Output Short-Circuit Duration ..... Continuous

Continuous Power Dissipation ( $T_A = +70^\circ\text{C}$ )  
 TQFN (derate 30.3mW/ $^\circ\text{C}$  above  $+70^\circ\text{C}$ ) ..... 2424.2mW  
 Operating Temperature Range .....  $-40^\circ\text{C}$  to  $+125^\circ\text{C}$   
 Junction Temperature .....  $+150^\circ\text{C}$   
 Storage Temperature Range .....  $-65^\circ\text{C}$  to  $+150^\circ\text{C}$   
 Lead Temperature (soldering, 10s) .....  $+300^\circ\text{C}$   
 Soldering Temperature (reflow) .....  $+260^\circ\text{C}$

**Note 1:** Self-protected against transient voltages exceeding these limits for  $\leq 50\text{ns}$  under normal operation and loads up to the maximum rating output current.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

## Package Information

### 20 TQFN-EP

|                     |                           |
|---------------------|---------------------------|
| Package Code        | T2044+4C                  |
| Outline Number      | <a href="#">21-100172</a> |
| Land Pattern Number | <a href="#">90-0409</a>   |

### 20 SW TQFN-EP

|   |                           |
|---|---------------------------|
| Package Code                                | T2044Y+4C                 |
| Outline Number                              | <a href="#">21-100068</a> |
| Land Pattern Number                         | <a href="#">90-0409</a>   |
| <b>THERMAL RESISTANCE, FOUR-LAYER BOARD</b> |                           |
| Junction to Ambient ( $\theta_{JA}$ )       | $33^\circ\text{C/W}$      |
| Junction to Case ( $\theta_{JC}$ )          | $2^\circ\text{C/W}$       |

For the latest package outline information and land patterns (footprints), go to [www.maximintegrated.com/packages](http://www.maximintegrated.com/packages). Note that a "+", "#", or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

Package thermal resistances were obtained using the method described in JEDEC specification JESD51-7, using a four-layer board. For detailed information on package thermal considerations, refer to [www.maximintegrated.com/thermal-tutorial](http://www.maximintegrated.com/thermal-tutorial).

## Electrical Characteristics

( $V_{PV} = V_{AV} = 5.0V$ ,  $T_A = T_J = -40^\circ\text{C}$  to  $+125^\circ\text{C}$ , unless otherwise noted. Typical values are at  $T_A = +25^\circ\text{C}$  under normal conditions, unless otherwise noted.) (*Note 2*)

| PARAMETER               | SYMBOL   | CONDITIONS                                    |                            | MIN | TYP  | MAX | UNITS         |
|-------------------------|----------|---|----------------------------|-----|------|-----|---------------|
| Supply Voltage Range    | $V_{IN}$ | Fully operational                             |                            | 3.0 |      | 5.5 | V             |
| Undervoltage Lockout    | UVLO     | Rising  |                            |     | 2.85 | 3   | V             |
|                         |          | Falling                                       |                            |     | 2.55 |     |               |
| Shutdown Supply Current | $I_{IN}$ | EN = low                                      | $T_A = +25^\circ\text{C}$  |     | 2.5  | 5   | $\mu\text{A}$ |
|                         |          |   | $T_A = +125^\circ\text{C}$ |     | 4.5  |     |               |
| Supply Current          | $I_{IN}$ | EN = high, $I_{OUT} = 0\text{mA}$ , skip mode |                            |     | 300  |     | $\mu\text{A}$ |

## Electrical Characteristics (continued)

( $V_{PV} = V_{AV} = 5.0V$ ,  $T_A = T_J = -40^{\circ}C$  to  $+125^{\circ}C$ , unless otherwise noted. Typical values are at  $T_A = +25^{\circ}C$  under normal conditions, unless otherwise noted.) ([Note 2](#))

| PARAMETER                               | SYMBOL           | CONDITIONS   |                                   | MIN  | TYP  | MAX   | UNITS  |
|---|------------------|--|-----------------------------------|------|------|-------|--------|
| PWM Switching Frequency                 | f <sub>SW</sub>  | Internally generated   |                                   | 2.0  | 2.2  | 2.4   | MHz    |
| Spread Spectrum                         |                  | CONFIG.SS = 1  |                                   | +3   |      |       | %      |
| Voltage Accuracy                        | V <sub>OUT</sub> | I <sub>LOAD</sub> = 0A to 6A, 3.0V ≤ V <sub>PV</sub> ≤ 5.5V                  | 0.80V to 1.5875V                  | -2   | +2   |       | %      |
|   |                  | I <sub>LOAD</sub> = 0A to 6A, 3.0V ≤ V <sub>PV</sub> ≤ 5.5V                  | 0.50V to 0.79V                    | -16  | +21  |       | mV     |
| pMOS On-Resistance                      |                  | V <sub>PV</sub> = V <sub>AV</sub> = 5V, I <sub>LX</sub> = 1A                 |                                   | 31   |      | 55    | mΩ     |
| nMOS On-Resistance                      |                  | V <sub>PV</sub> = V <sub>AV</sub> = 5V, I <sub>LX</sub> = 1A                 |                                   | 18   |      | 31    | mΩ     |
| pMOS Current-Limit Threshold            |                  |  |                                   | 7.76 | 9.70 | 11.64 | A      |
| nMOS Zero Crossing Threshold            |                  |  |                                   | 60   |      |       | mA     |
| LX Leakage Current                      |                  | V <sub>PV</sub> = V <sub>AV</sub> = 6V, LX = PGND or PV                      | T <sub>A</sub> = +25°C            | 0.5  |      | 5     | μA     |
|   |                  |  | T <sub>A</sub> = +125°C           | 4    |      |       |        |
| Duty-Cycle Range                        |                  | PWM mode   |                                   |      |      | 100   | %      |
| Minimum On-Time                         |                  |  |                                   | 36   |      | 75    | ns     |
| THERMAL OVERLOAD                        |                  |  |                                   |      |      |       |        |
| Thermal-Shutdown Temperature            |                  | T <sub>J</sub> rising  |                                   | 165  |      |       | °C     |
| Hysteresis                              |                  |  |                                   | 15   |      |       | °C     |
| POWER-GOOD OUTPUT (PG)                  |                  |  |                                   |      |      |       |        |
| PG Overvoltage (OV) Threshold, Rising   |                  | Percentage of nominal output, output voltage rising, blanked during slewing  | 0.5V < V <sub>OUT</sub> < 0.79V   | 104  | 108  | 112   | %      |
|   |                  |  | 0.8V < V <sub>OUT</sub> < 1.5875V | 105  | 108  | 111   |        |
| PG Undervoltage (UV) Threshold, Falling |                  | Percentage of nominal output, output voltage falling, blanked during slewing | 0.5V < V <sub>OUT</sub> < 0.79V   | 88   | 92   | 96    | %      |
|   |                  |  | 0.8V < V <sub>OUT</sub> < 1.5875V | 89   | 92   | 95    |        |
| Active Timeout Period                   |                  |  |                                   | 256  |      |       | Clocks |
| UV/OV Propagation Delay                 |                  |  |                                   | 5    |      |       | μs     |
| PG Output High-Leakage Current          |                  |  |                                   |      |      | 1     | μA     |
| PG Output Low Level                     |                  | 3.0V ≤ V <sub>PV</sub> ≤ 5.5V, 3.0V ≤ V <sub>AV</sub> ≤ 5.5V, sinking -2mA   |                                   |      |      | 0.2   | V      |
| DIGITAL INPUTS (SYNC, EN, ADDR)         |                  |  |                                   |      |      |       |        |
| Input High Level                        | V <sub>IH</sub>  |  |                                   | 1.5  |      |       | V      |
| Input Low Level                         | V <sub>IL</sub>  |  |                                   |      |      | 0.5   | V      |

## Electrical Characteristics (continued)

( $V_{PV} = V_{AV} = 5.0V$ .  $T_A = T_J = -40^{\circ}C$  to  $+125^{\circ}C$ , unless otherwise noted. Typical values are at  $T_A = +25^{\circ}C$  under normal conditions, unless otherwise noted.) ([Note 2](#))

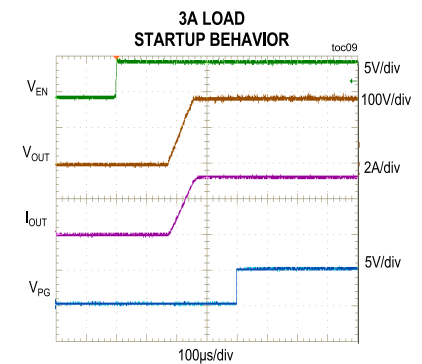
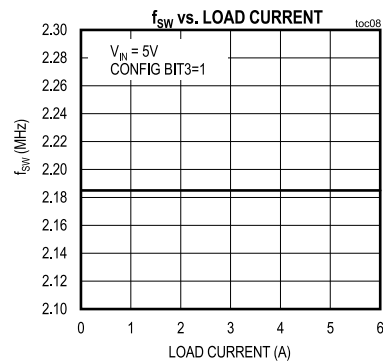
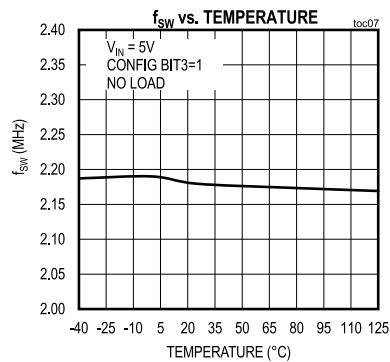
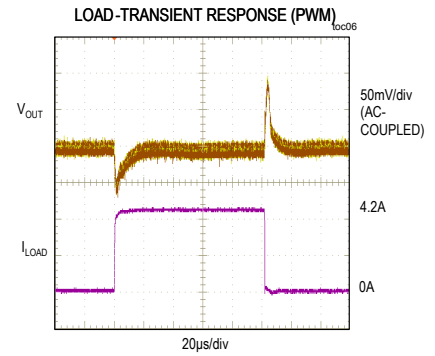
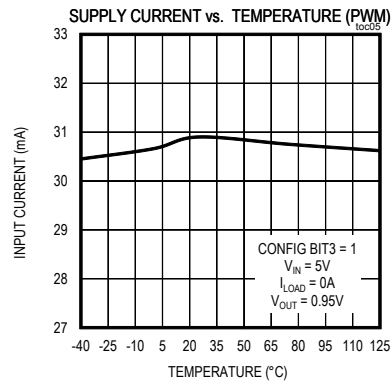
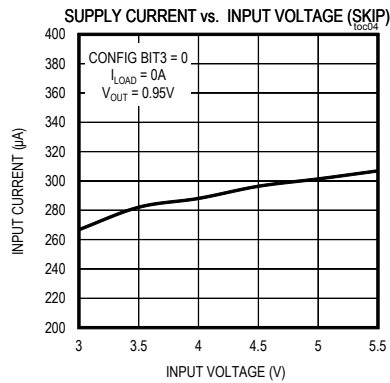
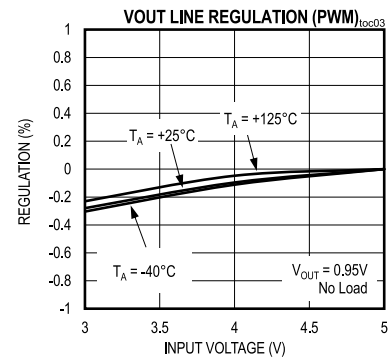
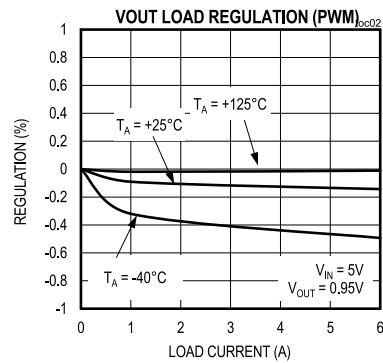
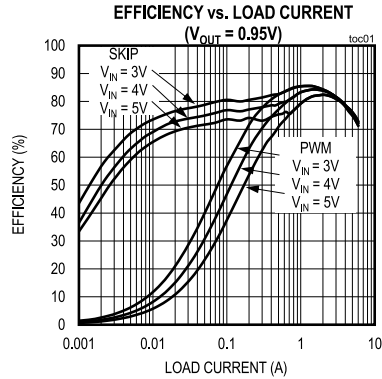
| PARAMETER                        | SYMBOL        | CONDITIONS   | MIN | TYP | MAX | UNITS     |
|----------------------------------|---------------|--|-----|-----|-----|-----------|
| Input Hysteresis                 |               |  |     | 0.1 |     | V         |
| EN Input Leakage Current         |               | $0V \leq V_{PV} \leq 5.5V$ ,<br>$0V \leq V_{AV} \leq 5.5V$ |     | 0.1 |     | $\mu A$   |
| Enable Time                      |               | Rising EN to beginning of soft-start                       |     | 140 |     | $\mu s$   |
| SYNC Input Pulldown              |               |  |     | 100 | 150 | $k\Omega$ |
| SYNC Input Frequency Range       |               |  | 1.8 |     | 2.6 | MHz       |
| <b>SYNC OUTPUT</b>               |               |  |     |     |     |           |
| Output Low                       | $V_{OL}$      | $I_{SINK} = 3mA$   |     |     | 0.4 | V         |
| Output High                      | $V_{OH}$      | $V_{PV} = V_{AV} = 5.0V$ , $I_{SOURCE} = 3mA$              | 4.2 |     |     | V         |
| <b>DIGITAL INPUTS (SDA, SCL)</b> |               |  |     |     |     |           |
| Input High Level                 | $V_{IH\_I2C}$ |  | 1.3 |     |     | V         |
| Input Low Level                  | $V_{IL\_I2C}$ |  |     |     | 0.5 | V         |
| Input Hysteresis                 |               |  |     | 0.1 |     | V         |
| Input Leakage Current            |               | $0V \leq V_{PV} \leq 5.5V$ ,<br>$0V \leq V_{AV} \leq 5.5V$ |     | 0.1 |     | $\mu A$   |
| <b>I<sup>2</sup>C INTERFACE</b>  |               |  |     |     |     |           |
| Clock Frequency                  | $f_{SCL}$     |  |     |     | 3.4 | MHz       |
| Setup Time (Repeated) START      | $t_{SU:STA}$  | ( <a href="#">Note 3</a> )                                 | 160 |     |     | ns        |
| Hold Time (Repeated) START       | $t_{HD:STA}$  | ( <a href="#">Note 3</a> )                                 | 160 |     |     | ns        |
| SCL Low Time                     | $t_{LOW}$     | ( <a href="#">Note 3</a> )                                 | 160 |     |     | ns        |
| SCL High Time                    | $t_{HIGH}$    | ( <a href="#">Note 3</a> )                                 | 60  |     |     | ns        |
| Data Setup Time                  | $t_{SU:DAT}$  | ( <a href="#">Note 3</a> )                                 | 50  |     |     | ns        |
| Data Hold Time                   | $t_{HD:DAT}$  | ( <a href="#">Note 3</a> )                                 | 0   |     | 70  | ns        |
| Setup Time for STOP Condition    | $t_{SU:STO}$  | ( <a href="#">Note 3</a> )                                 | 160 |     |     | ns        |
| Spike Suppression                |               | ( <a href="#">Note 3</a> )                                 |     | 20  |     | ns        |
| SDA Output Low                   | $V_{OL\_SDA}$ | $I_{SINK} = 13mA$  |     |     | 0.4 | V         |

**Note 2:** All units are 100% production tested at  $T_A = +25^{\circ}C$ . All temperature limits are guaranteed by design.

**Note 3:** Guaranteed by design. Not production tested.

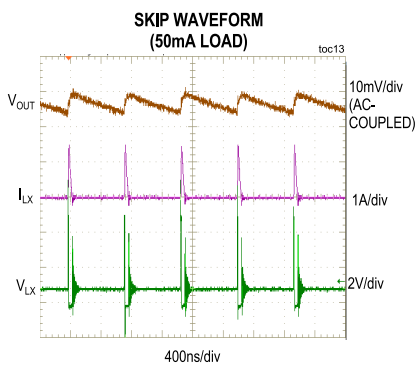
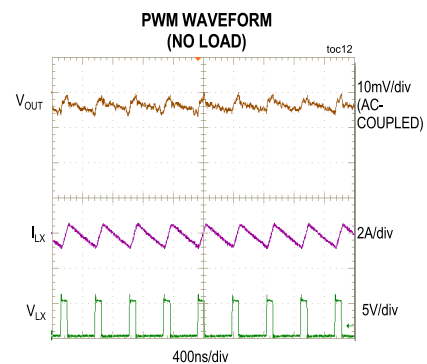
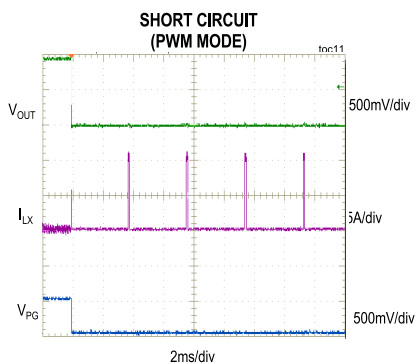
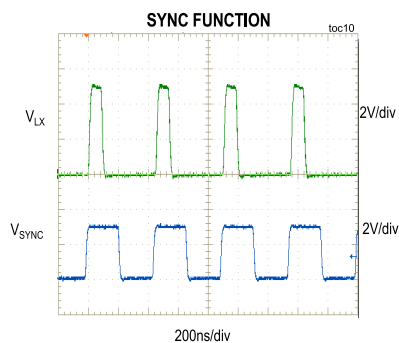
## Typical Operating Characteristics

( $T_A = +25^\circ\text{C}$ , unless otherwise noted.)

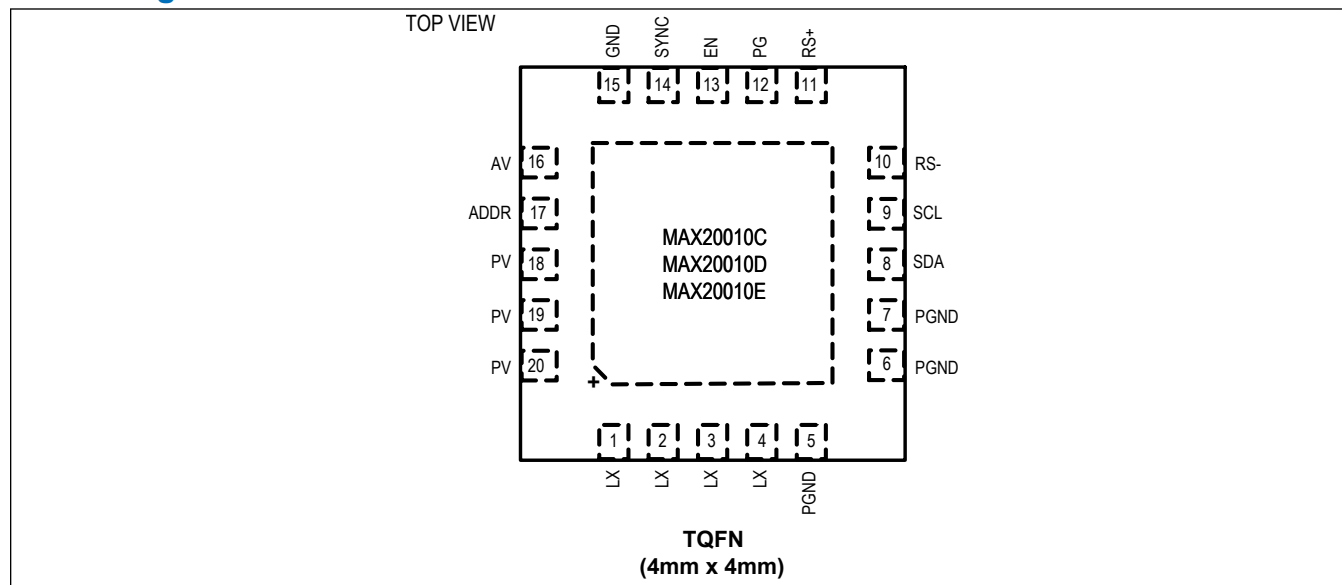


## Typical Operating Characteristics (continued)

( $T_A = +25^\circ\text{C}$ , unless otherwise noted.)



## Pin Configuration



## Pin Description

| PIN   | NAME | FUNCTION   |
|-------|------|--|
| 1–4   | LX   | Inductor Connection. Connect LX to the switched side of the inductor. Connect all LX pins together.  |
| 5–7   | PGND | Power Ground. Connect all PGND pins together.  |
| 8     | SDA  | I <sup>2</sup> C Data I/O  |
| 9     | SCL  | I <sup>2</sup> C Clock Input   |
| 10    | RS-  | Buck Regulator Remote Voltage-Sense Negative Input   |
| 11    | RS+  | Buck Regulator Remote Voltage-Sense Positive Input   |
| 12    | PG   | Open-Drain Power-Good Output. This output remains low for 120μs after the output has reached its regulation level (see the <a href="#">Electrical Characteristics</a> table). To obtain a logic signal, pull up PG with an external resistor.  |
| 13    | EN   | Active-High Enable Input. When EN is high, the device enters soft-start. When EN is low, the device enters soft-shutdown.  |
| 14    | SYNC | SYNC I/O. When configured as an input, connect SYNC to GND or leave unconnected to enable skipmode operation under light loads. Connect SYNC to AV or an external clock to enable fixed-frequency, forced-PWM (FPWM) mode operation. When configured as an output, connect SYNC to other devices' SYNC inputs. |
| 15    | GND  | Analog Ground  |
| 16    | AV   | Analog Input Supply. Filter AV using a 100Ω resistor from PV and a 1μF ceramic capacitor from AV to GND.   |
| 17    | ADDR | I <sup>2</sup> C Address Select. See the <a href="#">Ordering Information</a> table for default I <sup>2</sup> C settings.   |
| 18–20 | PV   | Power Input Supply. Connect a 4.7μF or larger ceramic capacitor from PV to PGND. Connect all PV pins together.   |
| -     | EP   | Exposed Pad. Connect EP to ground. Connecting the exposed pad to ground does not remove the requirement for proper ground connections to PGND. The exposed pad is attached with epoxy to the substrate of the die, making it an excellent path to remove heat from the IC.                                     |

## Detailed Description

The MAX20010C/MAX20010D/MAX20010E ICs are high-efficiency, synchronous step-down converters that operate with a 3.0V to 5.5V input voltage range and provide a 0.5V to 1.5875V output voltage range. The ICs deliver up to 6A of load current and achieve  $\pm 2\%$  output error over load, line, and temperature ranges. The MAX20010D/MAX20010E offers improved transient performance.

Optional spread-spectrum frequency modulation minimizes radiated electromagnetic emissions due to the switching frequency. The I<sup>2</sup>C-programmable I/O (SYNC) enables system synchronization.

Integrated low  $R_{DS(ON)}$  switches help improve efficiency at heavy loads and make the layout a much simpler task with respect to discrete solutions. The ICs are offered with a factory-preset output voltage that is dynamically adjustable through the I<sup>2</sup>C interface. The output voltage can be set to any desired value between 0.5V and 1.27V in 10mV steps, and between 0.625V and 1.5875V in 12.5mV steps.

Additional features include adjustable soft-start, power-good delay, DVS rate, overcurrent, and overtemperature protections (see [Figure 1](#)).



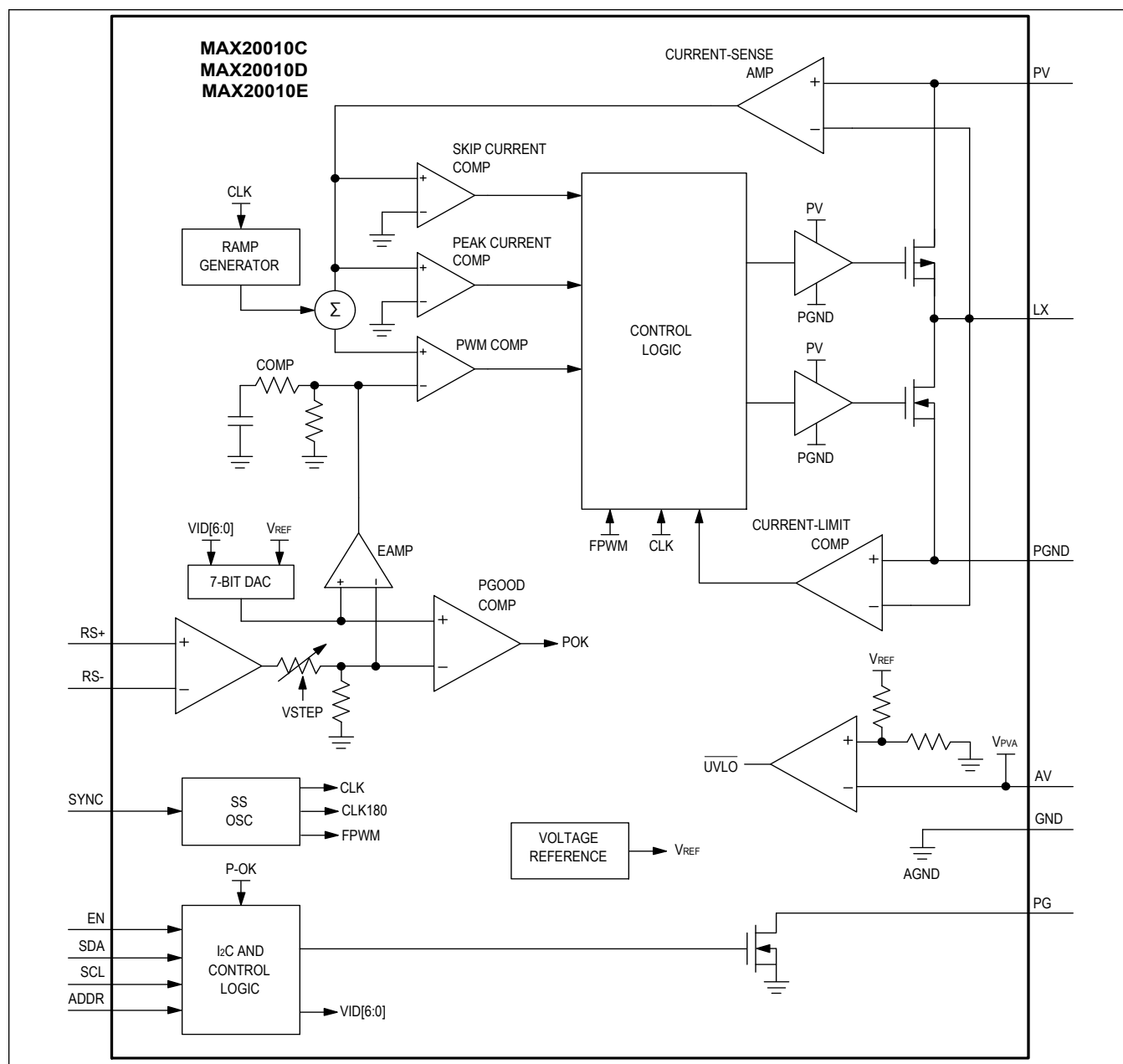


Figure 1. Internal Block Diagram

## I<sup>2</sup>C Interface

The ICs feature an I<sup>2</sup>C, 2-wire serial interface consisting of a serial-data line (SDA) and serial-clock line (SCL). SDA and SCL facilitate communication between the ICs and the master at clock rates up to 3.4MHz. The master, typically a microcontroller, generates SCL and initiates data transfer on the bus. [Figure 2](#) shows the 2-wire interface timing diagram. A master device communicates with the ICs by transmitting the proper address followed by the data word. Each transmit sequence is framed by a START (S) or Repeated START (Sr) condition and a STOP (P) condition. Each word transmitted over the bus is 8 bits long and is always followed by an acknowledge clock pulse.

The SDA line operates as both an input and an open-drain output. A pullup resistor greater than 500Ω is required on the

SDA bus. The SCL line operates as an input only. A pullup resistor greater than  $500\Omega$  is required on SCL if there are multiple masters on the bus, or if the master in a single-master system has an open-drain SCL output. Series resistors in line with SDA and SCL are optional. The SCL and SDA inputs suppress noise spikes to assure proper device operation even on a noisy bus.

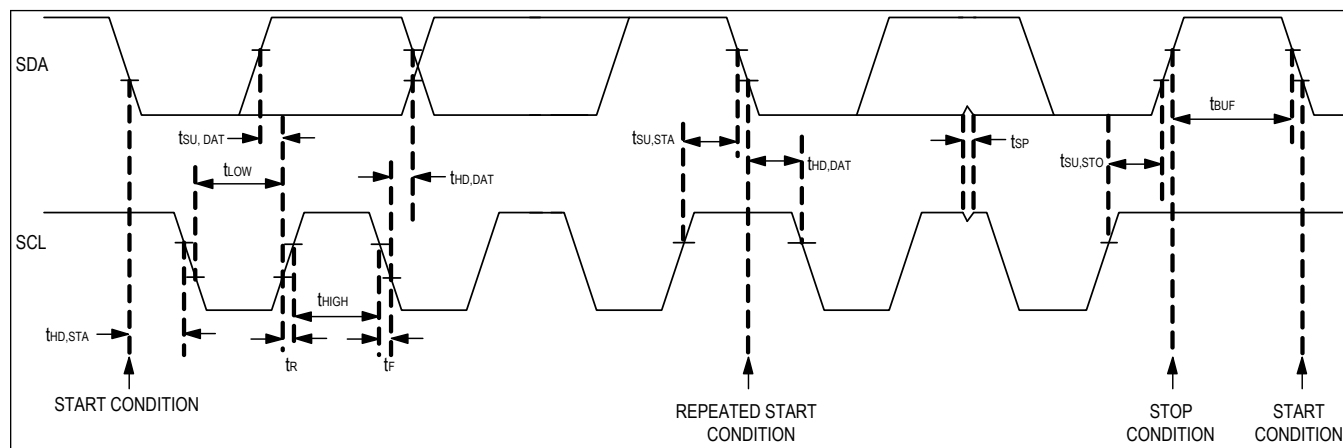


Figure 2. I<sup>2</sup>C Timing Diagram

## Bit Transfer

One data bit is transferred during each SCL cycle. The data on SDA must remain stable during the high period of the SCL pulse. Changes in SDA while SCL is high are control signals (see the [START and STOP Conditions](#) section). SDA and SCL idle high when the I<sup>2</sup>C bus is not busy.

## START and STOP Conditions

A master device initiates communication by issuing a START condition. A START condition is a high-to-low transition on SDA with SCL high. A STOP condition is a low-to-high transition on SDA while SCL is high ([Figure 3](#)).

A START (S) condition from the master signals the beginning of a transmission to the IC. The master terminates transmission, and frees the bus, by issuing a STOP (P) condition. The bus remains active if a Repeated START (Sr) condition is generated instead of a STOP condition.

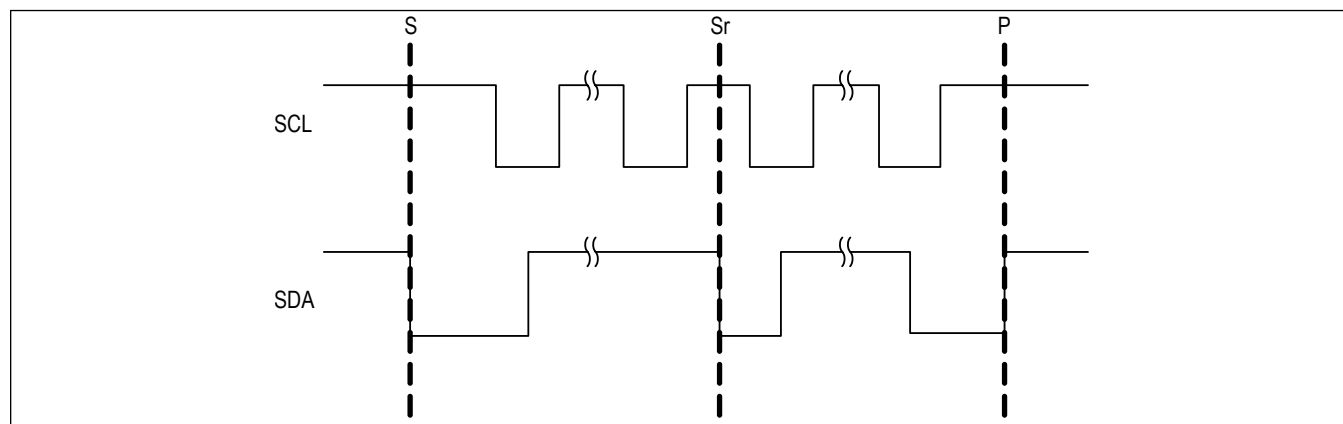


Figure 3. START, STOP, and Repeated START Conditions

## Early STOP Condition

The ICs recognize a STOP condition at any point during data transmission, except if the STOP condition occurs in the

same high pulse as a START condition.

### Clock Stretching

In general, the clock-signal generation for the I<sup>2</sup>C bus is the responsibility of the master device. The I<sup>2</sup>C specification allows slow slave devices to alter the clock signal by holding down the clock line. The process in which a slave device holds down the clock line is typically called clock stretching. The ICs do not use any form of clock stretching to hold down the clock line.

### I<sup>2</sup>C General Call Address

The ICs do not implement the I<sup>2</sup>C specification's "general call address." If the IC sees the general call address (0b0000\_0000), it does not issue an acknowledge.

### Slave Address

Once the device is enabled, the I<sup>2</sup>C slave address is defined as the 7 most significant bits (MSBs) followed by the R/W bit which completes the 8-bit I<sup>2</sup>C transaction. Set the R/W bit to 0 to configure the IC to write mode. Set the R/W bit to 1 to configure the IC to read mode. The address is the first byte of information sent to the device after the START condition. The ADDR pin (A0) can be used to change the default I<sup>2</sup>C slave address. See [Table 1](#) for the 7-bit I<sup>2</sup>C slave addresses and the 8-bit Write/Read addresses.

### Acknowledge

The acknowledge bit (ACK) is a clocked 9th bit that the ICs use to handshake receipt each byte of data ([Figure 4](#)). The device pulls down SDA during the master-generated 9th clock pulse. The SDA line must remain stable and low during the high period of the acknowledge clock pulse. Monitoring ACK allows for detection of unsuccessful data transfers. An unsuccessful data transfer occurs if a receiving device is busy or if a system fault has occurred. In the event of an unsuccessful data transfer, the bus master can reattempt communication.

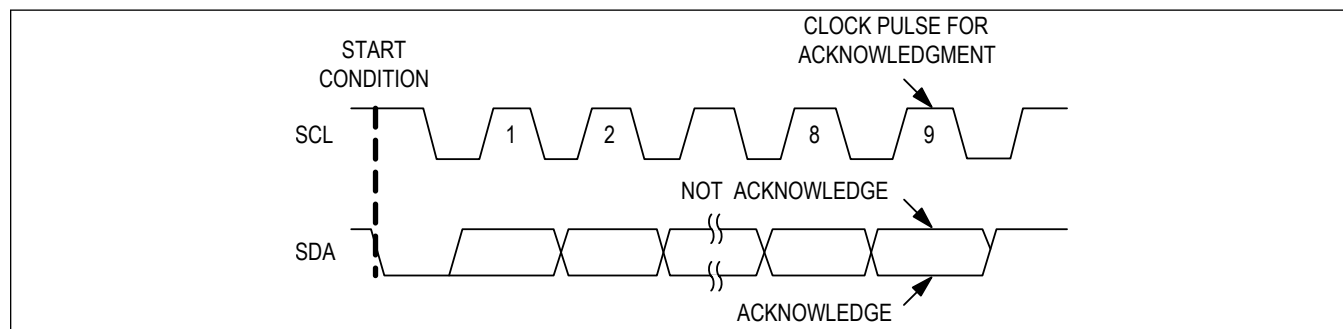


Figure 4. Acknowledge Condition

**Table 1. I<sup>2</sup>C Slave Addresses**

| A6 | A5 | A4 | A3 | A2* | A1* | A0 | I <sup>2</sup> C ADDR | WRITE | READ |
|----|----|----|----|-----|-----|----|-----------------------|-------|------|
| 0  | 1  | 1  | 1  | 0   | 0   | 0  | 0x38                  | 0x70  | 0x71 |
| 0  | 1  | 1  | 1  | 0   | 0   | 1  | 0x39                  | 0x72  | 0x73 |
| 0  | 1  | 1  | 1  | 0   | 1   | 0  | 0x3A                  | 0x74  | 0x75 |
| 0  | 1  | 1  | 1  | 0   | 1   | 1  | 0x3B                  | 0x76  | 0x77 |
| 0  | 1  | 1  | 1  | 1   | 0   | 0  | 0x3C                  | 0x78  | 0x79 |
| 0  | 1  | 1  | 1  | 1   | 0   | 1  | 0x3D                  | 0x7A  | 0x7B |
| 0  | 1  | 1  | 1  | 1   | 1   | 0  | 0x3E                  | 0x7C  | 0x7D |
| 0  | 1  | 1  | 1  | 1   | 1   | 1  | 0x3F                  | 0x7E  | 0x7F |

\*See the [Ordering Information](#) table for the 7-bit default settings for ADDR=0.

### Write Data Format

A write to the device includes:

- Transmission of a START condition
- Slave address with the write bit set to 0
- 1 byte of data to the register address
- 1 byte of data to the command register
- STOP condition

([Figure 5](#) illustrates the proper format for one frame)

### Read Data Format

A read from the device includes:

- Transmission of a START condition
- Slave address with the write bit set to 0
- 1 byte of data to the register address
- Restart condition
- Slave address with the read bit set to 1
- 1 byte of data to the command register
- STOP condition

([Figure 5](#) illustrates the proper format for one frame)

### Writing to a Single Register

[Figure 6](#) shows the protocol for the I<sup>2</sup>C master device to write 1 byte of data to the ICs. This protocol is the same as the SMBus specification's "write byte" protocol.

The "write byte" protocol is as follows:

1. Master sends a START command (S).
2. Master sends the 7-bit slave address followed by a write bit (R/W = 0).
3. Addressed slave asserts an acknowledge (A) by pulling SDA low.
4. Master sends an 8-bit register pointer.
5. Slave acknowledges the register pointer.
6. Master sends a data byte.
7. Slave updates with the new data.
8. Slave acknowledges or not acknowledges the data byte. The next rising edge on SDA loads the data byte into its target register and the data becomes active.
9. Master sends a STOP condition (P) or a Repeated START condition (Sr).

### Writing Multiple Bytes Using Register-Data Pairs

[Figure 7](#) shows the protocol for the I<sup>2</sup>C master device to write multiple bytes to the ICs using register-data pairs. This protocol allows the I<sup>2</sup>C master device to address the slave only once and then send data to multiple registers in a random order. Registers can be written continuously until the master issues a STOP condition.

The "multiple byte register-data pair" protocol is as follows:

1. Master sends a START command.
2. Master sends the 7-bit slave address followed by a write bit.
3. Addressed slave asserts an acknowledge by pulling SDA low.
4. Master sends an 8-bit register pointer.
5. Slave acknowledges the register pointer.
6. Master sends a data byte.
7. Slave acknowledges the data byte. The next rising edge on SDA loads the data byte into its target register and the data becomes active.
8. Steps 4–7 are repeated as many times as the master requires.
9. Master sends a STOP condition. During the rising edge of the stop-related SDA edge, the data byte that was

previously written is loaded into the target register and becomes active.

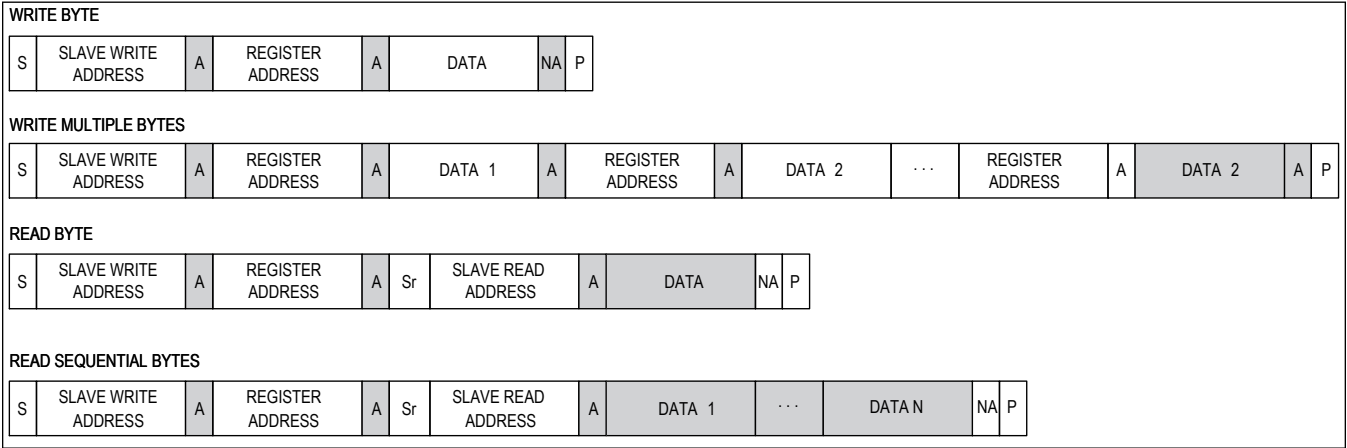


Figure 5. Data Format of I<sup>2</sup>C Interface

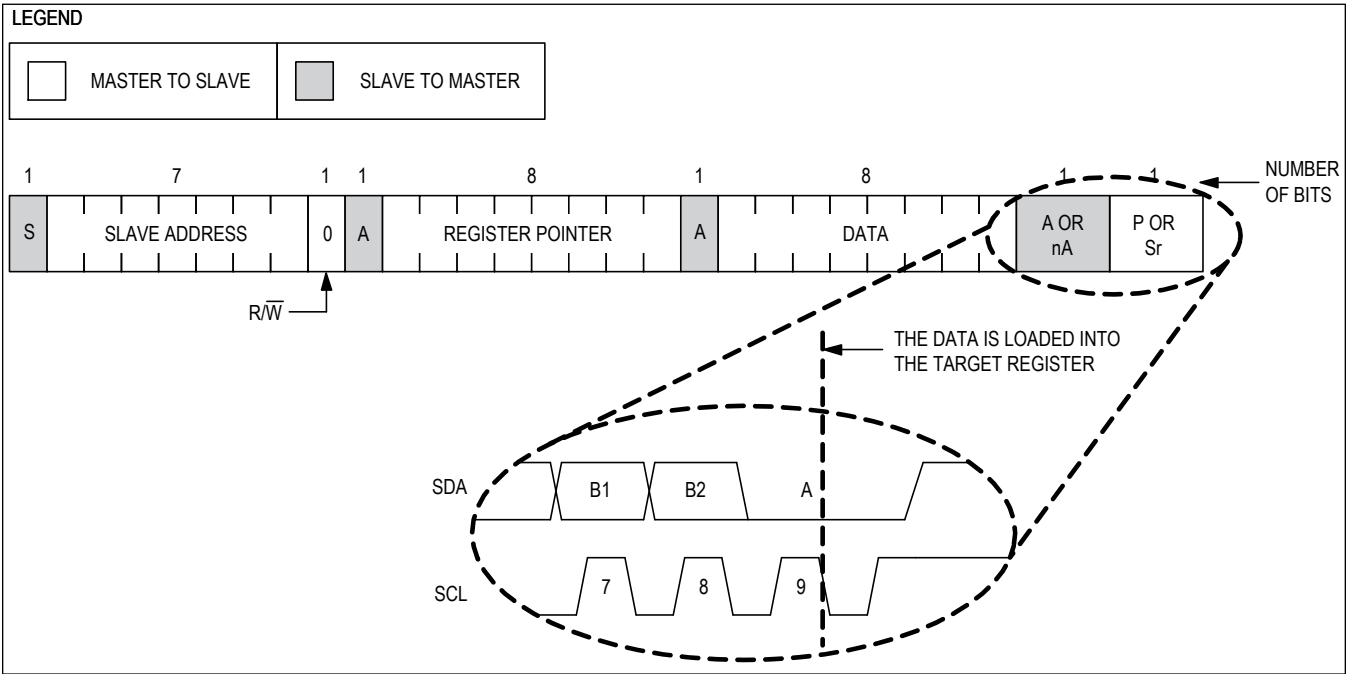


Figure 6. Write Byte Format

PG Output

The ICs feature an open-drain PGOOD output that asserts low when the output voltage exceeds the PG\_OV and PG\_UV thresholds. PG remains low for a fixed timeout period after the output is within the regulation window. Connect PG to a logic supply using a pullup resistor.

Soft-Start

The ICs include a programmable startup fixed soft-start rate. Soft-start time limits startup inrush current by forcing the output voltage to ramp up towards its regulation point.

**Enable (EN)**

EN high triggers soft-start and EN low starts soft-shutdown sequence. When EN is used to shut down the buck output, it should stay low for a minimum of 1ms for the soft-shutdown sequence to complete in order to guarantee that the PG pin deassertion does not occur immediately when EN goes high. If the PG pin is unused or early deassertion of the PG pin does not cause a system issue, then there is no restriction on the EN pin timing.

**Shutdown**

During shutdown, the output voltage is ramped down at the 5.5mV/μs slew rate. Once the controlled ramp is stopped, the output voltage is typically around 0.15V at no load. If the IC is re-enabled before shutdown is complete, PG will deassert immediately and not wait for the output to be in the regulation window.

**Spread-Spectrum Option**

The ICs, featuring spread-spectrum (SS) operation, vary the internal operating frequency down by 3% relative to the internally generated operating frequency of 2.2MHz (typ). This function does not apply to externally applied oscillation frequency.

**Synchronization (SYNC)**

SYNC is factory-programmable I/O (see [Ordering Information](#) for the available options). When SYNC is configured as an input, a logic-high on the FPWM bit enables SYNC to accept signal frequencies in the range of  $1.8\text{MHz} < f_{\text{SYNC}} < 2.6\text{MHz}$ . When SYNC is configured as an output, it outputs the internal PWM switching frequency.

**Current-Limit/Short-Circuit Protection**

The current-limit feature protects the ICs against short-circuit and overload conditions at the output. After soft-start is completed, if  $V_{\text{OUT}}$  is less than 50% of the set value and the IC is in current limit, the IC shuts off for 4ms (at 2.2MHz switching frequency) and repeats soft-start. This cycle repeats until the short or overload condition is removed. See the short-circuit (PWM) waveform for an example.

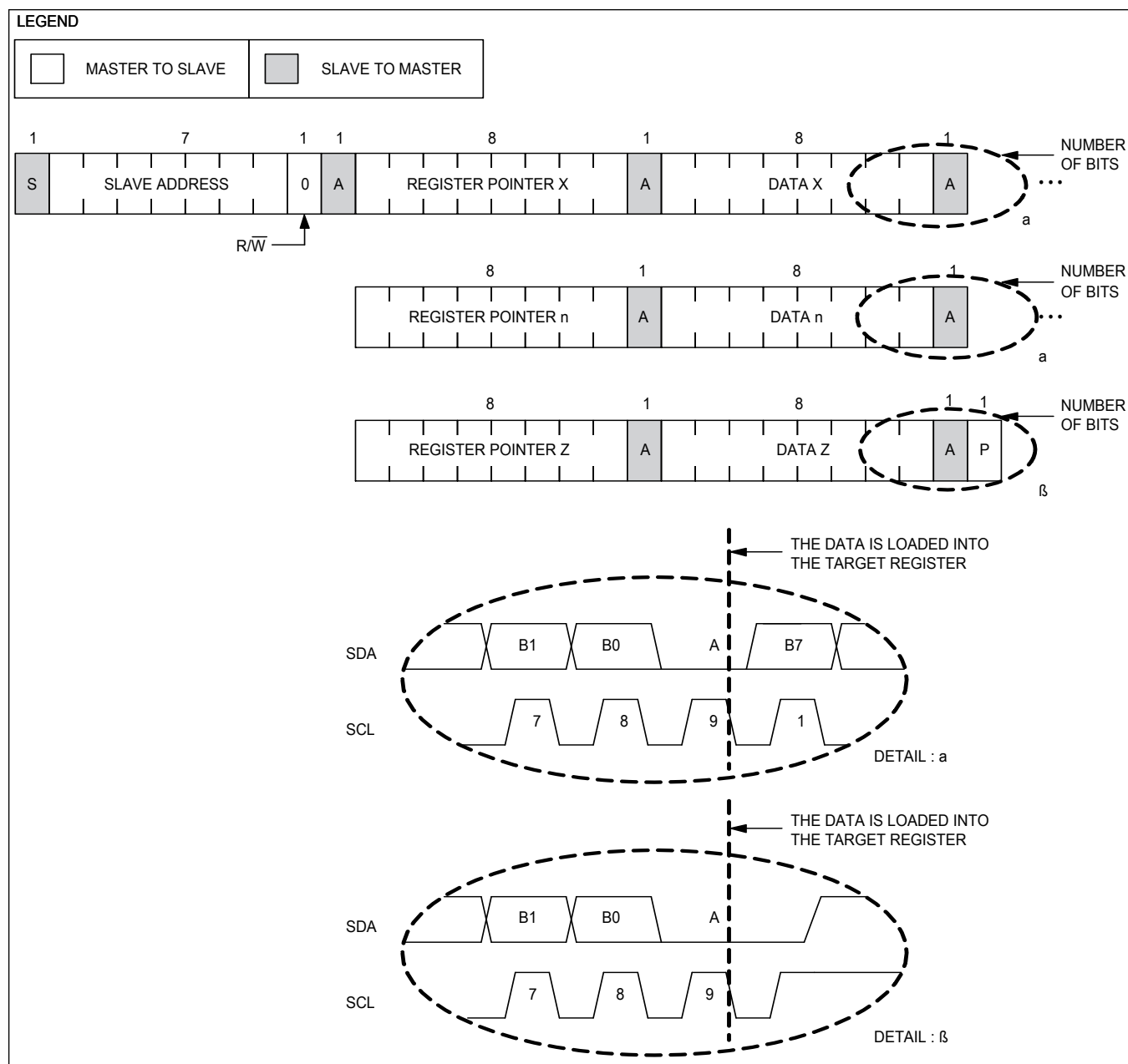


Figure 7. Write Register (Data-Pair Format)

**Table 2. Register Map**

| REG    | BIT 7 | BIT 6 | BIT 5 | BIT 4 | BIT 3 | BIT 2 | BIT 1 | BIT 0 | REGISTER ADDRESS | R/W | POWER-ON RESET |
|--------|-------|-------|-------|-------|-------|-------|-------|-------|------------------|-----|----------------|
| ID     | DEV3  | DEV2  | DEV1  | DEV0  | R3    | R2    | R1    | R0    | 0x00             | R   | 0x00           |
| —      | —     | —     | —     | —     | —     | —     | —     | —     | 0x01             | R/W | 0x00           |
| VIDMAX | —     | VMAX6 | VMAX5 | VMAX4 | VMAX3 | VMAX2 | VMAX1 | VMAX0 | 0x02             | R/W | OTP            |

**Table 2. Register Map (continued)**

|           |           |           |           |           |           |           |           |           |      |     |      |
|-----------|-----------|-----------|-----------|-----------|-----------|-----------|-----------|-----------|------|-----|------|
| Reserved* | Reserved* | —         | —         | —         | —         | —         | Reserved* | Reserved* | 0x03 | R/W | 0x02 |
| STATUS    | INTERR    | Reserved* | VRHOT     | UV        | OV        | OC        | VMERR     | 0         | 0x04 | R   | 0x00 |
| CONFIG    | VSTEP     | —         | —         | —         | FPWM      | SS        | SO1       | SO0       | 0x05 | R/W | OTP  |
| SLEW      | —         | —         | —         | —         | SR3       | SR2       | SR1       | SR0       | 0x06 | R/W | OTP  |
| VID       | —         | VID6      | VID5      | VID4      | VID3      | VID2      | VID1      | VID0      | 0x07 | R/W | OTP  |
| Reserved* | —         | —         | Reserved* | Reserved* | Reserved* | Reserved* | Reserved* | Reserved* | 0x2B | R/W | 0x00 |

**\*Note:** Reserved registers and bits are not used for readback; they are reserved for internal use.

**Table 3. Identification Registers (ID)**

| ID       |       |  |       |       |       |       |       |       |  |
|----------|-------|--|-------|-------|-------|-------|-------|-------|--|
| BIT NO.  | BIT 7 | BIT 6  | BIT 5 | BIT 4 | BIT 3 | BIT 2 | BIT 1 | BIT 0 |  |
| NAME     | DEV3  | DEV2   | DEV1  | DEV0  | R3    | R2    | R1    | R0    |  |
| POR      | 0     | 0  | 0     | 0     | 0     | 0     | 0     | 0     |  |
| BIT      |       | BIT DESCRIPTION                                |       |       |       |       |       |       |  |
| DEV[7:4] |       | Device ID: MAX20010C/MAX20010D/MAX20010E = 0x0 |       |       |       |       |       |       |  |
| R[3:0]   |       | 0x3  |       |       |       |       |       |       |  |

**Table 4. Maximum Voltage-Setting Registers (VIDMAX)**

| VIDMAX    |     |  |       |       |       |       |       |       |
|-----------|-----|--|-------|-------|-------|-------|-------|-------|
| BIT NO.   | 7   | 6  | 5     | 4     | 3     | 2     | 1     | 0     |
| NAME      | —   | VMAX6  | VMAX5 | VMAX4 | VMAX3 | VMAX2 | VMAX1 | VMAX0 |
| POR       | OTP | OTP  | OTP   | OTP   | OTP   | OTP   | OTP   | OTP   |
| BIT       |     | BIT DESCRIPTION  |       |       |       |       |       |       |
| VMAX[6:0] |     | Maximum Voltage Setting:<br>If VID[] > VMAX[], a fault is set and the actual voltage will be capped by VMAX[]. See <a href="#">Table 9</a> for voltage selections. |       |       |       |       |       |       |

**Table 5. Configuration Registers (CONFIG)**

| CONFIG  |       |  |       |       |       |       |       |       |
|---------|-------|--|-------|-------|-------|-------|-------|-------|
| BIT NO. | BIT 7 | BIT 6  | BIT 5 | BIT 4 | BIT 3 | BIT 2 | BIT 1 | BIT 0 |
| NAME    | VSTEP | —  | —     | —     | FPWM  | SS    | SO1   | SO0   |
| POR     | OTP   | OTP  | OTP   | OTP   | OTP   | OTP   | OTP   | OTP   |
| BIT     |       | BIT DESCRIPTION  |       |       |       |       |       |       |
| VSTEP   |       | Voltage Step Size—Sets the voltage step size for the LSB of SETVOUT: 0 = 10mV<br>1 = 12.5mV  |       |       |       |       |       |       |
| FPWM    |       | Forced-PWM Mode:<br>0 = Mode controlled by SYNC pin. When SYNC is output device is always FPWM mode.<br>1 = Forced-PWM Mode. Overrides SYNC skip mode setting when SYNC is an input. |       |       |       |       |       |       |
| SS      |       | Spread-Spectrum Clock Setting:<br>0 = Disabled<br>1 = +3% spread   |       |       |       |       |       |       |
| SO[1:0] |       | SYNC I/O Select:<br>00 = Master: Input, rising edge starts cycle<br>01 = Master: Input, falling edge starts cycle<br>10 = Master: Output, falling edge starts cycle<br>11 = Unused   |       |       |       |       |       |       |



**Table 6. Status Registers (STATUS)**

| STATUS  |        |           |       |       |       |       |       |       |
|---------|--------|-----------|-------|-------|-------|-------|-------|-------|
| BIT NO. | BIT 7  | BIT 6     | BIT 5 | BIT 4 | BIT 3 | BIT 2 | BIT 1 | BIT 0 |
| NAME    | INTERR | Reserved* | VRHOT | UV    | OV    | OC    | VMERR | 0     |
| POR     | 0      | 0         | 0     | 0     | 0     | 0     | 0     | 0     |

| BIT      | BIT DESCRIPTION   |
|----------|---|
| INTERR   | Internal Hardware Error:<br>This bit is set to 1 when ATE trimming and testing is not complete.                                       |
| Reserved | Reserved registers and bits are not used for readback; they are reserved for internal use.  |
| VRHOT    | Thermal-Shutdown Indication:<br>This bit indicates if thermal shutdown has occurred since the last time the STATUS register was read. |
| UV       | VOUT Undervoltage:<br>This bit indicates if the output is currently under the target voltage.   |
| OV       | VOUT Overvoltage:<br>This bit indicates if the output is currently over the target voltage.   |
| OC       | VOUT Overcurrent:<br>This bit indicates if an overcurrent event has occurred since the last time the STATUS register was read.        |
| VMERR    | VOUT MAX Error: Set to 1 if VID[] > VOUTMAX[] is in normal mode.  |

**Table 7. Slew-Rate Registers (SLEW)**

| SLEW    |       |       |       |       |       |       |       |       |
|---------|-------|-------|-------|-------|-------|-------|-------|-------|
| BIT NO. | BIT 7 | BIT 6 | BIT 5 | BIT 4 | BIT 3 | BIT 2 | BIT 1 | BIT 0 |
| NAME    | —     | —     | —     | —     | SR3   | SR2   | SR1   | SR0   |
| POR     | OTP   | OTP   | OTP   | OTP   | OTP   | OTP   | OTP   | OTP   |

| SR[3:0]           | SOFT-START SLEW RATE (mV/μs)* | DVS SLEW RATE (mV/μs)* |
|-------------------|-------------------------------|------------------------|
| XXXX0000          | 22                            | 22                     |
| XXXX0001          | 11                            | 22                     |
| XXXX0010          | 5.5                           | 22                     |
| XXXX0011          | 11                            | 11                     |
| XXXX0100          | 5.5                           | 11                     |
| XXXX0101          | 44                            | 44                     |
| XXXX0110          | 22                            | 44                     |
| XXXX0111          | 11                            | 44                     |
| XXXX1000          | 5.5                           | 44                     |
| XXXX1001          | 5.5                           | 5.5                    |
| XXXX1010—XXXX1111 | Reserved                      | Reserved               |

\*Note: VSTEP = '0'; when VSTEP = '1', increase by a factor of 1.25.

**Table 8. Output-Voltage Registers, VID**

| VID     |       |       |       |       |       |       |       |       |
|---------|-------|-------|-------|-------|-------|-------|-------|-------|
| BIT NO. | BIT 7 | BIT 6 | BIT 5 | BIT 4 | BIT 3 | BIT 2 | BIT 1 | BIT 0 |
| NAME    | —     | VID6  | VID5  | VID4  | VID3  | VID2  | VID1  | VID0  |
| POR     | OTP   | OTP   | OTP   | OTP   | OTP   | OTP   | OTP   | OTP   |

| BIT | BIT DESCRIPTION |
|-----|-----------------|
|-----|-----------------|

|          |   |
|----------|---|
| VID[6:0] | Target Voltage Setting:<br>VOUT ramps at the programmed DVS ramp until it reaches VSET. See <a href="#">Table 9</a> for voltage selections. |
|----------|---|

**Table 9. VID Output-Voltage Selections**

| VID[6:0] | VOUT (V)<br>(VSTEP = 0) | VOUT (V)<br>(VSTEP = 1) | VID[6:0] | VOUT (V)<br>(VSTEP = 0) | VOUT (V)<br>(VSTEP = 1) | VID[6:0] | VOUT (V)<br>(VSTEP = 0) | VOUT (V)<br>(VSTEP = 1) |
|----------|-------------------------|-------------------------|----------|-------------------------|-------------------------|----------|-------------------------|-------------------------|
| 0x00     | OFF                     | OFF                     | 0x20     | 0.810                   | 1.0125                  | 0x40     | 1.130                   | 1.4125                  |
| 0x01     | 0.500                   | 0.6250                  | 0x21     | 0.820                   | 1.0250                  | 0x41     | 1.140                   | 1.4250                  |
| 0x02     | 0.510                   | 0.6375                  | 0x22     | 0.830                   | 1.0375                  | 0x42     | 1.150                   | 1.4375                  |
| 0x03     | 0.520                   | 0.6500                  | 0x23     | 0.840                   | 1.0500                  | 0x43     | 1.160                   | 1.4500                  |
| 0x04     | 0.530                   | 0.6625                  | 0x24     | 0.850                   | 1.0625                  | 0x44     | 1.170                   | 1.4625                  |
| 0x05     | 0.540                   | 0.6750                  | 0x25     | 0.860                   | 1.0750                  | 0x45     | 1.180                   | 1.4750                  |
| 0x06     | 0.550                   | 0.6875                  | 0x26     | 0.870                   | 1.0875                  | 0x46     | 1.190                   | 1.4875                  |
| 0x07     | 0.560                   | 0.7000                  | 0x27     | 0.880                   | 1.1000                  | 0x47     | 1.200                   | 1.5000                  |
| 0x08     | 0.570                   | 0.7125                  | 0x28     | 0.890                   | 1.1125                  | 0x48     | 1.210                   | 1.5125                  |
| 0x09     | 0.580                   | 0.7250                  | 0x29     | 0.900                   | 1.1250                  | 0x49     | 1.220                   | 1.5250                  |
| 0x0A     | 0.590                   | 0.7375                  | 0x2A     | 0.910                   | 1.1375                  | 0x4A     | 1.230                   | 1.5375                  |
| 0x0B     | 0.600                   | 0.7500                  | 0x2B     | 0.920                   | 1.1500                  | 0x4B     | 1.240                   | 1.5500                  |
| 0x0C     | 0.610                   | 0.7625                  | 0x2C     | 0.930                   | 1.1625                  | 0x4C     | 1.250                   | 1.5625                  |
| 0x0D     | 0.620                   | 0.7750                  | 0x2D     | 0.940                   | 1.1750                  | 0x4D     | 1.260                   | 1.5750                  |
| 0x0E     | 0.630                   | 0.7875                  | 0x2E     | 0.950                   | 1.1875                  | 0x4E     | 1.270                   | 1.5875                  |
| 0x0F     | 0.640                   | 0.8000                  | 0x2F     | 0.960                   | 1.2000                  |          |                         |                         |
| 0x10     | 0.650                   | 0.8125                  | 0x30     | 0.970                   | 1.2125                  |          |                         |                         |
| 0x11     | 0.660                   | 0.8250                  | 0x31     | 0.980                   | 1.2250                  |          |                         |                         |
| 0x12     | 0.670                   | 0.8375                  | 0x32     | 0.990                   | 1.2375                  |          |                         |                         |
| 0x13     | 0.680                   | 0.8500                  | 0x33     | 1.000                   | 1.2500                  |          |                         |                         |
| 0x14     | 0.690                   | 0.8625                  | 0x34     | 1.010                   | 1.2625                  |          |                         |                         |
| 0x15     | 0.700                   | 0.8750                  | 0x35     | 1.020                   | 1.2750                  |          |                         |                         |
| 0x16     | 0.710                   | 0.8875                  | 0x36     | 1.030                   | 1.2875                  |          |                         |                         |
| 0x17     | 0.720                   | 0.9000                  | 0x37     | 1.040                   | 1.3000                  |          |                         |                         |
| 0x18     | 0.730                   | 0.9125                  | 0x38     | 1.050                   | 1.3125                  |          |                         |                         |
| 0x19     | 0.740                   | 0.9250                  | 0x39     | 1.060                   | 1.3250                  |          |                         |                         |
| 0x1A     | 0.750                   | 0.9375                  | 0x3A     | 1.070                   | 1.3375                  |          |                         |                         |
| 0x1B     | 0.760                   | 0.9500                  | 0x3B     | 1.080                   | 1.3500                  |          |                         |                         |
| 0x1C     | 0.770                   | 0.9625                  | 0x3C     | 1.090                   | 1.3625                  |          |                         |                         |
| 0x1D     | 0.780                   | 0.9750                  | 0x3D     | 1.100                   | 1.3750                  |          |                         |                         |
| 0x1E     | 0.790                   | 0.9875                  | 0x3E     | 1.110                   | 1.3875                  |          |                         |                         |
| 0x1F     | 0.800                   | 1.0000                  | 0x3F     | 1.120                   | 1.4000                  |          |                         |                         |

**PWM/Skip Modes**

The ICs feature a SYNC input that puts the converter either in skip mode or forced-PWM mode of operation. See the [Pin Description](#) table for mode details. In PWM mode, the converter switches at a constant frequency with variable on-time. In skip mode, the converter's switching frequency is load-dependent until the output load reaches a certain threshold. At higher load current, the switching frequency does not change and the operating mode is similar to the PWM mode. Skip mode helps improve efficiency in light-load applications by transferring more energy to the output during each on cycle, so the converter does not switch MOSFETs on and off as often as is the case in PWM mode. Consequently, the gate

charge and switching losses are much lower in skip mode.

### **Overtemperature Protection**

Thermal-overload protection limits the total power dissipation in the ICs. When the junction temperature exceeds 165°C (typ), an internal thermal sensor shuts down the internal bias regulator and the step-down controller, allowing the ICs to cool. The thermal sensor turns on the ICs again after the junction temperature cools by 15°C.

## Applications Information

### Input Capacitor

The input filter capacitor reduces peak currents drawn from the power source and reduces noise and voltage ripple on the input caused by the circuit's switching.

The input capacitor RMS current requirement ( $I_{RMS}$ ) is defined by the following equation:

$$I_{RMS} = I_{LOAD(MAX)} \frac{\sqrt{V_{OUT}(V_{PV\_} - V_{OUT})}}{V_{PV\_}}$$

$I_{RMS}$  has a maximum value when the input voltage equals twice the output voltage ( $V_{PV\_} = 2V_{OUT}$ ), so  $I_{RMS(MAX)} = I_{LOAD(MAX)}/2$ .

Choose an input capacitor that exhibits less than +10°C self-heating temperature rise at the RMS input current for optimal long-term reliability:

$$ESP_{IN} = \frac{\Delta V_{ESR}}{I_{OUT} + \frac{\Delta I_L}{2}}$$

where:

$$\Delta I_L = \frac{(V_{PV\_} - V_{OUT}) \times V_{OUT}}{V_{PV\_} \times f_{SW} \times L}$$

and:

$$C_{IN} = \frac{I_{OUT} \times D(1 - D)}{\Delta V_Q \times f_{SW}}$$

and:

$$D = \frac{V_{OUT}}{V_{PV\_}}$$

$I_{OUT}$  is the maximum output current, D is the duty cycle.

### Inductor Selection

The ICs are optimized to use a nominal 0.22μH inductor value. 0.15μH to 0.33μH inductors can also be used.

Inductors are rated for maximum saturation current. The maximum inductor current equals the maximum load current in addition to half the peak-to-peak ripple current:

$$I_{PEAK} = I_{LOAD(MAX)} + \frac{\Delta I_{INDUCTOR}}{2}$$

The actual peak-to-peak inductor ripple current is calculated in the previous  $\Delta I_L$  equation.

The saturation current should be  $> I_{PEAK}$ , or at least in a range where the inductance does not degrade significantly.

### Output Capacitor

The MAX20010C is stable with 2x47μF (typ) or more of X7R ceramic capacitance on the output, while the MAX20010D/MAX20010E is stable with 3x47μF (typ). Phase and gain margin must be measured with the worst-case-derated output capacitance to ensure stability. Larger capacitance values can be used to minimize  $V_{SAG}$  and  $V_{SOAR}$  during load transients.

### Setting the Output Voltage Externally

An external resistive divider can be used to set the output voltage higher than the programmed VID voltage. This should only be done with MAX20010EATPA/V+. To set the output voltage, connect a resistive divider from the output (OUT) to RS+ to GND, as shown in [Figure 8](#).  $V_{OUT}$  should not exceed 5V. Select RFB2 (RS+ to GND resistor)  $\leq 50k\Omega$ . Calculate

$R_{FB}$  (OUT to  $RS+$  resistor) with the following equation:

$$R_{FB1} = R_{FB2} \left[ \left( \frac{V_{OUT}}{V_{RS+}} \right) - 1 \right]$$

where  $V_{RS+}$  = programmed VID voltage. Capacitor  $C_{FB1}$  can help improve the phase margin when using a resistive divider. Determine  $C_{FB1}$  from the following equation:

$$C_{FB1} = 1 / (2 \times \pi \times R_{FB1} \times 80k)$$

When setting the output voltage externally, scale the inductance according to the  $V_{OUT}/V_{RS+}$  ratio. MAX20010EATPA/V+ parts are programmed with double internal slope compensation to allow for smaller inductance values. Set the inductance using the following equation:

$$L = V_{OUT} / V_{RS+} \times 220nH / 2$$

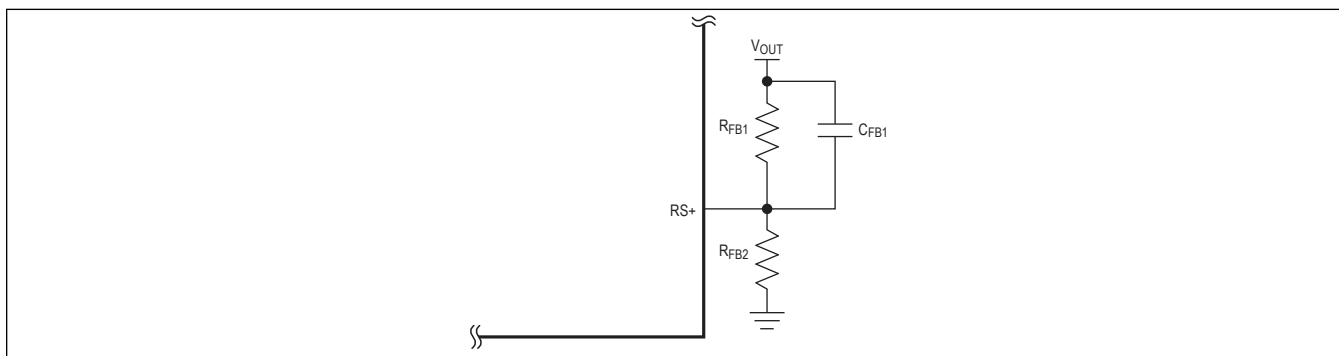


Figure 8. Adjustable Output-Voltage Setting

## Ordering Information

| PART               | PIN-<br>PACKAGE | V <sub>OUT</sub><br>(V) | V <sub>MAX</sub> [6:0] | CONFIG | VID[6:0]      | SLEW | I <sup>2</sup> C ADDR = 0 |
|--------------------|-----------------|-------------------------|------------------------|--------|---------------|------|---------------------------|
| MAX20010CATPB/V+   | 20 TQFN-EP*     | 1.24                    | 0x4B (1.24V)           | 0x08   | 0x4B (1.24V)  | 0x04 | 0x38                      |
| MAX20010CATPD/V+   | 20 TQFN-EP*     | 0.82                    | 0x3C (1.09V)           | 0x0E   | 0x21 (0.82V)  | 0x09 | 0x38                      |
| MAX20010CATPE/V+   | 20 TQFN-EP*     | 0.80                    | 0x29 (0.90V)           | 0x08   | 0x1F (0.80V)  | 0x09 | 0x3A                      |
| MAX20010CATPF/V+   | 20 TQFN-EP*     | 0.80                    | 0x29 (0.90V)           | 0x08   | 0x1F (0.80V)  | 0x03 | 0x3A                      |
| MAX20010CATPJ/V+   | 20 TQFN-EP*     | 1.20                    | 0x4C (1.25V)           | 0x08   | 0x47 (1.20V)  | 0x03 | 0x38                      |
| MAX20010CATPL/V+   | 20 TQFN-EP*     | 1.00                    | 0x42 (1.15V)           | 0x06   | 0x33 (1.00V)  | 0x03 | 0x38                      |
| MAX20010CATPM/V+   | 20 TQFN-EP*     | 1.00                    | 0x3D (1.10V)           | 0x08   | 0x33 (1.00V)  | 0x03 | 0x38                      |
| MAX20010CATPQ/V+   | 20 TQFN-EP*     | 0.60                    | 0x1F (0.80V)           | 0x08   | 0x0B (0.60V)  | 0x03 | 0x38                      |
| MAX20010CATPT/V+** | 20 TQFN-EP*     | 1.275                   | 0x39 (1.325V)          | 0x8C   | 0x35 (1.275V) | 0x03 | 0x38                      |
| MAX20010CATPU/V+   | 20 TQFN-EP*     | 1.03                    | 0x3B (1.08V)           | 0x0C   | 0x36 (1.03V)  | 0x00 | 0x38                      |
| MAX20010CATPW/V+   | 20 TQFN-EP*     | 0.80                    | 0x29 (0.90V)           | 0x04   | 0x1F (0.80V)  | 0x04 | 0x38                      |
| MAX20010CATPX/V+   | 20 TQFN-EP*     | 1.00                    | 0x42 (1.15V)           | 0x04   | 0x33 (1.00V)  | 0x04 | 0x38                      |
| MAX20010CATPY/V+   | 20 TQFN-EP*     | 0.75                    | 0x2E (0.95V)           | 0x00   | 0x1A (0.75V)  | 0x02 | 0x38                      |
| MAX20010DATPN/V+   | 20 TQFN-EP*     | 1.00                    | 0x42 (1.15V)           | 0x08   | 0x33 (1.00V)  | 0x03 | 0x38                      |
| MAX20010DATPO/V+   | 20 TQFN-EP*     | 0.91                    | 0x42 (1.15V)           | 0x08   | 0x2A (0.91V)  | 0x03 | 0x38                      |
| MAX20010DATPO/VY+  | 20 SW TQFN-EP*  | 0.91                    | 0x42 (1.15V)           | 0x08   | 0x2A (0.91V)  | 0x03 | 0x38                      |
| MAX20010DATPP/V+   | 20 TQFN-EP*     | 0.87                    | 0x42 (1.15V)           | 0x08   | 0x26 (0.87V)  | 0x03 | 0x38                      |
| MAX20010DATPQ/V+   | 20 TQFN-EP*     | 0.92                    | 0x42 (1.15V)           | 0x08   | 0x2B (0.92V)  | 0x03 | 0x38                      |
| MAX20010DATPR/V+   | 20 TQFN-EP*     | 0.90                    | 0x42 (1.15V)           | 0x08   | 0x29 (0.90V)  | 0x00 | 0x38                      |
| MAX20010DATPT/V+   | 20 TQFN-EP*     | 0.75                    | 0x42 (1.15V)           | 0x08   | 0x1A (0.75V)  | 0x03 | 0x38                      |
| MAX20010DATPY/V+   | 20 TQFN-EP*     | 1.10                    | 0x42 (1.15V)           | 0x08   | 0x3D (1.10V)  | 0x03 | 0x38                      |
| MAX20010EATPA/V+   | 20 TQFN-EP*     | 1.20                    | 0x4C (1.25V)           | 0x08   | 0x47 (1.20V)  | 0x03 | 0x38                      |
| MAX20010EATPB/V+** | 20 TQFN-EP*     | 0.50                    | 0x10 (0.65V)           | 0x08   | 0x01 (0.50V)  | 0x09 | 0x38                      |

/V denotes an automotive-qualified part.

+Denotes a lead(Pb)-free/RoHS-compliant package.

\*EP = Exposed pad.

\*\*Future product—contact factory for availability.

## Revision History

| REVISION<br>NUMBER | REVISION<br>DATE | DESCRIPTION  | PAGES<br>CHANGED       |
|--------------------|------------------|--|------------------------|
| 0                  | 9/17             | Initial release  | —                      |
| 1                  | 3/18             | Updated Table 7, Output Capacitor section, and Ordering Information  | 16, 18–19              |
| 2                  | 4/18             | Updated Package Information table and Table 7. Added MAX20010DATPR/V+ as a future product to the Ordering Information table.   | 2, 16, 19              |
| 3                  | 8/18             | Updated equation in the Setting the Output Voltage Externally section. Added MAX-20010CATPE/V+** as a future product and removed future product designation from MAX20010DATPR/V+ in the Ordering Information table.   | 19                     |
| 4                  | 11/18            | Updated Package Information table. Added MAX20010DATPT/V+ and MAX20010DAT-PO/VY+ to the Ordering Information table. Added MAX20010CATPU/V+ as a future product to the Ordering Information table.  | 2, 19                  |
| 5                  | 3/19             | Removed future-product notation from MAX20010CATPE/V+ and MAX20010CATPU/V+ in the Ordering Information table   | 19                     |
| 6                  | 2/20             | Added MAX20010E product variant to the following sections: General Description, Typical Application Circuit, Pin Configuration, Detailed Description, Figure 1: Internal Block Diagram, Table3: Identification Registers (ID) - Dev[7.4], Output Capacitor. Updated and added equations to: Setting the Output Voltage Externally section. Added MAX20010E-ATPA/V+ to the Ordering Information table. Updated ordering table to use 7-bit addresses. | 1, 7, 8, 14,<br>18, 19 |
| 7                  | 9/21             | Added "Enable (EN)" subsection. Updated "Shutdown" subsection. Updated Table 2. Added MAX20010CATPB/V+, MAX20010CATPT/V+, and MAX20010CATPY/V+ as future products to the Ordering Information table. Added MAX20010CATPF/V+, MAX20010DATPQ/V+, MAX20010CATPW/V+, MAX20010CATPX/V+, and MAX20010DATPY/V+ to the Ordering Information table.   | 14, 16, 22             |
| 8                  | 10/21            | Added future product notation to MAX20010CATPW/V+ and MAX20010CATPX/V+   | 22                     |
| 9                  | 11/21            | Removed future product notation from MAX20010CATPW/V+, MAX20010CATPX/V+, and MAX20010CATPY/V+  | 22                     |
| 10                 | 1/22             | Updated Package Information table  | 2                      |
| 11                 | 7/22             | Added MAX20010EATPB/V+ as a future product to the Ordering Information table.  | 22                     |

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[MAX20010DATPT/V+T](#) [MAX20010DATPO/V+](#) [MAX20010DATPO/VY+](#) [MAX20010DATPN/V+T](#)  
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[MAX20010DATPQ/V+T](#) [MAX20010DATPY/V+](#) [MAX20010DATPY/V+T](#)