Click here to ask about the production status of specific part numbers.

MAX16984A

Automotive High-Current Step-Down Converter with USB Protection/Host Charger Adapter Emulator

General Description

The MAX16984A combines a 5V automotive-grade step-down converter capable of driving up to 3.0A, a USB host charger adapter emulator, and USB protection switches for automotive USB host applications. The USB protection switches provide high-ESD, short-circuit protection and feature integrated host-charger port-detection circuitry adhering to the USB 2.0 BC 1.2 Battery Charging Specification, Samsung® and Chinese Telecommunication Industry Standard YD/T 1591-2009. They also include circuitry for Samsung 2.0A, iPod®/iPhone®/iPad® 2.4A dedicated charging modes. The HVD+ and HVD- ESD protection features include protection to ±15kV Air/±8kV Contact on the HVD+ and HVD- outputs to the IEC 61000-4-2 model and 330Ω, 330pF ISO model.

The high-efficiency step-down DC-DC converter operates from a voltage up to 28V and is protected from load dump transients up to 40V. The device is optimized for high-frequency operation and includes I^2C or resistor-programmable frequency selection from 310kHz to 2.2MHz to allow optimization of efficiency, noise, and board space based on application requirements. The fully synchronous DC-DC converter integrates high-side and low-side MOSFETs with an external SYNC input/output, and can be configured for spread-spectrum operation. Skip mode is available in light/no-load conditions to minimize quiescent current. The converter can deliver up to 3A of continuous current at 105°C. The MAX16984A has an integrated spread-spectrum oscillator to improve EMI performance.

The MAX16984A also includes a USB load current-sense amplifier and configurable feedback adjustment circuit designed to provide automatic USB voltage adjustment to compensate for voltage drops in captive cables associated with automotive applications. The MAX16984A limits the USB load current using both a fixed internal peak current threshold of the DC-DC converter and a user-configurable external USB load current-sense amplifier threshold.

Applications

- Automotive Radio and Navigation
- USB Port for Host and Hub Applications
- Automotive Connectivity
- Telematics
- Dedicated USB Power Charger

Benefits and Features

- Integrated DC-DC and USB Host Charge Emulator Enables 1-Chip Solution Directly from Car Battery to Portable Device
  - 4.5V to 28V (40V Load Dump) Operating Voltage
  - 5V, 3.0A Output Current Capability
  - Low-Q Current Skip and Shutdown Modes
  - Soft-Start Reduces Inrush Current
- Low-Noise Features Prevent Interference with AM Band and Portable Devices
  - Fixed-Frequency 310kHz to 2.2MHz Operation
  - Forced-PWM Option at No Load
  - Spread Spectrum for EMI Reduction
  - SYNC Input/Output for Frequency Parking
- Optimal USB Power and Communication for Portable Devices
  - User-Adjustable Voltage Gain Adjusts Output Between 5V and 7V for Cable Compensation
  - ±5% Accuracy User-Adjustable USB Current Limit
  - 4Ω USB 2.0 1GHz Data Switches
  - Integrated Samsung/iPod/iPhone/iPad Charge-Detection Termination Resistors
  - Supports USB BC1.2 Charging Downstream Port (CDP) and Dedicated Charging Port (DCP) Modes
  - Supports Chinese Telecommunication Industry Standard YD/T 1591-2009
  - Compatible with USB On-the-Go Specification
  - High-Speed Pass-Through Mode (SDP)
- Robust Design Keeps Vehicle System and Portable Devices Safe in Automotive Environment
  - Short-to-Battery Protection on DC-DC Converter
  - Short-to-Battery Protection on USB Pins
  - ±15kV Air/±8kV Contact ISO 10605*
  - ±15kV Air/±8kV Contact IEC 61000-4-2*
  - ±15kV Air/±8kV Contact (330Ω, 330pF)*
  - Advanced Diagnostics Through I^2C Bus
  - Reduced Inrush Current with Soft-Start
  - Over-temperature Protection
  - -40°C to +125°C Operating Temperature Range
  - 32-Pin, 5mm x 5mm, TQFN Package

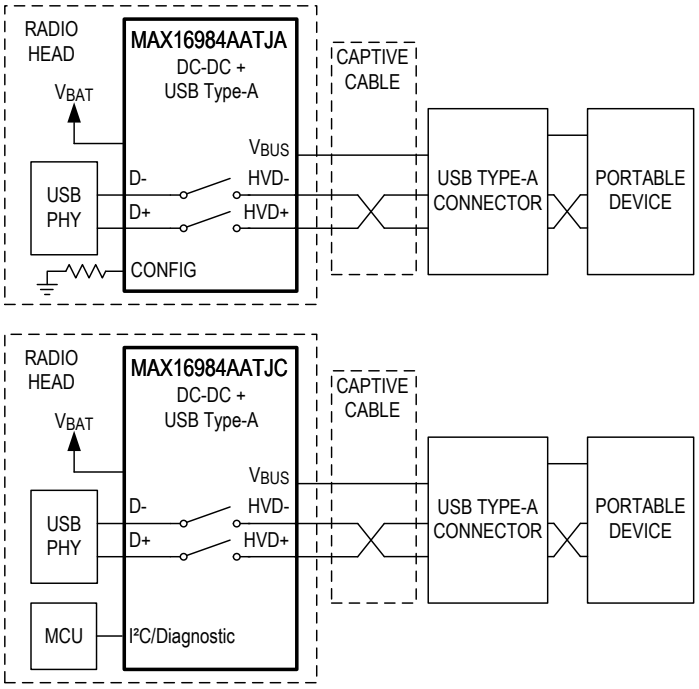
*Tested in Typical Application Circuit as used on the MAX16984A Evaluation Kit

Ordering Information and *Typical Application Circuit* appear at end of data sheet.

19-100762; Rev 3; 05/21

maxim integrated™

Simplified Block Diagram



Absolute Maximum Ratings

SUPSW to PGND ..... -0.3V to +40V
HVEN to PGND ..... -0.3V to V_{SUPSW} + 0.3V
LX to PGND (Note 1) ..... -0.3V to V_{SUPSW} + 0.3V
SYNC to AGND ..... -0.3V to V_{BIAS} + 0.3V
SENSN, SENSP, VBMON to AGND ..... -0.3V to V_{SUPSW} + 0.3V
AGND to PGND ..... -0.3V to +0.3V
BST to PGND ..... -0.3V to +46V
BST to LX ..... -0.3V to +6V
IN, CONFIG1, ENBUCK, SDA (CONFIG2), SCL (CONFIG3), BIAS, DATA_MODE, FAULT, SHIELD, INT (ATTACH) to AGND ..... -0.3V to +6V
HVDP, HVDM to AGND ..... -0.3V to +18V
DP, DM to AGND ..... -0.3V to V_{IN} + 0.3V

LX Continuous RMS Current 3.5A
Output Short-Circuit Duration ..... Continuous
Thermal Characteristics .....
Continuous Power Dissipation (T_A = +70°C)
TQFN Single-Layer Board .....
(derate 21.3mW/°C above +70°C) 1702.10mW
TQFN Multilayer Board .....
(derate 34.5mW/°C above +70°C) 2758.6mW
Operating Temperature Range ..... -40ºC to 125ºC
Junction Temperature ..... +150ºC
Storage Temperature Range ..... -40ºC to +150ºC
Lead Temperature (soldering, 10s) 300ºC
Soldering Temperature (reflow) ..... +260ºC

Note 1: Self-protected from transient voltages exceeding these limits ≤ 50ns in circuit under normal operation.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Package Information

32-Pin TQFN

Package Code	T3255+4C
Outline Number	21-0140
Land Pattern Number	90-0012
THERMAL RESISTANCE, SINGLE-LAYER BOARD	
Junction-to-Ambient (θ_{JA})	47ºC/W
Junction-to-Case Thermal Resistance (θ_{JC})	1.70ºC/W
THERMAL RESISTANCE, FOUR-LAYER BOARD	
Junction-to-Ambient (θ_{JA})	29ºC/W
Junction-to-Case Thermal Resistance (θ_{JC})	1.70ºC/W

For the latest package outline information and land patterns (footprints), go to *www.maximintegrated.com/packages*. Note that a "+", "#", or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

Package thermal resistances were obtained using the method described in JEDEC specification JESD51-7, using a four-layer board. For detailed information on package thermal considerations, refer to *www.maximintegrated.com/thermal-tutorial*.

Electrical Characteristics

(V_{SUPSW} = 14V, V_{ENBUCK} = V_{IN} = 3.3V, temperature = T_A = T_J = -40°C to +125°C, unless otherwise noted. Typical values are T_A = +25°C under normal conditions.) (Note 3)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
POWER SUPPLY AND ENABLE						
Supply Voltage Range	V_{SUPSW}	(Note 2)	4.5		28	V
Load Dump Event Supply Voltage Range	V_{SUPSW_LD}	t < 1s			40	V
Supply Current	I_{SUPSW}	V_{SUPSW} = 18V; V_{HVEN} = 0V; V_{IN} = 0V; V_{CONN} = 0V, Off State		10	20	µA
		HVEN = 14V; buck switching; no load; skip mode		1.8		mA
		HVEN = 14V; buck switching; no load; FPWM mode		28		
BIAS Voltage	V_{BIAS}	5.75V ≤ V_{SUPSW} ≤ 28V	4.5	4.7	5.25	V
BIAS Current Limit			50	150		mA
BIAS Undervoltage Lockout	V_{UV_BIAS}	V_{BIAS} rising	3.0	3.3	3.6	V
BIAS Undervoltage Lockout Hysteresis				0.2		V
SUPSW Undervoltage Lockout		V_{SUPSW} rising	3.9		4.42	V
SUPSW Undervoltage Lockout Hysteresis				0.2		V
IN Voltage Range	V_{IN}		3		3.6	V
IN Overvoltage Lockout	V_{IN_OVLO}	V_{IN} rising	3.8	4	4.3	V
IN Input Current	I_{IN}				10	µA
HVEN Rising Threshold	V_{HVEN_R}		0.6	1.5	2.4	V
HVEN Falling Threshold	V_{HVEN_F}				0.4	V
HVEN Hysteresis	V_{HVEN}			0.2		V
HVEN Delay Rising	t_{HVEN_R}		2.5		15	µs
HVEN Delay Falling	t_{HVEN_F}		5	12	25	µs
HVEN Input Leakage		V_{HVEN} = V_{SUPSW} = 18V, V_{HVEN} = 0V			10	µA
DP, DM ANALOG USB SWITCHES						
On-Channel -3dB Bandwidth	BW	R_L = R_S = 50Ω		1000		MHz
Analog Signal Range			0		3.6	V
Protection Trip Threshold	V_{OV_D}		3.65	3.85	4.1	V
Protection Response Time	t_{FP_D}	V_{IN} = 4.0V, $V_{HVD±}$ = 3.3V to 4.3V step, R_L = 15kΩ on D±, delay to $V_{D±}$ < 3V		2		µs
On-Resistance Switch A	R_{ON_SA}	I_L = 10mA, $V_{D\_}$ = 0V to V_{IN}, V_{IN} = 3.0V to 3.6V		4	8	Ω
On-Resistance Match between Channels Switch A	ΔR_{ON_SA}	I_L = 10mA, $V_{D\_}$ = 1.5V or 3.0V			0.2	Ω

Electrical Characteristics (continued)

(V_{SUPSW} = 14V, V_{ENBUCK} = V_{IN} = 3.3V, temperature = T_A = T_J = -40°C to +125°C, unless otherwise noted. Typical values are T_A = +25°C under normal conditions.) (Note 3)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
On-Resistance Flatness Switch A	$R_{FLAT(ON)A}$	I_L = 10mA,$V_{D\_}$ = 0V or 0.4V		0.01		Ω
On-Resistance of HVD+/HVD- short	R_{SHORT}	V_{DP} = 1V, I_{DM} = 500µA		90	180	Ω
HVD+/HVD- On-Leakage Current	I_{HVD_ON}	$V_{HVD±}$ = 3.6V or 0V	-7		+7	µA
HVD+/HVD- Off-Leakage Current	I_{HVD_OFF}	V_{HVD+} -= 18V or V_{HVD-} = 18V, $V_{D±}$ = 0V			150	µA
D+/D- Off-Leakage Current	I_{D_OFF}	$V_{HVD±}$ = 18V, $V_{D±}$ = 0V	-1		+1	µA
CURRENT-SENSE AMPLIFIER (SENSP, SENSN) AND ANALOG INPUTS (VBMON)						
Gain		10mV < V_{SENSP} - V_{SENSN} < 110mV, GAIN[4:0] = 0b11111		19.4		V/V
Cable Compensation LSB	R_{LSB}			18		mΩ
Overcurrent Threshold	ILIM_SET	ILIM[2:0] = 0b111, R_{SENSE} = 33mΩ	3.04	3.14	3.30	A
		ILIM[2:0] = 0b110, R_{SENSE} = 33mΩ	2.6	2.75	2.9	
		ILIM[2:0] = 0b101, R_{SENSE} = 33mΩ	2.1	2.25	2.4	
		ILIM[2:0] = 0b100, R_{SENSE} = 33mΩ	1.62	1.7	1.78	
		ILIM[2:0] = 0b011, R_{SENSE} = 33mΩ	1.05	1.13	1.21	
		ILIM[2:0] = 0b010, R_{SENSE} = 33mΩ	0.8	0.86	0.92	
		ILIM[2:0] = 0b001, R_{SENSE} = 33mΩ	0.55	0.6	0.65	
		ILIM[2:0] = 0b000, R_{SENSE} = 33mΩ	0.3	0.33	0.36	
SENSN Discharge Current	I_{SENSN_DIS}		11	18	32	mA
Startup Wait Time	t_{BUCK_WAIT}			100		ms
SENSN Discharge Time	t_{DIS_POR}	Discharge after POR		10		ms
	t_{DIS_CD}	DATA_MODE or CD[1] toggle (into and out of DCP mode), DCDC_ON toggle		2		s
Forced Buck Off-Time	$t_{BUCKOFF\_CD}$	DATA_MODE or CD[1] toggle (into and out of DCP mode), DCDC_ON toggle; see reset criteria		2		s
Attach Comparator Load Current Rising Threshold		Common mode input = 5.15V	5	16	28	mA
Attach Comparator Hysteresis		Common mode input = 5.15V		2.5		mA
SENSN Undervoltage Threshold (Falling)	V_{UV_SENSN}		4	4.375	4.75	V
SENSN Overvoltage Threshold (Rising)	V_{OV_SENSN}		7	7.46	7.9	V
SENSN Short-Circuit Threshold (Falling)			1.75	2	2.25	V

Electrical Characteristics (continued)

(V_{SUPSW} = 14V, V_{ENBUCK} = V_{IN} = 3.3V, temperature = T_A = T_J = -40°C to +125°C, unless otherwise noted. Typical values are T_A = +25°C under normal conditions.) (Note 3)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
SENSN Undervoltage Fault Blanking Time				16		ms
SENSN Overvoltage Fault Blanking Time	t_{B,OV_SENSN}	From overvoltage condition to $\overline{FAULT}$ asserted		3	6	µs
SENSN Discharge Threshold Falling		V_{SENSN} falling	0.47	0.51	0.57	V
REMOTE FEEDBACK ADJUSTMENT						
SHIELD Input Voltage Range			0.1		0.75	V
Gain			1.935	2	2.065	V/V
Input Referred Offset Voltage				±2.0		mV
DIGITAL INPUTS (SDA, SCL, ENBUCK, DATA_MODE)						
Input Leakage Current		V_{PIN} = 5.5V, 0V	-5		+5	µA
Logic-High	V_{IH}		1.6			V
Logic-Low	V_{IL}				0.5	V
USB 2.0 HOST CHARGER EMULATOR (HVD+/HVD-, D+/D-)						
Input Logic-High	V_{IH}		2.0			V
Input Logic-Low	V_{IL}				0.8	V
Data Sink Current	I_{DAT_SINK}	V_{DAT_SINK} = 0.25V to 0.4V	50	100	150	µA
Data Detect Voltage High	V_{DAT_REFH}		0.4			V
Data Detect Voltage Low	V_{DAT_REFL}				0.25	V
Data Detect Voltage Hysteresis	V_{DAT_HYST}			60		mV
Data Source Voltage	V_{DAT_SRC}	I_{SRC} = 200µA	0.5		0.7	V
SYNCHRONOUS STEP-DOWN DC-DC CONVERTER						
PWM Output Voltage	V_{SENSP}	7V ≤ V_{SUPSW} ≤ 28V, no load		5.15		V
Skip Mode Output Voltage	V_{SENSP_SKIP}	7V ≤ V_{SUPSW} ≤ 18V, no load (Note 2)		5.25		V
Load Regulation		7V ≤ V_{SUPSW} ≤ 18V, for 5V nominal output setting		51		mΩ
Output Voltage Accuracy		8V ≤ V_{SUPSW} ≤ 18V, 2.4A, V_{SENSP} - V_{SENSN} = 79.2mV, GAIN[4:0] = 0b11111 cable compensation.	6.33		6.68	V
Spread-Spectrum Range		SS enabled		±3.4		%
SYNC Switching Threshold High	V_{SYNC_HI}	Rising	1.4			V
SYNC Switching Threshold Low	V_{SYNC_LO}	Falling			0.4	V
SYNC Internal Pulldown				200		kΩ

Electrical Characteristics (continued)

(V_{SUPSW} = 14V, V_{ENBUCK} = V_{IN} = 3.3V, temperature = T_A = T_J = -40°C to +125°C, unless otherwise noted. Typical values are T_A = +25°C under normal conditions.) (Note 3)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
SYNC Input Clock Acquisition Time	t_{SYNC}	(Note 3)		1		Cycles
High-Side Switch On-Resistance	R_{ONH}	I_{LX} = 1A		54	95	mΩ
Low-Side Switch On-Resistance	R_{ONL}	I_{LX} = 1A		72	135	mΩ
BST Input Current	I_{BST}	V_{BST} - V_{LX} = 5V, high-side on		2.2		mA
LX Current-Limit Threshold		All Other Variants		5		A
		MAX16984AATJM, MAX16984AATJN		6		
Skip Mode Peak Current Threshold	I_{SKIP_TH}			1		A
Negative Current Limit				1.2		A
Soft-Start Ramp Time	t_{SS}			8		ms
LX Rise Time		(Note 3)		3		ns
LX Fall Time		(Note 3)		4		ns
BST Refresh Algorithm Low-Side Minimum On-Time				60		ns
$\overline{FAULT}$, $\overline{INT}$ ($\overline{ATTACH}$), SYNC OUTPUTS						
Output-High Leakage Current		$\overline{FAULT}$, $\overline{INT}$ ($\overline{ATTACH}$), = 5.5V	-10		+10	µA
Output Low Level		Sinking 1mA			0.4	V
SYNC Output High Level		Sourcing 1mA, SYNC configured as output	V_{BIAS} - 0.4			V
CONFIG RESISTORS CONVERTER						
CONFIG1-3 Current Leakage		V_{CONFIG} = 0V to 4V			±5	µA
Minimum Window Amplitude			-4		+4	%
ADC						
Resolution				8		Bits
ADC Gain Error				±2		LSBs
Offset Error	Offset_ADC			±1		LSB
OSCILLATORS						
Internal High-Frequency Oscillator	HFOSC		7	8	9	MHz
Buck Oscillator Frequency	f_{SW}	FSW[2:0] = 0b000	1.95	2.2	2.45	MHz
Buck Oscillator Frequency	f_{SW}	FSW[2:0] = 0b101	340	410	480	kHz
THERMAL OVERLOAD						
Thermal Warning Temperature				140		°C

Electrical Characteristics (continued)

(V_{SUPSW} = 14V, V_{ENBUCK} = V_{IN} = 3.3V, temperature = T_A = T_J = -40°C to +125°C, unless otherwise noted. Typical values are T_A = +25°C under normal conditions.) (Note 3)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Thermal Warning Hysteresis				10		°C
Thermal Shutdown Temperature				165		°C
Thermal Shutdown Hysteresis				10		°C
I²C						
Serial Clock Frequency	f_{SCL}				400	kHz
Bus Free Time Between STOP and START Condition	t_{BUF}		1.3			µs
START Condition Setup Time	$t_{SU:STA}$		0.6			µs
START Condition Hold Time	$t_{HD:STA}$		0.6			µs
STOP Condition Setup Time	$t_{SU:STO}$		0.6			µs
Clock Low Period	t_{LOW}		1.3			µs
Clock High Period	t_{HIGH}		0.6			µs
Data Setup Time	$t_{SU:DAT}$		100			ns
Data Hold Time	$t_{HD:DAT}$	From 50% SCL falling to SDA change	0.3		0.6	µs
Pulse Width of Spike Suppressed	t_{SP}			50		ns
ESD PROTECTION (ALL PINS)						
ESD Protection Level	V_{ESD}	Human Body Model		±2		kV
ESD PROTECTION (HVDP, HVDM)						
ESD Protection Level	V_{ESD}	ISO 10605 Air-Gap (330pF, 2kΩ)		±15		kV
		ISO 10605 Contact (330pF, 2kΩ)		±8		
		IEC 61000-4-2 Air-Gap (150pF, 330Ω)		±15		
		IEC 61000-4-2 Contact (150pF, 330Ω)		±8		
		ISO 10605 Air-Gap (330pF, 330Ω)		±15		
		ISO 10605 Contact (330pF, 330Ω)		±8		

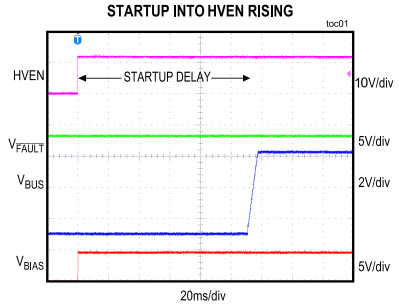
Note 2: Device is designed for use in applications with continuous operation of 14V. Device meets electrical table up to maximum supply voltage.

Note 3: Specification with minimum and maximum limits are 100% production tested at T_A = 25ºC and are guaranteed over the operating temperature range by design and characterization. Actual typical values may vary and are not guaranteed.

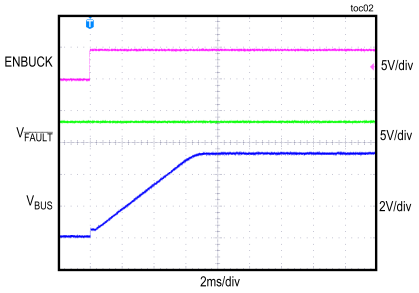
Typical Operating Characteristics

(T_A = +25°C, unless otherwise noted.)

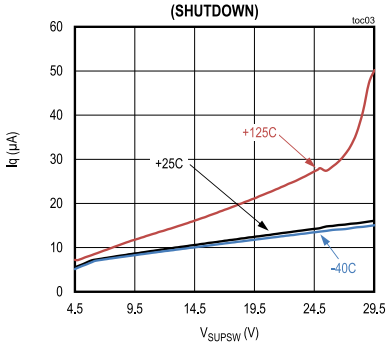
STARTUP INTO HVEN RISING



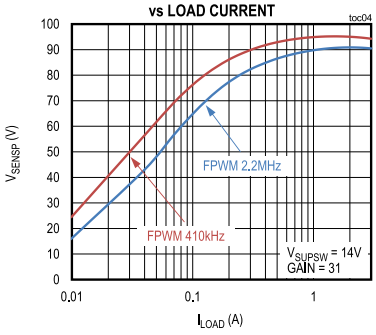
STARTUP INTO ENBUCK RISING



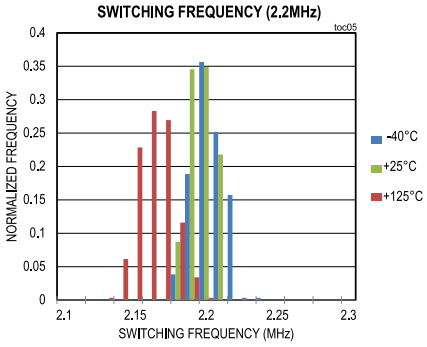
SUPPLY CURRENT vs VOLTAGE (SHUTDOWN)



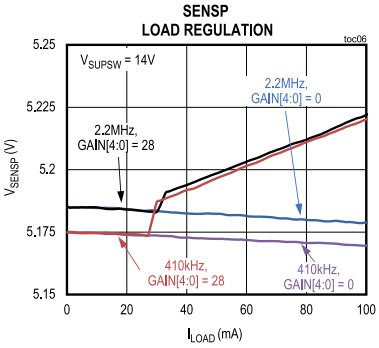
BUCK EFFICIENCY vs LOAD CURRENT



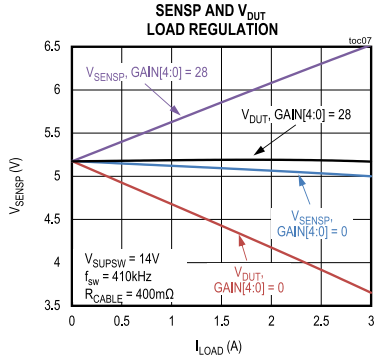
SWITCHING FREQUENCY (2.2MHz)



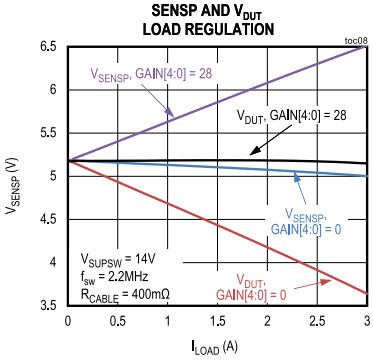
SENSP LOAD REGULATION



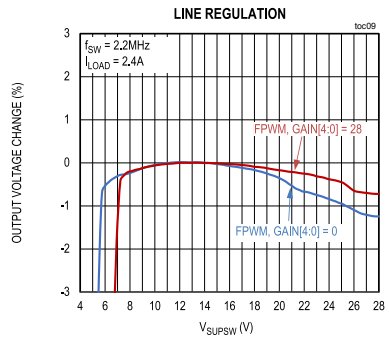
SENSP AND V_{DUT} LOAD REGULATION



SENSP AND V_{DUT} LOAD REGULATION



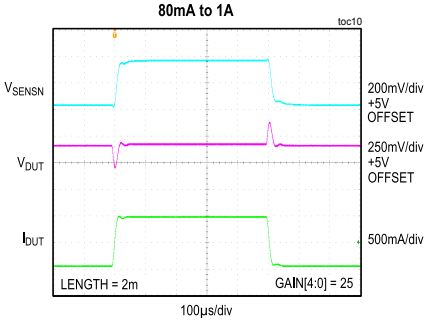
LINE REGULATION



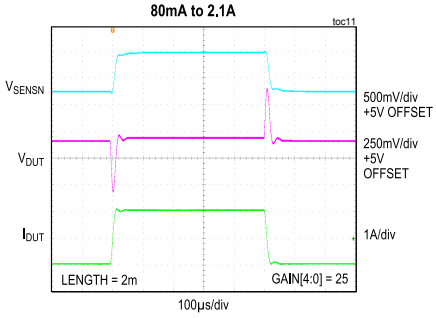
Typical Operating Characteristics (continued)

(T_A = +25°C, unless otherwise noted.)

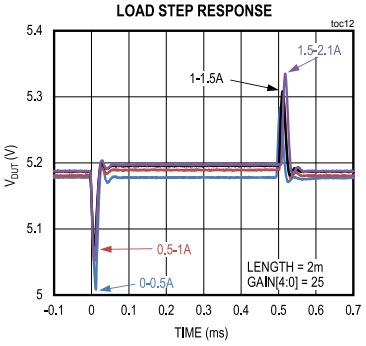
LOAD STEP RESPONSE
80mA to 1A



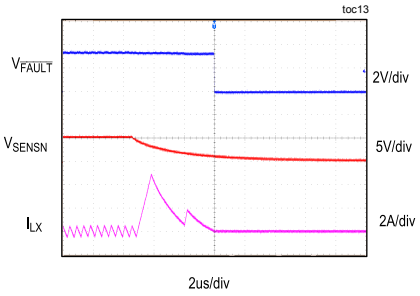
LOAD STEP RESPONSE
80mA to 2.1A



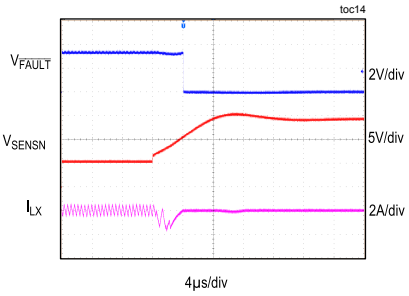
LOAD STEP RESPONSE



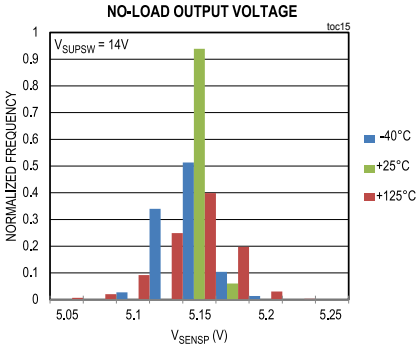
SENSN
SHORT TO GROUND



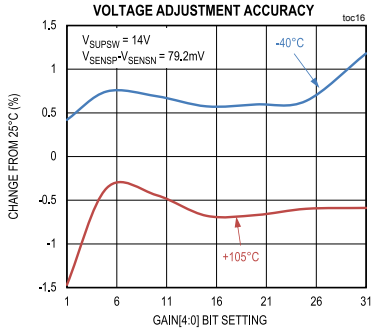
SENSN
SHORT TO V_{BAT} (14V)



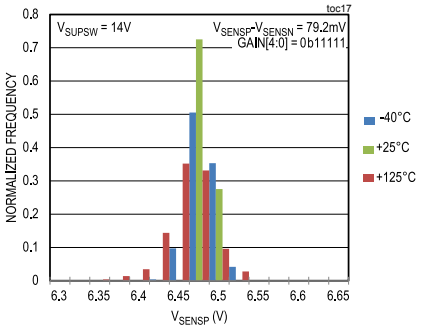
NO-LOAD OUTPUT VOLTAGE



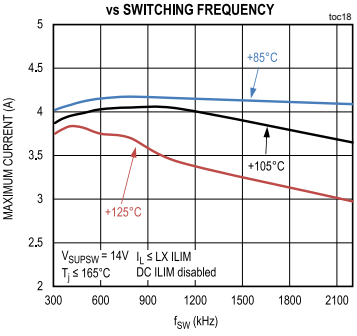
VOLTAGE ADJUSTMENT ACCURACY



OUTPUT VOLTAGE ACCURACY



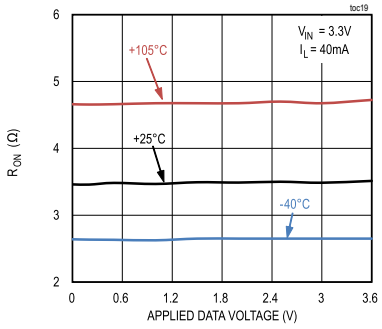
MAXIMUM USB LOAD CURRENT
vs SWITCHING FREQUENCY



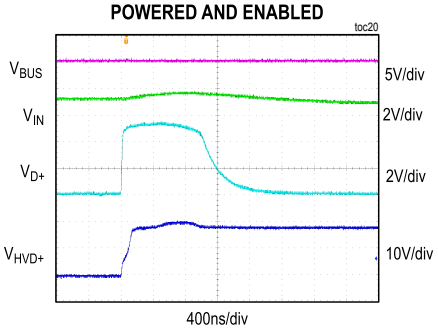
Typical Operating Characteristics (continued)

(T_A = +25°C, unless otherwise noted.)

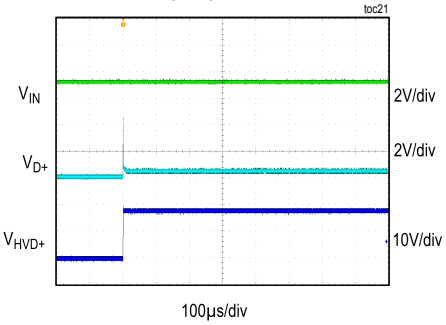
DATA SWITCH R_{ON} vs. APPLIED DATA VOLTAGE



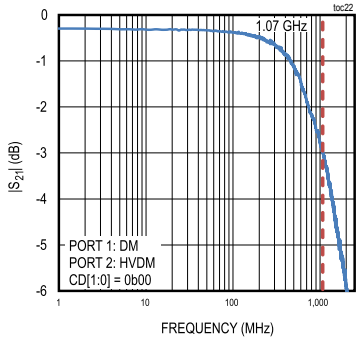
HVD+/- SHORT TO VBAT (18V) POWERED AND ENABLED



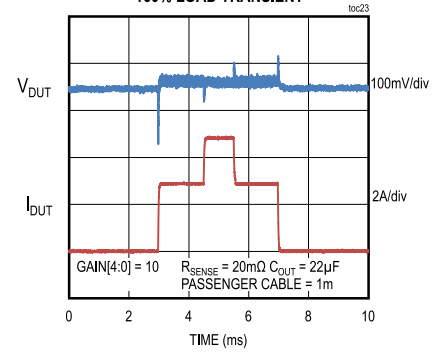
HVD+/- SHORT TO VBAT (18V) UNPOWERED



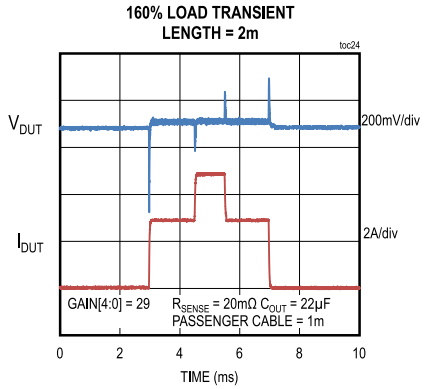
SINGLE-ENDED BANDWIDTH



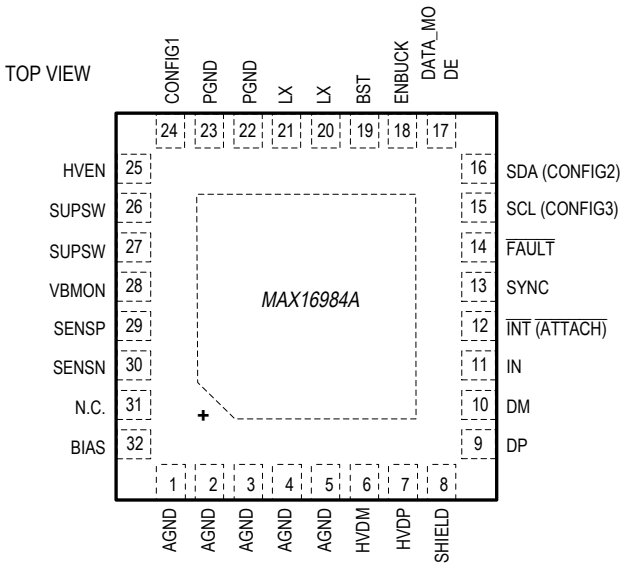
160% LOAD TRANSIENT



160% LOAD TRANSIENT LENGTH = 2m



Pin Configuration



TQFN
5mm x 5mm

Pin Description

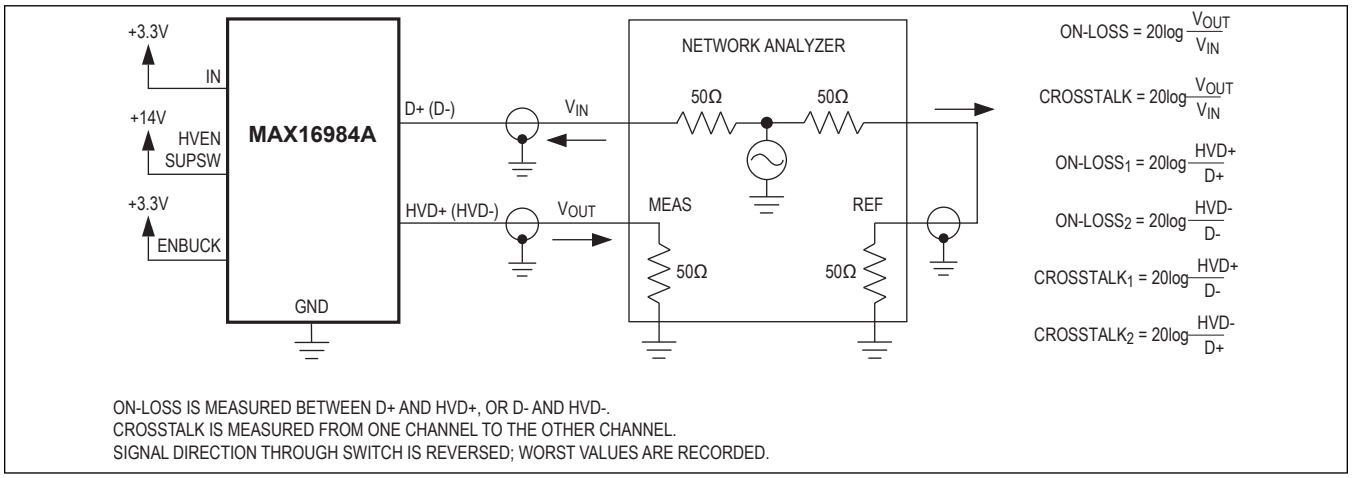
PIN	NAME	FUNCTION
1–5	AGND	Analog Ground
6	HVDM	High-Voltage-Protected USB Differential Data D- Output. Connect HVD- to the downstream USB connector D- pin.
7	HVDP	High-Voltage-Protected USB Differential Data D+ Output. Connect HVD+ to the downstream USB connector D+ pin.
8	SHIELD	Remote feedback input, special order only. See Figure 2.
9	DP	USB Differential Data D+ Input. Connect D+ to the low-voltage USB transceiver D+ pin.
10	DM	USB Differential Data D- Input. Connect D- to the low-voltage USB transceiver D- pin.
11	IN	Logic Enable Input. Connect to I/O voltage of USB transceiver. IN is also used for clamping during overvoltage events on HVD+ or HVD-. Connect a 1µF– 10µF ceramic capacitor from IN to GND.
12	$\overline{\text{INT}}$ ($\overline{\text{ATTACH}}$)	In I^2C variants, functions as an active-low INT pin. In standalone variants, functions as active-low Attach. Connect a 100kΩ pullup resistor to IN.
13	SYNC	Switching Frequency Input/Output for Synchronization with Other DC-DC Supplies. See *Applications Information* section.
14	$\overline{\text{FAULT}}$	Active-Low, Open-Drain Fault Indicator Output. Connect a 100kΩ pullup resistor to the IN pin. Tie to AGND if not used.
15	SCL (CONFIG3)	SCL/Configuration 3. For the I²C variants, this serves as the SCL pin. For the standalone variants, this serves as CONFIG3 pin. Connect a resistor to AGND to configure gain and current limit. See Table 6.
16	SDA (CONFIG2)	SDA/Configuration 2. For the I²C variants, this serves as the SDA pin. For the standalone variants, this serves as the CONFIG2 pin. Connect a resistor to AGND to configure cable compensation. See Table 6.

Pin Description (continued)

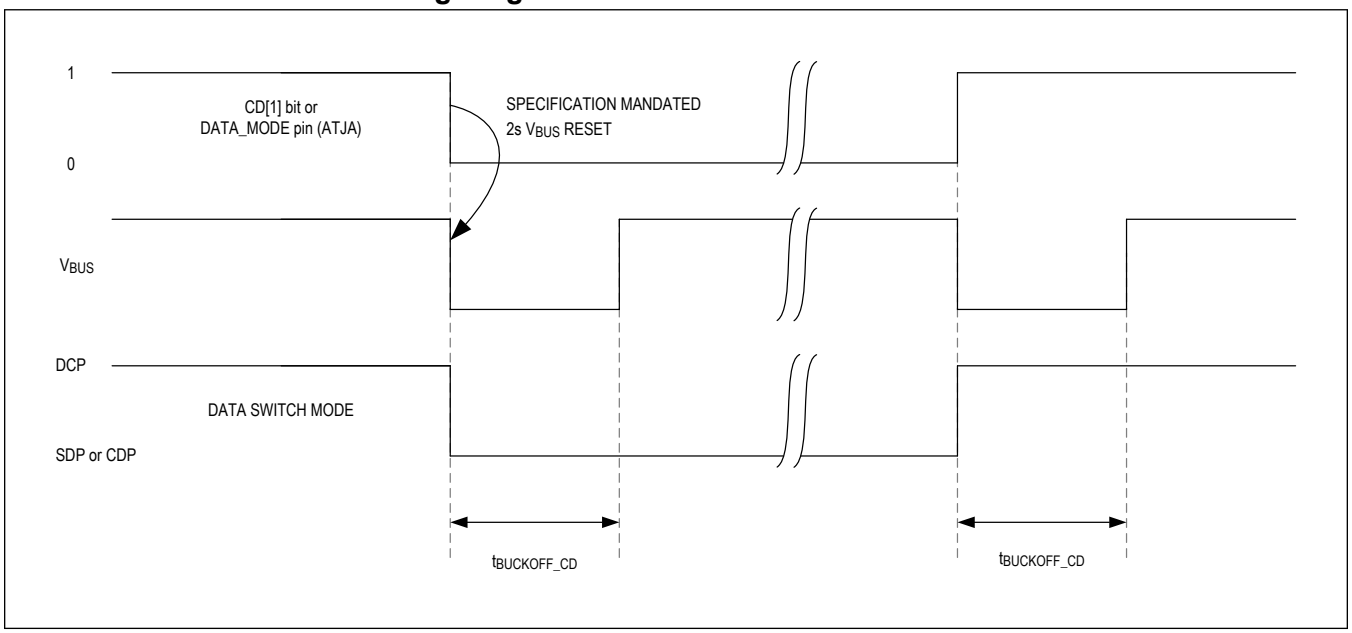
PIN	NAME	FUNCTION
17	DATA_MODE	Selects Between the Two Default Modes of Data Switch Operation. See Table 3.
18	ENBUCK	DC-DC Enable Input. Drive high/low to enable/disable the buck converter.
19	BST	High-Side Driver Supply. Connect a 0.1µF capacitor from BST to LX.
20, 21	LX	Inductor Connection. Connect an inductor from LX to the DC-DC converter output (SENSP).
22, 23	PGND	Power Ground
24	CONFIG1	Config1 input. Connect a resistor to GND or directly to BIAS. See Table 4 and Table 5.
25	HVEN	Active-High System Enable. HVEN is battery-voltage tolerant.
26, 27	SUPSW	Internal High-Side Switch Supply Input. V_{SUPSW} provides power to the internal switch and LDO. Connect a 10µF ceramic capacitor in parallel with a 47µF electrolytic capacitor from SUPSW to PGND. See the *DC-DC Switching Frequency Selection* section.
28	VBMON	USB V_{BUS} Monitor.
29	SENSP	DC-DC Converter Feedback Input and Current-Sense Amplifier Positive Input. DC-DC bulk capacitance placed here. Connect to positive terminal of current-sense resistor and the main output of the converter. Used for internal voltage regulation loop.
30	SENSN	Current-Sense Amp Negative Input. Connect to negative terminal of current sense resistor.
31	N.C.	No Connection
32	BIAS	5V Linear Regulator Output. Connect a 2.2µF ceramic capacitor from BIAS to GND. BIAS powers the internal circuitry.
—	EP	Exposed Pad. Connect EP to multiple GND planes with 3 x 3 via grid (minimum).

Functional Diagrams

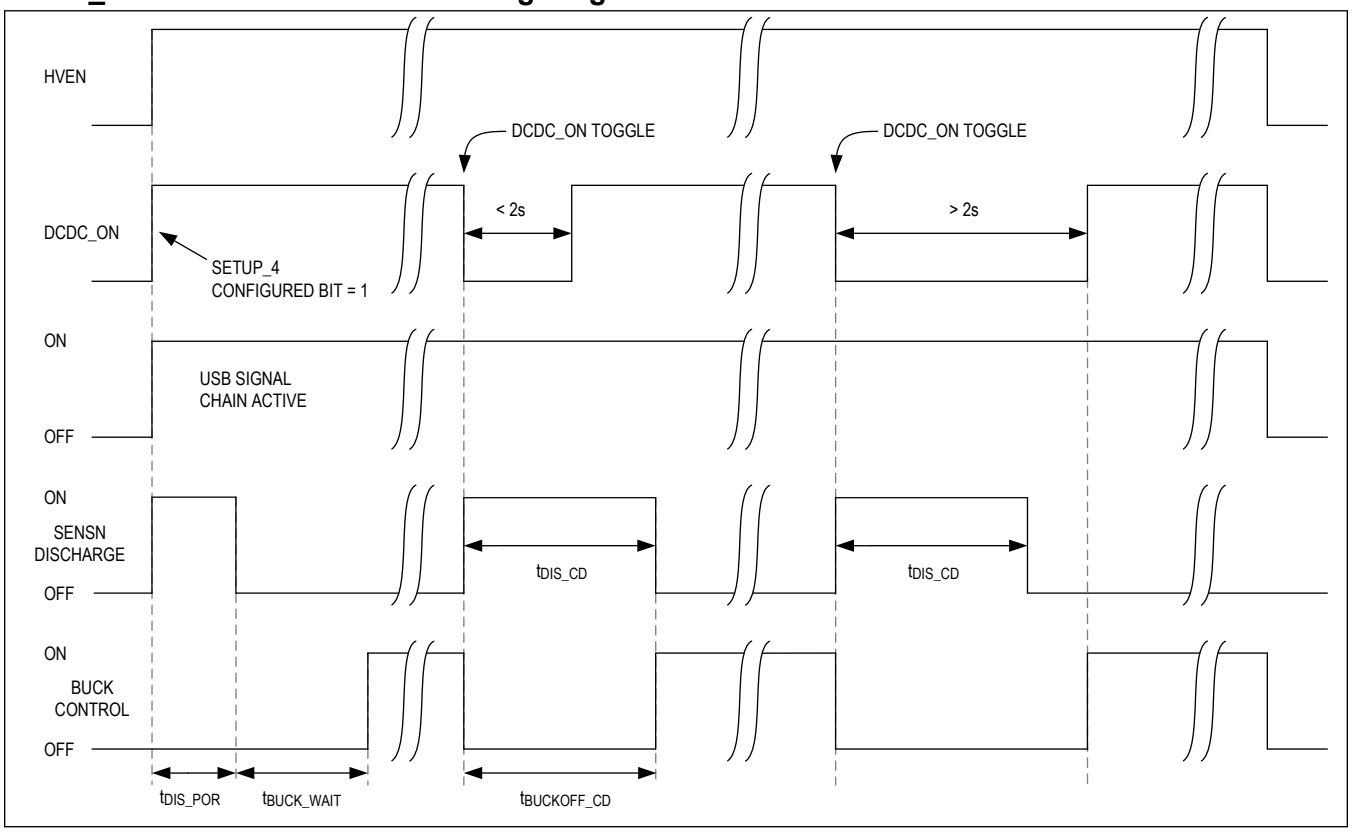
On-Channel -3dB Bandwidth and Crosstalk



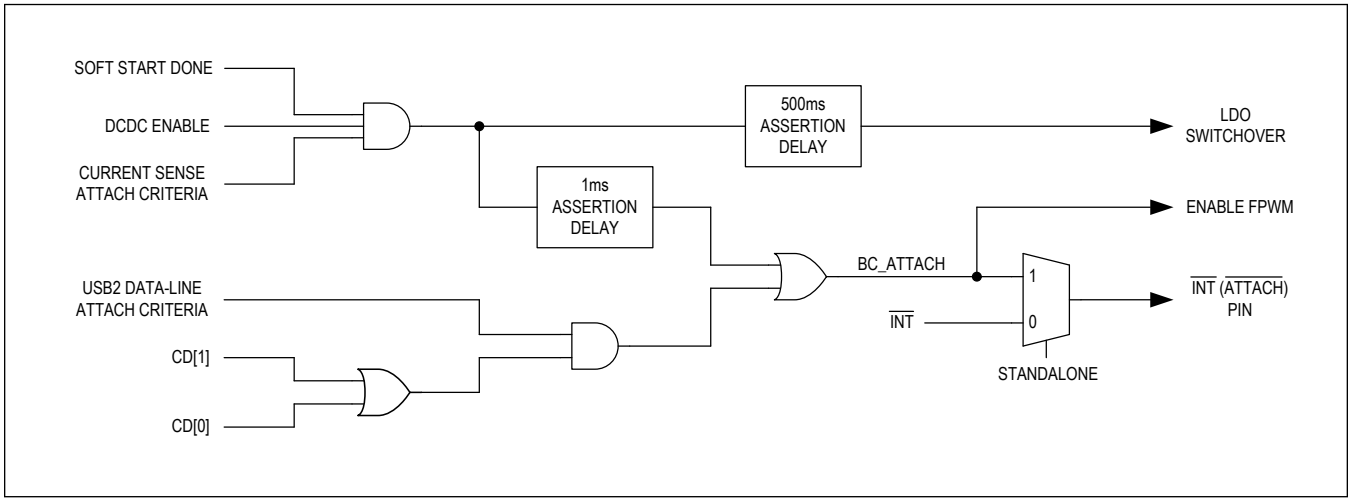
DCP Reset Behavior and Timing Diagram



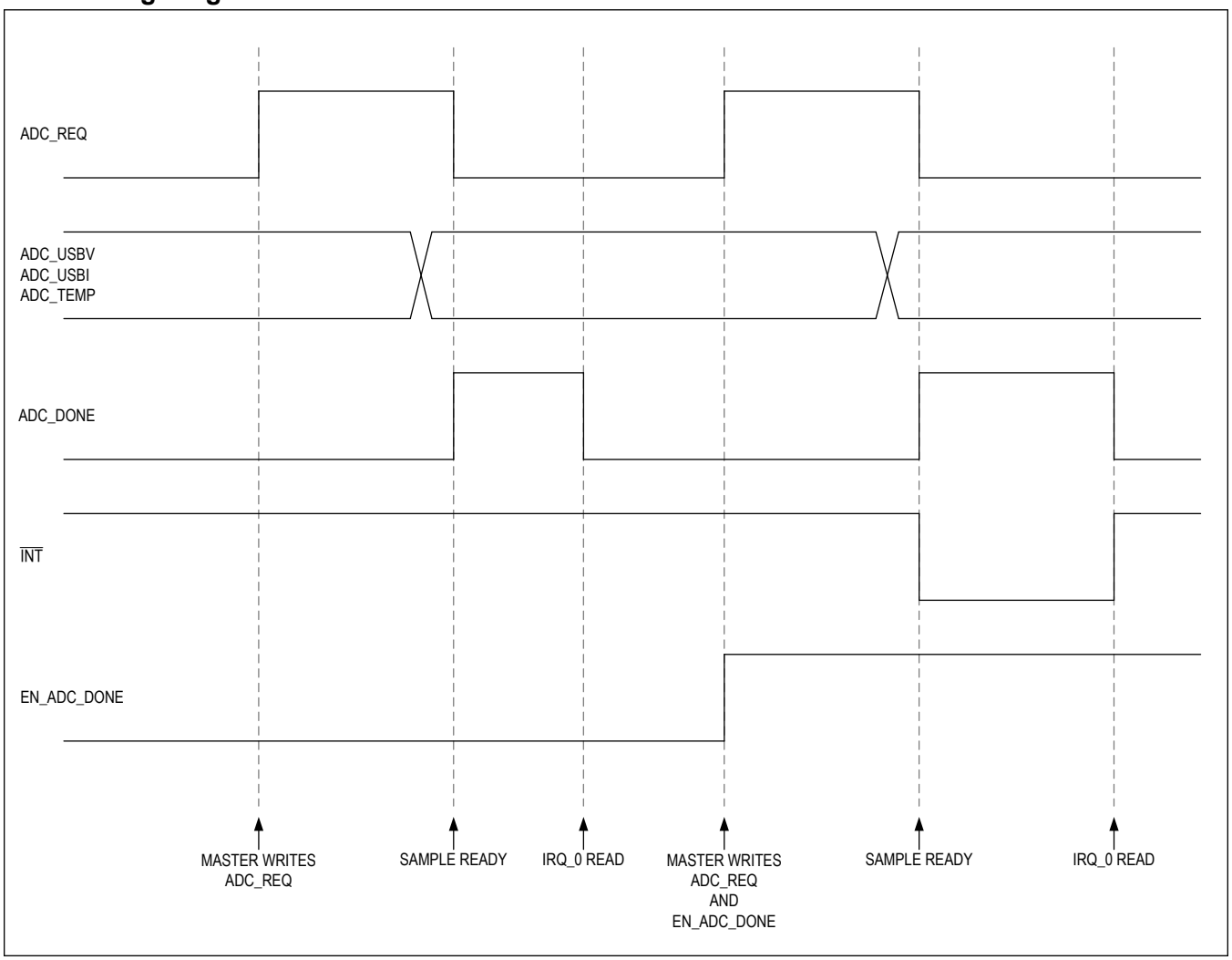
DCDC_ON Reset Behavior and Timing Diagram



ATTACH Logic Diagram



ADC Timing Diagram



Detailed Description

The MAX16984A combines a 5V/3A automotive grade step-down converter, a USB host charger adapter emulator, and USB protection switches. The device variants offer options for both standalone/GPIO and I^2C configuration and control. This device family is designed for high-power USB ports in automotive radio, navigation, connectivity, USB hub, and dedicated charging applications.

The USB protection switches provide high-ESD and short- circuit protection for the low-voltage internal data lines of the multimedia processor's USB transceiver and support USB Hi-Speed (480Mbps) and USB Full-Speed (12Mbps) pass-through operation. The MAX16984A features integrated host-charger port-detection circuitry adhering to the USB 2.0 Battery Charging Specification BC1.2 and also includes dedicated bias resistors for Samsung 2.0A/iPod/iPhone/iPad 2.4A dedicated charging modes.

The high-efficiency step-down DC-DC converter operates from a voltage up to 28V and is protected from load-dump transients up to 40V. The device includes resistor-programmable frequency selection from 310kHz to 2.2MHz to allow optimization of efficiency, noise, and board space based on the application requirements. The converter can deliver up to 3A of continuous current at 125°C.

The MAX16984A also includes a high-side current-sense amplifier and configurable feedback-adjustment circuit designed to provide automatic USB voltage adjustment to compensate for voltage drops in captive cables associated with automotive applications.

Detailed Block Diagram

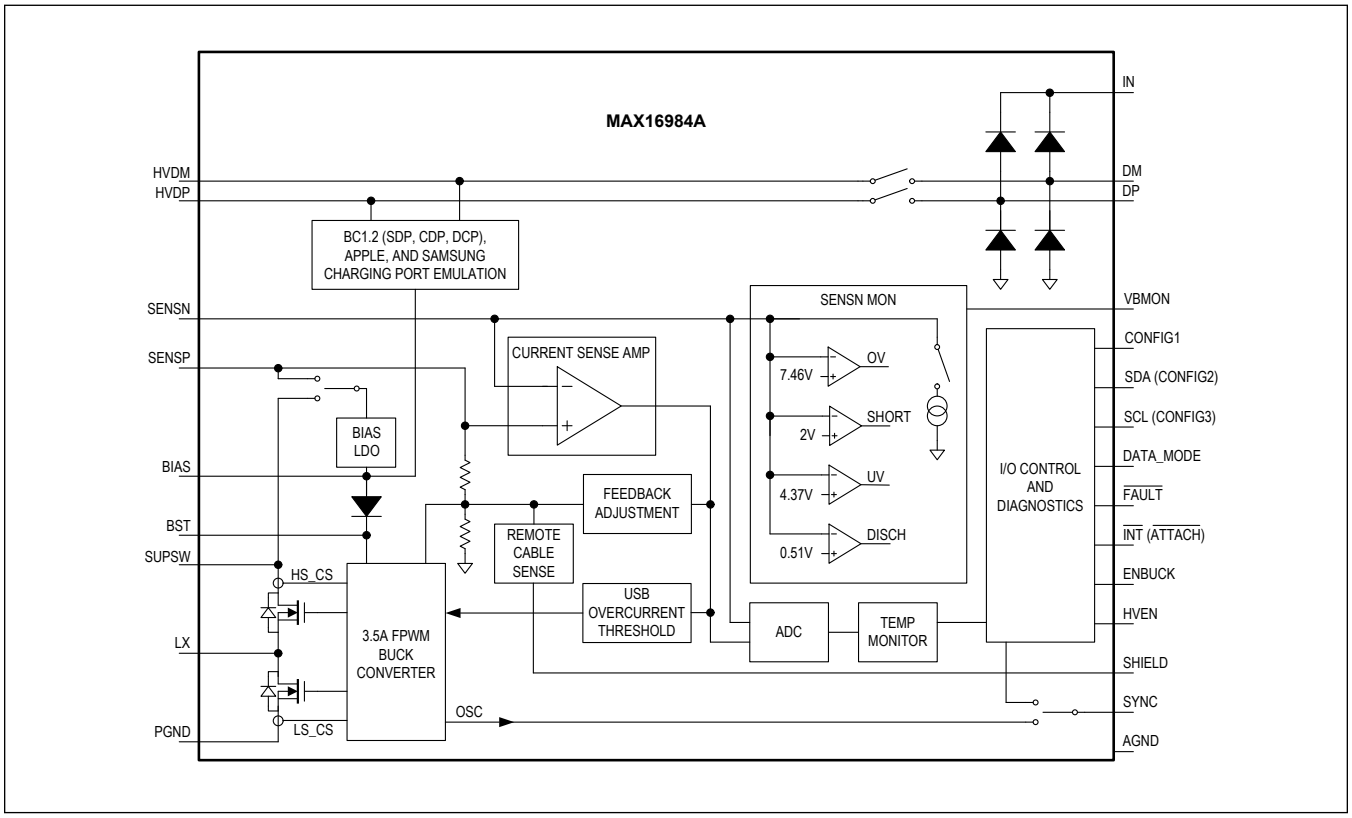


Figure 1. Detailed Block Diagram

Power-Up and Enabling

System Enable (HVEN)

HVEN is used as the main enable to the device and initiates system start-up and configuration. If HVEN is at a logic-low level, SUPSW power consumption is reduced and the device enters a standby, low quiescent current level. HVEN is compatible with inputs from 3.3V logic up to automotive battery. After a system reset (e.g., HVEN toggle, BIAS UV), the I^2C variant asserts the INT pin to indicate that the IC has not been configured. The buck converter is forced off until the CONFIGURED bit of SETUP_4 is written to a 1. This ensures that a portable device cannot attach before the IC registers are correctly set for the application.

DC-DC Enable (ENBUCK)

The buck regulator on the MAX16984A is controlled by the ENBUCK pin for standalone variants, and by both the ENBUCK pin and the I^2C interface for I^2C variants. DCDC_ON, the logical AND of ENBUCK and EN_DCDC, determines if the buck converter can be enabled. On standalone variants, EN_DCDC is always high and only ENBUCK can be used to enable the buck converter. On I^2C variants, setting ENBUCK low overrides an I^2C EN_DCDC enable command, which allows compatibility with USB hub controllers. For a typical USB hub application, connect ENBUCK to the enable output of the USB hub controller. This allows the USB hub controller to enable and disable the USB power port using software commands. ENBUCK can be directly connected to the BIAS or IN pin for applications that do not require GPIO control of the DC-DC converter enable.

3.3V Input (IN)

IN is used to clamp the D+ and D- pins during an ESD or overvoltage event on the HVD+ and HVD- pins. This clamping protects the downstream USB transceiver. The presence of these clamping diodes requires that IN remain set to 3.3V at all times for USB communication to occur. The IN pin features an overvoltage lockout that disables the data switches if IN is above V_{IN_OVLO}. Bypass IN with a 1µF ceramic capacitor, place it close to the IN pin, and connect it to the same 3.3V supply that is shared with the multimedia processor or hub transceiver.

Linear Regulator Output (BIAS)

BIAS is the output of a 5V linear regulator that powers the internal logic and control circuitry for the device. BIAS is internally powered from SUPSW or SENSP and automatically powers up when HVEN is high and SUPSW voltage exceeds V_{UV_SUPSW}. The BIAS output contains an undervoltage lockout that keeps the internal circuitry disabled when BIAS is below V_{UV_BIAS}. The linear regulator automatically powers down when HVEN is low, and a low shutdown current mode is entered. Bypass BIAS to GND with a 2.2µF ceramic capacitor.

Power-On Sequencing

HVEN, ENBUCK, and IN do not have a power-up sequence requirement by design. However, the desired system behavior should be considered for the state of these pins at startup. The D+ and D- pins are clamped to IN, therefore IN should be set to 3.3V before any USB communication is required. It is recommended that IN is set to 3.3V before HVEN is set high. ENBUCK acts as the master disable for the DC-DC converter. If ENBUCK is low when HVEN is set high, all variants keep the buck converter in the disabled state until ENBUCK is set high.

Step-Down DC-DC Regulator

Step-Down Regulator

The MAX16984A features a current-mode, step-down converter with integrated high-side and low-side MOSFETs. The low-side MOSFET enables fixed-frequency, forced-PWM operation under light loads. The DC-DC regulator features a cycle-by-cycle current limit and intelligent transition from skip mode to forced-PWM mode that makes the device ideal for automotive applications.

Wide Input Voltage Range

The device is specified for a wide 4.5V to 28V input voltage range. SUPSW provides power to the internal BIAS linear

regulator and internal power switch. Certain conditions such as cold cranking can cause the voltage at the output to drop below the programmed output voltage. Under such conditions, the device operates in a high duty-cycle mode to facilitate minimum dropout from input to output.

Maximum Duty-Cycle Operation

The MAX16984A has a maximum duty cycle of 98% (typ). The IC monitors the off-time (time for which the low-side FET is on) in both PWM and skip modes for every switching cycle. Once the off-time of 150ns (typ) is detected continuously for 7.5µs, the low-side FET is forced on for 60ns (typ) every 7.5µs. The input voltage at which the device enters dropout changes depending on the input voltage, output voltage, switching frequency, load current, and design efficiency. The input voltage at which the devices enter dropout can be approximated as:

$$V_{SUPSW} = \frac{V_{OUT} + \left(I_{LOAD} \times R_{ONH}\right)}{0.98}$$

Note: The equation above does not take into account the efficiency and switching frequency but will provide a good first-order approximation. Use the R_{ONH} number from the maximum column in the *Electrical Characteristics* table.

Output Voltage (SENSP)

The device features a precision internal feedback network that is connected to SENSP and that is used to set the output voltage of the DC-DC converter. The network nominally sets the average DC-DC converter output voltage to 5.15V in forced-PWM and 5.25V in skip mode.

Soft-Start

When the DC-DC converter is enabled, the regulator soft-starts by gradually ramping up the output voltage from 0V to 5.15V over approximately 8ms. This soft-start feature reduces inrush current during startup. Soft-start is guaranteed into compliant USB loads (see the *USB Loads* section).

Reset Behavior

The MAX16984A implements a discharge function on SENSN any time that the DC-DC regulator is disabled for any reason. When the discharge function is activated, current (I_{SENSN_DIS}) is drained through a current-limited FET, and a reset timer is also started. This timer prevents the DC-DC regulator from starting up again until the timer has expired. This allows for easy compatibility with USB specifications and removes the need for long discharge algorithms to be implemented in system software. See the relevant *Functional Diagrams* for reset timer details.

Reset Criteria

The MAX16984A DC-DC converter automatically resets for all undervoltage, overvoltage, overcurrent and overtemperature fault conditions. See Table 8 for details. The fault retry timer is configurable in the SETUP_3 register. This timer is activated after a fault condition is removed and prevents the buck converter from switching on until the timer expires.

Another internal retry timer is enabled after DCDC_ON is set low or a transition of the CD[1] bit (switching between a data mode and a dedicated charging mode). DCDC_ON toggle causes buck shutdown and prevent the buck from switching on until $t_{BUCKOFF\_CD}$ expires.

Switching Frequency Configuration

The DC-DC switching frequency can be referenced to an internal oscillator or from an external clock signal on the SYNC pin. The internal oscillator frequency is set by the FSW[2:0] bits of the SETUP_1 register, which has a POR value corresponding to 2.2MHz. The internal oscillator can be programmed through I^2C to eight discrete values from 310kHz to 2.2MHz. For standalone variants, the f_{SW} configuration value is loaded from the CONFIG1 pin at startup with four discrete values from 310kHz to 2.2MHz available.

Switching Frequency Synchronization (SYNC Pin)

When the SYNC pin is configured to operate as an output, skip mode operation is disallowed, and the internal oscillator frequency is driven by the SYNC pin. This allows other devices to synchronize with the MAX16984A 180 degrees out of

phase for EMI reduction.

When SYNC is configured as an input, the SYNC pin becomes a logic-level input that can be used for both operating-mode selection and frequency control. Connecting SYNC to GND or an external clock enables fixed-frequency, forced-PWM mode. Connecting SYNC to a logic-high signal allows intelligent skip-mode operation. The device can be externally synchronized to frequencies within ±20% of the programmed internal oscillator frequency.

Forced-PWM Operation

In forced-PWM mode, the device maintains fixed-frequency PWM operation over all load conditions, including no-load conditions.

Intelligent Skip-Mode Operation and Attach Detection

When the SYNC pin is configured as an input, but neither a clocked signal nor a logic-low level exists on the SYNC pin, the MAX16984A operates in skip mode at very light load/no load conditions. Intelligent device attach detection is used to determine when a device is attached to the USB port. The device intelligently exits skip mode and enters forced-PWM mode when a device is attached and remains in forced-PWM mode as long as the attach signal persists. This minimizes the EMI concerns caused by automotive captive USB cables and poorly shielded consumer USB cables. The device attach event is also signaled by the ATTACH pin (standalone variants) or ATTACH bits (I^2C variants). The criteria for device attach detection and intelligent skip-mode operation are shown in Table 1.

Table 1. DC-DC Converter Intelligent Skip Mode Truth Table

SYNC PIN	SYNC_DIR	DATA SWITCH CHARGE DETECTION MODE	CDP ATTACH DETECTION	DCP ATTACH DETECTION	CURRENT SENSE ATTACH DETECTION	DC-DC CONVERTER OPERATION
x	OUT	x	x	x	x	Forced-PWM Mode: Continuous
0	IN	x	x	x	x	Forced-PWM Mode: Continuous
Clocked	IN	x	x	x	x	Forced-PWM Mode: Continuous
1	IN	High-Speed Pass Through (SDP) Mode	x	x	0	Intelligent Skip Mode: No Device Attached
1	IN	High-Speed Pass Through (SDP) Mode	x	x	1	Forced-PWM Mode: Device Attached
1	IN	BC1.2 Auto CDP Mode	0	x	0	Intelligent Skip Mode: No Device Attached
1	IN	BC1.2 Auto CDP Mode	1	x	x	Forced-PWM Mode: Device Attached
1	IN	BC1.2 Auto CDP Mode	x	x	1	Forced-PWM Mode: Device Attached
1	IN	2.4A Auto DCP Mode	x	0	0	Intelligent Skip Mode: No Device Attached

Table 1. DC-DC Converter Intelligent Skip Mode Truth Table (continued)

SYNC PIN	SYNC_DIR	DATA SWITCH CHARGE DETECTION MODE	CDP ATTACH DETECTION	DCP ATTACH DETECTION	CURRENT SENSE ATTACH DETECTION	DC-DC CONVERTER OPERATION
1	IN	2.4A Auto DCP Mode	x	1	x	Forced-PWM Mode: Device Attached
1	IN	2.4A Auto DCP Mode	x	x	1	Forced-PWM Mode: Device Attached

Spread-Spectrum Option

Spread-spectrum operation is offered to improve the EMI performance of the MAX16984A. Spread-spectrum operation is enabled by the SS_EN bit of the SETUP_0 register, which is preloaded on startup from the CONFIG1 pin for both standalone and I^2C variants. The internal operating frequency modulates the switching frequency by up to ±3.4% relative to the internally generated operating frequency. This results in a total spread-spectrum range of 6.8%. Spread-spectrum mode is only active when operating from the internal oscillator. Spread-spectrum clock dithering is not possible when operating from an external clock.

Current Limit

The MAX16984A limits the USB load current using both a fixed internal peak current threshold of the DC-DC converter, as well as a user-programmable external DC load current-sense amplifier threshold. This allows the current limit to be adjusted between 500mA to 3A depending on the application requirements, while protecting the system in the event of a fault. Upon exceeding either the DC-DC peak or user-programmable current thresholds, the high-side FET is immediately switched off and current-limit algorithms are initiated. When the external current limit lasts for longer than 16ms, the $\overline{FAULT}$ pin asserts and the VBUS_ILIM bit of the IRQ_1 register is set. Once the load current exceeds the programmed threshold, the DC-DC converter acts as a constant-current source. This may cause the output voltage to droop. The ILIM_ITRIP bit of the SETUP_2 register determines the output voltage droop required to initiate a DC-DC converter reset during VBUS_ILIM. When ILIM_ITRIP = 0, the USB current limit is detected for 16ms and the output voltage falls below V_{UV_SENSN}, the DC-DC converter resets. The DC-DC converter also resets if the internal LX peak current threshold is exceeded for four consecutive switching cycles and the output voltage droops to less than 2.0V.

In some cases, the designer may want to increase the load to 160%, refer to *USB Output Current Limit* for details.

Output Short-Circuit Protection

The DC-DC converter output (SENSP, SENSN) is protected against both short-to-ground and short-to-battery conditions. If a short-to-ground or undervoltage condition is encountered, the DC-DC converter immediately resets, asserts the $\overline{FAULT}$ pin, flags the fault in the IRQ_1 register, and then reattempts soft-start after the 2s reset delay. This pattern repeats until the short circuit has been removed. If a short-to-battery is encountered ($V_{SENSN} > V_{OV\_SENSN}$), the buck converter shuts down, the $\overline{FAULT}$ pin is asserted, and the fault is flagged in the IRQ_1 register. The buck converter stays shut down until the fault condition resolves and the 2s timer expires.

Thermal Overload Protection

Thermal-overload protection limits the total power dissipated by the device. A thermal protection circuit monitors the die temperature. If the die temperature exceeds +165°C, the device shuts down, so it can cool. Once the device has cooled by 10°C, the device is enabled again. This results in a pulsed output during continuous thermal-overload conditions, protecting the device during fault conditions. For continuous operation, do not exceed the absolute maximum junction temperature of +150°C. See the Thermal Considerations section for more information.

Pre-Thermal Overload Warning

The MAX16984A I^2C variants feature a thermal overload warning flag which sets the THM_WARN bit of the IRQ_2 register when the die temperature crosses +140°C. This allows a system software implementation of thermal foldback or load shedding algorithms to prevent a thermal overload condition.

USB Current Limit and Output Voltage Adjustment

Current-Sense Amplifier (SENSP, SENSN)

MAX16984A features an internal USB load current-sense amplifier to monitor the DC load current delivered to the USB port. The V_{SENSE} voltage (V_{SENSP} - V_{SENSN}) is used internally to provide precision DC current-limit and voltage-compensation functionality. A 33mΩ sense resistor should be placed between SENSP and SENSN.

In some cases, the designer may want to increase the load to 160%, refer to *USB Output Current Limit* for details.

USB DC Current Limit Configuration

The MAX16984A allows configuration of the precision DC current limit by the ILIM[2:0] bits of the SETUP_2 register. I^2C configuration enables selection of eight discrete DC current limit values. See SETUP_2 for current limit configuration values.

Standalone variants of the device allow selection of a subset of the eight available current limit options by reading the CONFIG3 resistor. See Table 6 and the *Applications Information* section for more information.

In some cases, the designer may want to increase the load to 160%, refer to *USB Output Current Limit* for details.

Voltage Feedback Adjustment Configuration

The MAX16984A compensates voltage drop for up to 474mΩ of USB cable in typical USB charging applications. I^2C variants of the device allow this configuration by the GAIN[4:0] bits of the SETUP_1 register. See GAIN[4:0] for voltage gain configuration. Standalone variants of the device allow configuration by the CONFIG2 resistor, which sets GAIN[3:0], and the CONFIG3 resistor, which sets GAIN[4]. See the SETUP_1 register map and the *Applications Information* section for more information.

In some cases, the designer may want to increase the load to 160%, refer to *USB Output Current Limit* for details.

Remote-Sense Feedback Adjustment

The remote-sense feature (available by custom order only) provides another option to adjust the output voltage by sensing the ground node on the USB port at the far-end of the captive cable; either with the cable shield or with an additional sensing wire. This feature automatically senses the cable resistance and adjusts the voltage compensation without changing the GAIN[4:0] setting.

The user needs to compensate the voltage drop because of the sense resistor, the load line behavior of the buck, and any difference between the V_{BUS} and GND conductors. See Figure 2 and contact the factory for support and how to order.

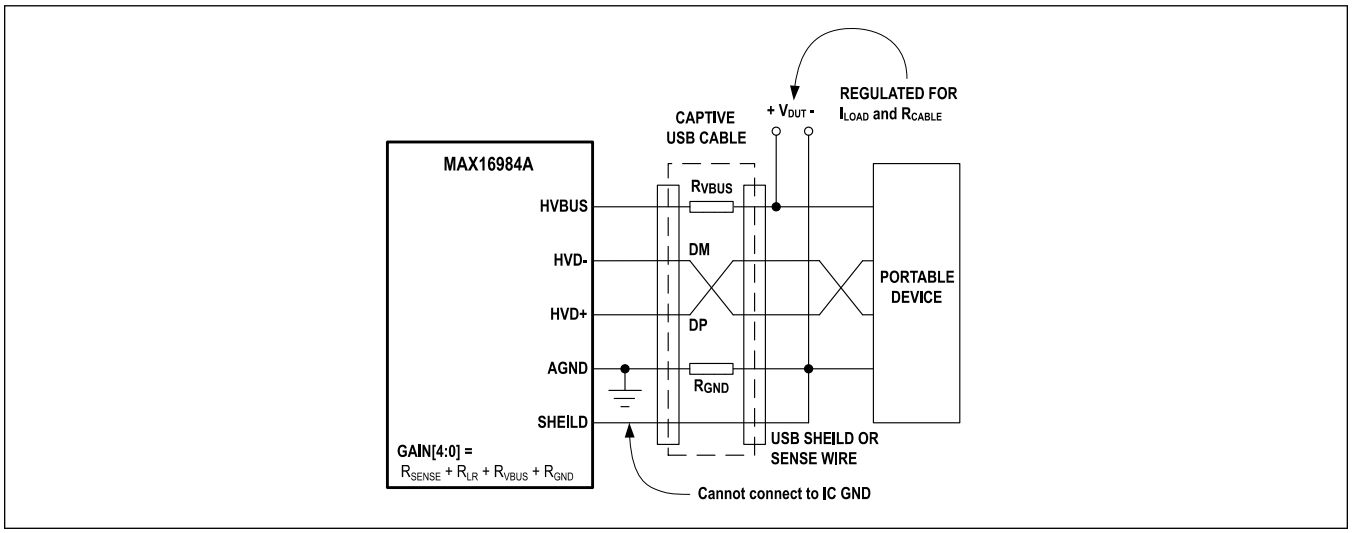


Figure 2. Remote Cable-Sense Diagram

USB Protection Switches and BC1.2 Host Charger Emulation

USB Protection Switches

MAX16984A provides automotive-grade ESD and shortcircuit protection for the low-voltage USB data lines of high-integration multimedia processors. HVDP/HVDM protection consists of ESD and OVP (overvoltage protection) for 1.5Mbps, 12Mbps, and 480Mbps USB transceiver applications. This is accomplished with a very low-capacitance FET in series with the D+ and D- data paths.

The MAX16984A high-voltage variant does not require an external ESD array, and protects the HVD+ and HVD pins to ±15kV Air-Gap/±8kV Contact Discharge with the 150pF/330Ω IEC 61000-4-2 model and the 330pF/330Ω model, as well as protecting up to ±15kV Air-Gap/±8kV Contact Discharge with the 330pF/2kΩ ISO 10605 model. The MAX16984A provides robust, automotive-grade protection while maintaining a 1GHz -3dB insertion loss. This ensures optimum eye diagram at the end of a captive cable. The HVD+ and HVD- short-circuit protection features include protection for a short to the USB +5V BUS and a short to the +18V car battery. These protection features prevent damage to the low-voltage USB transceiver when shorts occur in the vehicle harness or customer USB connector/cable. Short-to-GND protection is provided by the upstream USB transceiver.

USB Host Charger Emulator

The USB protection switches integrate the latest USB-IF Battery Charging Specification Revision 1.2 SDP, CDP and DCP circuitry, as well as 2.4A resistor bias for Apple-compliant devices. Legacy Samsung Galaxy 1.2V divider and China YD/T1591-2009 compatibility is also provided in DCP mode.

Table 2. Data Switch Mode Truth Table (I^2C Variants)

PART NUMBER	DEVICE INPUTS					SA	SB	DATA SWITCH MODE
	HVEN	IN	CD[1]	CD[0]	DATA_MODE			
MAX16984AATJC, MAX16984AATJM	0	X	X	X	X	0	0	Off
	1	0	X	X	1	Invalid Mode (IN = 3.3V required for all modes)		
	1	0	0	X	0	Invalid Mode (IN = 3.3V required for all modes)		
	1	1	0	0	0	1	0	Hi-Speed Pass-Through (SDP)
	1	1	0	1	0	On if CDP = 0	On if CDP = 1	BC1.2 Auto-CDP (CDP)
	1	1	X	X	1	On if CDP = 0	On if CDP = 1	BC1.2 Auto-CDP (CDP)
	1	1	1	0	0	0	1	Auto-DCP/Apple 2.4A (DCP)
	1	1	1	1	0	0	1	Auto-DCP/Apple 1A (DCP)

Table 3. Data Switch Mode Truth Table (Standalone Variants)

PART NUMBER	DEVICE INPUTS			SA	SB	DATA SWITCH MODE
	HVEN	IN	DATA_MODE			
X	0	X	X	0	0	Off
	1	0	X	Invalid Mode (IN = 3.3V required for all modes)		
MAX16984AATJB, MAX16984AATJN	1	1	0	1	0	Hi-Speed Pass-Through (SDP)
	1	1	1	On if CDP = 0	On if CDP = 1	BC1.2 Auto-CDP (CDP)
MAX16984AATJA	1	1	0	On if CDP = 0	On if CDP = 1	BC1.2 Auto-CDP (CDP)
	1	1	1	0	1	Auto-DCP/Apple 2.4A (DCP)

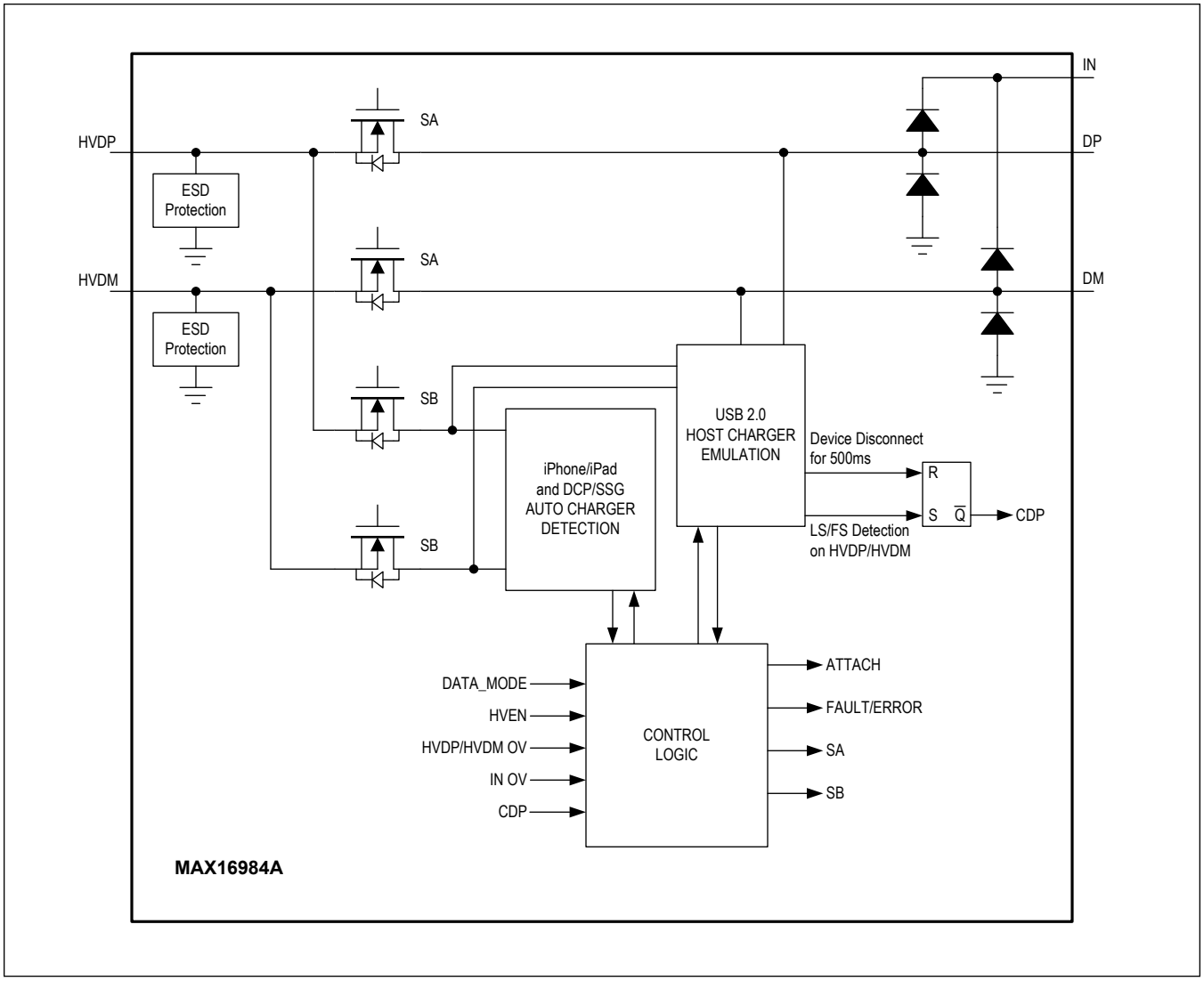


Figure 3. Data Switch and Charge-Detection Block Diagram

USB On-The-Go and Dual-Role Applications

The MAX16984A is fully compatible with USB on-the-go (OTG) and dual-role applications. A negotiated role swap (HNP or Apple CarPlay) requires no software interaction with the IC. When there is no negotiation before the SOC enters peripheral mode, the MAX16984A must be in Hi-Speed pass-through (SDP mode) before and during the role swap. All variants except MAX16984AATJA default to SDP mode on startup if the DATA_MODE pin is logic-low. This configuration allows a role swap immediately on startup without microcontroller interaction.

I²C, Control, and Diagnostics

I²C Configuration (CONFIG1 and I²C)

The MAX16984A I²C variants allow basic device configuration through a resistor placed to GND on the CONFIG1 pin. The configuration parameters correlating to the chosen resistor are preloaded into their respective I²C registers on startup when HVEN is toggled high. After startup, the user is free to change the affected I²C registers as desired.

For I²C variants, CONFIG1 sets the startup value of the DC-DC spread-spectrum enable bit SS_EN and the SYNC

direction control bit SYNC_DIR. CONFIG1 also sets the LSBs of the I²C slave address. The configuration table for the I²C variant CONFIG table is shown in Table 4.

Table 4. CONFIG1 Pin Table (I²C Variants)

RESISTANCE (Ω, typ)	STEP	SS_EN	SYNC_DIR	I²C_ADDR LSBs
Short to GND	**0**	1 (ON)	1 (IN)	00
619	**1**	1 (ON)	1 (IN)	01
976	**2**	1 (ON)	1 (IN)	10
1370	**3**	1 (ON)	1 (IN)	11
1820	**4**	1 (ON)	0 (OUT)	00
2370	**5**	1 (ON)	0 (OUT)	01
3090	**6**	1 (ON)	0 (OUT)	10
3920	**7**	1 (ON)	0 (OUT)	11
4990	**8**	0 (OFF)	1 (IN)	00
6340	**9**	0 (OFF)	1 (IN)	01
8250	**10**	0 (OFF)	1 (IN)	10
11000	**11**	0 (OFF)	1 (IN)	11
15400	**12**	0 (OFF)	0 (OUT)	00
23700	**13**	0 (OFF)	0 (OUT)	01
44200	**14**	0 (OFF)	0 (OUT)	10
Short to BIAS (or R > 71.5kΩ)	**15**	0 (OFF)	0 (OUT)	11

Standalone Configuration (CONFIG1–CONFIG3)

The MAX16984A standalone variants allow full device configuration from three resistors placed among the three CONFIG pins and GND. For standalone variants, SDA and SCL serve as CONFIG2 and CONFIG3, respectively.

CONFIG1 sets the internal oscillator switching frequency, SYNC pin direction, and DC-DC spread spectrum mode. CONFIG2 sets the 4 LSBs of the voltage adjustment gain (GAIN[3:0]). CONFIG3 sets the USB DC current limit, and MSB of voltage adjustment gain (GAIN[4]). See Table 5 and Table 6 for standalone variant CONFIG options. See the *Applications Information* section for setting selection and *Ordering Information* for variant part number information.

In some cases, the designer may want to increase the load to 160%, refer to *USB Output Current Limit* for details.

Table 5. CONFIG1 Pin Table (Standalone Variants)

RESISTANCE (Ω, typ)	STEP	SS_EN	SYNC_DIR	FSW (kHz)
Short to GND	**0**	ON	IN	2200
619	**1**	ON	IN	488
976	**2**	ON	IN	350
1370	**3**	ON	IN	310
1820	**4**	ON	OUT	2200
2370	**5**	ON	OUT	488
3090	**6**	ON	OUT	350
3920	**7**	ON	OUT	310
4990	**8**	OFF	IN	2200
6340	**9**	OFF	IN	488
8250	**10**	OFF	IN	350
11000	**11**	OFF	IN	310

Table 5. CONFIG1 Pin Table (Standalone Variants) (continued)

RESISTANCE (Ω, typ)	STEP	SS_EN	SYNC_DIR	FSW (kHz)
15400	**12**	OFF	OUT	2200
23700	**13**	OFF	OUT	488
44200	**14**	OFF	OUT	350
Short to BIAS (or R > 71.5kΩ)	**15**	OFF	OUT	310

Table 6. CONFIG2 and CONFIG3 Pin Table (Standalone Variants)

		CONFIG2	CONFIG3	
RESISTANCE (Ω, typ)	**STEP**	**GAIN[3:0]**	**GAIN[4]**	**CURRENT LIMIT ILIM_SET (A)**
Short to GND	**0**	0b0000	0	0.55
619	**1**	0b0001	0	1.62
976	**2**	0b0010	0	2.60
1370	**3**	0b0011	0	3.04
1820	**4**	0b0100	1	0.55
2370	**5**	0b0101	1	1.62
3090	**6**	0b0110	1	2.60
3920	**7**	0b0111	1	3.04
4990	**8**	0b1000	X	
6340	**9**	0b1001		
8250	**10**	0b1010		
11000	**11**	0b1011		
15400	**12**	0b1100		
23700	**13**	0b1101		
44200	**14**	0b1110		
Short to BIAS (or R > 71.5kΩ)	**15**	0b1111		

I²C Diagnostics and Event Handling

The I²C-based diagnostic functionality is independent of the $\overline{\text{FAULT}}$ pin. Setting the IRQMASK bit for a specific fault condition does not mask the $\overline{\text{FAULT}}$ pin for the respective fault. IRQMASK register functionality affects only the behavior of the $\overline{\text{INT}}$ pin. This allows the $\overline{\text{FAULT}}$ pin to be tied to overcurrent fault input of a hub controller or SoC, while the I²C interface is simultaneously used by the system software for advanced diagnostic functionality.

Interrupt and Attach Output ($\overline{\text{INT}}$($\overline{\text{ATTACH}}$))

The MAX16984A $\overline{\text{INT}}$($\overline{\text{ATTACH}}$) pin functions as an interrupt ($\overline{\text{INT}}$) for I²C variants. The $\overline{\text{INT}}$ pin asserts an interrupt based on the configuration of the IRQ_MASK_0, IRQ_MASK_1, and IRQ_MASK_2 registers. Interrupt configuration allows the $\overline{\text{INT}}$ pin to assert any of the featured fault detection, as well as on device attachment, and USB voltage/current ADC conversion completion. The $\overline{\text{INT}}$ pin only asserts while a masked IRQ bit is asserted, which means its behavior is also dependent on the AUTOCLR bit.

Standalone variants of the MAX16984A feature an open-drain, active-low, $\overline{\text{ATTACH}}$ output that serves as the attach detection pin. For standalone variants, the $\overline{\text{ATTACH}}$ pin can be used for GPIO input to a microprocessor, or to drive an LED for attach/charge indication.

The $\overline{\text{INT}}$($\overline{\text{ATTACH}}$) assertion logic is shown in *ATTACH Logic Diagram*.

I²C Output Voltage and Current Measurement

The MAX16984A I²C variant allows measurement of the instantaneous SENSN voltage, DC output current, and die temperature using an integrated ADC. To initiate a measurement, set the ADC_REQ bit of the ADC_REQUEST register. The ADC_REQ bit is cleared by the IC once the measurement is complete and the ADC samples are available. Additionally, the ADC_DONE bit of the IRQ_0 register will be set when the sample is available. ADC_DONE can be masked to assert an interrupt when the sample is ready.

The sampled measurements can be read from the ADC_USBV, ADC_USBI, and ADC_TEMP registers. The new sample persists in the register until another sample request is initiated by setting the ADC_REQ bit.

All measurements provide 8 bits of resolution. The measured SENSN voltage has a range of 0V to 19.8V. Convert the sample to a voltage as follows

$$V_{SENSN} = \frac{19.8V}{256} \cdot \text{ADC\_USBV (Volts)}.$$

The measured SENSE voltage has a range from 0 to 116mV. Convert the sample to a current as follows

$$I_{LOAD} = \frac{116mV}{256} \cdot \frac{\text{ADC\_USBI}}{R_{SENSE}} \text{ (Amps)}.$$

The measured die temp has a range from -40ºC to 170ºC and a temperature resolution of 3.5ºC. Convert the sample to a die temperature by T_J = 3.5ºC · ADC_TEMP - 270 (ºC).

I²C Interface

The MAX16984A features an I²C, 2-wire serial interface consisting of a serial-data line (SDA) and a serial clock line (SCL). SDA and SCL facilitate communication between the MAX16984A and the master at clock rates up to 400kHz. The master, typically a microcontroller, generates SCL and initiates data transfer on the bus. Figure 4 shows the 2-wire interface timing diagram.

A master device communicates to the MAX16984A by transmitting the proper address followed by the data word. Each transmit sequence is framed by a START (S) or REPEATED START (Sr) condition and a STOP (P) condition. Each word transmitted over the bus is 8 bits long and is always followed by an acknowledge clock pulse. The MAX16984A SDA line operates as both an input and an open-drain output. A pullup resistor greater than 500Ω is required on the SDA bus.

The MAX16984A SCL line operates as an input only. A pullup resistor greater than 500Ω is required on SCL if there are multiple masters on the bus, or if the master in a single-master system has an open-drain SCL output. Series resistors in line with SDA and SCL are optional. The SCL and SDA inputs suppress noise spikes to assure proper device operation even on a noisy bus.

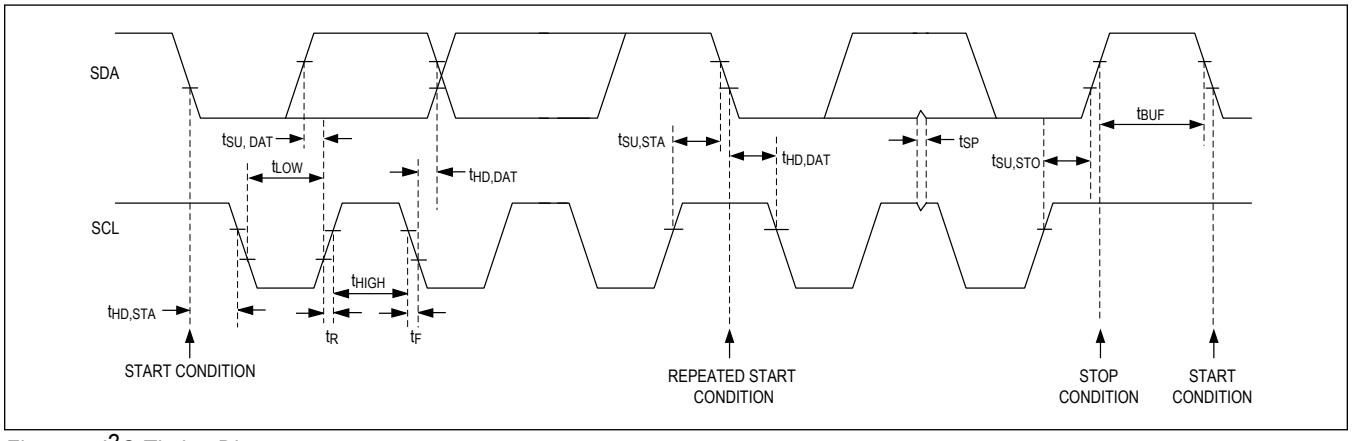


Figure 4. I²C Timing Diagram

Bit Transfer

One data bit is transferred during each SCL cycle. The data on SDA must remain stable during the high period of the

SCL pulse. Changes in SDA while SCL is high are considered control signals (see the STOP and START Conditions section). SDA and SCL idle high when the I²C bus is not busy.

STOP and START Conditions

A master device initiates communication by issuing a START condition. A START condition is a high-to-low transition on SDA with SCL high. A STOP condition is a low-to-high transition on SDA while SCL is high (Figure 5). A START (S) condition from the master signals the beginning of a transmission to the MAX16984A . The master terminates transmission, and frees the bus, by issuing a STOP (P) condition. The bus remains active if a REPEATED START (Sr) condition is generated instead of a STOP condition.

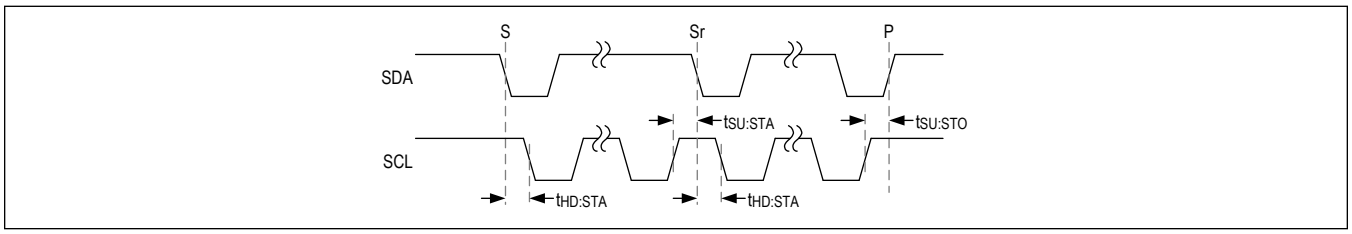


Figure 5. START, STOP and REPEATED START Conditions

Early STOP Condition

The MAX16984A recognizes a STOP condition at any point during data transmission, unless the STOP condition occurs in the same high pulse as a START condition.

Clock Stretching

In general the clock signal generation for the I²C bus is the responsibility of the master device. The I²C specification allows slow slave devices to alter the clock signal by holding down the clock line. The process in which a slave device holds down the clock line is typically called clock stretching. The MAX16984A does not use any form of clock stretching to hold down the clock line.

I²C General Call Address

The MAX16984A does not implement the I²C specifications general call address. If the MAX16984A sees the general call address (0b0000_0000), it does not issue an acknowledge.

I²C Slave Addressing

Once the device is enabled, the I²C slave address is set by the CONFIG1 pin.

The address is defined as the 7 most significant bits (MSBs) followed by the R/$\overline{W}$ bit. Set the R/$\overline{W}$ bit to 1 to configure the device to read mode. Set the R/$\overline{W}$ bit to 0 to configure the device to write mode. The address is the first byte of information sent to the device after the START condition.

Table 7. I²C Slave Addresses

CONFIG1 CODE	A6	A5	A4	A3	A2	A1	A0	7-BIT ADDRESS	WRITE	READ
0b00	0	1	1	0	0	0	0	0x30	0x60	0x61
0b01	0	1	1	0	0	0	1	0x31	0x62	0x63
0b10	0	1	1	0	0	1	0	0x32	0x64	0x65
0b11	0	1	1	0	0	1	1	0x33	0x66	0x67

Acknowledge

The acknowledge bit (ACK) is a clocked 9th bit that the device uses to handshake receipt each byte of data (Figure 6). The device pulls down SDA during the master generated 9th clock pulse. The SDA line must remain stable and low during the high period of the acknowledge clock pulse. Monitoring ACK allows for detection of unsuccessful data transfers. An unsuccessful data transfer occurs if a receiving device is busy or if a system fault has occurred. In the event

of an unsuccessful data transfer, the bus master can reattempt communication.

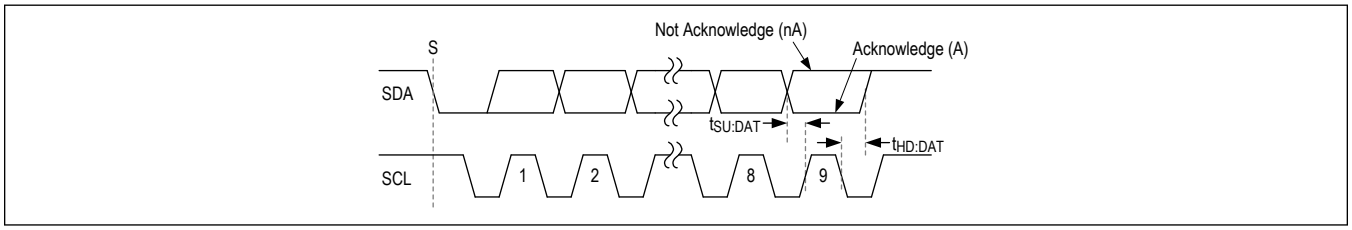


Figure 6. Acknowledge Condition

Write Data Format

A write to the device includes transmission of a START condition, the slave address with the write bit set to 0, one byte of data to a register address, one byte of data to the command register, and a STOP condition. Figure 7 illustrates the proper format for one frame.

Read Data Format

A read from the device includes transmission of a START condition, the slave address with the write bit set to 0, one byte of data from a register address, restart condition, the slave address with read bit set to 1, one byte of data to the command register, and a STOP condition. Figure 7 illustrates the proper format for one frame.

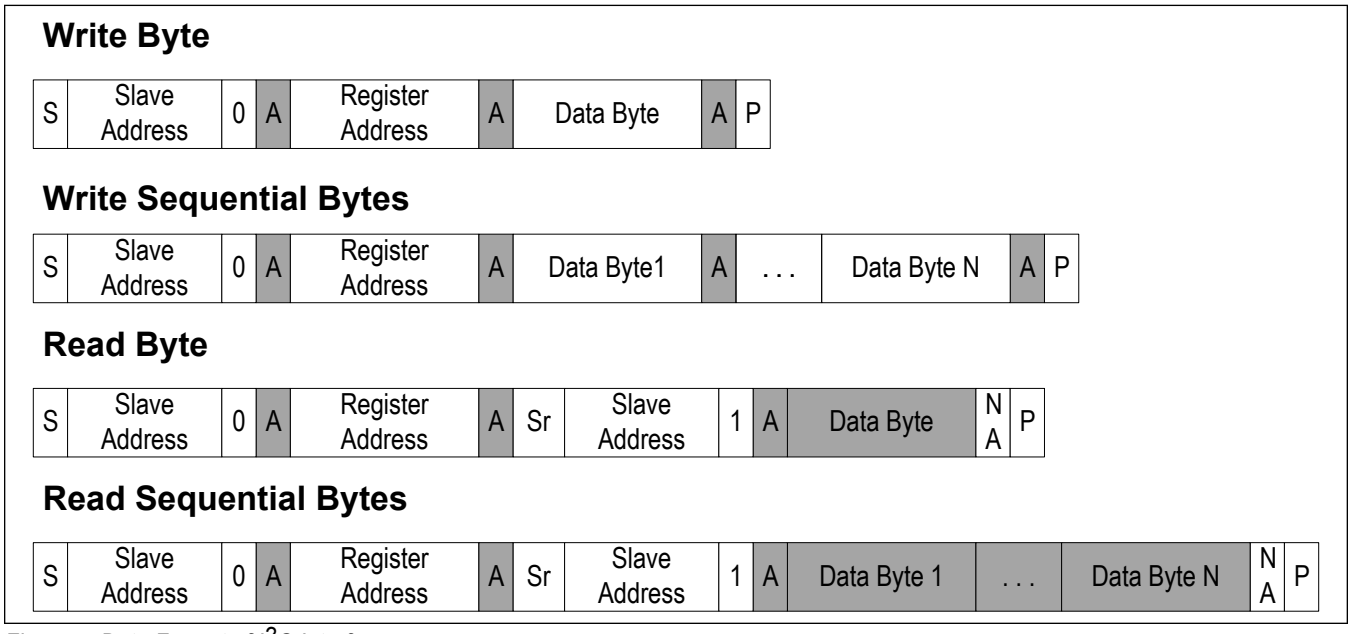


Figure 7. Data Format of I²C Interface

Fault Detection and Diagnostics

Fault Detection

The MAX16984A features advanced device protection features with automatic fault handing and recovery. Table 8 summarizes the conditions that generate a fault, and the actions taken by the device. For all variants, the FAULT output remains asserted as long as a fault condition persists.

For I²C variants, the IRQ registers provide detailed information on the source of the fault condition, and the IRQMASK

registers allow selection of the criteria for assertion of the I²C Interrupt pin, $\overline{INT}$. The IRQ register bits clear when read. However, the IRQ bits that represent a present fault condition continue to reassert after they are cleared, so long as the fault condition persists. If the IRQMASK registers are configured to assert $\overline{INT}$ for a present fault, the $\overline{INT}$ pin deasserts when the IRQ register that asserted the interrupt is read. The $\overline{INT}$ pin subsequently reasserts if the fault condition persists.

Fault Output Pin ($\overline{FAULT}$)

The MAX16984A features an open-drain, active-low $\overline{FAULT}$ output. The MAX16984A is designed to eliminate false $\overline{FAULT}$ reporting by using an internal deglitch and fault blanking timer. This ensures $\overline{FAULT}$ is not incorrectly asserted during normal operation such as starting into high-capacitance loads. The $\overline{FAULT}$ pin can be tied directly to the over-current fault input of a hub controller or SoC.

Table 8. Fault Conditions

EVENT	IRQ REGISTER BITS (I²C ONLY)	DEBOUNCE PRIOR TO ACTION	ACTION TAKEN
Thermal Shutdown	THM_SHD	Immediate	Assert $\overline{FAULT}$ pin and associated IRQ bit, shut down DC-DC converter, and open data switches. When fault resolves and RETRY_TMR expires, release $\overline{FAULT}$ pin, enable the DC-DC converter.
Thermal Warning	THM_WARN	20 ms	Assert associated IRQ bit.
IN Overvoltage	IN_OV	Immediate	Assert $\overline{FAULT}$ pin and associated IRQ bit, shut down DC-DC converter, open data switches, and reset BC1.2. When fault resolves and RETRY_TMR expires, release $\overline{FAULT}$ pin, close data switches, and enable the DC-DC converter.
HVDP/ HVDM Overvoltage	DATA_OV	Immediate	Assert $\overline{FAULT}$ pin and associated IRQ bit, shut down DC-DC converter, open data switches, and reset BC1.2. When fault resolves and RETRY_TMR expires, release $\overline{FAULT}$ pin, close data switches, and enable the DC-DC converter.
USB DC Overcurrent	VBUS_ILIM	16 ms	Assert $\overline{FAULT}$ pin and associated IRQ bit after overcurrent condition persists for 16ms. When overcurrent resolves and RETRY_TMR expires, release $\overline{FAULT}$ pin.
USB DC Overcurrent and SENSN < 4.38V	VBUS_ILIM_UV	16 ms	ILIM_ITRIP = 0: Assert $\overline{FAULT}$ pin and associated IRQ bit, and shut down DC-DC converter after overcurrent and undervoltage condition persists for 16ms. Release $\overline{FAULT}$ pin, and enable DC-DC converter once RETRY_TMR expires after shutdown. I²C variant and ILIM_ITRIP = 1: Assert $\overline{FAULT}$ pin and associated IRQ bit after overcurrent condition persists for 16ms. When overcurrent resolves and RETRY_TMR expires, release $\overline{FAULT}$ pin.
SENSN < 4.38V	VBUS_UV	16 ms	Assert $\overline{FAULT}$ pin and associated IRQ bit after undervoltage condition persists for 16ms. When undervoltage resolves and RETRY_TMR expires, release $\overline{FAULT}$ pin.
USB DC Overcurrent and SENSN < 2V	VBUS_SHT_GND	Immediate	Assert $\overline{FAULT}$ pin and associated IRQ bit, shut down DC-DC converter, and open data switches. Release $\overline{FAULT}$ pin, and enable DC-DC converter once RETRY_TMR expires after shutdown.
LX Overcurrent for 4 Consecutive Cycles and SENSN < 2V	VBUS_SHT_GND	Immediate	Assert $\overline{FAULT}$ pin and associated IRQ bit, shut down DC-DC converter, and open data switches. Release $\overline{FAULT}$ pin, and enable DC-DC converter once RETRY_TMR expires after shutdown.
SENSN Overvoltage	VBUS_OV	Immediate	Assert $\overline{FAULT}$ pin and associated IRQ bit, shut down DC-DC converter, and open data switches. When fault resolves and RETRY_TMR expires, release $\overline{FAULT}$ pin, enable DC-DC converter, and data switches.

Register Map

Summary Table

ADDRESS	NAME	MSB							LSB
USER_CMDS									
0x00	SETUP_0[7:0]	–	–	EN_DCDC	VOUT[2:0]			SYNC_DIR	SS_EN
0x01	SETUP_1[7:0]	FSW[2:0]			GAIN[4:0]				
0x02	SETUP_2[7:0]	–	–	–	ILIM_ITRIP	–	ILIM[2:0]		
0x03	SETUP_3[7:0]	RETRY_TMR[1:0]		CD[1:0]		–	–	–	–
0x04	SETUP_4[7:0]	–	–	–	–	–	–	–	CONFIGURED
0x05	ADC_REQUEST[7:0]	–	–	–	–	–	–	–	ADC_REQ
0x07	IRQ_MASK_0[7:0]	IRQ_AUTOCLR	–	–	–	EN_BC_ATTACH_IRQ	–	EN_BC_ATTACH_EV	EN_ADC_DONE
0x08	IRQ_MASK_1[7:0]	–	–	EN_VBUS_ILIM_UV	EN_VBUS_ILIM	EN_VBUS_OV	EN_VBUS_UV	EN_VBUS_SHT_GND	EN_THM_SHD
0x09	IRQ_MASK_2[7:0]	–	–	–	–	EN_THM_WARN	EN_IN_OV	EN_DATA_OV	–
0x0A	IRQ_0[7:0]	UNCONFIGURED	–	–	–	BC_ATTACH_IRQ	–	BC_ATTACH_EV	ADC_DONE
0x0B	IRQ_1[7:0]	–	–	VBUS_ILIM_UV	VBUS_ILIM	VBUS_OV	VBUS_UV	VBUS_SHT_GND	THM_SHD
0x0C	IRQ_2[7:0]	–	–	–	–	THM_WARN	IN_OV	DATA_OV	–
0x0D	STATUS_0[7:0]	–	–	–	–	BC_ATTACH	–	–	–
0x10	ADC_0[7:0]	ADC_USBI[7:0]							
0x11	ADC_1[7:0]	ADC_USBV[7:0]							
0x12	ADC_2[7:0]	ADC_TEMP[7:0]							

Register Details

SETUP_0 (0x0)

BIT	7	6	5	4	3	2	1	0
Field	–	–	EN_DCDC	VOUT[2:0]			SYNC_DIR	SS_EN
Reset	–	–	0b1	0b000				
Access Type	–	–	Write, Read	Write, Read			Write, Read	Write, Read

BITFIELD	BITS	DESCRIPTION	DECODE
EN_DCDC	5	DC/DC Converter Enable. Internally AND'ed with the ENBUCK pin.	0 = Disable V_{BUS} Buck Converter 1 = Enable V_{BUS} Buck Converter

BITFIELD	BITS	DESCRIPTION	DECODE
VOUT	4:2	V_{BUS} Output Level Selection	0b000 = 5V 0b001 = 9V 0b010 = 12V 0b011 = 15V 0b100 = 18V (protected battery pass-through) 0b101 = 5V 0b110 = 5V 0b111 = 5V
SYNC_DIR	1	SYNC Pin Direction Selection Initial value set by CONFIG1 resistor.	0 = Output 1 = Input
SS_EN	0	Spread Spectrum Enable Initial value set by CONFIG1 resistor.	0 = Disable Spread Spectrum Function 1 = Enable Spread Spectrum Function

SETUP_1 (0x1)

BIT	7	6	5	4	3	2	1	0
Field	FSW[2:0]			GAIN[4:0]				
Reset	0b000			0b00000				
Access Type	Write, Read			Write, Read				

BITFIELD	BITS	DESCRIPTION	DECODE
FSW	7:5	DC/DC Convertor Switching Frequency Selection	0b000 = 2200 kHz 0b001 = 1200 kHz 0b010 = 790 kHz 0b011 = 600 kHz 0b100 = 488 kHz 0b101 = 410 kHz 0b110 = 350 kHz 0b111 = 310 kHz

BITFIELD	BITS	DESCRIPTION	DECODE
GAIN	4:0	The gain of the voltage correction applied to the buck converter output (based on DC load sensed by current sense amp). R_{SENSE} = 33mΩ.	0: 0mΩ 1: 18mΩ 2: 36mΩ 3: 54mΩ 4: 72mΩ 5: 90mΩ 6: 108mΩ 7: 126mΩ 8: 144mΩ 9: 162mΩ 10: 180mΩ 11: 198mΩ 12: 216mΩ 13: 234mΩ 14: 252mΩ 15: 270mΩ 16: 288mΩ 17: 306mΩ 18: 324mΩ 19: 342mΩ 20: 360mΩ 21: 378mΩ 22: 396mΩ 23: 414mΩ 24: 432mΩ 25: 450mΩ 26: 468mΩ 27: 486mΩ 28: 504mΩ 29: 522mΩ 30: 540mΩ 31: 558mΩ

SETUP_2 (0x2)

BIT	7	6	5	4	3	2	1	0
Field	–	–	–	ILIM_ITRIP	–	ILIM[2:0]		
Reset	–	–	–	0b0	–	0b111		
Access Type	–	–	–	Write, Read	–	Write, Read		

BITFIELD	BITS	DESCRIPTION	DECODE
ILIM_ITRIP	4	Determines the buck's retry behavior under USB DC current limit conditions.	0 = VBUS_ILIM_UV fault enabled. 1 = VBUS_ILIM_UV fault disabled.
ILIM	2:0	USB DC Current-Limit Threshold, R_{SENSE} = 33mΩ.	USB DC Current-Limit Threshold (min in Amps) 0b000 = 0.3 0b001 = 0.55 0b010 = 0.8 0b011 = 1.05 0b100 = 1.62 0b101 = 2.1 0b110 = 2.6 0b111 = 3.04

SETUP_3 (0x3)

BIT	7	6	5	4	3	2	1	0
Field	RETRY_TMR[1:0]		CD[1:0]		–	–	–	–
Reset	0b00				–	–	–	–
Access Type	Write, Read		Write, Read		–	–	–	–

BITFIELD	BITS	DESCRIPTION	DECODE
RETRY_TMR	7:6	Determines the length of the RETRY timer after a fault condition.	0b00 = 2.0s 0b01= 1.0s 0b10 = 0.5s 0b11= 16ms
CD	5:4	BC1.2 Charge Detection Configuration Selection. This register is pre-loaded based on the part number variant and the status of the DATA_MODE pin.	0b00 = High Speed Pass Through (SDP) 0b01 = Auto-CDP 0b10 = Auto-DCP / Apple 2.4A 0b11 = Auto-DCP / Apple 1.0A

SETUP_4 (0x4)

BIT	7	6	5	4	3	2	1	0
Field	–	–	–	–	–	–	–	CONFIGURED
Reset	–	–	–	–	–	–	–	0b0
Access Type	–	–	–	–	–	–	–	Write, Read

BITFIELD	BITS	DESCRIPTION	DECODE
CONFIGURED	0	I^2C configuration complete indicator Upon power-up, the buck converter is prevented from turning on until this bit is written to a one, indicating the part is fully configured for its intended mode of operation.	0 = I^2C Configuration Pending 1 = I^2C Configuration Complete

ADC_REQUEST (0x5)

BIT	7	6	5	4	3	2	1	0
Field	–	–	–	–	–	–	–	ADC_REQ
Reset	–	–	–	–	–	–	–	0b0
Access Type	–	–	–	–	–	–	–	Write, Read

BITFIELD	BITS	DESCRIPTION	DECODE
ADC_REQ	0	ADC V/I Sample Request When a one is written, ADC V/I sampling is initiated. This bit is cleared once the requested sampling is complete and the ADC results are updated. The status of the ADC conversion (data ready) can be monitored in the IRQ0 register.	0 = No ADC Sample Requested 1 = ADC Sample Requested

IRQ_MASK_0 (0x7)

A Read-Write register that configures which of the conditions in the IRQ_0 register will assert an Interrupt. See the IRQ_0 register for condition descriptions.

BIT	7	6	5	4	3	2	1	0
Field	IRQ_AUTOCLR	–	–	–	EN_BC_ATTACH_IRQ	–	EN_BC_ATTACH_EV	EN_ADC_DONE
Reset	0b0	–	–	–	0b0	–	0b0	0b0
Access Type	Write, Read	–	–	–	Write, Read	–	Write, Read	Write, Read

BITFIELD	BITS	DESCRIPTION	DECODE
IRQ_AUTOCLR	7	IRQ Auto Clear	0 = IRQ register flags are latched on until read. 1 = IRQ register flags are automatically cleared when the error condition is removed.
EN_BC_ATTACH_IRQ	3	BC1.2 ATTACH STATUS Interrupt Enable	0 = Not included in Interrupt 1 = Included in Interrupt
EN_BC_ATTACH_EV	1	BC1.2 ATTACH EVENT Interrupt Enable	0 = Not included in Interrupt 1 = Included in Interrupt
EN_ADC_DONE	0	ADC_DONE Interrupt Enable	0 = Not included in Interrupt 1 = Included in Interrupt

IRQ_MASK_1 (0x8)

A Read-Write register that configures which of the conditions in the IRQ_1 register will assert an Interrupt. See the IRQ_1 register for condition descriptions.

BIT	7	6	5	4	3	2	1	0
Field	–	–	EN_VBUS_ILIM_UV	EN_VBUS_ILIM	EN_VBUS_OV	EN_VBUS_UV	EN_VBUS_SHT_GND	EN_THM_SHD
Reset	–	–	0b0	0b0	0b0	0b0	0b0	0b0
Access Type	–	–	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read

BITFIELD	BITS	DESCRIPTION	DECODE
EN_VBUS_ILIM_UV	5	VBUS_ILIM_UV Interrupt Enable	0 = Not included in Interrupt 1 = Included in Interrupt
EN_VBUS_ILIM	4	VBUS_ILIM Interrupt Enable	0 = Not included in Interrupt 1 = Included in Interrupt
EN_VBUS_OV	3	VBUS_OV Interrupt Enable	0 = Not included in Interrupt 1 = Included in Interrupt
EN_VBUS_UV	2	VBUS_UV Interrupt Enable	0 = Not included in Interrupt 1 = Included in Interrupt
EN_VBUS_SHT_GND	1	VBUS_SHT_GND Interrupt Enable	0 = Not included in Interrupt 1 = Included in Interrupt
EN_THM_SHD	0	THM_SHD Interrupt Enable	0 = Not included in Interrupt 1 = Included in Interrupt

IRQ_MASK_2 (0x9)

A Read-Write register that configures which of the conditions in the IRQ_2 register will assert an Interrupt. See the IRQ_2 register for condition descriptions.

BIT	7	6	5	4	3	2	1	0
Field	–	–	–	–	EN_THM_WARN	EN_IN_OV	EN_DATA_OV	–
Reset	–	–	–	–	0b0	0b0	0b0	–
Access Type	–	–	–	–	Write, Read	Write, Read	Write, Read	–

BITFIELD	BITS	DESCRIPTION	DECODE
EN_THM_WARN	3	THM_WARN Interrupt Enable	0 = Not included in Interrupt 1 = Included in Interrupt
EN_IN_OV	2	IN_OV Interrupt Enable	0 = Not included in Interrupt 1 = Included in Interrupt
EN_DATA_OV	1	DATA_OV Interrupt Enable	0 = Not included in Interrupt 1 = Included in Interrupt

IRQ_0 (0xA)

A read only register that includes flags which indicate a number of operating conditions. These flags can assert an interrupt by setting the corresponding bit in the MASK register.

IRQ_0 holds notifications of expected operations rather than error/fault conditions.

BIT	7	6	5	4	3	2	1	0
Field	UNCONFIGURED	–	–	–	BC_ATTACH_IRQ	–	BC_ATTACH_EV	ADC_DONE
Reset	0b0	–	–	–	0b0	–	0b0	0b0
Access Type	Read Clears All	–	–	–	Read Clears All	–	Read Clears All	Read Clears All

BITFIELD	BITS	DESCRIPTION	DECODE
UNCONFIGURED	7	I^2C Unconfigured Indicator Bit	0 = Device is fully configured (CONFIGURED written to 1) 1 = Device is not fully configured (CONFIGURED has not been written to 1)
BC_ATTACH_IRQ	3	BC1.2 ATTACH Indicator This bit indicates a BC1.2 device attach is observed via the HVDP/HVDM pins.	0 = No device attached 1 = Device attached
BC_ATTACH_EV	1	BC1.2 ATTACH Event Detected This bit indicates a BC1.2 device attach was initiated and/or terminated as observed via the HVDP/HVDM pins.This bit differs from BC_ATTACH (which indicates the current BC1.2 attach status in real time) in that it is issued only when the status changes from unattached to attached or vice-versa. Clear on Read. Not affected by IRQ_AUTOCLR.	0 = No attach or detach event detected since least read 1 = New attach and/or detach event detected
ADC_DONE	0	ADC Meaurement Complete Indicator. Clear on Read.	0 = No new data available since least read 1 = New data available

IRQ_1 (0xB)

A read only register that includes flags which indicate a number of error conditions. These flags can assert an interrupt by setting the corresponding bit in the MASK register.

BIT	7	6	5	4	3	2	1	0
Field	–	–	VBUS_ILIM_UV	VBUS_ILIM	VBUS_OV	VBUS_UV	VBUS_SHT_GND	THM_SHD
Reset	–	–	0b0	0b0	0b0	0b0	0b0	0b0
Access Type	–	–	Read Clears All	Read Clears All	Read Clears All	Read Clears All	Read Clears All	Read Clears All

BITFIELD	BITS	DESCRIPTION	DECODE
VBUS_ILIM_UV	5	V_{BUS} Current Limit and SENSN UV Fault Detected Disabled when ILIM_ITRIP = 1. Clear on Read if condition is resolved.	0 = No event 1 = Event detected
VBUS_ILIM	4	V_{BUS} Current Limit Condition Detected Disabled when ILIM_ITRIP = 0. Clear on Read if condition is resolved.	0 = No event 1 = Event detected
VBUS_OV	3	V_{BUS} Overvoltage Fault Detected Detected on SENSN pin. Clear on Read if condition is resolved.	0 = No event 1 = Event detected
VBUS_UV	2	V_{BUS} Under Voltage Fault Detected Detected on SENSN pin. Clear on Read if condition is resolved.	0 = No event 1 = Event detected
VBUS_SHT_GND	1	V_{BUS} Short to Ground Fault Detected Detected on SENSN pin. Clear on Read if condition is resolved.	0 = No event 1 = Event detected
THM_SHD	0	Over Temperature Fault Detected Asserts when the die temperature exceeds 165°C (typ). Clear on Read if condition is resolved.	0 = No event 1 = Event detected

IRQ_2 (0xC)

A read only register that includes flags which indicate a number of error conditions. These flags can assert an interrupt by setting the corresponding bit in the MASK register.

BIT	7	6	5	4	3	2	1	0
Field	–	–	–	–	THM_WARN	IN_OV	DATA_OV	–
Reset	–	–	–	–	0b0	0b0	0b0	–
Access Type	–	–	–	–	Read Clears All	Read Clears All	Read Clears All	–

BITFIELD	BITS	DESCRIPTION	DECODE
THM_WARN	3	Thermal Warning Condition Detected Asserts when the temperature has reached 140°C (typ). Clear on Read if condition is resolved.	0 = No event 1 = Event detected
IN_OV	2	IN Pin Overvoltage Fault Detected Clear on Read if condition is resolved.	0 = No event 1 = Event detected
DATA_OV	1	DATA Pin Overvoltage Fault Detected Clear on Read if condition is resolved.	0 = No event 1 = Event detected

STATUS_0 (0xD)

A read only register that includes information on the current status of the IC.

BIT	7	6	5	4	3	2	1	0
Field	–	–	–	–	BC_ATTACH	–	–	–
Reset	–	–	–	–	0b0	–	–	–
Access Type	–	–	–	–	Read Only	–	–	–

BITFIELD	BITS	DESCRIPTION	DECODE
BC_ATTACH	3	BC1.2 ATTACH Status Indicator This bit indicates the current device attach status via the HVDP/HVDM pins. More details can be read in the STATUS_1 register.	0 = No device currently attached 1 = Device currently attached

ADC_0 (0x10)

BIT	7	6	5	4	3	2	1	0
Field	ADC_USBI[7:0]							
Reset	0x00							
Access Type	Read Only							

BITFIELD	BITS	DESCRIPTION	DECODE
ADC_USBI	7:0	USB Load Current ADC Measurement Result	I_{LOAD} = ((116mV/256) * ADC_USBI)/R_{SENSE} (amperes)

ADC_1 (0x11)

BIT	7	6	5	4	3	2	1	0
Field	ADC_USBV[7:0]							
Reset	0x00							
Access Type	Read Only							

BITFIELD	BITS	DESCRIPTION	DECODE
ADC_USBV	7:0	USB Voltage ADC Measurement Result	V_{SENSP} = (19.8V/256) * ADC_USBV (volts), when VOUT[2:0] = 0b000

ADC_2 (0x12)

BIT	7	6	5	4	3	2	1	0
Field	ADC_TEMP[7:0]							
Reset	0x00							
Access Type	Read Only							

BITFIELD	BITS	DESCRIPTION	DECODE
ADC_TEMP	7:0	Die Temp ADC Measurement Result	Die Temp = 3.5°C * ADC_TEMP - 270 (°C)

Applications Information

Migrating from MAX16984 to MAX16984A

The MAX16984A offers several improvements compared to the original MAX16984, such as higher USB protection switch bandwidth and greater output current capability. There are, however, some notable differences between the devices that prevent drop-in replacement. In Table 9 below, the differing pins and associated functions are summarized as a guide for migrating to the MAX16984A.

Table 9. Feature and Function Differences Between MAX16984 and MAX16984A.

MAX16984 PIN OR FUNCTION	FUNCTION DESCRIPTION	MAX16984A EQUIVALENT
SYNC pin	Synchronization input or sets FPWM/skip-mode using internal clock source.	SYNC pin with same behavior as MAX16984 when configured as input. SYNC direction is configured via CONFIG1 resistor or I²C.
FOSC pin	Resistor-programmable switching frequency input.	Switching frequency is configured via CONFIG1 resistor or I²C.
CD0, CD1 pins	Charger detection configuration (HS pass-through/CDP/Auto-DCP)	Use of I²C or standalone variants combined with DATA_MODE pin enables support for HS pass-through/Auto-CDP/Auto-DCP modes.
FBPER, FBMAX, FBCAP pins	Feedback voltage percentage, feedback voltage compensation ratio and feedback compensation capacitor connections.	Voltage compensation feedback is fully integrated, external components no longer needed. Voltage compensation, measured in mΩ of cable resistance between MAX16984A and the load, is configured with the Gain setting via CONFIG2/CONFIG3 resistors or I²C.
SENSO pin	Resistor-programmable DC current-limit.	DC current-limit configured via I²C or CONFIG3 and R_{SENSE} resistors.
SUP pin	Bias regulator supply input.	No equivalent. Bias regulator for MAX16984A is supplied directly from main input (SUPSW).
ENBUCK pin	Active-high system enable, battery-voltage tolerant.	HVEN pin with same behavior as MAX16984.
Spread-spectrum	Internally generated switching frequency is modulated ±3.25% with MAX16984S device suffix.	Spread-spectrum is configured via CONFIG1 resistor or I²C.
CDP handshake	Requires active management by the USB host to toggle CD0 after a USB device begins enumeration or enters High-Speed mode.	MAX16984A implements Auto-CDP, which automatically transitions to HS pass-through mode when the device may attempt USB enumeration. No active management is necessary by the host with Auto-CDP.
Auto-DCP handshake	Auto-DCP includes USB BC1.2 DCP, Apple (1A or 2.1A) and China YD/T 1591-2009.	MAX16984A Auto-DCP adds Samsung 1.2V divider network support and replaces Apple 2.1A with Apple 2.4A divider networks.

DC-DC Switching Frequency Selection

The switching frequency (f_{SW}) for the MAX16984A is programmable through the CONFIG1 resistor (on standalone variants) or by I²C register writes.

Higher switching frequencies allow for smaller PCB area designs with lower inductor values and less output capacitance. Consequently, peak currents and I²R losses are lower at higher switching frequencies, but core losses, gate charge currents, and switching losses increase.

To avoid AM band interference, operation between 500kHz and 1.8MHz is not recommended.

DC-DC Input Capacitor Selection

The input capacitor supplies the instantaneous current needs of the buck converter and reduces the peak currents drawn

from the upstream power source. The input bypass capacitor is a determining factor in the input voltage ripple.

The input capacitor RMS current rating requirement ($I_{IN(RMS)}$) is defined by the following equation:

$$I_{IN(RMS)} = I_{LOAD}\frac{\sqrt{V_{SENSP} \times \left(V_{SUPSW} - V_{SENSP}\right)}}{V_{SUPSW}}$$

$I_{IN(RMS)}$ has a maximum value when the input voltage equals twice the output voltage ($V_{SUPSW} = 2 \cdot V_{SENSP}$), so $I_{IN(MAX)} = \frac{1}{2} \cdot I_{LOAD(MAX)}$. I_{LOAD} is the measured operating load current, while $I_{LOAD(MAX)}$ refers to the maximum load current.

Choose an input capacitor that exhibits less than 10ºC self-heating temperature rise at the RMS input current for optimal long-term reliability.

The input voltage ripple is composed of V_Q (caused by the capacitor discharge) and V_{ESR} (caused by the ESR of the capacitor). Use low-ESR ceramic capacitors with high ripple current capability at the input. Assume the contribution from the ESR and capacitor discharge is equal to 50%. Calculate the input capacitance and ESR required for a specified input voltage ripple using the following equations:

$$ESR_{IN} = \frac{\Delta V_{ESR}}{I_{LOAD(MAX)} + \frac{\Delta I_L}{2}}$$

where:

$$\Delta I_L = \frac{\left(V_{SUPSW} - V_{SENSP}\right) \times V_{SENSP}}{V_{SUPSW} \times f_{SW} \times L}$$

and:

$$C_{IN} = \frac{I_{LOAD(MAX)} \times D\left(1 - D\right)}{\Delta V_Q \times f_{SW}} \text{ where } D = \frac{V_{SENSP}}{V_{SUPSW}}$$

Where D is the buck converter duty cycle.

Bypass SUPSW with 0.1µF parallel to 10µF of ceramic capacitance close to the SUPSW and PGND pins. The ceramic input capacitor of a buck converter has a high $\frac{di}{dt}$, minimize the PCB current-loop area to reduce EMI. Bypass SUPSW with 47µF of bulk electrolytic capacitance to dampen line transients.

DC-DC Output Capacitor Selection

To ensure stability and compliance with USB and Apple specifications, follow the recommended output filters listed in Table 10. For proper functionality, a minimum amount of ceramic capacitance must be used, regardless of f_{SW}. Additional capacitance for lower switching frequencies can be low-ESR electrolytic types (< 0.25Ω).

DC-DC Output Inductor Selection

Three key inductor parameters must be considered when selecting an inductor: inductance value (L), inductor saturation current (I_{SAT}), and DC resistance (R_{DCR}). To select the proper inductance value, the ratio of inductor peak-to-peak AC current to DC average current (LIR) must be selected. A small LIR will reduce the RMS current in the output capacitor and results in small output ripple voltage, but this requires a larger inductor. A good compromise between size and loss is LIR = 0.35 (35%). Determine the inductor value using the equation below,

$$L = \frac{V_{SENSP} \times \left(V_{SUPSW} - V_{SENSP}\right)}{V_{SUPSW} \times f_{SW} \times I_{LOAD(MAX)} \times LIR}$$

where V_{SUPSW} and V_{SENSP} are typical values (such that efficiency is optimum for nominal operating conditions). Ensure the inductor I_{SAT} is above the buck converter's cycle-by-cycle peak current limit.

Table 10. Recommended Output Filters For I_{LOAD} of 3A

f_{SW} (kHz)	L_{OUT} (µH)	RECOMMENDED C_{OUT}
2200	1.5	22µF ceramic
488	8.2	3 x 22µF ceramic
488	8.2	22µF ceramic + low-ESR 68µF electrolytic (< 0.25Ω)
248	20	22µF ceramic + low-ESR 68µF electrolytic (< 0.25Ω)

Layout Considerations

Proper PCB layout is critical for robust system performance. See the MAX16984A EV kit data sheet for a recommended layout. Minimize the current-loop area and the parasitics of the DC-DC conversion circuitry to reduce EMI. The input capacitor placement should be prioritized because in a buck converter the ceramic input capacitor has high $\frac{di}{dt}$.

Place the input capacitor, power inductor, and output capacitor as close as possible to the IC SUPSW and PGND pins. Shorter traces should be prioritized over wider traces.

A low-impedance ground connection between the input and output capacitor is required (route through the ground pour on the exposed pad). Connect the exposed pad to ground. Place multiple vias in the pad to connect to all other ground layers for proper heat dissipation. Failure to do so can result in the IC repeatedly reaching thermal shutdown. Do not use separate power and analog ground planes. Instead, use a single common ground and manage currents through component placement. High-frequency return current flows through the path of least impedance (through the ground pour directly underneath the corresponding traces).

USB traces must be routed as a 90Ω differential pair with an appropriate keep-out area. Avoid routing USB traces near clocks and high-frequency switching nodes. The length of the routing should be minimized and avoid 90° turns, excessive vias, and RF stubs.

Determining USB System Requirements

The nominal cable resistance (with tolerance) for both the USB power wire (BUS) and return GND should be determined from the cable manufacturer. In addition, be sure to include the resistance from any inline or PCB connectors. Determine the desired operating temperature range for the application, and consider the change in resistance over temperature.

A typical application presents a 200mΩ BUS resistance with a matching 200mΩ resistance in the ground path. In this application, the voltage drop at the far end of the captive cable is 800mV when the load current is 2A. This voltage drop requires the voltage-adjustment circuitry of the ICs to increase the output voltage to comply with the USB and Apple specifications.

USB Loads

The MAX16984A is compatible with both USB-compliant and noncompliant loads. A compliant USB device is not allowed to sink more then 30mA and must not present more than 10µF of capacitance when initially attached to the port. The device then begins its D+/D- connection and enumeration process. After completion of the connect process, the device can pull 100mA/150mA and must not present a capacitance > 10µF. This is considered the hot-inserted, USB-compliant load of 44Ω||10µF. For noncompliant USB loads, the ICs can also support both hot insertion and soft-start into a USB load of 2Ω||330µF.

USB Output Current Limit

The USB load current is monitored by an internal current-sense amplifier through the voltage created across R_{SENSE}. MAX16984A offers a digitally adjustable USB current-limit threshold. See SETUP_2 or Table 6 to select an appropriate resistor value for the desired current limit.

Some systems require the need to supply up to 160% of $I_{LOAD(MAX)}$ for brief periods. It is possible to increase the MAX16984A current limit beyond 3.04A (min) by decreasing R_{SENSE} using this scaling factor:

$$R_{SENSE} = 33m\Omega \cdot \frac{3.04A}{1.6 \cdot I_{LOAD(MAX)}}$$

USB Voltage Adjustment

Figure 8 shows a DC model of the voltage-correction function of MAX16984A. Without voltage adjustment (V_{ADJ} = 0, GAIN[4:0] = 0), the voltage seen by the device at the end of the cable will decrease linearly as load current increases. To compensate for this, the output voltage of the buck converter should increase linearly with load current. The slope of SENSP is called R_{COMP} such that $V_{ADJ} = R_{COMP} \cdot I_{LOAD}$ and $R_{COMP} = GAIN[4:0] \cdot R_{LSB} \cdot \frac{R_{SENSE}}{33m\Omega}$ (see Figure 9). The R_{COMP} adjustment values available on MAX16984A are listed in the GAIN[4:0] register description and are based on a 33mΩ sense resistor.

For $V_{DUT} = V_{NO\_LOAD}$; $0 \le I_{LOAD}$, R_{COMP} must equal the sum of the system resistances. Calculate the minimum R_{COMP} for the system so that V_{DUT} stays constant:

$$R_{COMP\_SYS} = R_{LR} + R_{SENSE} + R_{PCB} + R_{CABLE\_VBUS} + R_{CABLE\_GND}$$

Where $R_{CABLE\_VBUS} + R_{CABLE\_GND}$ is the round-trip resistance of the USB cable (including the effect from the cable shield, if it conducts current), R_{LR} is the buck converter's load regulation expressed in mΩ (51mΩ typ.), and R_{PCB} is the resistance of any additional V_{BUS} parasitics (the V_{BUS} FET, PCB trace, ferrites, and the USB connectors). Find the setting for GAIN[4:0] using the minimum R_{COMP}.

$$GAIN[4:0] = ceiling\left(\frac{R_{COMP\_SYS}}{R_{LSB}} \cdot \frac{33m\Omega}{R_{SENSE}}\right)$$

The nominal DUT voltage can then be estimated at any load current by:

$$V_{DUT} = V_{NO\_LOAD} + R_{LSB} \cdot GAIN[4:0] \cdot \frac{R_{SENSE}}{33m\Omega} \cdot I_{LOAD} - R_{COMP\_SYS} \cdot I_{LOAD}$$

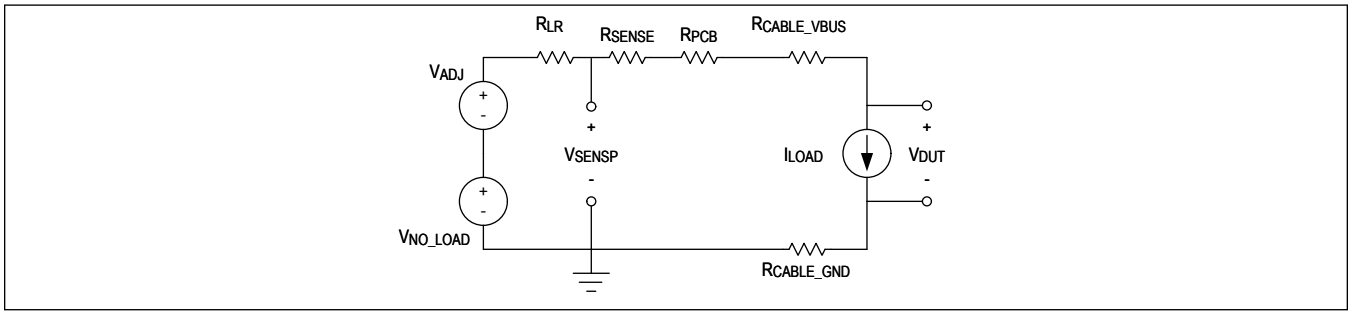


Figure 8. DC Voltage Adjustment Model

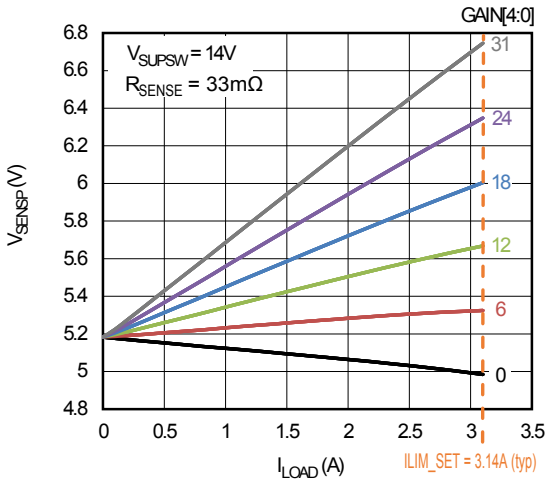


Figure 9. Increase in SENSP vs. USB Current

Tuning of USB Data Lines

USB Hi-Speed mode requires careful PCB layout with 90Ω controlled differential impedance, with matched traces of equal length, and with no stubs or test points. The MAX16984A includes highbandwidth USB data switches (> 1GHz). This means data-line tuning may not be required. However, all designs are recommended to include pads that would allow LC components to be mounted on the data lines so that tuning can easily be performed later, if necessary. Tuning components should be placed as close as possible to the IC data pins, on the same layer of the PCB as the IC. The proper configuration of the tuning components is shown in Figure 10. Figure 11 shows the reference eye diagram used in the test setup. Figure 12 shows the MAX16984A high-voltage eye diagram on the standard EVKIT with no tuning components. Tuning inductors should be high-Q wire-wound inductors. Contact Maxim's application team for assistance with the tuning process for your specific application.

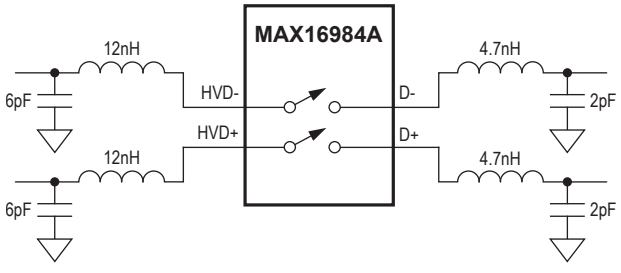


Figure 10. Tuning of Data Lines

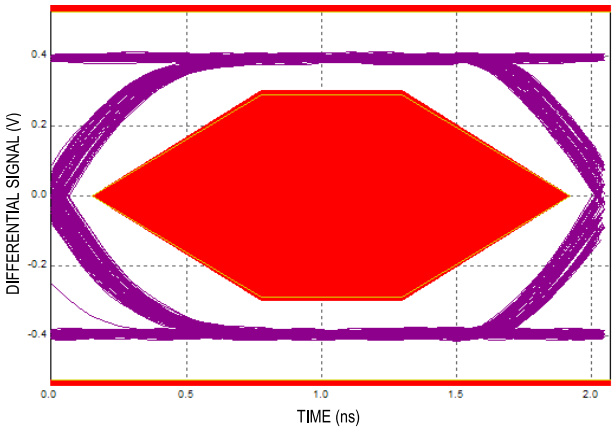


Figure 11. Near-Eye Diagram (with No Switch)

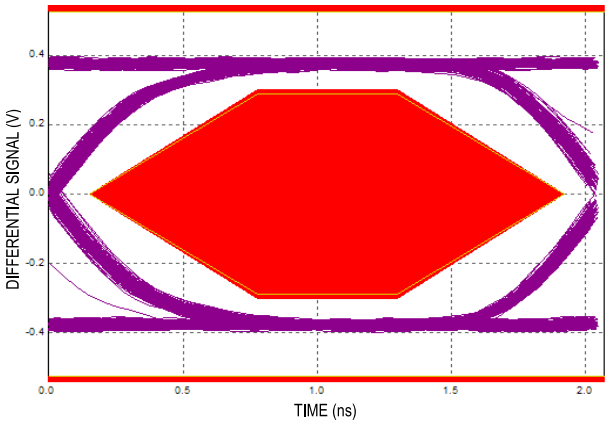


Figure 12. Untuned Near-Eye Diagram (with MAX16984A)

USB Data Line Common-Mode Choke Placement

Most automotive applications use a USB-optimized common-mode choke to mitigate EMI signals from both leaving and entering the module. Optimal placement for this EMI choke is at the module's USB connector. This common-mode choke does not replace the need for the tuning inductors previously mentioned.

ESD Protection

The high-voltage MAX16984A requires no external ESD protection. All Maxim devices incorporate structures to protect against electrostatic discharges encountered during handling and assembly. While competing solutions can latch up and require cycling to resume operation after an ESD

event, the MAX16984A does not latch up after ESD events. When used with the configuration shown in the *Typical Application Circuit*, the MAX16984A is characterized for protection to the following limits:

- ±15kV ISO 10605 (330pF, 2kΩ) Air-Gap
- ±8kV ISO 10605 (330pF, 2kΩ) Contact
- ±15kV IEC 61000-4-2 (150pF, 330Ω) Air-Gap
- ±8kV IEC 61000-4-2 (150pF, 330Ω) Contact

- ±15kV ISO 10605 (330pF, 330Ω) Air Gap
- ±8kV ISO 10605 (330pF, 330Ω) Contact

Note: All application-level ESD testing is performed on the standard evaluation kit.

ESD Test Conditions

ESD performance depends on a variety of conditions. Contact Maxim for test setup, test methodology, and test results.

Human Body Model

Figure 13 shows the Human Body Model, and Figure 15 shows the current waveform it generates when discharged into a low impedance. This model consists of a 100pF capacitor charged to the ESD voltage of interest, which is then discharged into the device through a 1.5kΩ resistor.

IEC 61000-4-2

The IEC 61000-4-2 standard covers ESD testing and performance of finished equipment. MAX16984A helps users design equipment that meets Level 4 of IEC 61000-4-2. The main difference between tests done using the Human Body Model and IEC 61000-4-2 is a higher peak current in IEC 61000-4-2. Because the series resistance is lower in the IEC 61000-4-2 ESD test model (Figure 14), the ESD withstand-voltage measured to this standard is generally lower than that measured using the Human Body Model Figure 16 shows the current waveform for the 8kV, IEC 61000-4-2 Level 4 ESD Contact Discharge test. The Air-Gap Discharge test involves approaching the device with a charged probe. The Contact Discharge method requires connecting the probe to the device before the probe is energized.

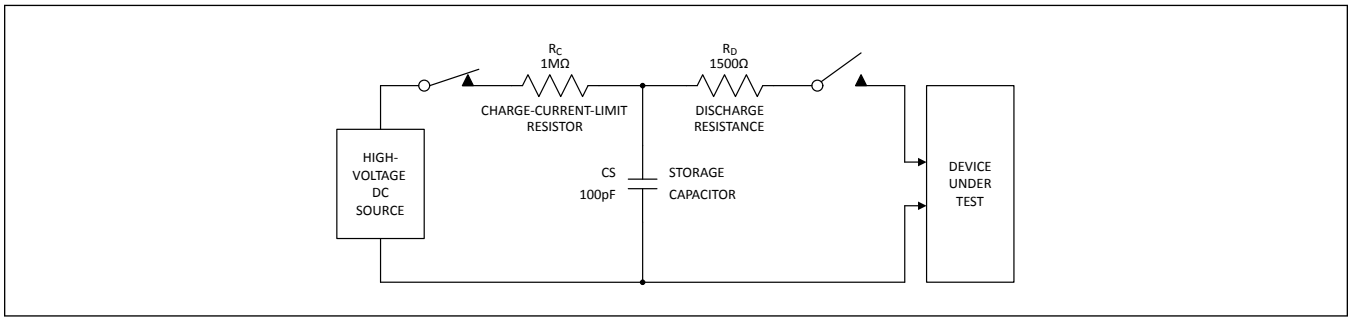


Figure 13. Human Body ESD Test Model

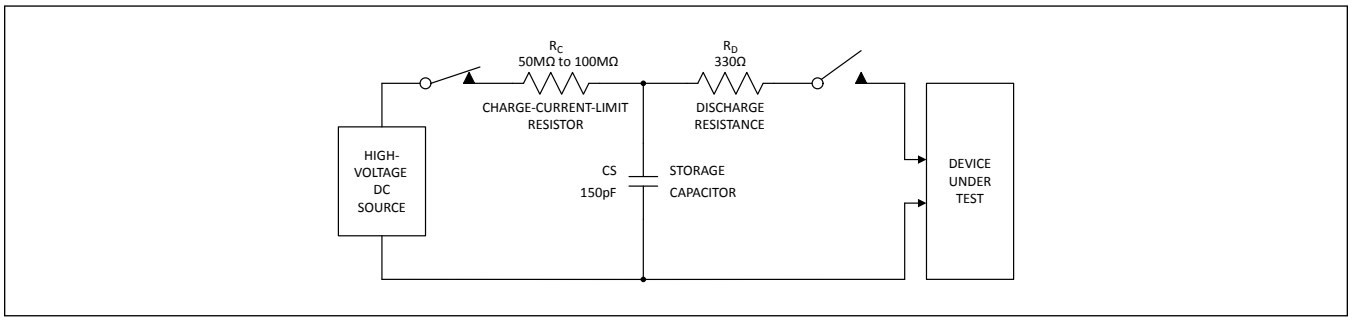


Figure 14. IEC 61000-4-2 ESD Test Model

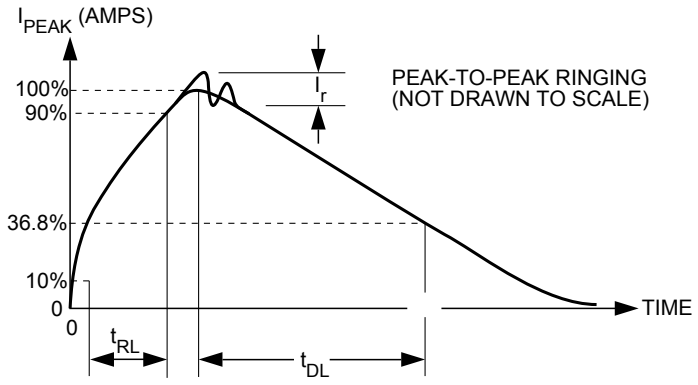


Figure 15. Human Body Current Waveform

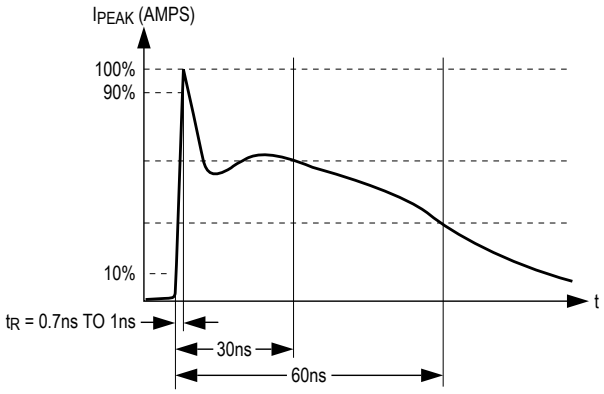
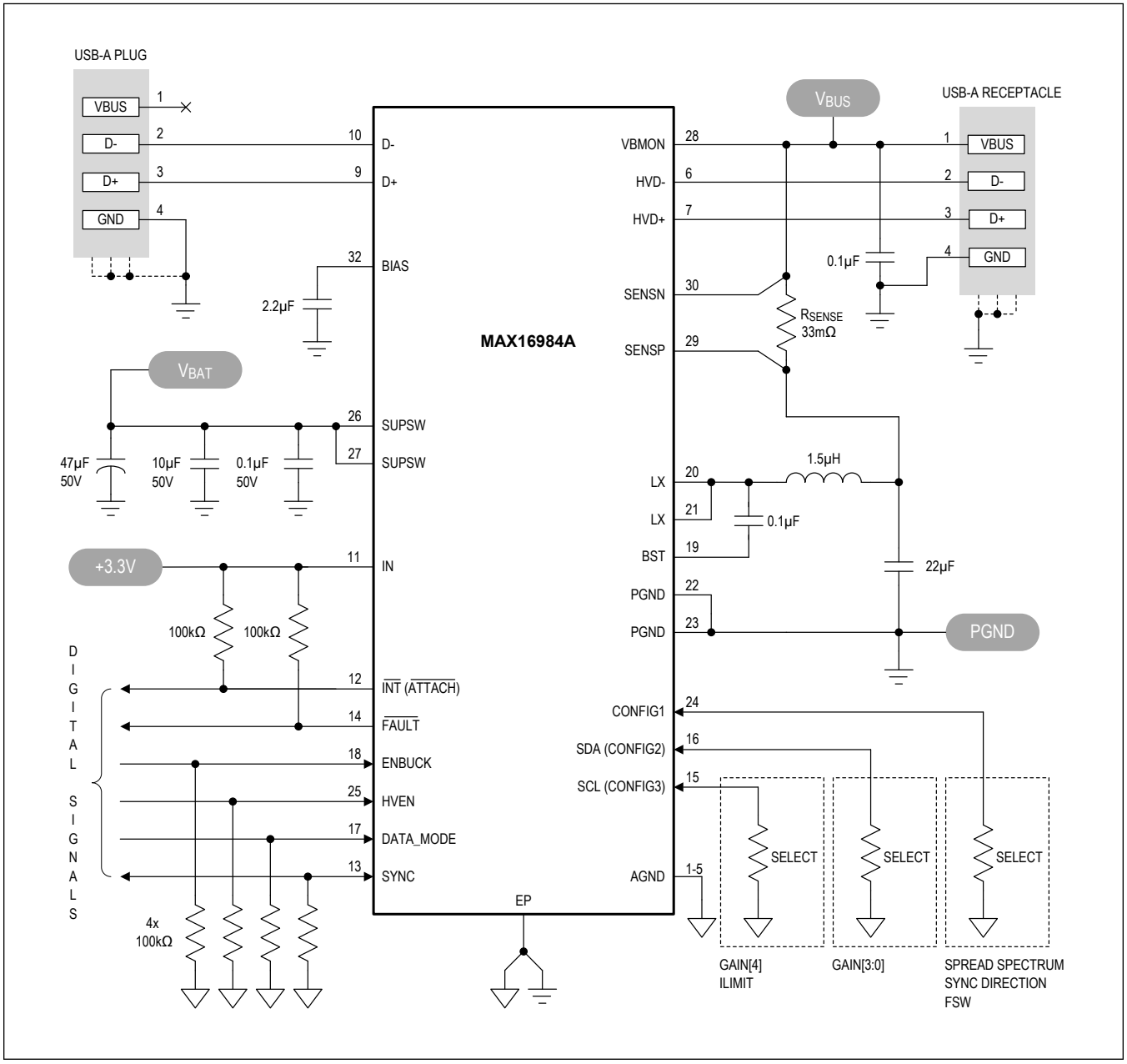


Figure 16. IEC 61000-4-2 Current Waveform

Typical Application Circuit



Ordering Information

PART NUMBER	TEMP RANGE	PIN-PACKAGE	STARTUP MODE (DATA_MODE PIN = 0)	I²C	NOMINAL OUTPUT CURRENT FOR MFi R30+ (A)
MAX16984AATJA/V+	-40°C to +125°C	32 TQFN-EP	Auto-CDP	No	2.4
MAX16984AATJB/V+			SDP mode		
MAX16984AATJC/V+				Yes	
MAX16984AATJM/V+*					3.0
MAX16984AATJN/V+*				No	

/V Denotes automotive qualified parts.

+Denotes a lead(Pb)-free/RoHS-compliant package.

**Future product—contact factory for availability.*

Revision History

REVISION NUMBER	REVISION DATE	DESCRIPTION	PAGES CHANGED
0	2/20	Initial release	—
1	6/20	Updated *Benefits and Features, Absolute Maximum Ratings, Package Information, Electrical Characteristics, Typical Operating Characteristics, Pin Descriptions, Detailed Description, Applications Information,* and *Ordering Information*.	1, 2, 3, 5, 6, 10, 12, 15–23, 26, 30
2	12/20	Updated *Benefits and Features, Electrical Characteristics, Detailed Description, and Applications Information*	1, 5, 6, 18–26, 28–33
3	5/21	Added MAX16984AATJC, MAX16984AATJM and MAX16984AATJN. Updated *General Description, Benefits and Features, Simplified Block Diagram, Absolute Maximum Ratings, Electrical Characteristics, Typical Operating Characteristics, Pin Configuration, Pin Description, DCP Reset Behavior and Timing Diagram, DCDC_ON Reset Behavior and Timing Diagram, ATTACH Logic Diagram, ADC Timing Diagram, Detailed Description, Detailed Block Diagram, System Enable (HVEN), DC-DC Enable (ENBUCK), Reset Criteria, Switching Frequency Configuration, Spread-Spectrum Option, Current Limit, Output Short-Circuit Protection, Pre-Thermal Overload Warning, USB DC Current Limit Configuration, Voltage Feedback Adjustment Configuration, Data Switch Mode Truth Table (I^2C Variants), Data Switch and Charge-Detection Block Diagram, I^2C, Control, and Diagnostics, Fault Detection, Fault Conditions, Register Map, Feature and Function Differences Between MAX16984 and MAX16984A, DC-DC Switching Frequency Selection, USB Output Current Limit, Typical Application Circuit* and *Ordering Information.*	1-49

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