Click here to ask about the production status of specific part numbers.

MAX14937

Two Channel, 5kV$_{RMS}$ I^{2}C Isolator

General Description

The MAX14937 is a two-channel, 5kV$_{RMS}$ I^{2}C digital isolator utilizing Maxim's proprietary process technology. For applications requiring 2.75kV$_{RMS}$ of isolation, see the MAX14933 data sheet. The device transfers digital signals between circuits with different power domains at ambient temperatures up to +125°C.

The device offers two bidirectional, open-drain channels for applications, such as I^{2}C, that require data to be transmitted in both directions on the same line. To prevent latch-up action, the A-side outputs comprise special buffers that regulate the logic-low voltage at 0.9V (max), and the input logic-low threshold is at least 50mV lower than the output logic-low voltage. The B side features conventional buffers that do not regulate logic-low output voltage.

The device features independent 2.25V to 5.5V supplies on each side of the isolator. The MAX14937 operates from DC to 1.7MHz and can be used in isolated I^{2}C busses with clock stretching.

The MAX14937 is available in a 16-pin, wide-body (10.3mm x 7.5mm) SOIC package, and is rated for operation at ambient temperatures of -40°C to +125°C.

Applications

- I^{2}C, SMBus, PMBus™ Interfaces
- Power Supplies
- Battery Management
- Instrumentation

Benefits and Features

- Robust Galvanic Isolation of Digital Signals
  - Withstands 5kV$_{RMS}$ for 60s (V$_{ISO}$)
  - Continuously Withstands 848V$_{RMS}$ (V$_{IOWM}$)
  - 1200V$_{PEAK}$ Repetitive Peak Voltage (V$_{IORM}$)
  - Withstands ±10kV Surge per IEC 61000-4-5
- Interfaces Directly with Most Micros and FPGAs
  - Accepts 2.25V to 5.5V Supplies
  - Bidirectional Data Transfer from DC to 1.7MHz
- Low Power Consumption
  - 5.3mA per Channel Typical at 1.7MHz

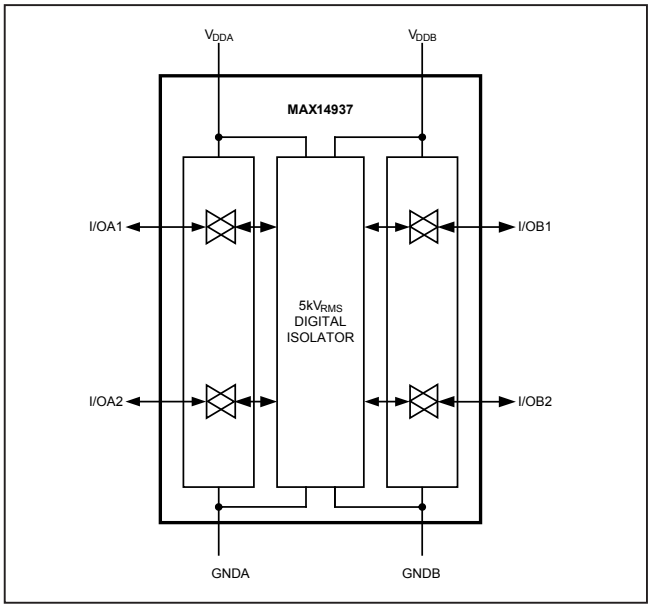
Safety Regulatory Approvals

(See *Safety Regulatory Approvals*)

- UL According to UL1577
- cUL According to CSA Bulletin 5A
- VDE 0884-11 Basic Insulation

***Ordering Information* appears at end of data sheet.**

Functional Diagram



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Absolute Maximum Ratings

V_{DDA} to GNDA .....-0.3V to +6V
V_{DDB} to GNDB .....-0.3V to +6V
I/OA_ to GNDA .....-0.3V to +6V
I/OB_ to GNDB .....-0.3V to +6V
Short-Circuit Duration
(I/OA_ to GNDA, I/OB_ to GNDB) .....Continuous

Continuous Power Dissipation (T_A = +70°C)
Wide SOIC (derate 14.1mW/ºC above +70°C) 1126.8mW
Operating Temperature Range ..... -40°C to +125°C
Maximum Junction Temperature ..... +150°C
Storage Temperature Range ..... -65°C to +150°C
Lead Temperature (soldering, 10s) ..... +300°C
Soldering Temperature (reflow) ..... +260°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Package Information

16 Wide SOIC

Package Code	W16M+8
Outline Number	**21-0042**
Land Pattern Number	**90-0107**
THERMAL RESISTANCE, FOUR-LAYER BOARD	
Junction-to-Ambient Thermal Resistance (θ_{JA})	71°C/W
Junction-to-Case Thermal Resistance (θ_{JC})	23°C/W

For the latest package outline information and land patterns (footprints), go to **www.maximintegrated.com/packages**. Note that a "+", "#", or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

Package thermal resistances were obtained using the method described in JEDEC specification JESD51-7, using a four-layer board. For detailed information on package thermal considerations, refer to **www.maximintegrated.com/thermal-tutorial**.

DC Electrical Characteristics

(V_{DDA} - V_{GNDA} = +2.25V to +5.5V, V_{DDB} - V_{GNDB} = +2.25V to +5.5V, T_A = -40°C to +125°C, unless otherwise noted. Typical values are at V_{DDA} - V_{GNDA} = +3.3V, V_{DDB} - V_{GNDB} = +3.3V, V_{GNDA} = V_{GNDB}, T_A = +25°C, unless otherwise noted.) (Notes 1 and 2)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
POWER SUPPLY							
Operating Supply Voltage	V_{DDA}	Relative to GNDA		2.25		5.5	V
	V_{DDB}	Relative to GNDB		2.25		5.5	V
Undervoltage-Lockout Threshold	$V_{UVLO\_}$	V_{DD} rising		1.7	2.0	2.2	V
Undervoltage-Lockout Threshold Hysteresis	V_{UVLO_HYST}				85		mV
Supply Current	I_{DDA}	Side A, all channels DC or 1.7MHz	V_{DDA} = 5V		6	9	mA
			V_{DDA} = 3.3V		6	9	
			V_{DDA} = 2.5V		5.9	9	
	I_{DDB}	Side B, all channels DC or 1.7MHz	V_{DDB} = 5V		4.8	8	
			V_{DDB} = 3.3V		4.8	8	
			V_{DDB} = 2.5V		4.7	8	
Static Output Loading	$I_{I/OA\_}$	Side A		0.5		3	mA
	$I_{I/OB\_}$	Side B		0.5		30	
LOGIC INPUTS AND OUTPUTS							
Input High Voltage	V_{IH}	$V_{I/OA\_}$ relative to GNDA		0.7			V
		$V_{I/OB\_}$ relative to GNDB		0.7 x V_{DDB}			
Input Low Voltage	V_{IL}	$V_{I/OA\_}$ relative to GNDA				0.5	V
		$V_{I/OB\_}$ relative to GNDB				0.3 x V_{DDB}	
Input/Output Logic-Low Level Difference	$DV_{I/OL}$	$I_{/OA\_}$ (Note 3), V_{OL} - V_{IL}		50			mV
Output Voltage Low	V_{OL}	$V_{I/OA\_}$ relative to GNDA, $I_{I/OA\_}$ = 3mA sink		600		900	mV
		$V_{I/OA\_}$ relative to GNDA, $I_{I/OA\_}$ = 0.5mA sink		600		850	
		$V_{I/OB\_}$ relative to GNDB, $I_{I/OB\_}$ = 30mA sink				400	
Leakage Current	I_L	I/OA_ = V_{DDA}, I/OB_ = V_{DDB}		-1		+1	µA
Input Capacitance	C_{IN}	I/OA_, I/OB_, f = 1MHz			5		pF

Dynamic Characteristics

(V_{DDA} - V_{GNDA} = +2.25V to +5.5V, V_{DDB} - V_{GNDB} = +2.25V to +5.5V, T_A = -40°C to +125°C, unless otherwise noted. Typical values are at V_{DDA} - V_{GNDA} = +3.3V, V_{DDB} - V_{GNDB} = +3.3V, V_{GNDA} = V_{GNDB}, T_A = +25°C, unless otherwise noted.) (Note 4)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Common-Mode Transient Immunity	CMTI	IN_ = GND_ or $V_{DD\_}$ (Note 5)			25		kV/µs
Maximum Frequency	f_{MAX}					1.7	MHz
Fall Time (Figure 1)	t_{FA}	I/OA_ = 0.9V_{DDA} to 0.9V	4.5V ≤ V_{DDA},V_{DDB} ≤ 5.5V, C_{LA} = 40pF, R_A = 1.6kΩ, C_{LB} = 400pF, R_B = 180Ω			80	ns
			3.0V ≤ V_{DDA},V_{DDB} ≤ 3.6V, C_{LA} = 40pF, R_A = 1kΩ, C_{LB} = 400pF, R_B = 120Ω			65	
			2.25V ≤ V_{DDA},V_{DDB} ≤ 2.75V, C_{LA} = 40pF, R_A = 810Ω, C_{LB} = 400pF, R_B = 91Ω			55	
	t_{FB}	I/OB_ = 0.9V_{DDB} to 0.1V_{DDB}	4.5V ≤ V_{DDA},V_{DDB} ≤ 5.5V, C_{LA} = 40pF, R_A = 1.6kΩ, C_{LB} = 400pF, R_B = 180Ω			35	
			3.0V ≤ V_{DDA},V_{DDB} ≤ 3.6V, C_{LA} = 40pF, R_A = 1kΩ, C_{LB} = 400pF, R_B = 120Ω			45	
			2.25V ≤ V_{DDA},V_{DDB} ≤ 2.75V, C_{LA} = 40pF, R_A = 810kΩ, C_{LB} = 400pF, R_B = 91Ω			75	
Propagation Delay (Figure 1)	t_{PLHAB}	I/OA_ = 0.5V_{DDA} to I/OB_ = 0.7V_{DDB}	4.5V ≤ V_{DDA},V_{DDB} ≤ 5.5V, C_{LA} = 0pF, R_A = 1.6kΩ, C_{LB} = 0pF, R_B = 180Ω			20	ns
			3.0V ≤ V_{DDA},V_{DDB} ≤ 3.6V, C_{LA} = 0pF, R_A = 1kΩ, C_{LB} = 0pF, R_B = 120Ω			25	
			2.25V ≤ V_{DDA},V_{DDB} ≤ 2.75V, C_{LA} = 0pF, R_A = 810Ω, C_{LB} = 0pF, R_B = 91Ω			35	
	t_{PHLAB}	I/OA_ = 0.5V_{DDA} to I/OB_ = 0.4V	4.5V ≤ V_{DDA},V_{DDB} ≤ 5.5V, C_{LA} = 0pF, R_A = 1.6kΩ, C_{LB} = 0pF, R_B = 180Ω			80	
			3.0V ≤ V_{DDA},V_{DDB} ≤ 3.6V, C_{LA} = 0pF, R_A = 1kΩ, C_{LB} = 0pF, R_B = 120Ω			95	
			2.25V ≤ V_{DDA},V_{DDB} ≤ 2.75V, C_{LA} = 0pF, R_A = 810Ω, C_{LB} = 0pF, R_B = 91Ω			110	

Dynamic Characteristics (continued)

(V_{DDA} - V_{GNDA} = +2.25V to +5.5V, V_{DDB} - V_{GNDB} = +2.25V to +5.5V, T_A = -40°C to +125°C, unless otherwise noted. Typical values are at V_{DDA} - V_{GNDA} = +3.3V, V_{DDB} - V_{GNDB} = +3.3V, V_{GNDA} = V_{GNDB}, T_A = +25°C, unless otherwise noted.) (Note 4)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Propagation Delay (Figure 1)	t_{PLHBA}	I/OB_ = 0.5V_{DDB} to I/OA_ = 0.7V_{DDA}	4.5V ≤ V_{DDA}, V_{DDB} ≤ 5.5V, C_{LA} = 0pF, R_A = 1.6kΩ, C_{LB} = 0pF, R_B = 180Ω			25	ns
			3.0V ≤ V_{DDA}, V_{DDB} ≤ 3.6V, C_{LA} = 0pF, R_A = 1kΩ, C_{LB} = 0pF, R_B = 120Ω			25	
			2.25V ≤ V_{DDA}, V_{DDB} ≤ 2.75V, C_{LA} = 0pF, R_A = 810Ω, C_{LB} = 0pF, R_B = 91Ω			35	
	t_{PHLBA}	I/OB_ = 0.5V_{DDB} to I/OA_ = 0.9V	4.5V ≤ V_{DDA}, V_{DDB} ≤ 5.5V, C_{LA} = 0pF, R_A = 1.6kΩ, C_{LB} = 0pF, R_B = 180Ω			115	
			3.0V ≤ V_{DDA}, V_{DDB} ≤ 3.6V, C_{LA} = 0pF, R_A = 1kΩ, C_{LB} = 0pF, R_B = 120Ω			115	
			2.25V ≤ V_{DDA}, V_{DDB} ≤ 2.75V, C_{LA} = 0pF, R_A = 810Ω, C_{LB} = 0pF, R_B = 91Ω			125	
Pulse-Width Distortion	PWD_{AB}	$\lvert t_{PLHAB} - t_{PHLAB} \rvert$	4.5V ≤ V_{DDA}, V_{DDB} ≤ 5.5V			65	ns
			3.0V ≤ V_{DDA}, V_{DDB} ≤ 3.6V			65	
			2.25V ≤ V_{DDA}, V_{DDB} ≤ 2.75V			80	
	PWD_{BA}	$\lvert t_{PLHBA} - t_{PHLBA} \rvert$	4.5V ≤ V_{DDA}, V_{DDB} ≤ 5.5V			95	
			3.0V ≤ V_{DDA}, V_{DDB} ≤ 3.6V			95	
			2.25V ≤ V_{DDA}, V_{DDB} ≤ 2.75V			100	

ESD Protection

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
ESD		Human body model, all pins		±4		kV

Note 1: All devices are 100% production tested at T_A = +125°C. Specifications over temperature are guaranteed by design.

Note 2: All currents into the device are positive; all currents out of the device are negative. All voltages are referenced to ground on the corresponding side of the device, unless otherwise noted.

Note 3: This is the minimum difference between the output logic-low level and the input logic threshold. This ensures that there is no possibility of the part latching up the bus to which it is connected.

Note 4: Not production tested. Guaranteed by design.

Note 5: CMTI is the maximum sustainable common-mode voltage slew rate while maintaining operation. CMTI applies to both rising and falling common-mode voltage edges. Tested with the transient generator connected between GNDA and GNDB (V_{CM} = 1000V).

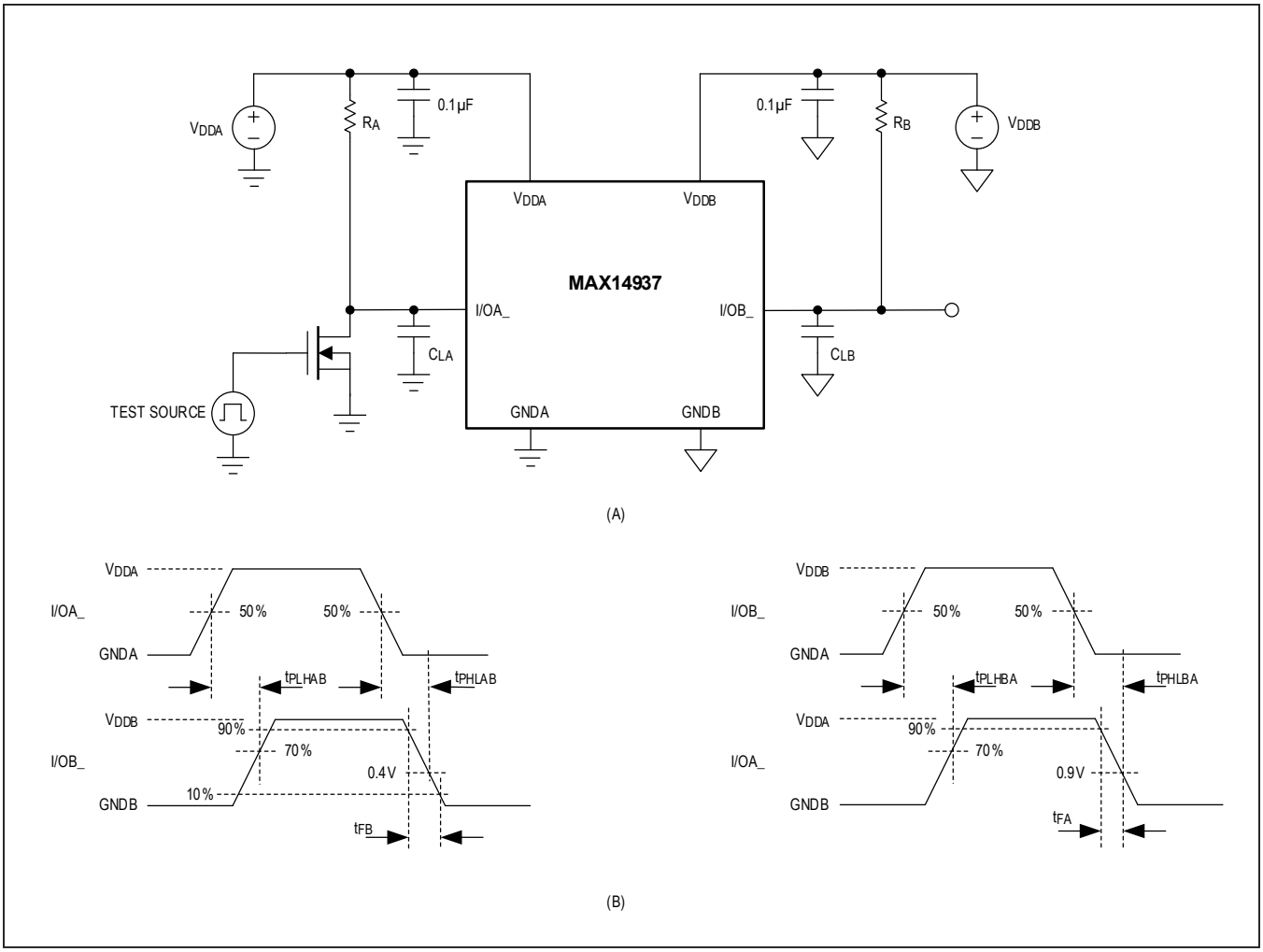


Figure 1. Test Circuit (A) and Timing Diagrams (B)

Safety Regulatory Approvals

UL
The MAX14937 is certified under UL1577. For more details, refer to file E351759.
Rated up to 5000V$_{RMS}$ isolation voltage for single protection.
cUL (Equivalent to CSA notice 5A)
The MAX14937 is certified up to 5000V$_{RMS}$ for single protection. For more details, refer to file E351759.
VDE
The MAX14937 is certified to DIN VDE V 0884-11: 2017-01. For details, see file ref. 5015017-4880-0001/272147/TL7/SCT. Basic Insulation, Maximum Transient Isolation Voltage 8400V$_{PK}$, Maximum Repetitive Peak Isolation Voltage 1200V$_{PK}$

This coupler is suitable for "safe electrical insulation" only within the safety ratings. Compliance with the safety ratings shall be ensured by means of suitable protective circuits.

IEC Insulation Testing

TUV
The MAX14937 is tested under TUV.
IEC 60950-1: Up to 1200V$_{PK}$ (848V$_{RMS}$) working voltage for basic insulation.
IEC 61010-1 (ed. 3): Up to 848V$_{RMS}$ working voltage for basic insulation. For details, see Technical Report number 095-72100581-100.
IEC 60601-1 (ed. 3): For details see Technical Report number 095-72100581-200.
Basic insulation 1 MOOP, 1200V$_{PK}$ (848V$_{RMS}$)
Withstand isolation voltage V$_{ISO}$ for 60s 5000V$_{RMS}$

Insulation Characteristics

PARAMETER	SYMBOL	CONDITIONS	VALUE	UNITS
Partial Discharge Test Voltage	V_{PR}	Method B1 = V_{IORM} x 1.875 (t = 1s, partial discharge < 5pC)	2250	V_P
Maximum Repetitive Peak Isolation Voltage	V_{IORM}	(Note 6)	1200	V_P
Maximum Working Isolation Voltage	V_{IOWM}	Continuous RMS voltage (Note 6)	848	V_{RMS}
Maximum Transient Isolation Voltage	V_{IOTM}	t = 1s (Note 6)	8400	V_P
Maximum Withstand Isolation Voltage	V_{ISO}	f_{SW} = 60Hz, duration = 60s (Note 6, 7)	5000	V_{RMS}
Maximum Surge Isolation Voltage	V_{IOSM}	Basic insulation, 1.2/50µs pulse per IEC 61000-4-5 (Note 6, 8)	10	kV
Insulation Resistance	R_{IO}	V_{IO} = 500V, T_A = 25°C	> 10^{12}	Ω
		V_{IO} = 500V, 100°C ≤ T_A ≤ 125°C	> 10^{11}	
		V_{IO} = 500V at T_S = 150°C	> 10^9	
Barrier Capacitance Side A to Side B	C_{IO}	f_{SW} = 1MHz (Note 9)	2	pF
Minimum Creepage Distance	CPG	Wide SOIC	8	mm
Minimum Clearance Distance	CLR	Wide SOIC	8	mm
Internal Clearance		Distance through insulation	0.015	mm
Comparative Tracking Index	CTI	Material Group II (IEC 60112)	575	
Climatic Category			40/125/21	
Pollution Degree (DIN VDE 0110, Table 1)			2	

Note 6: V_{ISO}, V_{IOTM}, V_{IOSM}, V_{IOWM}, and V_{IORM} are defined by the IEC 60747-5-5 standard.
Note 7: Products are qualified at V_{ISO} for 60s and 100% production tested at 120% of V_{ISO} for 1s.
Note 8: Devices are immersed in oil during surge characterization.
Note 9: Capacitance is measured with all pins on field-side and logic-side tied together.

Safety Limits

Damage to the IC can result in a low-resistance path to ground or to the supply and, without current limiting, the MAX14937 could dissipate excessive amounts of power. Excessive power dissipation can damage the die and result in damage to the isolation barrier, potentially causing downstream issues. Table 1 shows the safety limits for the MAX14937.

The maximum safety temperature (T_S) for the device is the 150°C maximum junction temperature specified in the *Absolute Maximum Ratings*. The power dissipation (P_D) and junction-to-ambient thermal impedance (θ_{JA}) determine the junction temperature. Thermal impedance values (θ_{JA} and θ_{JC}) are available in the *Package Information* section of the datasheet. Calculate the junction temperature (T_J) as:

$$T_J = T_A + (P_D \times \theta_{JA})$$

Figure 2 to Figure 3 show the thermal derating curves for the safety power limiting of the device and the safety current limiting of the device. Ensure that the junction temperature does not exceed 150°C.

Table 1. Safety Limiting Values for the MAX14937

PARAMETER	SYMBOL	TEST CONDITIONS	MAX	UNITS
Safety Current on Any Pin (No Damage to Isolation Barrier)	I_S	T_J = 150°C, T_A = 25°C	300	mA
Total Safety Power Dissipation	P_S	T_J = 150°C, T_A = 25°C	1760	mW
Maximum Safety Temperature	T_S		150	°C

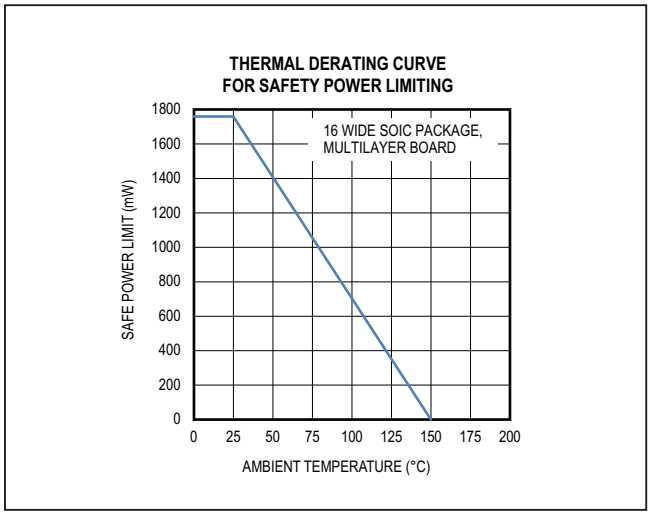


Figure 2. Thermal Derating Curve for Safety Power Limiting

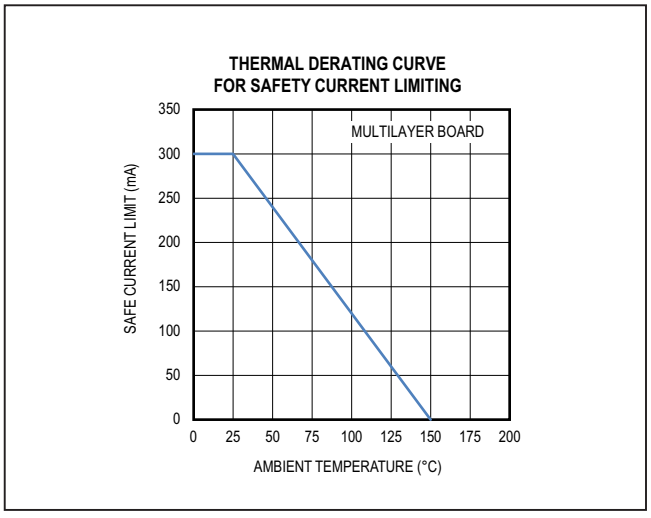
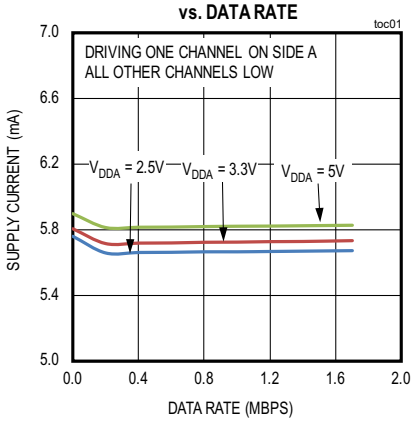


Figure 3. Thermal Derating Curve for Safety Current Limiting

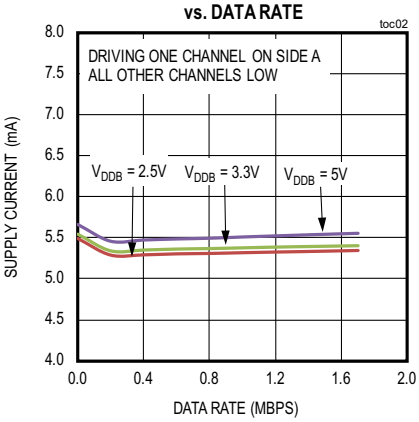
Typical Operating Characteristics

(V_{DDA} - V_{GNDA} = +3.3V, V_{DDB} - V_{GNDB} = +3.3V, V_{GNDA} = V_{GNDB}, T_A = +25°C, unless otherwise noted.)

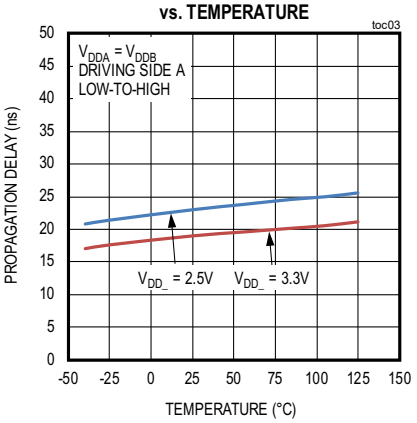
SIDE A SUPPLY CURRENT vs. DATA RATE



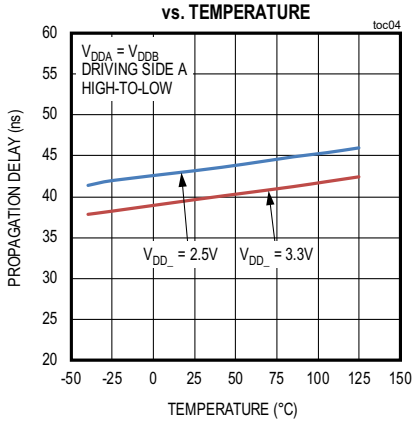
SIDE B SUPPLY CURRENT vs. DATA RATE



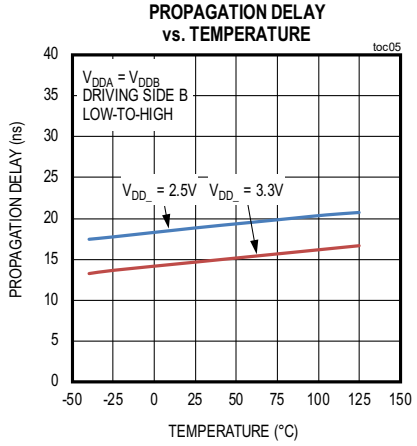
PROPAGATION DELAY vs. TEMPERATURE



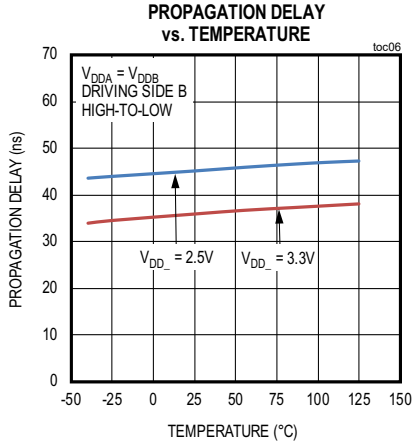
PROPAGATION DELAY vs. TEMPERATURE



PROPAGATION DELAY vs. TEMPERATURE



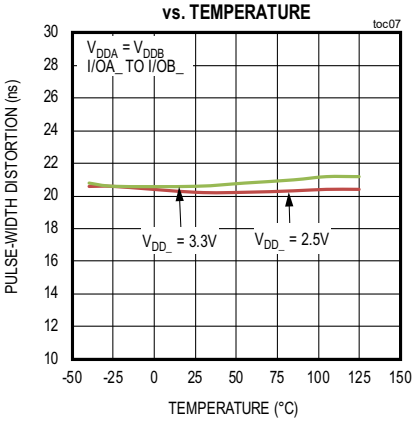
PROPAGATION DELAY vs. TEMPERATURE



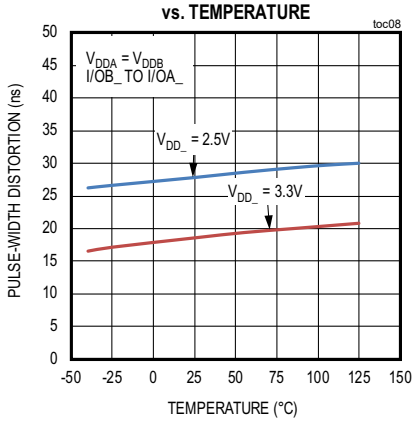
Typical Operating Characteristics (continued)

(V_{DDA} - V_{GNDA} = +3.3V, V_{DDB} - V_{GNDB} = +3.3V, V_{GNDA} = V_{GNDB}, T_A = +25°C, unless otherwise noted.)

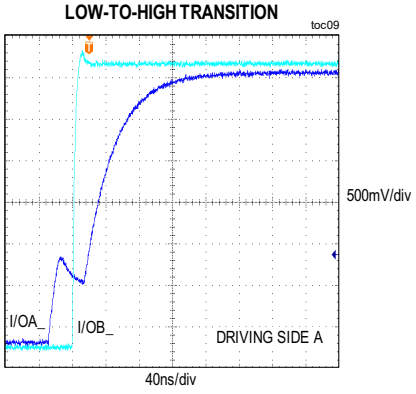
PULSE-WIDTH DISTORTION vs. TEMPERATURE



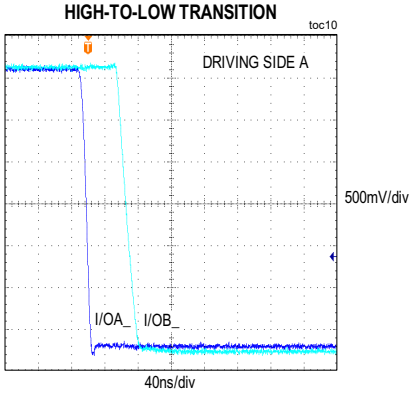
PULSE-WIDTH DISTORTION vs. TEMPERATURE



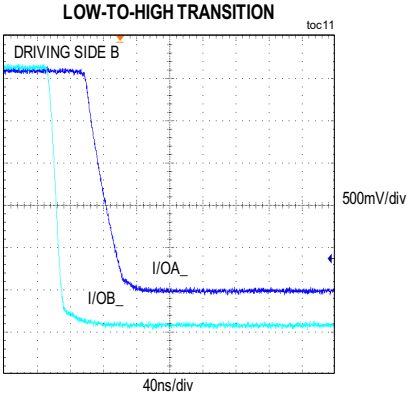
LOW-TO-HIGH TRANSITION



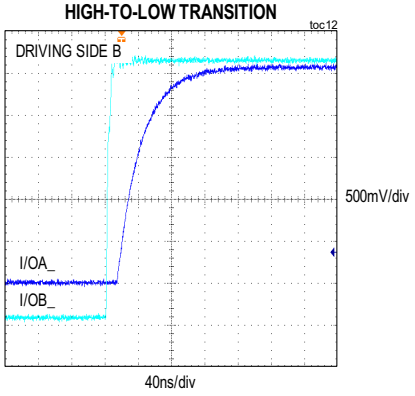
HIGH-TO-LOW TRANSITION



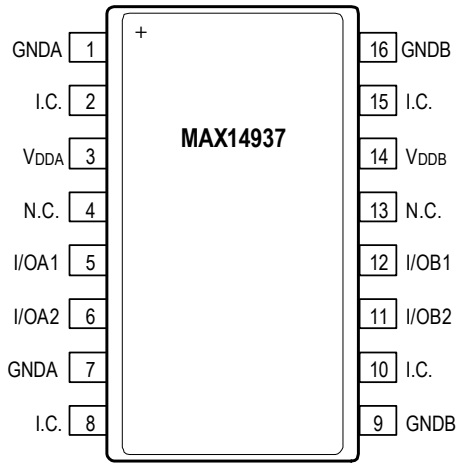
LOW-TO-HIGH TRANSITION



HIGH-TO-LOW TRANSITION



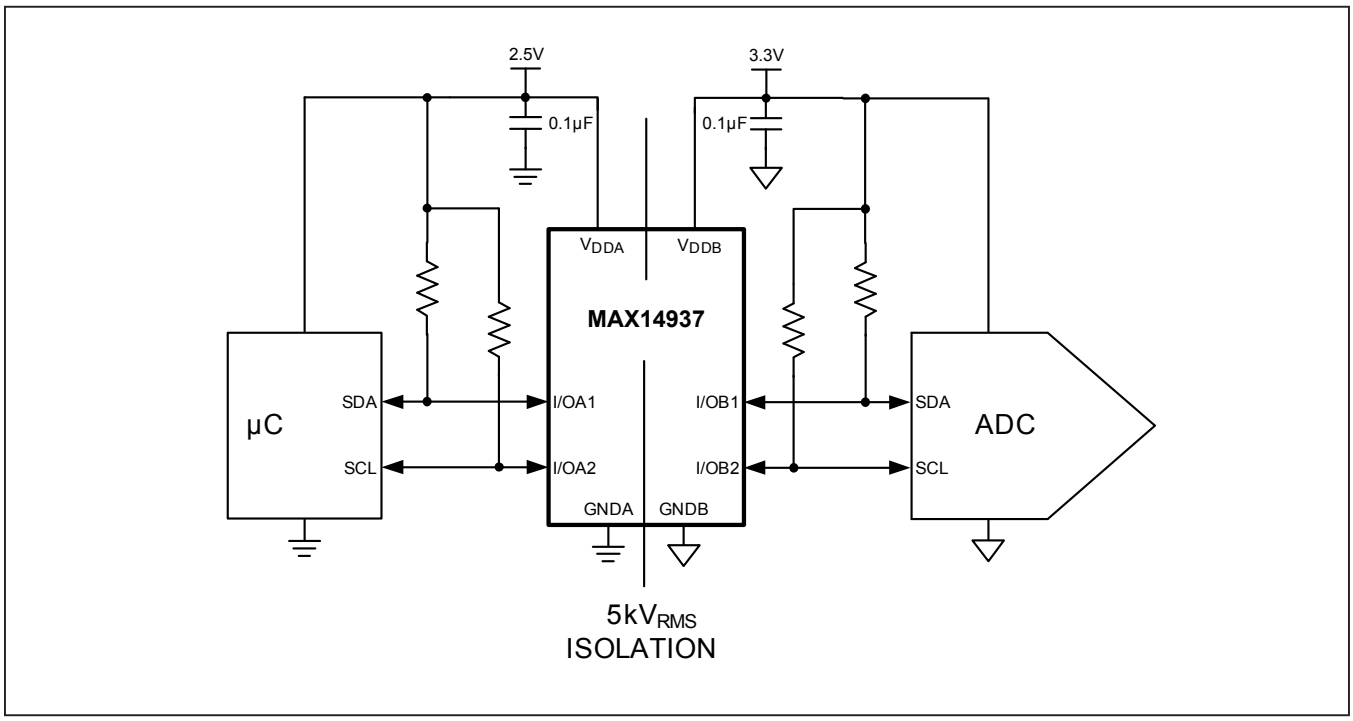
Pin Configuration



Pin Description

PIN	NAME	FUNCTION	VOLTAGE RELATIVE TO
1, 7	GNDA	Ground Reference For Side A. Ensure both pins 1 and 7 are connected to GNDA.	—
2, 8	I.C.	Internally Connected. Connect to GNDA or leave unconnected.	GNDA
3	V_{DDA}	Power Supply. Bypass V_{DDA} with a 0.1µF ceramic capacitor as close as possible to the pin.	GNDA
4, 13	N.C.	No Connection. Not internally connected.	—
5	I/OA1	Bidirectional Input/Output 1 On Side A. I/OA1 is translated to/from I/OB1 and is an open-drain output.	GNDA
6	I/OA2	Bidirectional Input/Output 2 On Side A. I/OA2 is translated to/from I/OB2 and is an open-drain output.	GNDA
9, 16	GNDB	Ground Reference For Side B.	—
10, 15	I.C.	Internally Connected. Connect to GNDB or leave unconnected.	GNDB
11	I/OB2	Bidirectional Input/Output 2 On Side B. I/OB2 is translated to/from I/OA2 and is an open-drain output.	GNDB
12	I/OB1	Bidirectional Input/Output 1 On Side B. I/OB1 is translated to/from I/OA1 and is an open-drain output.	GNDB
14	V_{DDB}	Power Supply. Bypass V_{DDB} with a 0.1µF ceramic capacitor as close as possible to the pin.	GNDB

Typical Application Circuit



Detailed Description

The MAX14937 is a two-channel, 5kV$_{RMS}$ I^{2}C isolator utilizing Maxim's proprietary process technology. For applications requiring 2.75kV$_{RMS}$ of isolation, refer to the MAX14933 data sheet. The MAX14937 transfers digital signals between circuits with different power domains at ambient temperatures up to +125°C.

The device offers two bidirectional, open-drain channels for applications, such as I^{2}C, that require data to be transmitted in both directions on the same line.

The device features independent 2.25V to 5.5V supplies on each side of the isolator. The device operates from DC to 1.7MHz and can be used in isolated I^{2}C busses with clock stretching. The wide temperature range and high isolation voltage make the device ideal for use in harsh industrial environments.

Digital Isolation

The device provides galvanic isolation for digital signals that are transmitted between two ground domains. Up to 1200V$_{PEAK}$ of continuous isolation is supported as well as transient differences of up to 5kV$_{RMS}$ for up to 60s.

Bidirectional Channels

The device features two bidirectional channels that have open-drain outputs. The bidirectional channels do not require a direction control input. A logic-low on one side causes the corresponding pin on the other side to be pulled low while avoiding data latching within the device. I/OA1 and I/OA2 outputs comprise special buffers that regulate the logic-low voltage at approximately 0.7V. The input logic-low threshold (V_{IL}) of I/OA1 and I/OA2 is at least 50mV lower than the output logic-low voltage of I/OA1 and I/OA2. This prevents an output logic-low on side A from being accepted as an input low and subsequently transmitted to side B; thus, preventing a latching action. I/OB1 and I/OB2 are conventional outputs that do not regulate the logic-low output voltage.

Due to their nature, the A-side output buffers of the MAX14937 cannot be connected together, or to a device with similar buffers or rise-time accelerators. The B-side output buffers of the MAX14937, instead can be connected together, or to any other bidirectional buffer or level translator.

The I/OA1, I/OA2, I/OB1, and I/OB2 pins have open-drain outputs, requiring pullup resistors to their respective supplies for logic-high outputs. The output low voltages are guaranteed for sink currents of up to 30mA for side B, and 3mA for side A (see the *DC Electrical Characteristics* table). The device supports I^{2}C clock stretching.

Startup and Undervoltage Lockout

The V_{DDA} and V_{DDB} supplies are both internally monitored for undervoltage conditions. Undervoltage events can occur during power-up, power-down, or during normal operation due to a sagging supply voltage. When an undervoltage event is detected on either of the supplies, all bidirectional outputs become high-impedance and are pulled high by the external pullup resistor on the open-drain outputs (Table 2). Figure 4 through Figure 7 show the behavior of the outputs during power-up and power-down.

Applications Information

Effect of Continuous Isolation on Lifetime

High-voltage conditions cause insulation to degrade over time. Higher voltages result in faster degradation. Even the high-quality insulating material used in the device can degrade over long periods of time with a constant high voltage across the isolation barrier.

Power-Supply Sequencing

The MAX14937 does not require special power-supply sequencing. The logic levels are set independently on either side by V_{DDA} and V_{DDB}. Each supply can be present over the entire specified range regardless of the level or presence of the other supply.

Power-Supply Decoupling

To reduce ripple and the chance of introducing data errors, bypass V_{DDA} and V_{DDB} with 0.1µF ceramic capacitors to GNDA and GNDB, respectively. Place the bypass capacitors as close as possible to the power-supply input.

Input/Output Capacitive Loads

For optimal performance, ensure that $C_{LA} \leq 40pF$ and $C_{LB} \leq 400pF$ (see Figure 1).

Layout Considerations

The PCB designer should follow some critical recommendations in order to get the best performance from the design.

- Keep the input/output traces as short as possible. To keep signal paths low-inductance, avoid using vias.
- Have a solid ground plane underneath the high-speed signal layer.
- Keep the area underneath the MAX14937 free from ground and signal planes. Any galvanic or metallic connection between the Side A and Side B defeats the isolation.

Table 2. Output Behavior During Undervoltage Conditions

V_{DDA}	V_{DDB}	$V_{I/OA\_}$	$V_{I/OB\_}$
Powered	Powered	1	1
Powered	Powered	0	0
Undervoltage	Powered	High-Z	High-Z
Powered	Undervoltage	High-Z	High-Z

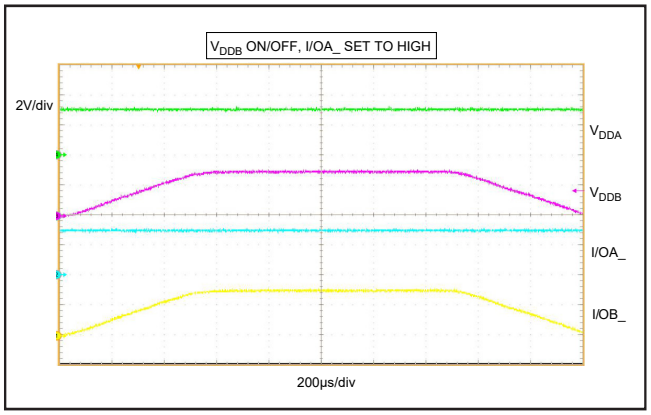


Figure 4. Undervoltage-Lockout Behavior (I/OB_ Set High)

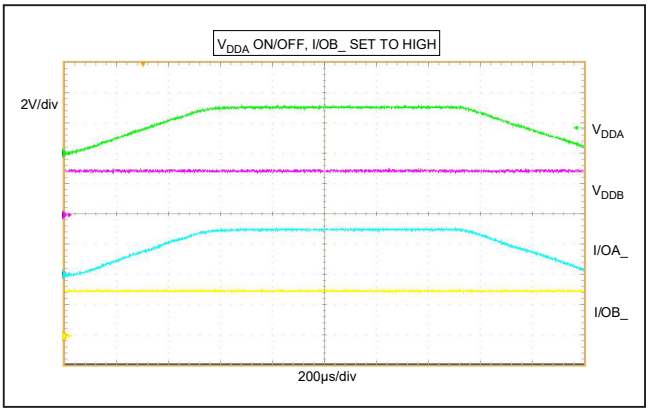


Figure 5. Undervoltage-Lockout Behavior (I/OA_ Set High)

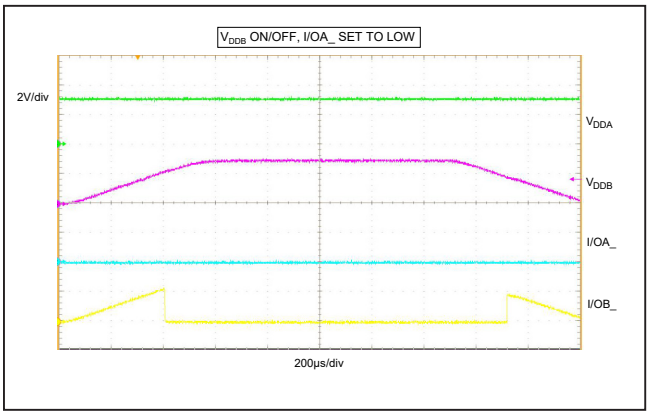


Figure 6. Undervoltage-Lockout Behavior (I/OB_ Set Low)

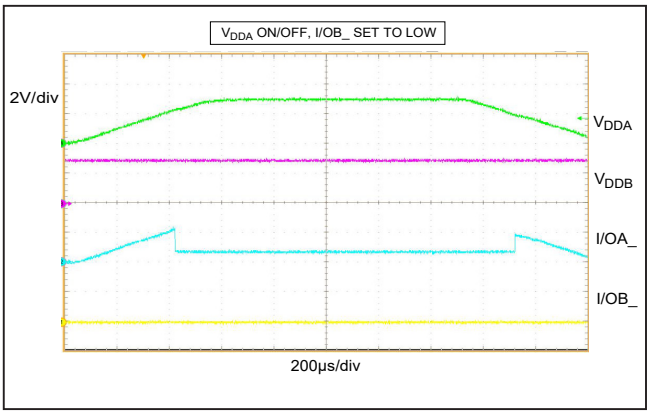


Figure 7. Undervoltage-Lockout Behavior (I/OA_ Set Low)

Ordering Information

PART	TEMP RANGE	PIN-PACKAGE
MAX14937AWE+	-40ºC to +125ºC	16 Wide SOIC

+Denotes a lead(Pb)-free/RoHS-compliant package.

Chip Information

PROCESS: BiCMOS

Revision History

REVISION NUMBER	REVISION DATE	DESCRIPTION	PAGES CHANGED
0	3/15	Initial release	—
1	5/16	Updated TUV information and added *IEC Insulation Testing* table	1, 6
2	1/17	Removed VDE pending	6
3	10/19	Updated *General Description* and replaced the *Bidirectional Channels* sections; corrected typos	1, 6, 12
4	11/20	Updated the *Safety Regulatory Approvals*, *Absolute Maximum Ratings, Dynamic Characteristics, Safety Regulatory Approvals, IEC Insulation Testing, Detailed Description,* and *Applications Information* sections; replaced the *Insulation Characteristics* table, *Figure 1*; added *Figure 2*, *3,* and *Table 1* and renumbered subsequent Figures and Tables	1, 2, 4–8, 13, 14

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