*Click **here** to ask an associate for production status of specific part numbers.*

MAX11259

24-Bit, 6-Channel, 16ksps, 6.2nV/√Hz PGA, Delta-Sigma ADC with I²C Interface

General Description

The MAX11259 is a 6-channel, 24-bit delta-sigma ADC that achieves exceptional performance while consuming very low power. Sample rates up to 16ksps allow precision DC measurements. The MAX11259 communicates via an I²C-compatible serial interface and is available in a small (3mm x 3mm) WLP package.

The MAX11259 offers a 6.2nV/√Hz noise programmable gain amplifier (PGA) with gain settings from 1x to 128x. The integrated PGA provides isolation of the signal inputs from the switched capacitor sampling network. The PGA also enables the MAX11259 to interface directly with high-impedance sources without compromising available dynamic range.

The MAX11259 operates from a single 2.7V to 3.6V analog supply, or split ±1.8V analog supplies, allowing the analog input to be sampled below ground. The digital supply range is 1.7V to 2.0V or 2.0V to 3.6V, allowing communication with 1.8V, 2.5V, 3V, or 3.3V logic.

Applications

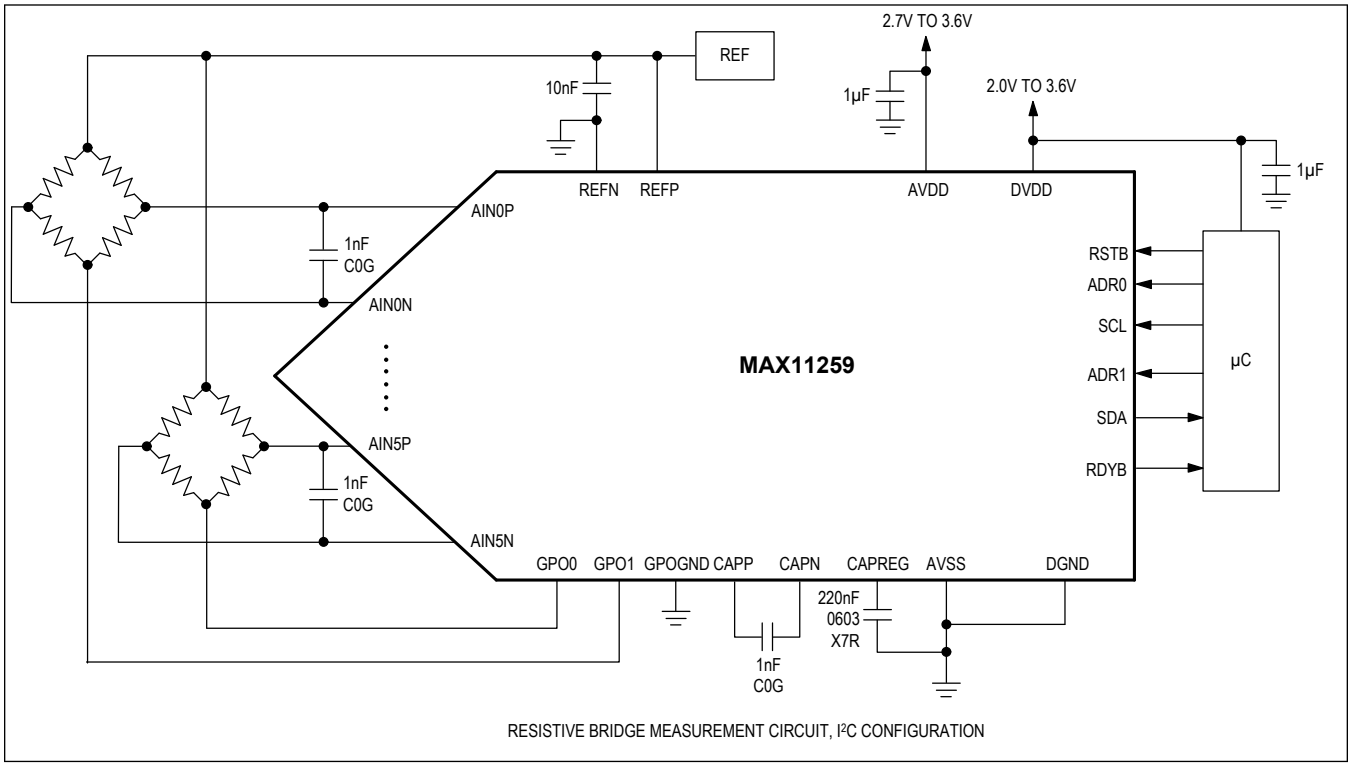
- Wearable Electronics
- Weigh Scales
- Pressure Sensors
- Battery-Powered Instrumentation

Benefits and Features

- High Resolution for Industrial Applications that Require a Wide Dynamic Range
  - 133dB SNR at 50sps
  - 124dB SNR at 1000sps
- Longer Battery Life for Portable Applications
  - 2.2mA Operating Mode Current
  - 1µA Sleep Current
- Single or Split Analog Supplies Provide Input Voltage Range Flexibility
  - 2.7V to 3.6V (Single Supply) or ±1.8V (Split Supply)
- Enables System Integration
  - Low Noise, 6.2nV/√Hz PGA with Gains of 1, 2, 4, 8, 16, 32, 64, 128
  - 6-Channel, Fully Differential Input
- Enables On-Demand Device and System Gain and Offset Calibration
  - User-Programmable Offset and Gain Registers
- Robust Performance in a Small Package
  - -40°C to +125°C Operating Temperature Range
  - WLP Package, 3mm x 3mm (6 x 6 Ball Array)

19-7749; Rev 1; 10/20

Typical Application Circuit



RESISTIVE BRIDGE MEASUREMENT CIRCUIT, I²C CONFIGURATION

Absolute Maximum Ratings

AVDD to AVSS ..... -0.3V to +3.9V
AVDD to DGND ..... -0.3V to +3.9V
DVDD to DGND ..... -0.3V to +3.9V
AVSS to DGND ..... -1.95V to +0.3V
DVDD to AVSS ..... -0.3V to +3.9V
AVSS to GPOGND ..... -1.95V to +0.3V
GPOGND to DGND ..... -1.95V to +0.3V
AIN_P, AIN_N,REFP, REFN, CAPP, CAPN to AVSS .. -0.3 to the lower of +3.9V or (V_{AVDD} + 0.3V)
GPO_ to GPOGND ... -0.3V to to the lower of +3.9V or (V_{AVDD} + 0.3V)
CAPREG to AVSS ..... -0.3V to +3.9V
CAPREG to DGND ..... -0.3V to +2.1V
All Other Bumps to DGND ..... -0.3V to the lower of +3.9V or (V_{DVDD} + 0.3V)
Maximum Continuous Current into Any Bumps Except GPOGND Bump ..... ±50mA
Maximum Continuous Current into GPOGND Bump ..... ±100mA
Continuous Power Dissipation (T_A = +70°C) WLP (derate 26.3mW/°C above +70°C) 2105mW
Operating Temperature Range ..... -40ºC to +125ºC
Junction Temperature ..... +150°C
Storage Temperature Range ..... -55°C to +150°C
Soldering Temperature (reflow) ..... +260°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Package Information

36 WLP

Package Code	W362C2+1
Outline Number	21-0898
Land Pattern Number	*Refer to Application Note 1891*
THERMAL RESISTANCE, FOUR-LAYER BOARD	
Junction to Ambient (θ_{JA})	38°C/W

Note 1: Package thermal resistances were obtained using the method described in JEDEC specification JESD51-7, using a four-layer board. For detailed information on package thermal *www.maximintegrated.com/thermal-tutorial.*considerations, refer to www.maximintegrated.com/thermal-tutorial.

Note 2: Refer to *Application Note 1891: Wafer-Level Packaging (WLP) and its Applications* for information about the thermal performance of WLP packaging.

For the latest package outline information and land patterns (footprints), go to *www.maximintegrated.com/packages*. Note that a "+", "#", or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

Package thermal resistances were obtained using the method described in JEDEC specification JESD51-7, using a four-layer board. For detailed information on package thermal considerations, refer to *www.maximintegrated.com/thermal-tutorial*.

Electrical Characteristics

(V_{AVDD} = 3.6V, V_{AVSS} = 0V, V_{DVDD} = 2.0V to 3.6V, V_{REFP} - V_{REFN} = V_{AVDD}, DATA RATE = 1ksps, PGA low-noise mode, single-cycle conversion mode (SCYCLE = 1). T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at T_A = +25°C.)(Note 3)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
STATIC PERFORMANCE (Single-Cycle Conversion Mode)							
Noise Voltage (Referred to Input)	V_n	PGA gain of 128, single-cycle mode at 1ksps data rate	PGA low-noise mode		0.19		μV_{RMS}
			PGA low-power mode		0.26		
		PGA gain of 128, single-cycle mode at 12.8ksps data rate	PGA low-noise mode		0.83		
			PGA low-power mode		1.16		
Integral Nonlinearity	INL				3	15	ppm
Zero Error	Z_{ERR}	After system zero-scale calibration			1		µV
Zero Drift	Z_{Drift}				50		nV/°C
Full-Scale Error	FSE	After system full-scale calibration (Notes 4 and 5)			2		ppmFSR
Full-Scale Error Drift	FSE_{Drift}				0.05		ppm FSR/°C
Common-Mode Rejection	CMR	DC rejection		110	130		dB
		50Hz/60Hz rejection (Note 6)		110	130		
		DC rejection with PGA gain 64		80	105		
		DC rejection with PGA gain 128			95		
AVDD, AVSS Supply Rejection Ratio	PSRRA	DC rejection		73	95		dB
		50Hz/60Hz rejection (Note 6)		75	95		
		DC rejection with PGA gain 128		65	75		
DVDD Supply Rejection Ratio	PSRRD	DC rejection		105	115		dB
		50Hz/60Hz rejection (Note 6)		105	115		
		DC rejection with PGA gain 128		90	110		
PGA							
Gain Setting				1		128	V/V
Noise-Spectral Density	NSD	Low-noise mode			6.2		nV/√Hz
		Low-power mode			10		
Gain Error, Not Calibrated	G_{ERR}	Gain = 1			0.75		%
		Gain = 2			1.2		
		Gain = 4			2		
		Gain = 8			3		
		Gain = 16			4.5		
		Gain = 32			6		
		Gain = 64			5.5		
		Gain = 128			2		
Output Voltage Range	$VOUT_{RNG}$			V_{AVSS} + 0.3		V_{AVDD} - 0.3	V

Electrical Characteristics (continued)

(V_{AVDD} = 3.6V, V_{AVSS} = 0V, V_{DVDD} = 2.0V to 3.6V, V_{REFP} - V_{REFN} = V_{AVDD}, DATA RATE = 1ksps, PGA low-noise mode, single-cycle conversion mode (SCYCLE = 1). T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at T_A = +25°C.)(Note 3)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
MUX						
Channel-to-Channel Isolation	ISO_{CH-CH}	DC		140		dB
GENERAL-PURPOSE OUTPUTS						
Resistance (On)	R_{ON}	GPO_ output current = 30mA, GPOGND connected to AVSS		3.5	10	Ω
Maximum Current (On)	I_{MAX}	Per output		30		mA
		Total from all outputs into GPOGND bump (Note 6)			90	
Leakage Current (Off)	I_{leak1}	Current into the GPOGND bump with one individual GPO_ bump connected to 3V		0.4		nA
	I_{leak3}	Current into the GPOGND bump with all GPO_ bumps connected to 3V		13	160	
POWER-UP DELAYS (Note 6)						
Power-Up Time	T_{PUPSLP}	SLEEP state (full power-down) to LDO wake-up V_{AVDD} = 2.7V, V_{DVDD} = 2.0V, CAPREG = 220nF		23	50	µs
	T_{PUPSBY}	STANDBY state (analog blocks powered down, LDO on) to Active		4	8	
RSTB Fall to RDYB '1'	t_{R2}	RDYB transition from '0' to '1' on falling edge of RSTB, internal clock mode (Note 6)			300	ns
	t_{R3}	RDYB transition from '0' to '1' on falling edge of RSTB, external clock mode, clock frequency = f_{CLK} (Note 6)			$2/f_{CLK}$	s
ANALOG INPUTS/REFERENCE INPUTS						
Common-Mode Input Voltage Range, V_{CM} = (V_{AIN_P} + V_{AIN_N})/2	CMI_{RNG}	Direct (PGA bypassed)	V_{AVSS}		V_{AVDD}	V
		PGA	V_{AVSS} + 0.4		V_{AVDD} - 1.3	
Input Voltage Range (AIN_P, AIN_N)	$V_{IN(RNG)}$	Direct (PGA bypassed)	V_{AVSS}		V_{AVDD}	V
		PGA	V_{AVSS} + 0.4		V_{AVDD} - 1.3	
Differential Input Voltage Range (AIN_P – AIN_N)	$V_{IN(DIFF)}$	Unipolar	0		V_{REF}	V
		Bipolar	$-V_{REF}$		$+V_{REF}$	
DC Input Leakage	I_{IN_LEAK}	SLEEP state enabled		±0.1		nA
Differential Input Conductance	G_{DIFF}	Direct (PGA bypassed) (Note 6)		±11.6		µA/V
Differential Input Current	I_{DIFF}	PGA enabled (Note 6)		±1.0		nA
Common-Mode Input Conductance	G_{CM}	Direct (PGA bypassed) (Note 6)		±1.0		µA/V
Common-Mode Input Current	I_{CM}	PGA enabled (Note 6)		±10		nA

Electrical Characteristics (continued)

(V_{AVDD} = 3.6V, V_{AVSS} = 0V, V_{DVDD} = 2.0V to 3.6V, V_{REFP} - V_{REFN} = V_{AVDD}, DATA RATE = 1ksps, PGA low-noise mode, single-cycle conversion mode (SCYCLE = 1). T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at T_A = +25°C.)(Note 3)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Reference Differential Input Resistance	R_{REF}	Active state		26		kΩ
Reference Differential Input Current	I_{REF_PD}	STANDBY and SLEEP state		±1		nA
Input Capacitance	C_{IN}	Direct (PGA bypassed)		2.5		pF
	CP_{GAIN}	PGA		0.25		
AIN_P, AIN_N Sampling Rate	f_S			4.096		MHz
Reference Voltage Range (REFP, REFN)	$V_{REF(RNG)}$	(Note 7)			V_{AVDD}	V
Differential Reference Voltage Range (REFP - REFN)	V_{REF}		1.5		V_{AVDD}	V
REFP, REFN Sampling Rate				4.096		MHz
SENSOR FAULT DETECT CURRENTS						
Current				1.1		µA
Initial Tolerance				±10		%
Drift				0.3		%/°C
DIGITAL SINC FILTER RESPONSE						
Bandwidth (-3dB)				0.203 x DATA RATE		Hz
Settling Time (Latency)				5/DATA RATE		s
LOGIC INPUTS						
Input Voltage Range	V_{IN}	For SDA and SCL bumps	0		V_{DVDD}	V
Input Current	$IDIGI_{LEAK}$	Leakage current			±1	µA
Input Low Voltage	V_{IL}				0.3 x V_{DVDD}	V
Input High Voltage	V_{IH}		0.7 x V_{DVDD}			V
Input Hysteresis	V_{HYS}			200		mV
GPIO Input Low Voltage	V_{IL_GPIO}				0.3	V
GPIO Input High Voltage	V_{IH_GPIO}		1.2			V
GPIO Input Hysteresis	V_{HYS_GPIO}			20		mV
LOGIC OUTPUTS						
Output Voltage Range	V_{OUT}	For SDA bump	0		V_{DVDD}	V
Output Low Level	V_{OL}	I_{OL} = 1mA			0.4	V
Output High Level (RDYB, GPIO_)	V_{OH}	I_{OH} = 1mA	0.9 x V_{DVDD}			V

Electrical Characteristics (continued)

(V_{AVDD} = 3.6V, V_{AVSS} = 0V, V_{DVDD} = 2.0V to 3.6V, V_{REFP} - V_{REFN} = V_{AVDD}, DATA RATE = 1ksps, PGA low-noise mode, single-cycle conversion mode (SCYCLE = 1). T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at T_A = +25°C.)(Note 3)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Floating State Leakage Current	$IDIGO_{LEAK}$				±10	µA
Floating State Output Capacitance	C_{DIGO}			9		pF
POWER REQUIREMENTS						
Negative Analog Supply Voltage	V_{AVSS}		-1.8		0	V
Positive Analog Supply Voltage	V_{AVDD}		V_{AVSS} + 2.7		V_{AVSS} + 3.6	V
Negative I/O Supply Voltage	V_{DGND}		0			V
Positive I/O Supply Voltage	V_{DVDD}	CAPREG not driven by external supply	2.0		3.6	V
		DVDD and CAPREG bumps connected together on the circuit board	1.7		2.0	
CAPREG Supply Voltage	V_{CAPREG}	Internal LDO enabled	1.8			V
		When CAPREG bump is driven externally, ensure it is connected directly to DVDD bump	1.7		2.0	
Analog Supply Current	$I_{AVDD(CNV)}$	Direct		2.2	3	mA
		PGA low-power mode		3.5	5.0	
		PGA low-noise mode		4.2	6.2	
DVDD Operating Current	$I_{DVDD(CNV)}$	V_{DVDD} = 2.0V, LDO enabled		0.65	1.1	mA
		V_{DVDD} = V_{CAPREG} = 2.0V, LDO disabled		0.58		
AVDD Sleep Current	$I_{AVDD(SLP)}$	V_{AVDD} = 3.6V, V_{AVSS} = 0V, V_{DVDD} = 2.0V		1		µA
DVDD Sleep Current	$I_{DVDD(SLP)}$	V_{DVDD} = 2.0V		0.3	4.5	µA
AVDD Standby Current	$I_{AVDD(SBY)}$	V_{AVDD} = 3.6V, V_{AVSS} = 0V, V_{DVDD} = 2.0V		1.5		µA
DVDD Standby Current	$I_{DVDD(SBY)}$	V_{DVDD} = 2.0V, LDO enabled		50	175	µA
		V_{DVDD} = V_{CAPREG} = 2.0V, LDO disabled		2.5		
UVLO Threshold Low to High	V_{LH}	AVDD, DVDD supply undervoltage lockout	0.75	1.2	1.7	V
		CAPREG supply undervoltage lockout	0.6	1.0	1.4	
UVLO Threshold High to Low	V_{HL}	AVDD, DVDD supply undervoltage lockout	0.6	1.1	1.6	V
		CAPREG supply undervoltage lockout	0.4	0.95	1.3	
UVLO Hysteresis	V_{HYS}	AVDD, DVDD supply undervoltage lockout		4		%
		CAPREG supply undervoltage lockout		5		

Electrical Characteristics (continued)

(V_{AVDD} = 3.6V, V_{AVSS} = 0V, V_{DVDD} = 2.0V to 3.6V, V_{REFP} - V_{REFN} = V_{AVDD}, DATA RATE = 1ksps, PGA low-noise mode, single-cycle conversion mode (SCYCLE = 1). T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at T_A = +25°C.)(Note 3)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
UVLO Delay Low to High or High to Low	T_{DEL}	AVDD, DVDD supply undervoltage lockout		10		µs
		CAPREG supply undervoltage lockout		3.5		
UVLO Glitch Suppression	T_P	AVDD, DVDD supply undervoltage lockout		10		ns
		CAPREG supply undervoltage lockout		10		

I²C Timing Requirements

(V_{AVDD} = 3.6V, V_{AVSS} = 0V, V_{DVDD} = 1.7V to 3.6V, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. For output bumps, C_{LOAD} = 20pF.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Serial Clock Frequency	f_{SCL}	Note 6 applies to minimum value	0.1		1	MHz
Bus Free Time Between STOP and START Condition	t_{BUF}		0.5			µs
Hold Time (Repeated) START Condition (After This Period, First Clock Pulse Is Generated)	$t_{HD;STA}$		0.26			µs
SCL Pulse-Width Low	t_{LOW}		0.5			µs
SCL Pulse-Width High	t_{HIGH}		0.26			µs
Setup Time for Repeated START Condition	$t_{SU;STA}$		0.26			µs
Data Hold Time	$t_{HD;DAT}$		0			µs
Data Setup Time	$t_{SU;DAT}$		50			ns
SDA and SCL Receiving Rise Time	t_r	(Note 6)			120	ns
SDA and SCL Receiving Fall Time	t_f	(Note 6)	20 x V_{DVDD}/5.5		120	ns
SDA Transmitting Fall Time	t_f		20 x V_{DVDD}/5.5		120	ns
Setup Time for STOP Condition	$t_{SU;STO}$		0.26			µs
Bus Capacitance Allowed	C_b	(Note 6)			550	pF
Pulse Width of Suppressed Spike	t_{SP}			50		ns

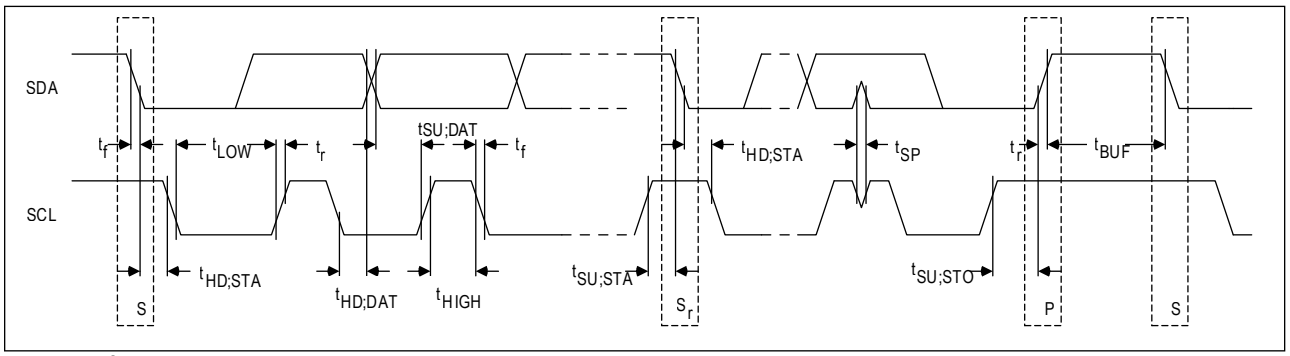


Figure 1. I2C Timing Diagram

Note 3: Limits are 100% tested at T_A = +25°C, unless otherwise noted. Limits over the operating temperature range and relevant supply voltage range are guaranteed by design and characterization.

Note 4: Full-scale error includes errors from gain and offset or zero-scale error.

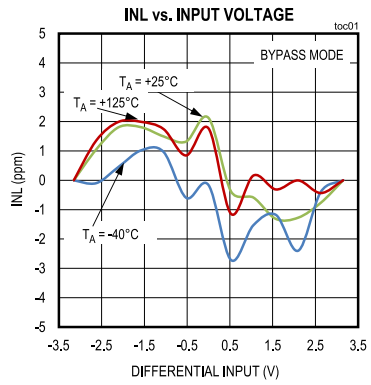
Note 5: ppmFSR is parts per million of full-scale range.

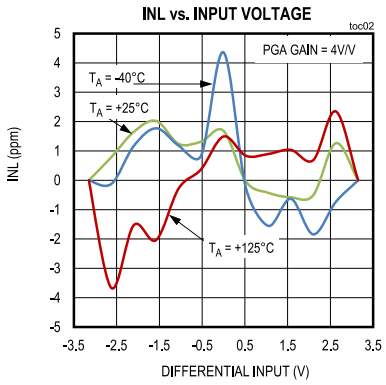
Note 6: These specifications are guaranteed by design, characterization, or I2C protocol.

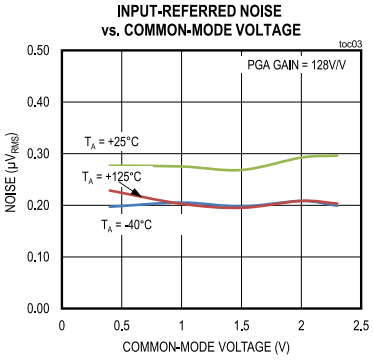
Note 7: Reference common mode $(V_{REFP} + V_{REFN})/2 \le (V_{AVDD} + V_{AVSS})/2 + 0.1V$.

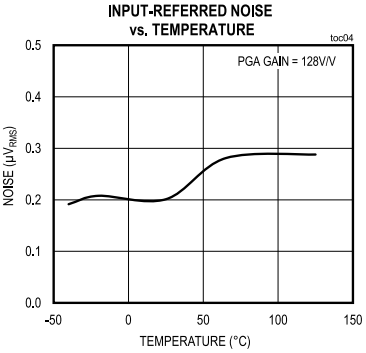
Typical Operating Characteristics

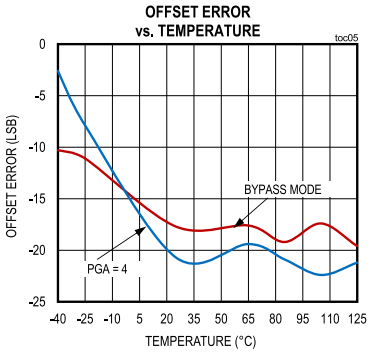
(V_{AVDD} = +3.6V, V_{AVSS} = 0V, V_{DVDD} = +2.0V, V_{REFP} - V_{REFN} = V_{AVDD}; T_A = T_{MIN} to T_{MAX}, LDO enabled, PGA enabled, unless otherwise noted. Data rate = 1ksps, single-cycle conversion mode (SCYCLE = 1) Typical values are at T_A = +25°C.)

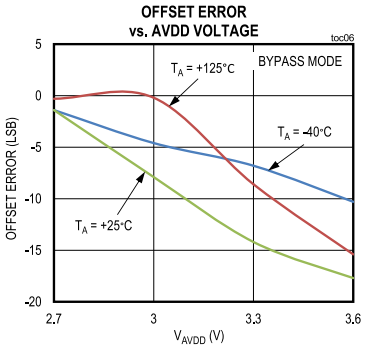


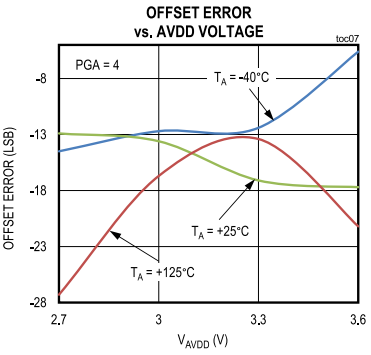


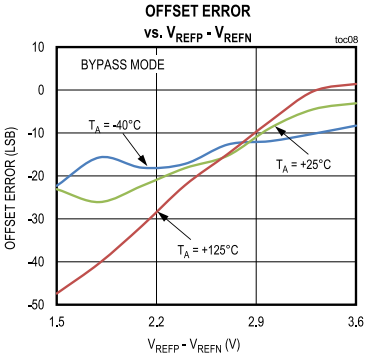


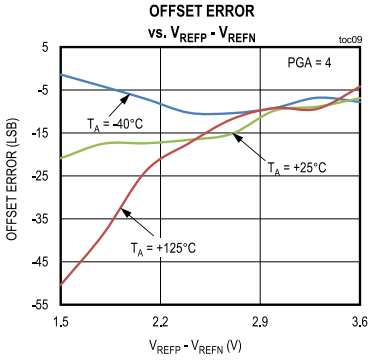






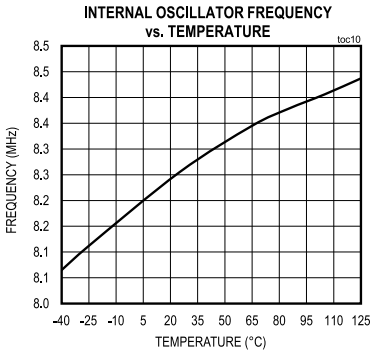


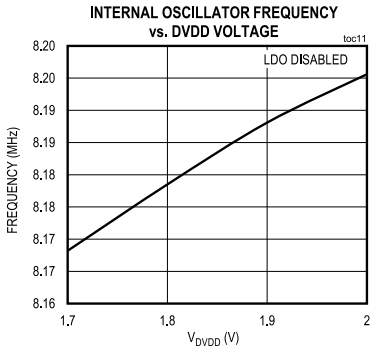


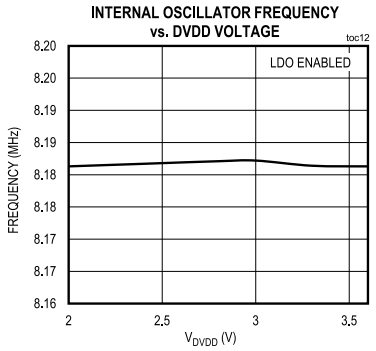


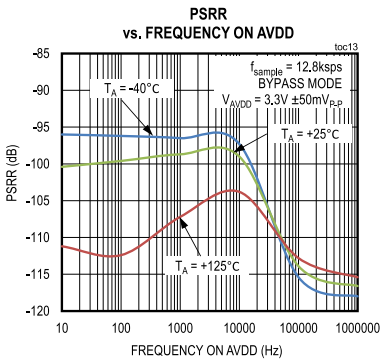
Typical Operating Characteristics (continued)

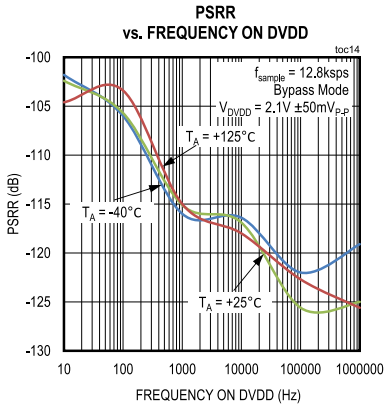
(V_{AVDD} = +3.6V, V_{AVSS} = 0V, V_{DVDD} = +2.0V, V_{REFP} - V_{REFN} = V_{AVDD}; T_A = T_{MIN} to T_{MAX}, LDO enabled, PGA enabled, unless otherwise noted. Data rate = 1ksps, single-cycle conversion mode (SCYCLE = 1) Typical values are at T_A = +25°C.)

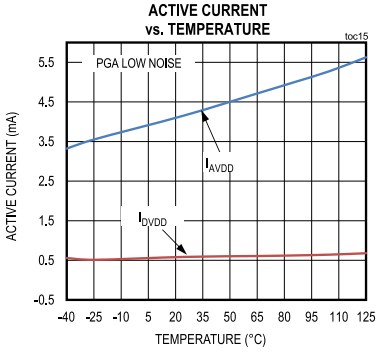


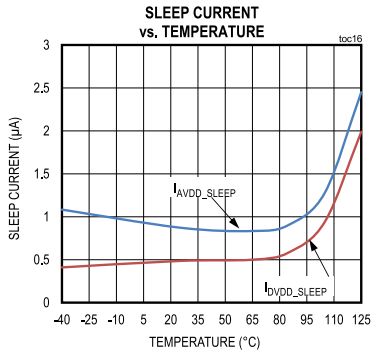


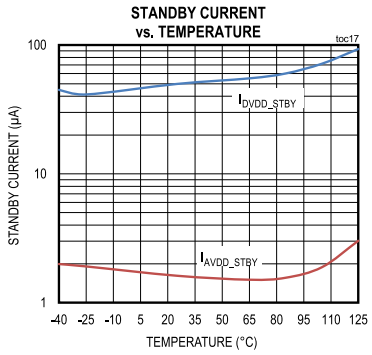


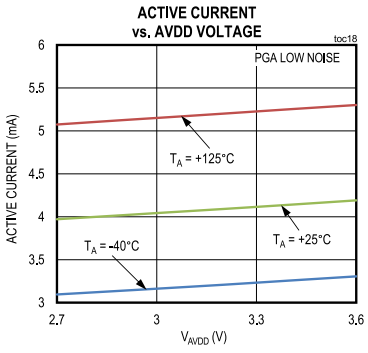






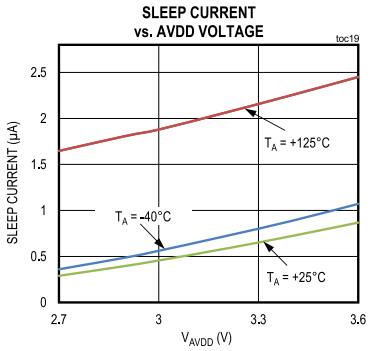


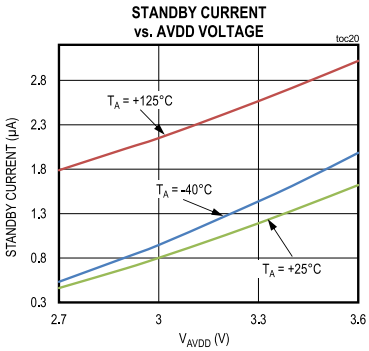


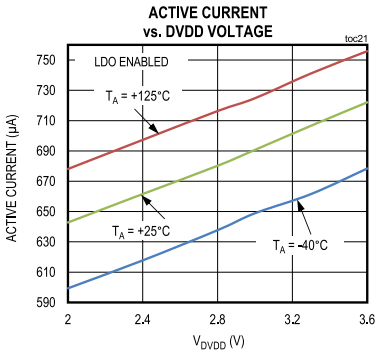


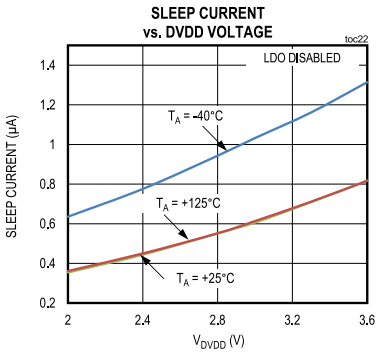
Typical Operating Characteristics (continued)

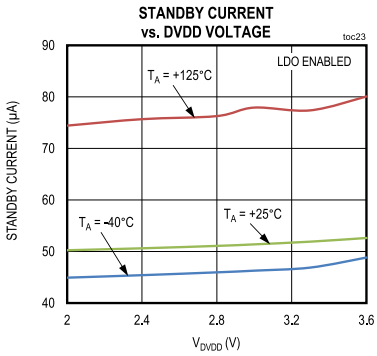
(V_{AVDD} = +3.6V, V_{AVSS} = 0V, V_{DVDD} = +2.0V, V_{REFP} - V_{REFN} = V_{AVDD}; T_A = T_{MIN} to T_{MAX}, LDO enabled, PGA enabled, unless otherwise noted. Data rate = 1ksps, single-cycle conversion mode (SCYCLE = 1) Typical values are at T_A = +25°C.)

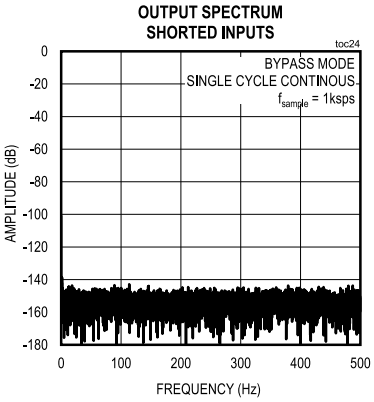


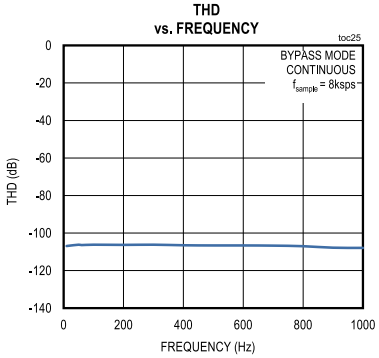


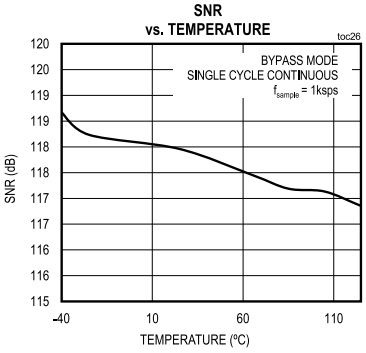




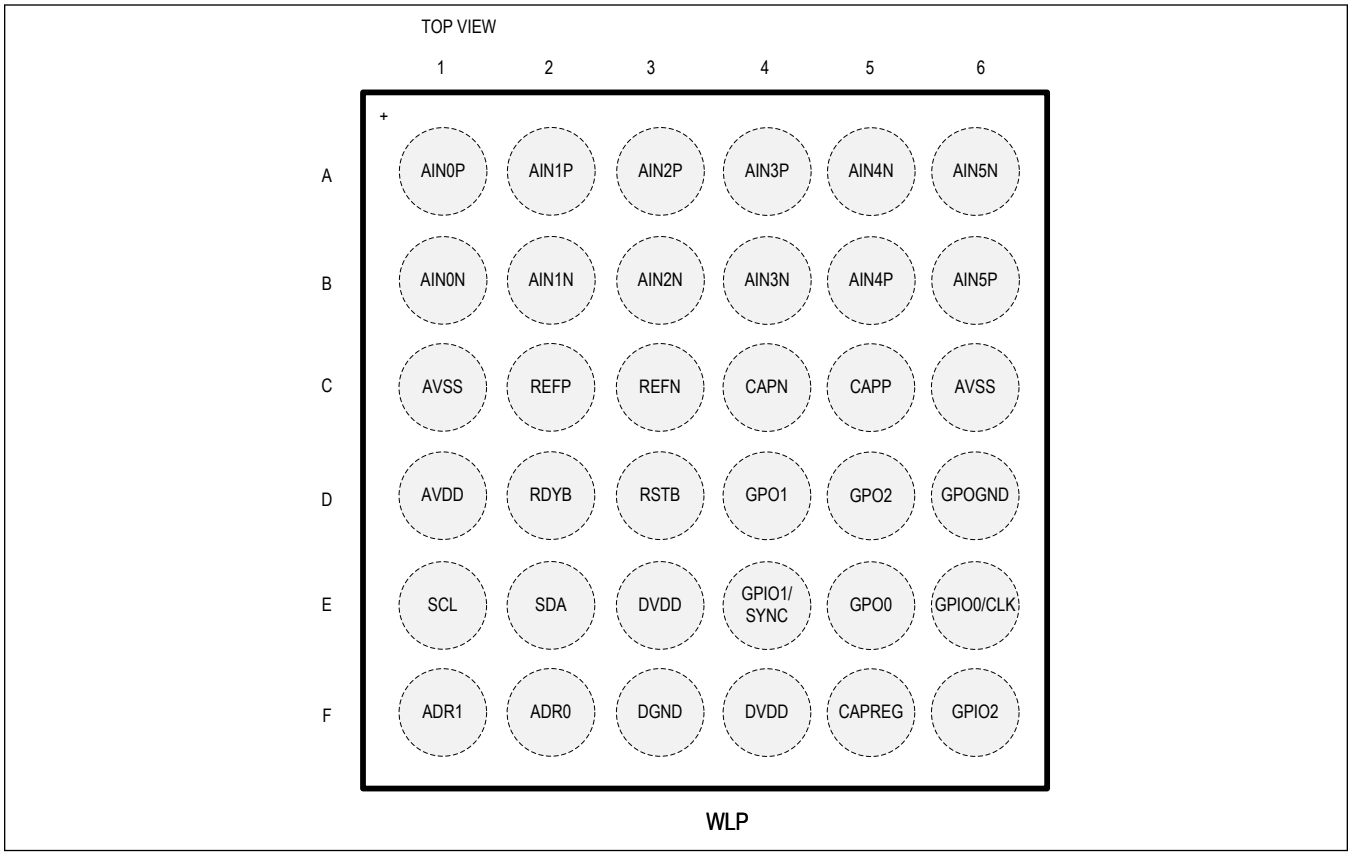








Bump Configuration



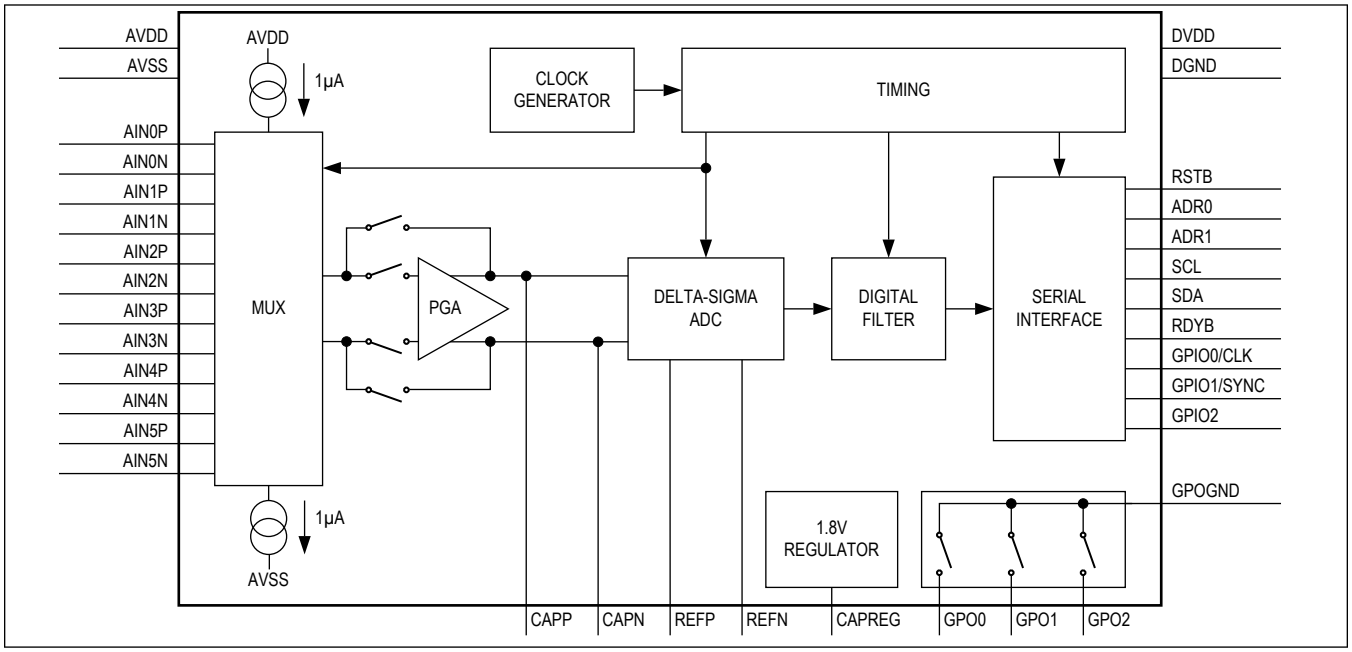
Bump Description

PIN	NAME	FUNCTION
A1	AIN0P	Positive Analog Input 0
A2	AIN1P	Positive Analog Input 1
A3	AIN2P	Positive Analog Input 2
A4	AIN3P	Positive Analog Input 3
A5	AIN4N	Negative Analog Input 4
A6	AIN5N	Negative Analog Input 5
B1	AIN0N	Negative Analog Input 0
B2	AIN1N	Negative Analog Input 1
B3	AIN2N	Negative Analog Input 2
B4	AIN3N	Negative Analog Input 3
B5	AIN4P	Positive Analog Input 4
B6	AIN5P	Positive Analog Input 5
C1	AVSS	Analog Ground
C2	REFP	Positive Reference Input
C3	REFN	Negative Reference Input
C4	CAPN	PGA Filter Input. Connect 1nF C0G capacitor between CAPP and CAPN.

Bump Description (continued)

PIN	NAME	FUNCTION
C5	CAPP	PGA Filter Input. Connect 1nF C0G capacitor between CAPP and CAPN.
C6	AVSS	Analog Ground
D1	AVDD	Positive Analog Supply
D2	RDYB	Active-Low Data Ready Output. RDYB goes low when a new conversion result is available in the data register. When a read operation of a full output word completes, RDYB returns high. RDYB is always driven.
D3	RSTB	Active-Low Power-On-Reset Input
D4	GPO1	Analog Switch Normally Open Terminal/General-Purpose Output 1. Register controlled, close position connects GPO1 to GPOGND. Current sink only.
D5	GPO2	Analog Switch Normally Open Terminal/General-Purpose Output 2. Register controlled, close position connects GPO2 to GPOGND. Current sink only.
D6	GPOGND	Analog Switch/General-Purpose Output, GND Terminal
E1	SCL	I2C Serial Clock Input
E2	SDA	I2C Serial Data
E3	DVDD	Digital Power Supply, 1.7V to 3.6V
E4	GPIO1/SYNC	Synchronization Input (default) or General-Purpose I/O. SYNC resets both the digital filter and the modulator. Connect SYNC from multiple MAX11259s in parallel to synchronize more than one ADC to an external trigger.
E5	GPO0	Analog Switch Normally Open Terminal/General-Purpose Output 0. Register controlled, close position connects GPO0 to GPOGND. Current sink only.
E6	GPIO0/CLK	General-Purpose I/O (Default) or External Clock Signal for the Device. When external clock mode is selected, provide a digital clock signal at this bump. The MAX11259 is specified with a clock frequency of 8.192MHz. Clock frequencies below 8.192MHz are supported. The data rate and digital filter notch frequencies scale with the clock frequency.
F1	ADR1	I2C Address Select Line 1
F2	ADR0	I2C Address Select Line 0
F3	DGND	Digital Ground
F4	DVDD	Digital Power Supply, 1.7V to 3.6V
F5	CAPREG	1.8V Subregulator Output. Connects to DVDD when driven externally by a 1.8V supply. Connect a 220nF or larger capacitor between CAPREG and DGND.
F6	GPIO2	General-Purpose I/O

Functional Diagram



Detailed Description

The MAX11259 is a 24-bit delta-sigma ADC that achieves exceptional performance consuming minimal power. Sample rates up to 16ksps support precision DC measurements. The built-in sequencer supports scanning of selected analog channels, programmable conversion delay, and math operations to automate sensor monitoring.

The fourth order delta-sigma modulator is unconditionally stable and measures six differential input voltages. The modulator is monitored for overrange conditions, which are reported in the status register. The digital filter is a variable decimation-rate SINC filter with overflow monitoring reported in the status register.

The programmable gain differential amplifier (PGA) is low noise and is programmable from 1 to 128. The PGA buffers the modulator and provides a high-impedance input to the analog channels.

System Clock

The MAX11259 incorporates a highly stable internal oscillator that provides the system clock. The system clock is trimmed to 8.192MHz, providing digital and analog timing. The MAX11259 also supports an external clock mode.

Voltage Reference Inputs

The MAX11259 provides differential inputs REFP and REFN for an external reference voltage. Connect the external reference directly across the REFP and REFN bumps to obtain the differential reference voltage. The V_{REFP} voltage should always be greater than the V_{REFN} voltage, and the common-mode voltage range is between 0.75V and V_{AVDD} - 0.75V.

Analog Inputs

The MAX11259 measures six pairs of differential analog inputs (AIN_P, AIN_N) in direct connection or buffered through the PGA. See the CTRL2: Control Register 2 (Read/Write) table for programming and enabling the PGA or direct connect mode. The default configuration is direct connect, with the PGA powered down.

Bypass/Direct Connect

The MAX11259 offers the option to bypass the PGA and route the analog inputs directly to the modulator. This option lowers the power of the device since the PGA is powered down.

Programmable Gain Amplifier (PGA)

The integrated PGA provides gain settings from 1x to 128x. (Figure 2). Direct connection is available to bypass the PGA and directly connect to the modulator. The PGA's absolute input voltage range is CMI_{RNG} and the PGA output voltage range is $VOUT_{RNG}$, as specified in the *Electrical Characteristics*.

Note that linearity and performance degrade when the specified input common-mode voltage of the PGA is exceeded. The input common-mode range and output common-mode range are shown in Figure 3. The following equations describe the relationship between the analog inputs and PGA output.

AINP = Positive input to the PGA

AINN = Negative input to the PGA

CAPP = Positive output of PGA

CAPN = Negative output of PGA

V_{CM} = Input common mode

GAIN = PGA gain

V_{REF} = ADC reference input voltage

$V_{IN} = V_{AINP} - V_{AINN}$

Note: Input voltage range is limited by the reference voltage as described by $V_{IN} \le \pm V_{REF}/GAIN$

$$V_{CM} = \frac{(V_{AINP} + V_{AINN})}{2}$$

$$V_{CAPP} = V_{CM} + GAIN \times (V_{AINP} - V_{CM})$$
$$V_{CAPN} = V_{CM} - GAIN \times (V_{CM} - V_{AINN})$$

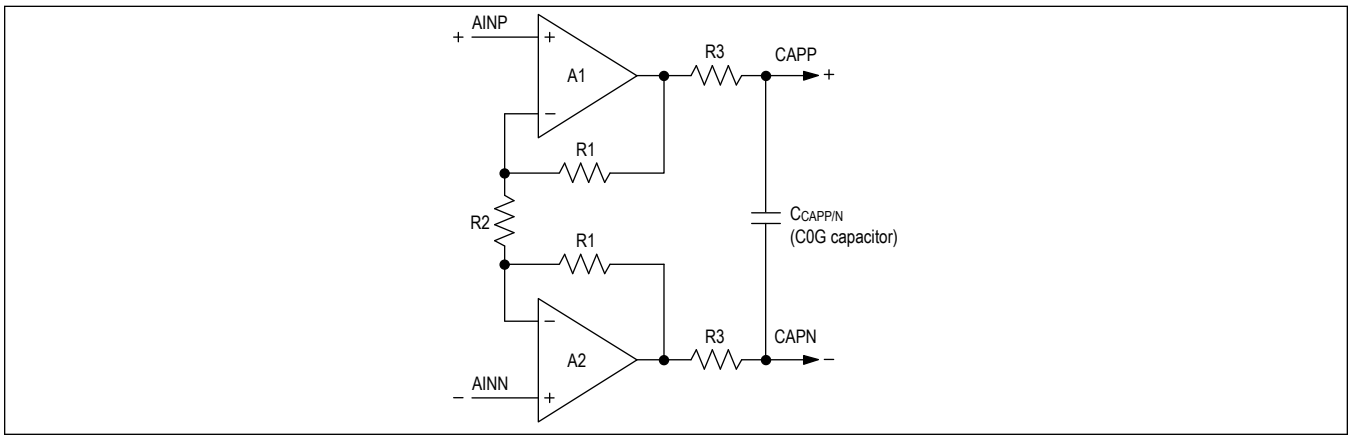


Figure 2. Simplified Equivalent Diagram of the PGA

PGA High Current

When V_{AVDD} voltage is above 2.9V and PGA is enabled, high I_{AVDD} current could be observed on the MAX11259 if PGA outputs are driven out of normal operating range and then rapidly driven back within the range during continuous conversion. The current can be as high as 30mA, depending on the AVDD supply voltage and PGA output voltage.

To trigger the PGA high-current state, drive the PGA output from normal low-side compliance range (> V_{AVSS} + 0.3V) to less than (V_{AVSS} + 40mV), and then drive back into compliance range (> V_{AVSS} + 0.3V) with a slew rate greater than 0.7V/µs while the device is performing continuous conversion.

The high-current state can also be triggered when interrupting a self-calibration in progress by starting a new conversion command when PGA is enabled, which internally creates the trigger condition.

PGA high-current state cannot be triggered with V_{AVDD} supply voltage below 2.9V.

When PGA high-current state is triggered, I_{AVDD} current could be 4.5 times as high as the normal I_{AVDD} current.

Exit Condition

PGA high-current state can always be exited by changing the MAX11259 to STANDBY or SLEEP state.

It will be automatically recovered when the MAX11259 is configured in mode 1 single-cycle conversion mode, mode 2, mode 3, or mode 4 if AutoScan Delay > 0. In these modes, the device automatically goes to STANDBY or SLEEP mode after the conversion.

When PGA high current state is triggered in mode 1 continuous conversion mode or mode 4 AutoScan Delay = 0, it can be recovered by issuing firmware command to cycle STANDBY or SLEEP state. To force the MAX11259 into STANDBY or SLEEP state, either issue a power-down command or write to one of the CTRL registers.

Input Voltage Range

The ADC input range is programmable for bipolar (-V_{REF} to +V_{REF}) or unipolar (0 to V_{REF}) ranges. The U/B bit in the CTRL1 register configures the MAX11259 for unipolar or bipolar transfer functions.

Data Rates

Table 1 lists the available data rates for the MAX11259, RATE[3:0] setting of the conversion command (see the *Modes and Registers* section). The single-cycle mode has an overhead of 48 digital master clocks that is approximately 5.86µs for a typical digital master clock frequency of 8.192MHz. The single-cycle effective column contains the data rate values including the 48 clock startup delays. The 48 clocks are required to stabilize the modulator at startup. In continuous conversion mode, the output data rate is five times the single-cycle rate up to a maximum of 16ksps. During continuous

conversions, the output sample data requires five 24-bit cycles to settle to a valid conversion from an input step, PGA gain changes, or a change of input channel through the multiplexer.

If self-calibration is used, 48 additional master clocks are required to process the data per conversion. Likewise, system calibration takes an additional 48 master clocks to complete.

If both self and system calibration are used, it takes an additional 80 master clocks to complete. If self and/or system calibration are used, the effective data rate will be reduced by these additional clock cycles per conversion.

Noise Performance

The MAX11259 provides exceptional noise performance. SNR is dependent on data rate, PGA gain, and power mode. Bandwidth is reduced at low data rates; both noise and SNR are improved proportionally. Table 2 and Table 3 summarize the noise performance for both single-cycle and continuous operation versus data rate, PGA gain, and power mode.

Table 1. Available Programmable Data Rates

	DATA RATE (sps)				
RATE[3:0]	CONTINUOUS	SINGLE CYCLE	CONVERSION ONLY	CONVERSION PLUS SELF- CALIBRATION*	CONVERSION PLUS SELF-CALIBRATION PLUS SYSTEM CALIBRATION*
0000	1.9	50	50.01	49.99	49.98
0001	3.9	62.5	62.51	62.48	62.47
0010	7.8	100	99.98	99.92	99.88
0011	15.6	125	124.95	124.86	124.80
0100	31.2	200	199.80	199.57	199.41
0101	62.5	250	249.66	249.29	249.05
0110	125	400	398.98	398.05	397.44
0111	250	500	498.34	496.89	495.93
1000	500	800	796.11	792.41	789.97
1001	1000	1000	991.86	986.13	982.35
1010	2000	1600	1578.72	1564.26	1554.77
1011	4000	2000	1974.16	1951.60	1936.84
1100	8000	3200	3114.26	3058.48	3022.39
1101	16000**	4000	3895.78	3808.89	3753.08
1110	Not available	6400	6135.27	5922.49	5788.64
1111	Not available	12800	11776.90	11017.10	10562.79

**The effective data rate is lower when the calibration is enabled due to additional MAC (multiply/accumulate) operations required after the conversion is complete to perform the calibration adjustment.*

***Only supported in Fast Mode Plus.*

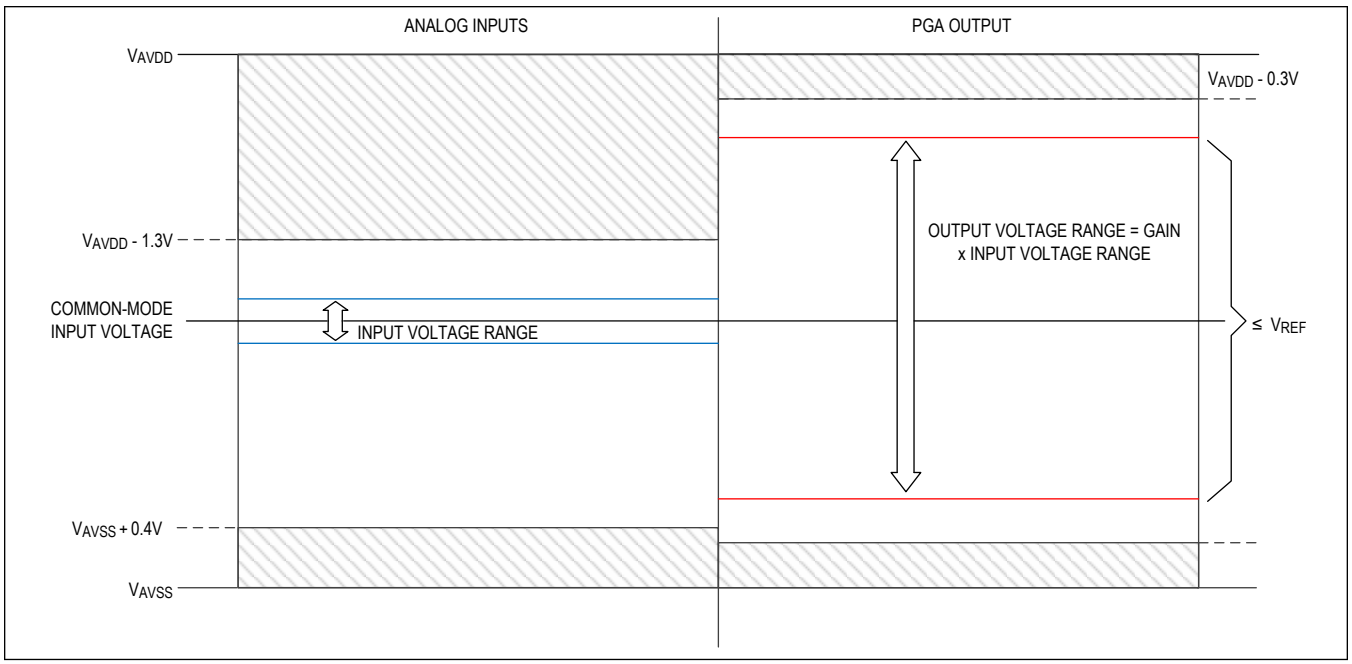


Figure 3. Analog Input Voltage Range Compared to PGA Output Range

Table 2. Noise vs. PGA Mode and Gain (Single-Cycle Conversion)

DATA RATE (sps)	SINGLE-CYCLE CONVERSION MODE INPUT-REFERRED NOISE VOLTAGE (μV_{RMS}) VS. PGA GAIN SETTING															
	1		2		4		8		16		32		64		128	
	LP	LN	LP	LN	LP	LN	LP	LN	LP	LN	LP	LN	LP	LN	LP	LN
50	0.81	0.58	0.38	0.27	0.18	0.13	0.10	0.07	0.09	0.07	0.08	0.06	0.08	0.06	0.08	0.06
62.5	0.88	0.63	0.48	0.34	0.21	0.15	0.12	0.09	0.09	0.07	0.08	0.06	0.08	0.05	0.08	0.05
100	1.18	0.84	0.61	0.44	0.30	0.21	0.17	0.12	0.12	0.08	0.09	0.07	0.09	0.07	0.10	0.07
125	1.24	0.89	0.59	0.42	0.31	0.22	0.18	0.13	0.12	0.08	0.10	0.07	0.10	0.07	0.10	0.07
200	1.38	0.99	0.68	0.49	0.35	0.25	0.21	0.15	0.15	0.10	0.12	0.08	0.11	0.08	0.11	0.08
250	1.38	0.99	0.72	0.52	0.39	0.28	0.23	0.16	0.16	0.11	0.13	0.09	0.12	0.09	0.12	0.09
400	1.63	1.16	0.85	0.61	0.45	0.32	0.27	0.19	0.19	0.14	0.16	0.12	0.15	0.11	0.16	0.11
500	1.79	1.28	0.93	0.66	0.48	0.34	0.29	0.21	0.21	0.15	0.18	0.13	0.17	0.12	0.18	0.13
800	2.12	1.51	1.10	0.79	0.61	0.43	0.36	0.26	0.27	0.20	0.24	0.17	0.23	0.16	0.23	0.16
1,000	2.38	1.70	1.25	0.89	0.69	0.49	0.41	0.29	0.31	0.22	0.27	0.19	0.26	0.18	0.26	0.19
1,600	3.21	2.29	1.67	1.19	0.89	0.64	0.56	0.40	0.41	0.29	0.36	0.26	0.35	0.25	0.35	0.25
2,000	3.76	2.69	1.95	1.39	1.04	0.74	0.65	0.47	0.48	0.34	0.43	0.30	0.41	0.29	0.42	0.30
3,200	4.41	3.15	2.28	1.63	1.25	0.89	0.78	0.55	0.58	0.41	0.51	0.36	0.49	0.35	0.49	0.35
4,000	5.18	3.70	2.68	1.91	1.48	1.06	0.91	0.65	0.69	0.49	0.60	0.43	0.58	0.41	0.59	0.42
6,400	7.34	5.24	3.83	2.73	2.08	1.48	1.29	0.92	0.98	0.70	0.86	0.61	0.81	0.58	0.83	0.59
12,800	10.84	7.74	5.59	3.99	3.01	2.15	1.85	1.32	1.37	0.98	1.23	0.88	1.17	0.83	1.16	0.83

LP = Low Power, LN = Low Noise

Table 3. Noise vs. PGA Mode and Gain (Continuous Conversion)

DATA RATE (sps)	CONTINUOUS CONVERSION MODE INPUT-REFERRED NOISE VOLTAGE (μV_{RMS}) VS. PGA GAIN SETTING															
	1		2		4		8		16		32		64		128	
	LP	LN	LP	LN	LP	LN	LP	LN	LP	LN	LP	LN	LP	LN	LP	LN
15.6	0.45	0.32	0.20	0.14	0.11	0.08	0.06	0.04	0.04	0.03	0.03	0.02	0.03	0.02	0.03	0.02
31.2	0.58	0.41	0.26	0.18	0.13	0.10	0.08	0.06	0.05	0.04	0.04	0.03	0.04	0.03	0.04	0.03
62.5	0.68	0.48	0.34	0.25	0.18	0.13	0.10	0.07	0.07	0.05	0.06	0.04	0.06	0.04	0.06	0.04
125	0.86	0.61	0.44	0.32	0.23	0.16	0.14	0.10	0.10	0.07	0.08	0.06	0.08	0.06	0.08	0.06
250	1.14	0.82	0.56	0.40	0.30	0.22	0.18	0.13	0.14	0.10	0.11	0.08	0.11	0.08	0.11	0.08
500	1.47	1.05	0.76	0.54	0.41	0.29	0.25	0.18	0.19	0.13	0.16	0.11	0.16	0.11	0.16	0.11
1000	1.99	1.42	1.03	0.73	0.56	0.40	0.35	0.25	0.26	0.19	0.23	0.16	0.21	0.15	0.22	0.16
2000	2.73	1.95	1.40	1.00	0.76	0.54	0.47	0.34	0.36	0.26	0.31	0.22	0.30	0.21	0.30	0.21
4000	3.68	2.63	1.86	1.33	1.03	0.73	0.64	0.45	0.49	0.35	0.42	0.30	0.40	0.28	0.41	0.29
8000	4.57	3.26	2.36	1.69	1.30	0.93	0.81	0.58	0.61	0.43	0.53	0.38	0.52	0.37	0.52	0.37
16000	5.22	3.73	2.66	1.90	1.48	1.06	0.93	0.67	0.68	0.49	0.61	0.44	0.58	0.41	0.60	0.43

LP = Low Power, LN = Low Noise

I2C Protocol

The I2C-compatible serial interface consists of the standard I2C bumps: SCL and SDA. The SCL and the SDA bumps are bidirectional lines, connected to a positive supply voltage via a current source or a pullup resistor. The data is clocked into the MAX11259 from the SDA bump on the rising edge of SCL. Data is clocked out of the MAX11259 on the SDA bump on the falling edge of SCL. The SCL/SDA have an open-drain pad for wired-AND connection on the bus. Data on the bus can be transferred at rates of up to 1Mbit/s since the MAX11259 supports the Fast Mode Plus protocol. Each device on the I2C bus is recognized by a unique device address and can operate as a transmitter and a receiver. The interface is backward-compatible with standard mode and fast mode.

Due to the variety of different devices (bipolar, CMOS, NMOS) that can be connected to the I2C bus, the input reference levels are set as 30% and 70% of V_{DD}. The data on the SDA line must be stable during high period of SCL. The HIGH or LOW state of the data line can only change when the clock line is LOW for a normal byte transfer except for START and STOP conditions.

All transactions begin with a START(S) and are terminated by a STOP(P). A HIGH to LOW transaction on the SDA line while SCL is HIGH defines a START condition. A LOW to HIGH transition on the SDA line while SCL is HIGH defines a STOP condition. The START and STOP are always generated by the I2C Master. The MAX11259 has a circuit to detect the START and STOP conditions. Every byte on the SDA line must be 8 bits long. The number of bytes that can be transmitted is unrestricted. Each byte must be followed by an acknowledge (ACK). Data is transferred with MSB first. The MAX11259 always sends out an ACK in response to master's request for reading or writing data which means the interface is always ready and it does not hold the master in wait state. If the MAX11259 receives a not acknowledge (NACK) from the master it will reset the I2C interface and wait for another START condition.

SCL (Serial Clock)

The SCL bump synchronizes data communication between the host device and the MAX11259. Data is latched into the MAX11259 on the rising edge of SCL and data is shifted out of the MAX11259 after the falling edge of SCL.

RDYB (Data Ready)

RDYB indicates the ADC conversion status and the availability of the conversion result. When RDYB is low, a conversion result is available. When RDYB is high, a conversion is in progress and the data for the current conversion is not available. RDYB is driven high after a complete read of the data register. RDYB resets to high four master clock cycles prior to the next DATA register update.

If data was read, then RDYB transitions from high to low at the output data rate. If the previous data was not read, then the RDYB transitions from low to high for four master clock cycles and then transitions from high to low. In continuous mode, RDYB remains high for the first four conversion results and on the 5th result, RDYB goes low.

For sequencer mode 2 and sequencer mode 3, the RDYB behavior for a multichannel conversion can be controlled by the SEQ:RDYBEN bit. The default value of SEQ:RDYBEN is ‘0’. When set to ‘0’, RDYB behaves the same for multichannel conversion and single channel operation. The RDYB toggles high to low after each channel is ready to update its corresponding data register. After the channel data is read, the RDYB will reset back to ‘1’. If the channel data is not read and the next channel is ready to update its data, the RDYB will toggle low to high four cycles before the data update (similar to a single channel operation), and then toggle high to low indicating the new channel’s conversion data is available. If ‘N’ channels are enabled, RDYB will toggle high to low ‘N’ times. If SEQ:RDYBEN is set to ‘1’, the RDYB event for each channel is suppressed. The RDYB toggles high to low when the last channel is ready to update its corresponding data register and a single high to low transition happens.

The STAT:SRDY[5:0] bits get set to ‘1’ when their corresponding channel finishes converting, irrespective of the RDYBEN setting for sequencer modes 2 and 3. The conversion status is available by reading the STAT:MSTAT bit. This stays high as long as the modulator is converting.

See Figure 4 for timing of RDYB.

SDA (Serial Data Input/Output)

The SDA line is considered an input when the master is transmitting the data to the MAX11259. The SDA line will be used as an output when the MAX11259 has data to be sent onto the I2C bus during a register read by the host master.

The slave in the MAX11259 implements mandatory requirements as specified in I2C standard, which are detections of START and STOP conditions and support for ACK/NACK. This slave supports 7-bit addressing and does not support the general call address.

I2C Sequence:

The master needs to send out the first byte with a valid device address. The last bit of the first byte is a R/$\overline{W}$ bit and the master needs to send a '0' in this bit. The device will ignore a '1' sent in this bit. This is followed by a COMMAND BYTE for the MAX11259 as described in the command structure. The MAX11259 then responds to the command request depending on the MODE bit in the command.

Writing a Command to the MAX11259 for Conversion/ Calibration/Power-Down

1. I2C START
2. I2C WRITE
   a. Send Device Address with a '0' in bit 8 indicating the master will send a command byte followed by the device address. (8’b0110000_0)
   b. Check Acknowledge
   c. Send Command byte to convert/power down/calibrate (8’b10_01_xxxx)
   d. Check acknowledge
3. I2C STOP

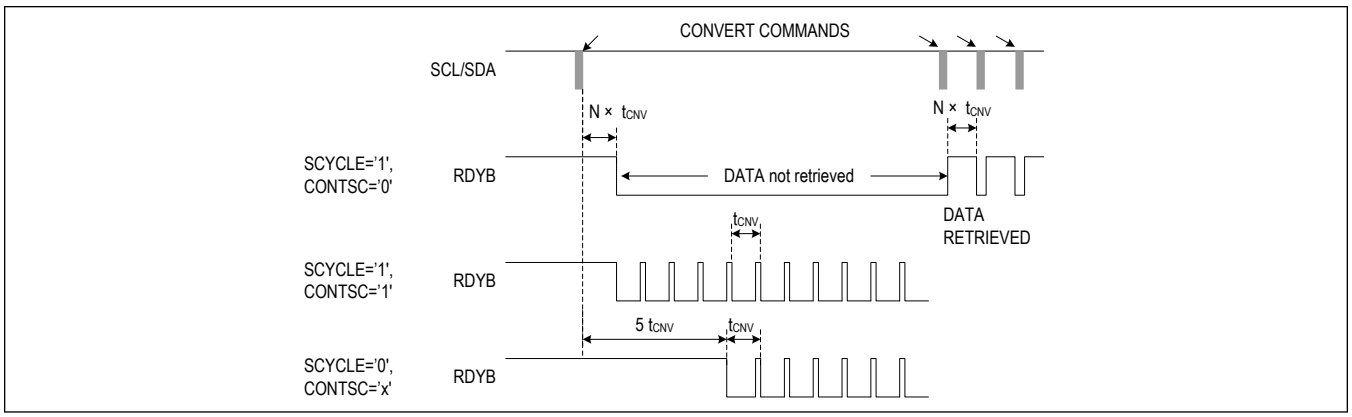


Figure 4. Timing of RDYB in All Conversion Configurations: Single-Cycle, Single-Cycle Continuous and Continuous. In sequencer mode 1 and in sequencer modes 2 and 3, with SEQ:RDYBEN='0' N = 1. In sequencer modes 2 and 3 with SEQ:RDYBEN='1' N = number of active channels.

Sequence to Execute I2C Write Operation

1. I2C START
2. I2C WRITE
   a. Send Device Address with a '0' in bit 8 indicating the master will send a command byte followed by the device address. (8'b0110000_0)
   b. Check Acknowledge
   c. Send Command byte to Write registers (8'b11_reg_addr[4:0]_0)
   d. Check acknowledge
   e. Send 8-bit register data MSB first
   f. Check Acknowledge
   g. …
   h. Check Acknowledge
3. I2C STOP

Sequence to Execute I2C Read Operation

1. I2C START
2. I2C WRITE
   a. Send Device Address with a '0' in bit 8 indicating the master will send a command byte followed by the device address. (8'b0110000_0)
   b. Check Acknowledge
   c. Send Command byte to Read registers (8'b11_reg_addr[4:0]_1)
   d. Check Acknowledge
3. I2C Repeat START
4. I2C WRITE
   a. Send Device Address with a '1' in bit 8 indicating the master will read the register data out.
   b. Check Acknowledge
5. I2C READ
   a. Receive 8 bits of Data
   b. Send Acknowledge
   c. …
   d. Receive 8 bits of Data
   e. Send Not Acknowledge
6. I2C STOP

I2C Timing Characteristics

The I2C timing diagram is shown in Figure 1. The bus timing requirements are specified in I2C Timing Requirements table. The data is sampled on the positive edge of SCL and launched on negative edge of SCL for ACK and DATA reads. This gives a sufficient hold time for the master to sample the data.

I2C Device Addressing Scheme

The I2C slave has a 7-bit long device address. The device address is followed by a R/$\overline{W}$ bit which is low for a write command and high for a read command.

The first three most significant bits of the device address are always 011. Slave address bits A[4:1] correspond by the matrix in Table 4 to the states of the device address bumps AD0 and AD1.

The AD0 and AD1 bumps can be connected to any of the three signals: DGND, DVDD, and SDA giving 3 possible addresses for each bump allowing up to 9 devices connected to the bus (see Figure 5).

Modes and Registers

The MAX11259 interface operates in two fundamental modes, either to issue a conversion command or to access registers. The mode of operation is selected by a command byte. Every I2C transaction to the MAX11259 starts with a command byte. The command byte begins with the MSB (B7) set to '1'. The next bit (B6) determines whether a conversion command is sent or register read/write access is requested.

Command Byte

The conversion command sets the mode of operation (conversion, calibration, or power-down) as well as the conversion speed of the MAX11259. The register read/write command specifies the register address as well as the direction of the access (read or write).

Channel Sequencing

Changing SEQUENCER Modes

Mode Exit (See Table 9. Register Map for Register Definitions)

To exit any of the three sequencer modes at any time program the following sequence:

1. Issue a power-down command to exit the conversion process to STANDBY or SLEEP, as defined in CTRL1:PD[1:0]:
   a. Write a conversion command byte (see Table 5. Command Byte Definition) and set MODE[1:0] of the command byte to '01'
2. Wait for STAT:PDSTAT[1:0] = '01' (SLEEP) or STAT:PDSTAT[1:0] = '10' (STANDBY).

Note: For all sequencer modes, the default exit state upon completion of all conversions is SLEEP. In sequencer mode 1, however, continuous conversion operation (CTRL1:SCYCLE='0') and continuous single-cycle conversion operation (CTRL1:SCYCLE='1' and CTRL1:CONTSC='1') are running continuously and must be terminated with the Mode Exit sequence.

Table 4. I2C Device Address Mapping

ADDRESS PINS		DEVICE ADDRESS							
AD1	AD0	A7	A6	A5	A4	A3	A2	A1	A0
DGND	DGND	0	1	1	0	0	0	0	~W/R
DGND	DVDD				0	0	0	1	~W/R
DGND	SDA				0	0	1	1	~W/R
DVDD	DGND				0	1	0	0	~W/R
DVDD	DVDD				0	1	0	1	~W/R
DVDD	SDA				0	1	1	1	~W/R
SDA	DGND				1	1	0	0	~W/R
SDA	DVDD				1	1	0	1	~W/R

Table 4. I²C Device Address Mapping (continued)

ADDRESS PINS		DEVICE ADDRESS							
SDA	SDA				1	1	1	1	~W/R

Note: *Up to 9 devices can be selected on the I²C bus using the above addressing scheme.*

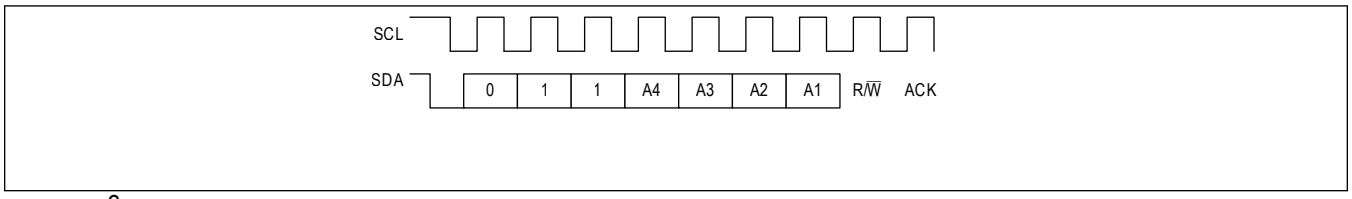


Figure 5. I²C Address Selection Byte Timing

Mode Change

To change sequencer modes or to update the SEQ register, program the following sequence:

1. Perform Sequencer Mode Exit (see the *Mode Exit* section).
2. Set up the following registers: SEQ, CTRL1.
   a. Set SEQ:MODE[1:0] to select the new sequencer mode
   b. Set CTRL1:PD[1:0] to STANDBY or SLEEP state to set the desired exit state if a conversion command with MODE[1:0] set to '01' is issued during the conversion.
3. Write the command byte (see Table 5).
   a. Set MODE[1:0] of the command byte to '11' (sequencer mode)
4. Wait for STAT:PDSTAT[1:0] = '00' to confirm conversion mode.

SEQUENCER MODE 1—Single-Channel Conversion with GPO Control and MUX Delays

This mode is used for single-channel conversions where the sequencer is disabled. Figure 6 illustrates the timing. To support high-impedance source networks, the convers on delay (SEQ:MDREN) feature must be enabled. The states of the GPO and GPIO bumps are configured using the GPO_DIR and GPIO_CTRL registers and can be modified anytime during mode 1 operation. The values of the CHMAP0/CHMAP1 registers and DELAY:GPO[7:0] bits are ignored in this mode.

Programming Sequence

Mode Entry

1. Set up the following registers: SEQ, DELAY, CTRL1, GPO_DIR, GPIO_CTRL.
   a. SEQ:MODE[1:0] = '00' for sequencer mode 1
   b. SEQ:MUX[2:0] to select the channel for conversion
   c. Enable SEQ:MDREN to delay conversion start to allow for input settling. Set DELAY:MUX[7:0] to the desired conversion delay
   d. Set CTRL1:SCYCLE for either single cycle (no latency) or continuous conversion
   e. If single-cycle conversion is selected, set CTRL1:CONTSC to '1' if continuous single-cycle conversion is desired
   f. Set CTRL1:PD[1:0] to STANDBY or SLEEP state to set the desired exit state if a conversion command with MODE[1:0] set to '01' is issued during the conversion
   g. Set register GPO_DIR and, if desired, GPIO_CTRL to enable or disable the desired GPO and GPIO bumps
2. Write a conversion command (see Table 5, Command Byte Definition).
   a. Set data rate using bits RATE[3:0] of the command byte
   b. Set MODE[1:0] of the command byte to '11' for sequencer mode
3. Monitor RDYB for availability of conversion results in the DATA register (See Figure 4 for RDYB timing).

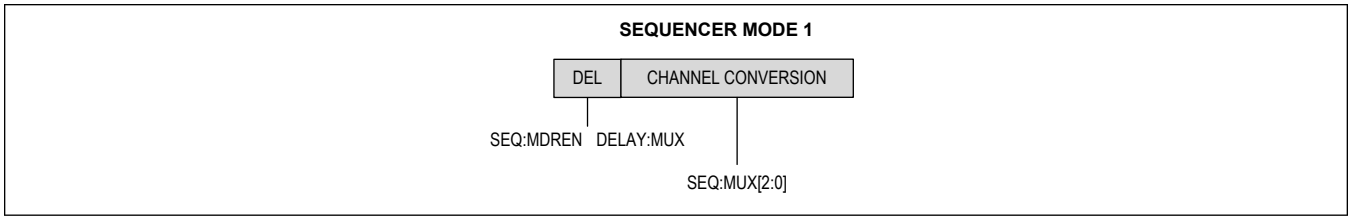


Figure 6. Sequencer Mode 1 Timing Diagram

Table 5. Command Byte Definition

	B7 (MSB)	B6	B5	B4	B3	B2	B1	B0
Conversion Command	1	0	MODE1	MODE0	RATE3	RATE2	RATE1	RATE0
Register Read/Write	1	1	RS4	RS3	RS2	RS1	RS0	R/$\overline{W}$

Table 6. Command Byte Decoding

BIT NAME	DESCRIPTION		
MODE[1:0]	The MODE bits are used to set the functional operation of the MAX11259 according to the following decoding.		
	MODE1	**MODE0**	**DESCRIPTION**
	0	0	Unused
	0	1	Power-down performed based on the CTRL1:PD[1:0] setting
	1	0	Calibration performed based on the CTRL1:CAL[1:0] setting
	1	1	Sequencer mode. The operation is based on the configuration of the SEQ register
RATE[3:0]	These bits determine the conversion speed of the MAX11259. The decoding is shown in Table 1.		
RS[4:0]	Register address as shown in Table 9.		
R/$\overline{W}$	The R/$\overline{W}$ bit enables either a read or a write access to the address specified in RS[4:0]. If R/$\overline{W}$ is set to '0', then data is written to the register. If the R/$\overline{W}$ bit is set to '1', then data is read from the register.		

Mode Exit

1. In single-cycle conversion mode (CTRL1:SCYCLE ='1') the sequencer exits into SLEEP state.
2. In continuous conversion mode (CTRL1: SCYCLE='0' or (CTRL:SCYCLE='1' and CTRL1:CONTSC ='1')), conversions continue nonstop until the mode is exited. To interrupt and exit continuous conversion or continuous single-cycle conversion follow the Changing SEQUENCER Modes—*Mode Exit* section to put the part into STANDBY or SLEEP state based on CTRL1:PD[1:0] set in step 1(f) of *Mode Entry* section.

Changing Input Channel During Continuous Single-Cycle Conversion in Mode 1

1. Issue a conversion command with MODE[1:0] set to '01' to exit the conversion process to STANDBY or SLEEP state (see the Changing SEQUENCER Modes—*Mode Exit* section).
2. Monitor STAT:PDSTAT = '10' or '01' to confirm exit to STANDBY or SLEEP state.
3. Set SEQ:MUX[2:0] to select the new channel for conversion
4. Write a conversion command (see Table 5) and set MODE[1:0] of command byte to '11'

SEQUENCER MODE 2 – Multichannel Scan with GPO Control and MUX Delays

This mode is used to sequentially convert a programmed set of channels in a preset order. Figure 7 illustrates the timing. The states of the GPO and GPIO bumps are configured using the GPO_DIR and GPIO_CTRL registers and can be modified anytime during mode 2 operation. In mode 2 register bits CHMAP0:CHn_ORD[2:0], CHMAP1:CHn_ ORD[2:0], CHMAP0:CHn_EN, and CHMAP1:CHn_EN are used to select channels and conversion order. Bits DELAY:GPO[7:0], CHMAP0:CHn_GPO[2:0], CHMAP0:CHn_GPOEN, CHMAP1:CHn_GPO[2:0], and CHMAP1:CHn_GPOEN are ignored in this mode. The bit CTRL1:CONTSC is ignored and bit CTRL1:SCYCLE = '0' is invalid in this mode.

Programming Sequence

Mode Entry

1. Set up the following registers: SEQ, CHMAP0, CHMAP1, DELAY, GPO_DIR, GPIO_CTRL, CTRL1
   a. SEQ:MODE[1:0] = '01' for sequencer mode 2
   b. If desired set SEQ:RDYBEN to '1' to signal data ready only when all channel conversions are completed
   c. Enable SEQ:MDREN to delay conversion start to allow for input settling. Set DELAY:MUX[7:0] to the desired conversion delay
   d. Set CHMAP0 and CHMAP1 to select the channels and channel order for conversion
   e. Set CTRL1:PD[1:0] to STANDBY or SLEEP state to set the desired exit state if a conversion command with MODE[1:0] set to '01' is issued during the conversion
   f. Set register GPO_DIR and GPIO_CTRL to enable or disable the desired GPO and GPIO bumps
   g. Set CTRL1:SCYCLE = '1' for single-cycle conversion mode
2. Write a conversion command (see Table 5).
   a. Set data rate using bits RATE[3:0] of the command byte
   b. Set MODE[1:0] of the command byte to '11'
3. Monitor RDYB (if SEQ:RDYBEN='0') and bits STAT:SRDY[5:0] for availability of per channel conversion results in DATA[x] registers.

Mode Exit

1. This mode exits to SLEEP state upon completion of sequencing all channels
2. To interrupt current sequencing perform mode exit, see the Changing SEQUENCER Modes—*Mode Exit* section. This device is put in STANDBY or SLEEP state based on CTRL1:PD[1:0] set in step 1(e) of *Mode Entry* section.

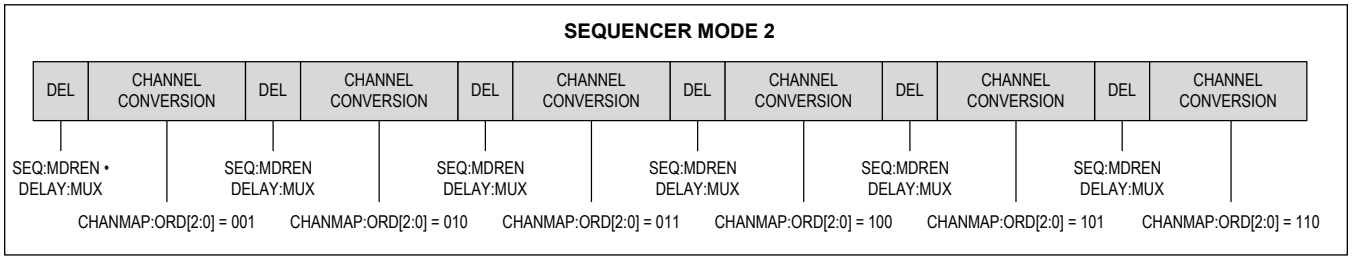


Figure 7. Sequencer Mode 2 Timing Diagram

SEQUENCER MODE 3 – Scan, With Sequenced GPO Controls

This mode is used to sequentially convert a programmed set of channels in a preset order and sequence the GPO/GPIO bumps concurrently. The GPO/GPIO bumps are used to bias external circuitry such as bridge sensors; the common reference (GPOGND) is typically ground. After all channel conversions have completed, the MAX11259 automatically powers down into SLEEP mode. Figure 8 illustrates the Sequencer Mode 3 timing diagram for a three-channel scan. As long as CTRL3:GPO_MODE is set to '1', registers GPO_DIR and GPIO_CTRL are ignored in this mode, as the GPO/GPIO bumps are controlled by the sequencer.

If CTRL3:GPO_MODE is set to '0', the GPO/GPIO bumps are directly controlled by the GPO_DIR and GPIO_CTRL registers and are not controlled by the sequencer.

Programming Sequence

Mode Entry

1. Set up the following registers: SEQ, CHMAP0, CHMAP1, DELAY, CTRL1, CTRL3
   a. SEQ:MODE[1:0]='10' for sequencer mode 3
   b. If desired, set SEQ:RDYBEN to '1' to signal data ready only when all channel conversions are completed
   c. Enable SEQ:MDREN if conversion start is to be delayed to allow for input settling. Set DELAY:MUX[7:0] to the desired conversion delay
   d. Set CTRL3:GPO_MODE to '1' to enable GPO/GPIO sequencing

e. Set CHMAP0 and CHMAP1 to enable the channels for conversion and to set the channel conversion order. Map the corresponding GPO/GPIO bumps to a channel.
f. Enable SEQ:GPODREN to add a delay before the multiplexer selects this channel for conversion. Set DELAY:GPO to a delay value sufficient for the bias to settle.
g. Set CTRL1:PD[1:0] to STANDBY or SLEEP state to set the desired exit state if a conversion command with MODE[1:0] set to '01' is issued during the conversion
h. Set CTRL1:SCYCLE = '1' for single conversion mode

2. Write the conversion command (see Table 5)
   a. Set the data rate using bits RATE[3:0] of the command byte
   b. Set MODE[1:0] of command byte to '11'
3. Monitor RDYB (if SEQ:RDYBEN = '0') and bits STAT:SRDY[5:0] for availability of per channel conversion results in DATA[x] registers.

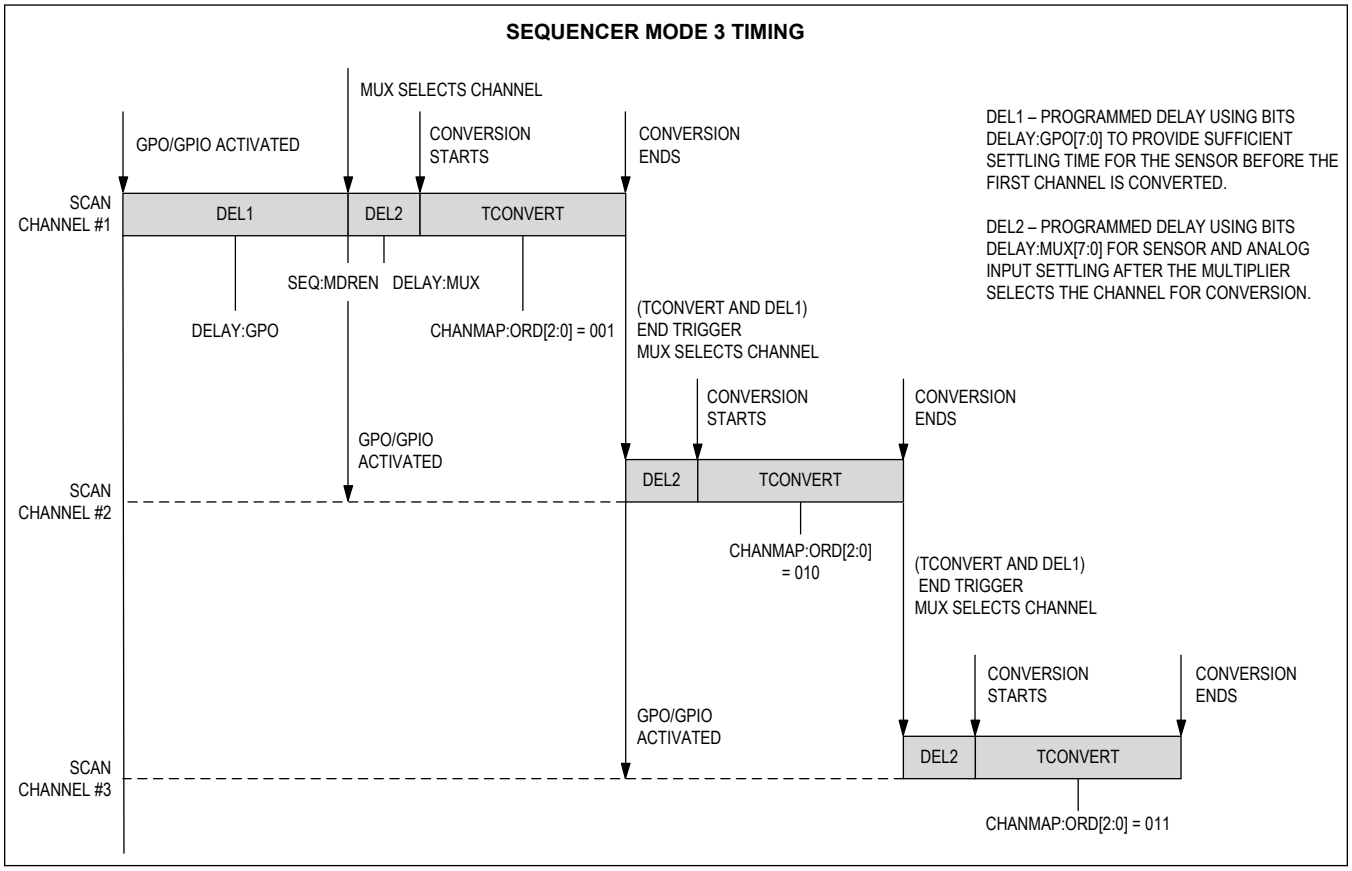


Figure 8. Sequencer Mode 3 Timing Diagram for a Three-Channel Scan

Mode Exit

1. This mode exits to SLEEP state upon completion of sequencing all channels and GPO/GPIO bumps.
2. To interrupt the current sequencing, perform mode exit. See the Changing SEQUENCER Modes—*Mode Exit* section. This puts the part in STANDBY or SLEEP state based on CTRL1:PD[1:0] set in step 1(g) of Mode Entry.

The bit CTRL1:CONTSC is ignored and bit CTRL1:SCYCLE = '0' is invalid in this mode.

Operating Examples—From Full Power-Down to Mode 3

In this example, channels 0, 1, and 2 are configured for conversion in mode 3. Channel 0 is configured last in the scan

order and the GPIO0 is mapped to this channel. Channel 1 is configured first in the scan order and GPO1 is mapped to this channel. Channel 2 is configured second in the scan order and GPO0 is mapped to this channel. Channels 0, 1, and 2 are enabled for scan and GPO/GPIO switching is also enabled. The RDYBEN is not set which generates a RDYB transition after each channel is converted. The PGA is configured for a gain of 128 and the data rate is 6,400sps in single-cycle mode. The MUX delays are enabled for all used channels and the GPO/GPIO delays are disabled. Reference I²C Command Sequence section.

Error Checking Sequencer Mode 3

The MAX11259 perform checks on registers CHMAP0 and CHMAP1. Error flags are set when invalid values are set:

STAT:GPOERR is set when more than one input channel is mapped to the same GPO/GPIO bump.
STAT:ORDERR is set when CHn_ORD is set as '000' or '111' and channel n is enabled using CHMAPx:CHn_EN.

Supplies and Power-On Sequence

The MAX11259 requires two power supplies, AVDD and DVDD. These power supplies can be sequenced in any order. The analog supply (AVDD) powers the analog inputs and the modulator. The DVDD supply powers the I²C interface. The low-voltage core logic can either be powered by the integrated LDO (default) or via DVDD. Figure 9 shows the two possible schemes. CAPREG denotes the internally generated supply voltage. If the LDO is used, the DVDD operating voltage range is from 2.0V to 3.6V. If the core logic is directly powered by DVDD (DVDD and CAPREG connected together), the DVDD operating voltage range is from 1.7V to 2.0V

Power-On Reset and Undervoltage Lockout

A global power-on reset (POR) is triggered until AVDD, DVDD, and CAPREG cross a minimum threshold voltage (V_{LH}), as shown in Figure 10.

To prevent ambiguous power-supply conditions from causing erratic behavior, voltage detectors monitor AVDD, DVDD, and CAPREG and hold the MAX11259 in reset when supplies fall below V_{HL} (see Figure 10). The analog undervoltage lockout (AVDD UVLO) prevents the ADC from converting when AVDD falls below V_{HL}. The CAPREG UVLO resets and prevents the low-voltage digital logic from operating at voltages below VHL. DVDD UVLO thresholds supersede CAPREG thresholds when CAPREG is externally driven. Figure 11 shows a flow diagram of the POR sequence. Glitches on supplies AVDD, DVDD, and CAPREG for durations shorter than T_P are suppressed without triggering POR or UVLO. For glitch durations longer than T_P, POR is triggered within T_{DEL} seconds. See the *Electrical Characteristics* table for values of V_{LH}, V_{HL}, T_P, and T_{DEL}.

I²C Command Sequence for Software Reset

I²C Transactions	Description
START; 011XXXX0; ACK;	Write to SEQ register
Write 0xD0; ACK;	Set MUX to 0b000, MODE to 0b10,
Write 0x12; ACK; STOP;	GPODREN to 0b0, MDREN to 0b1, RDYBEN to 0b0
START; 011XXXX0; ACK;	Write to DELAY register
Write 0xCA; ACK;	Set MUX[7:0] to 0xF0, GPO[7:0] to 0x00
Write 0xF0; ACK;	

I2C Transactions	Description
Write 0x00; ACK; STOP;	
START; 011XXXX0; ACK;	Write to CTRL3 register
Write 0xC6; ACK;	Set GPO_MODE to 0b1, all others to the default value;
Write 0x5C; ACK; STOP;	
START; 011XXXX0; ACK;	Write to CHMAP0 register
Write 0xCE; ACK;	CH2=0x0B: CH2_GPO=0b00,
Write 0x0B; ACK;	CH2_ORD=0b010, CH2_EN=0b1,
Write 0x0B; ACK;	CH2_GPOEN=0b1
Write 0x4F; ACK; STOP;	CH1=0x27: CH1_GPO=0b01,
	CH1_ORD=0b001, CH1_EN=0b1,
	CH1_GPOEN=0b1
	CH0=0x4F: CH0_GPO=0b10,
	CH0_ORD=0b011, CH0_EN=0b1,
	CH0_GPOEN=0b1
START; 011XXXX0; ACK;	Write to CTRL2 register
Write to CTRL2 register	set PGA gain to 0b111, LDOEN=0b1,
Write 0x3F; ACK; STOP;	LPMODE=0b1, PGAEN=0b1;

I2C Transactions	Description
START; 011XXXX0; ACK;	Convert using sequencer mode, data rate selected is 6,400 sps;
Write 0xBE; ACK; STOP;	
Wait	RDYB negative edge transition from ‘1’ to ‘0’ indicates conversion completed and DATA register ready for read
START; 011XXXX0; ACK;	Read register DATA1;
Write 0xD3; ACK;	
REPEATED START; 011XXXX1; ACK;	
Read One Byte of Data; ACK;	
Read One Byte of Data; ACK;	
Read One Byte of Data; NACK; STOP;	
Wait	RDYB negative edge transition from ‘1’ to ‘0’ indicates conversion completed and DATA register ready for read
START; 011XXXX0; ACK;	Read register DATA2
Write 0xD5; ACK;	
REPEATED START; 011XXXX1; ACK;	
Read One Byte of Data; ACK;	
Read One Byte of Data; ACK;	
Read One Byte of Data; NACK; STOP;	

I2C Transactions	Description
Wait	RDYB negative edge transition from '1' to '0' indicates conversion completed and DATA register ready for read
START; 011XXXX0; ACK;	Read register DATA0;
Write 0xD1; ACK;	
REPEATED START; 011XXXX1; ACK;	
Read One Byte of Data; ACK;	
Read One Byte of Data; ACK;	
Read One Byte of Data; NACK; STOP;	
SLEEP	Mode activity is completed. The MAX11254 powers down into SLEEP state waiting for the next command

Power-On Reset Timing

Power-on reset is triggered during power-up and undervoltage conditions as described above. Completion of the POR process is monitored by polling STAT:PDSTAT[1:0] = '10' for STANDBY state (see Figure 12.

Reset

Hardware Reset Using RSTB

The MAX11259 features an active-low RSTB bump to perform a hardware reset. Pulling the RSTB bump low stops any conversion in progress, reconfigures the internal registers to the power-on reset state and resets all digital filter states to zero. After the reset cycle is completed, the MAX11259 remains in STANDBY state and awaits further commands.

Software Reset

The host can issue a software reset to restore the default state of the MAX11259. A software reset sets the interface registers back into their default states and resets the internal state machines. However, a software reset does not emulate the complete POR or hardware reset sequence.

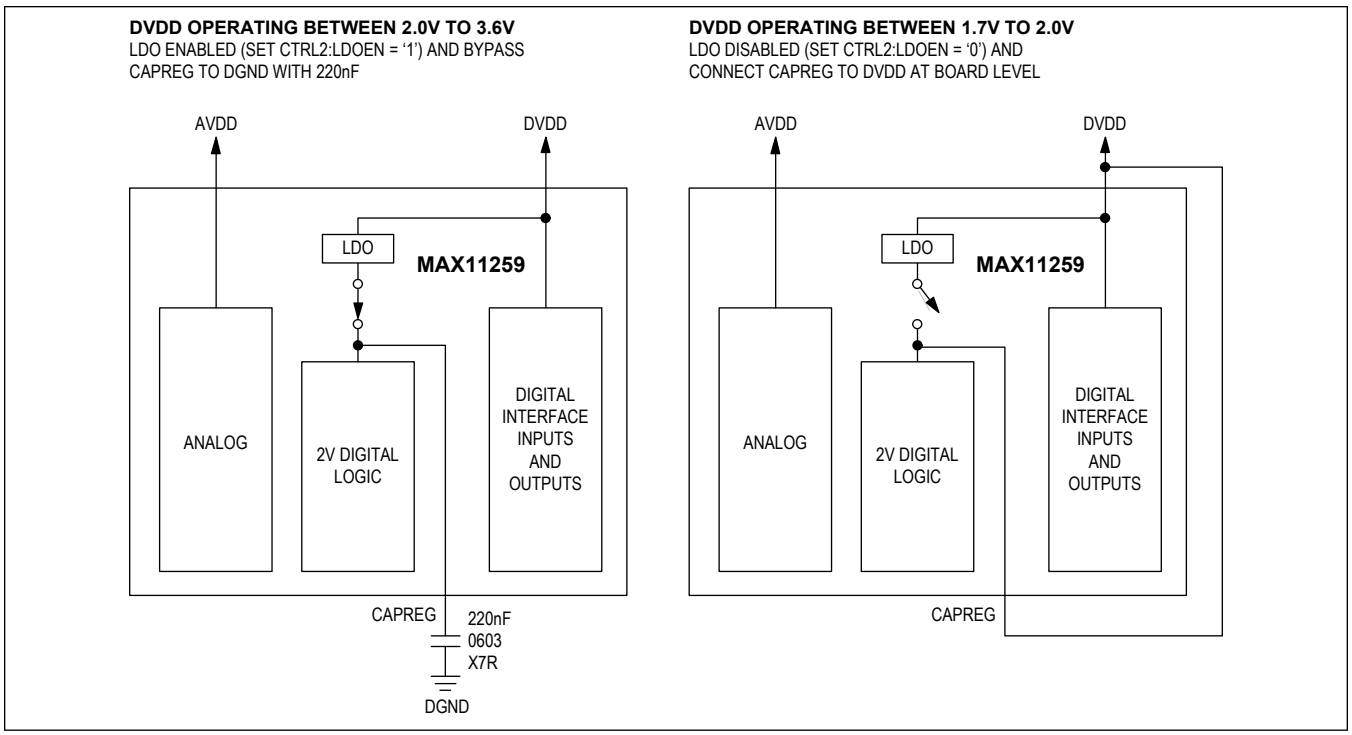


Figure 9. MAX11259 Digital Power Architecture

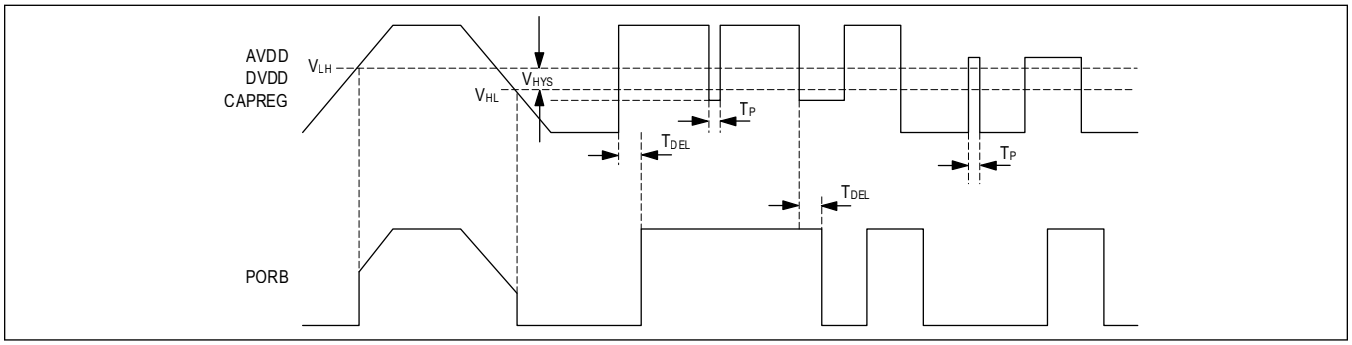


Figure 10. Undervoltage Lockout Characteristic Voltage Levels and Timing

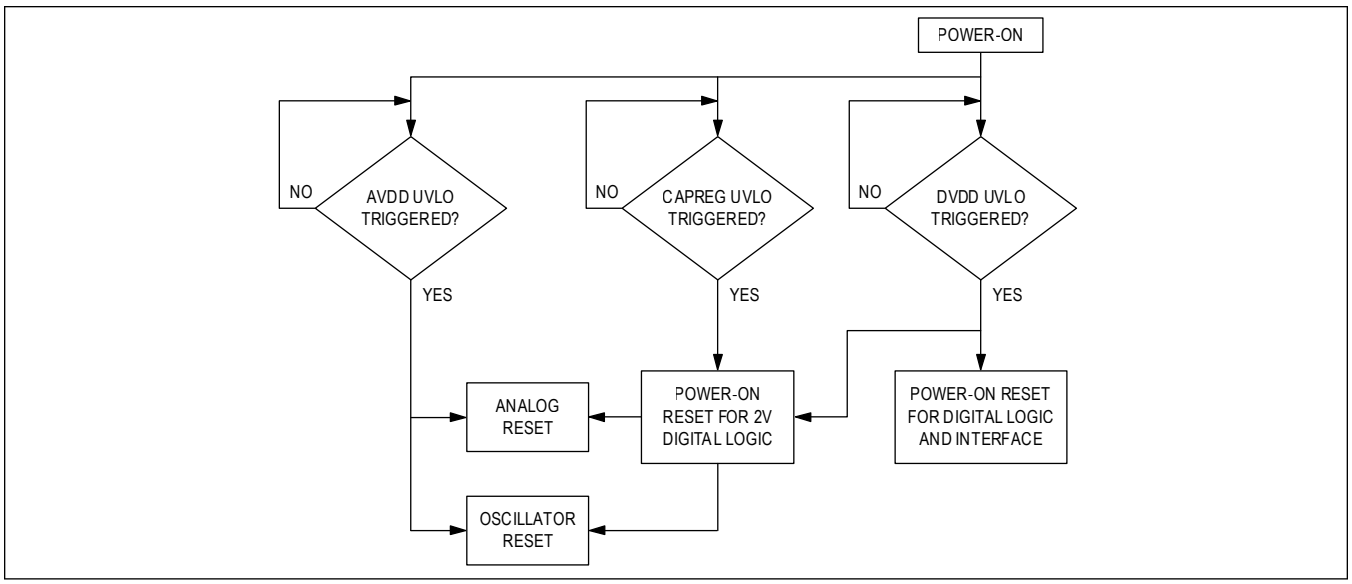


Figure 11. MAX11259 UVLO and POR Flow Diagram

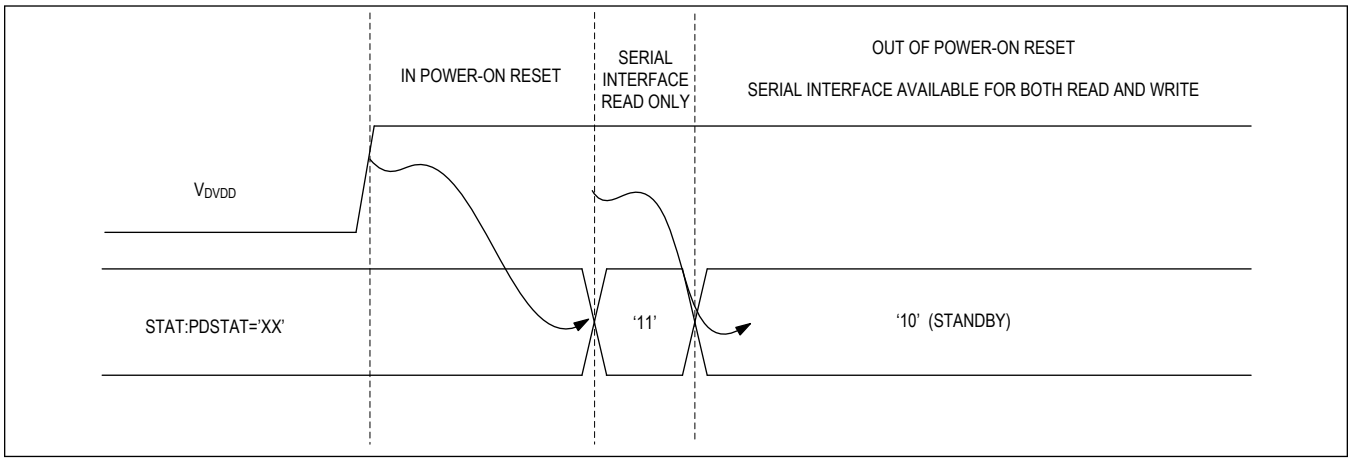


Figure 12. Power-On Reset and PDSTAT Timing

Two I2C transactions are required to issue a software reset: First set CTRL1:PD[1:0] to '11' (RESET). Then issue a conversion command with MODE[1:0] set to '01'.

To confirm the completion of the reset operation, STAT:PDSTAT and STAT:INRESET must be monitored. Figure 13 shows the state transition for the RESET command and the relative timing of STAT register update. During reset, INRESET = '1' and PDSTAT= '11'. The I2C interface cannot be written until MAX11259 enters STANDBY state where PDSTAT = '10'. To confirm completion of the RESET command, monitor for INRESET = '0' and PDSTAT = '10'.0 Table 7 summarizes the maximum delay for reset operation.

Power-Down States

To reduce overall power consumption, the MAX11259 features two power-down states: STANDBY and SLEEP. In SLEEP mode all circuitry is powered down, and the supply currents are reduced to leakage currents. In STANDBY mode the internal LDO and a low-frequency oscillator are powered up to enable fast start-up. After POR or a hardware reset the MAX11259 is in STANDBY mode until a command is issued.

Changing Power-Down States

Mode transition times are dependent on the current mode of operation. STAT:PDSTAT is updated at the end of all mode changes and is a confirmation of a completed transaction. The MAX11259 does not use a command FIFO or queue. The user must confirm the completed transaction by polling STAT:PDSTAT after the expected delay, as described in Table 7. Once the transition is complete, it is safe to send the next command. Verify that STAT:PDSTAT indicates the desired state before issuing a conversion command. Writes to any CTRL register during a conversion aborts the conversion and returns the MAX11259 to STANDBY state.

SLEEP STATE TO STANDBY STATE (FAST)

1. Set CTRL1:PD[1:0] = '10' for STANDBY state.
2. Set SEQ:MODE[1:0] = '00' for sequencer mode 1
3. Issue a conversion command with MODE[1:0] set to 11'.
4. Monitor STAT:PDSTAT[1:0] = '00' for active state.
5. Write the conversion command with MODE[1:0] set to 01'.
6. Monitor STAT:PDSTAT = '10' for completion.

STANDBY STATE TO SLEEP STATE (FAST)

1. Set CTRL1:PD[1:0] = '01' for STANDBY state.
2. Set SEQ:MODE[1:0] = '00' for sequencer mode 1
3. Issue a conversion command with MODE[1:0] set to 11'.
4. Monitor STAT:PDSTAT[1:0] = '00' for active state.
5. Write the conversion command with MODE[1:0] set to 01'.
6. Monitor STAT:PDSTAT = '01' for completion.

Calibration

Two types of calibration are available: self calibration and system calibration. Self calibration is used to reduce the MAX11259's gain and offset errors during changing operating conditions such as supply voltages, ambient temperature, and time. System calibration is used to reduce the gain and offset error of the entire signal path. This enables calibration of board level components and the integrated PGA. System calibration requires the MAX11259's inputs to be reconfigured for zero scale and full scale during calibration. The GPO/GPIO bumps can be used for this purpose. See Figure 14 for details of the calibration signal flow.

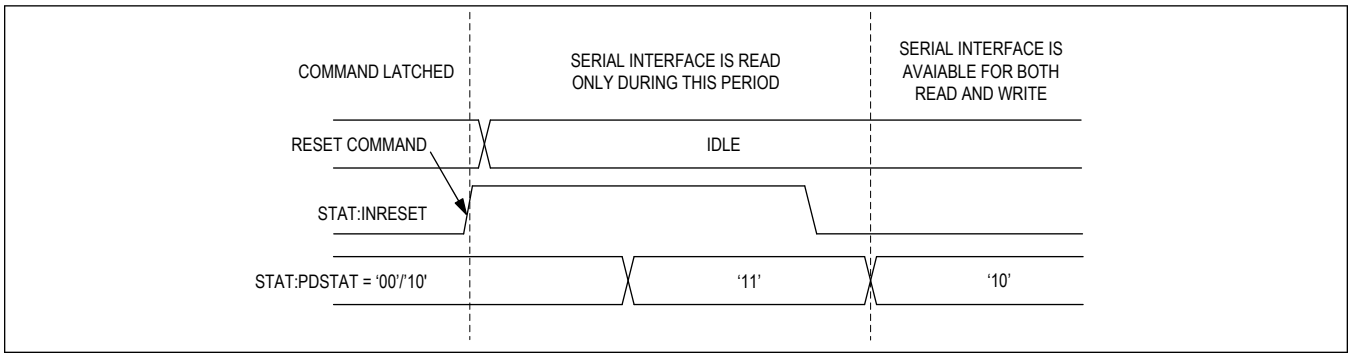


Figure 13. STAT:INRESET and STAT:PDSTAT Timing

Table 7. Maximum Delay Time for Mode Transitions

COMMAND ISSUED*	MAX11259 STATE BEFORE COMMAND	COMMAND INTERPRETATION	MAXIMUM DELAY TIME TO NEXT STATE†	MAX11259 STATE AFTER COMMAND
SLEEP	RESET	Command ignored	0	RESET
	SLEEP	Command ignored	0	SLEEP
	STANDBY	MAX11259 powers down into SLEEP mode	20ms	SLEEP
	STANDBY (fast)	Issue a conversion command and then monitor STAT:PDSTAT[1:0] for change of mode; then send conversion command with MODE[1:0] set to ‘01’	15µs	SLEEP
	Calibration	Calibration stops, MAX11259 powers down into SLEEP mode	3µs	SLEEP
	Conversion	Conversion stops, MAX11259 powers down into SLEEP mode	3µs	SLEEP
CONVERT	SLEEP	Mode change from SLEEP to conversion SAT: PDSTAT changes to ‘00’	T_{PUPSLP} + 3µs	Conversion
	STANDBY	STANDBY to conversion	T_{PUPSBY} + 3µs	Conversion
STANDBY	RESET	Command ignored	0	RESET
	SLEEP	MAX11259 changes to STANDBY	20ms	STANDBY
	SLEEP (fast)	Issue a conversion command and then monitor STAT:PDSTAT[1:0] for change of mode; then send conversion command with MODE[1:0] set to ‘01’	85µs	STANDBY
	STANDBY	Command ignored	0	STANDBY
	Calibration	Calibration stops	3µs	STANDBY
	Conversion	Conversion stops	3µs	STANDBY
RESET	RESET	Command ignored	0	RESET
	SLEEP	Command ignored	0	SLEEP
	STANDBY	Register values reset to default	28ms	STANDBY
	Calibration	Calibration stops, register values reset to default	6µs	STANDBY
	Conversion	Conversion stops, register values reset to default	6µs	STANDBY
POR	OFF	From complete power-down to STANDBY mode	10ms	STANDBY
RSTB	Any	From any state to STANDBY mode	10ms	STANDBY

*The commands are defined as follows:

SLEEP: Set CTRL1:PD[1:0] to ‘01’; issue a conversion command with MODE[1:0] set to ‘01’

STANDBY: Set CTRL1:PD[1:0] to ‘10’; issue a conversion command with MODE[1:0] set to ‘01’

RESET: Set CTRL1:PD[1:0] to ‘11’; issue a conversion command with MODE[1:0] set to ‘01’

CONVERT: Any conversion command with MODE[1:0] set to ‘11’

POR: Power-on reset during initial power-up or UVLO

RSTB: Hardware reset with RSTB bump

†See the *Electrical Characteristics* for T_{PUPSLP} and T_{PUPSBY}

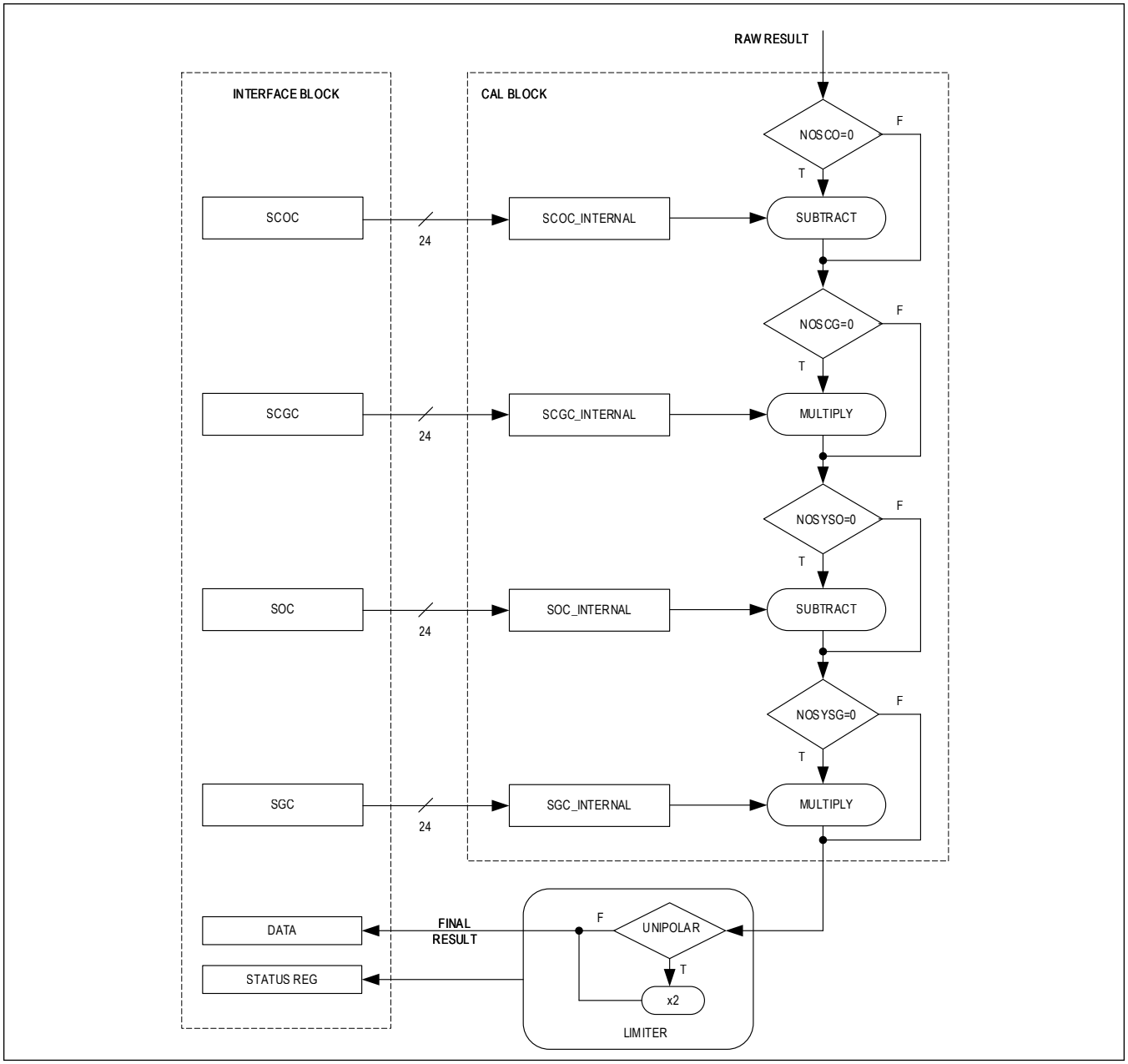


Figure 14. Calibration Flow Diagram

The calibration coefficients are stored in the registers SCOC, SCGC, SOC, and SGC. Data written to these registers is stored within the I2C domain and copied to internal registers before a conversion starts to process the raw data (see Figure 14). An internal or system calibration only updates the internal register values and does not alter the contents stored in the I2C domain. The bit CTRL3:CALREGSEL decides whether the internal contents or the contents stored in the I2C domain are read back during a read access of these registers. Bits NOSCO, NOSCG, NOSYSO, NOSYSG enable or disable the use of the individual calibration coefficients during data processing. See Figure 14, Calibration Flow Diagram.

Self-Calibration

The self-calibration is an internal operation and does not disturb the analog inputs. The self-calibration command can only

be issued in sequencer mode 1 (SEQ:MODE[1:0] = '00'). Self-calibration is accomplished in two independent phases, offset and gain. The first phase disconnects the inputs to the modulator and shorts them together internally to develop a zero-scale signal. A conversion is then completed and the results are post-processed to generate an offset coefficient which cancels all internally generated offsets. The second phase connects the inputs to the reference to develop a full-scale signal. A conversion is then completed and the results are post-processed to generate a full-scale coefficient, which scales the converters full-scale analog range to the full-scale digital range.

The entire self-calibration sequence requires two independent conversions, one for offset and one for full scale. The conversion rate is 50sps in the single-cycle mode. This rate provides the lowest noise and most accurate calibrations.

The self-calibration operation excludes the PGA. A system level calibration is available in order to calibrate the PGA signal path.

A self-calibration is started as follows: Set CTRL1:CAL[1:0] to '00' (self-calibration). Then issue a conversion command with the MODE[1:0] bits set to '10' (calibration). A self-calibration requires 200ms to complete.

System Calibration

This mode is used when calibration of board level components and the integrated PGA is required. The system calibration command is only available in sequencer mode 1.

A system calibration requires the input to be configured to the proper level for calibration. The offset and full-scale system calibrations are, therefore, performed using separate commands. The channel selected in the SEQ:MUX bits is used for system calibrations.

To perform a system offset calibration, the inputs must be configured for zero scale. The inputs do not necessarily need to be shorted to 0V as any voltage within the range of the calibration registers can be nulled in this calibration.

A system offset calibration is started as follows: Set CTRL1:CAL[1:0] to '01' (system offset calibration). Then issue a conversion command with the MODE[1:0] bits set to '10' (calibration). The system offset calibration requires 100ms to complete.

To perform a system full-scale calibration, the inputs must be configured for full scale. The input full-scale value does not necessarily need to be equal to V_{REF} since the input voltage range of the calibration registers can scale up or down appropriately within the range of the calibration registers.

A system full-scale calibration is started as follows: Set CTRL1:CAL[1:0] to '10' (system full-scale calibration). Then issue a conversion command with the MODE[1:0] bits set to '10' (calibration). The system full-scale calibration requires 100ms to complete. The GPO/GPIO bumps can be used during a system calibration.

All four calibration registers (SOC, SGC, SCOC, and SCGC) can be written by the host to store special calibration values. The new values will be copied to the internal registers at the beginning of a new conversion.

GPIOs

The MAX11259 provides three general-purpose input/ output ports that are programmable through the GPIO_ CTRL register. Enable the GPIO bumps by setting bits GPIO2_EN, GPIO1_EN, and GPIO0_EN, respectively. Set the DIR bits to select the bumps to be configured as inputs or outputs. All bumps are inputs by default. When programmed as output, set the DIO bits to set the bump state to '0' or '1'.

Conversion Synchronization Using SYNC Bump and External Clock

The SYNC bump—in conjunction with an external clock— can be used to synchronize the data conversions to external events. Set GPIO_CTRL:GPIO1_EN to '0' and GPI_CTRL:GPIO0_EN to '0' to configure the GPIO1/SYNC and GPIO0/ CLK bumps. Configure sync mode by setting CTRL3:SYNC_MODE to '1' and external clock mode by setting CTRL2:EXTCLK to '1'.

The synchronization mode is used to detect if the current conversions are synchronized to a continuous pulse signal with a period greater than the data rate. Ideally, the frequency of the synchronization signal is an integer multiple of the conversion rate. The synchronization mode records the number of device master clock cycles between a RDYB assertion and the rising edge of the next SYNC pulse. At the following SYNC pulse, the number of master clock cycles between a RDYB assertion and the rising edge of the SYNC pulse is evaluated again and com- pared to the recorded value. If the new number of master clock cycles differs by more than one from the recorded value, the conversion in progress is stopped, the digital filter contents are reset, and a new conversion starts. As the digital filter is reset, the full digital

filter latency is required before valid results are available. If the new master clock count is within the ±1 count limit, the conversions continue uninterrupted.

Figure 15 shows the timing relationship between the MAX11259 master clock and the SYNC signal. Due to startup delays, any SYNC pulses before the first RDYB assertion (low-going edge) are ignored. The first rising edge on the SYNC bump after a RDYB assertion establishes the relationship between the SYNC signal and the conversion timing.

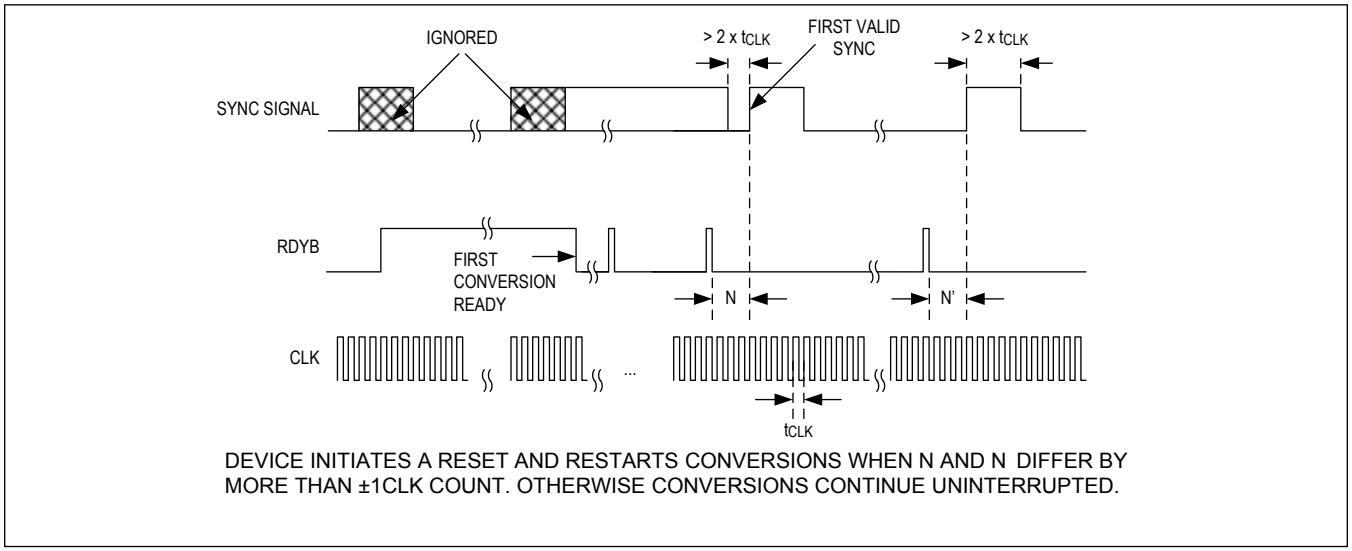


Figure 15. Timing Relationship between SYNC Signal, External Clock and RDYB

Table 8. Analog Overrange Behavior for Different Operating Conditions and Modes

	STAT REGISTER		
INPUT VOLTAGE	**AOR**	**DOR**	**DATA**
$-V_{REF} < V_{IN} < V_{REF}$	0	0	RESULT
$V_{REF} < V_{IN} < V_{OVRRNG}$	1	0	RESULT
$-V_{OVRRNG} < V_{IN} < -V_{REF}$	1	0	RESULT
$V_{IN} > V_{OVRRNG}$	1	1	0x7FFFFF
$V_{IN} < -V_{OVRRNG}$	1	1	0x800000

The DATA values shown are for bipolar ranges with two's complement number format. V_{OVRRNG} is the overrange voltage value typically > 120% of V_{REF}.

Components of the ADC

Modulator

MODULATOR DIGITAL OVERRANGE

The output of the SINC filter is monitored for overflow. When SINC filter overflow is detected, the STAT:DOR bit is set to '1' and a default value is loaded into the DATA register depending on the polarity of the overload. A positive overrange causes 0x7FFFFF to be written to the DATA register. A negative overrange causes 0x800000 to be written to the DATA register. See Table 8.

MODULATOR ANALOG OVERRANGE

The modulator analog overrange is used to signal the user that the input analog voltage has exceeded preset limits defined by the modulator operating range. These limits are approximately 120% of the applied reference voltage. When analog overrange is detected the STAT:AOR bit is set to '1' after DATA is updated. The AOR bit will always correspond

to the current value in the DATA register. See Table 8.

SINC Filter

The digital filter is a mode-configurable digital filter and decimator that processes the data stream from the fourth order delta-sigma modulator and implements a fifth order SINC function with an averaging function to produce a 24-bit wide data stream.

The SINC filter allows the MAX11259 to achieve very high SNR. The bandwidth of the fifth order SINC filter is approximately twenty percent of the data rate. See Figure 16 and Figure 17 for the filter response of 12.8ksps and 4ksps, respectively. See Figure 18 for the bandwidth of the individual signal stages.

Applications Information

Connecting an External 1.8V Supply to DVDD for Digital I/O and Digital Core

The voltage range of the DVDD I/O supply is specified from 2.0V to 3.6V if the internal LDO is used to power the digital core. If a lower I/O supply voltage is desired, the internal LDO can be disabled, and DVDD and CAPREG can be connected together as shown in Figure 19. In this mode of operation, DVDD can vary from 1.7V to 2.0V. The internal LDO must be disabled by setting CTRL2:LDOEN to '0'.

Split Supplies

The MAX11259 supports unipolar and split analog power supplies for input range flexibility. Using a split analog supply enables sampling below ground reference. The true bipolar input range is up to ±1.8V. See Figure 3 for analog input voltage range for both unipolar and split supplies.

Sensor Fault Detection

The MAX11259 includes a 1µA current source and a 1µA current sink. The source pulls current from AVDD to AIN_P and sink from AIN_N to AVSS. The currents are enabled by register bit CTRL3:CSSEN. These currents are used to detect damaged sensors in either open or shorted state. The current sources and sinks are functional over the normal input operating voltage range, as specified.

These currents are used to test sensors for functional operation before taking measurements on that input channel. With the source and sink enabled, the currents flow into the external sensor circuit and measurement of the input voltage is used to diagnose sensor faults. A full-scale reading could indicate a sensor is open circuit or overloaded or that the ADC's reference is absent. If a zero-scale is read back, this may indicate the sensor is short-circuited.

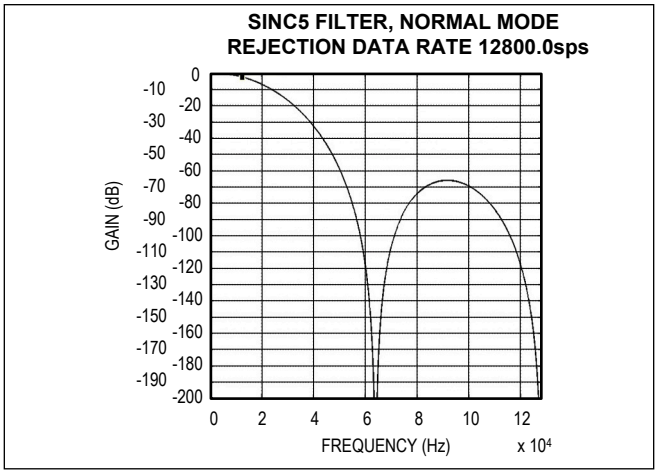


Figure 16. Digital Filter Frequency Response for 12.8ksps Single-Cycle Data Rate

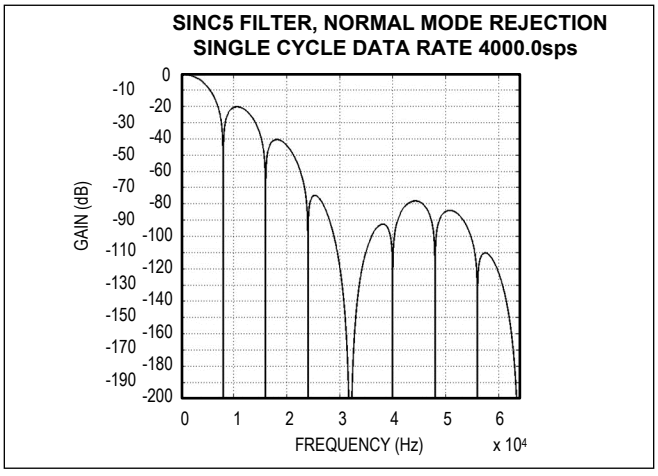


Figure 17. Digital Filter Frequency Response for 4ksps Single-Cycle Data Rate

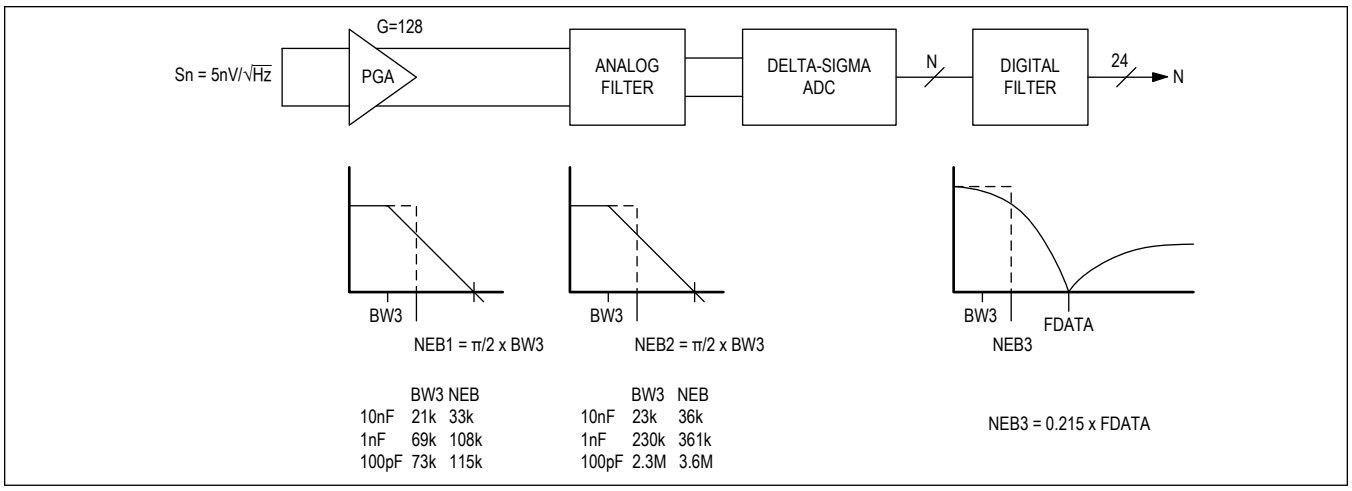


Figure 18. Signal Path Block Diagram Including Bandwidth of Each Stage

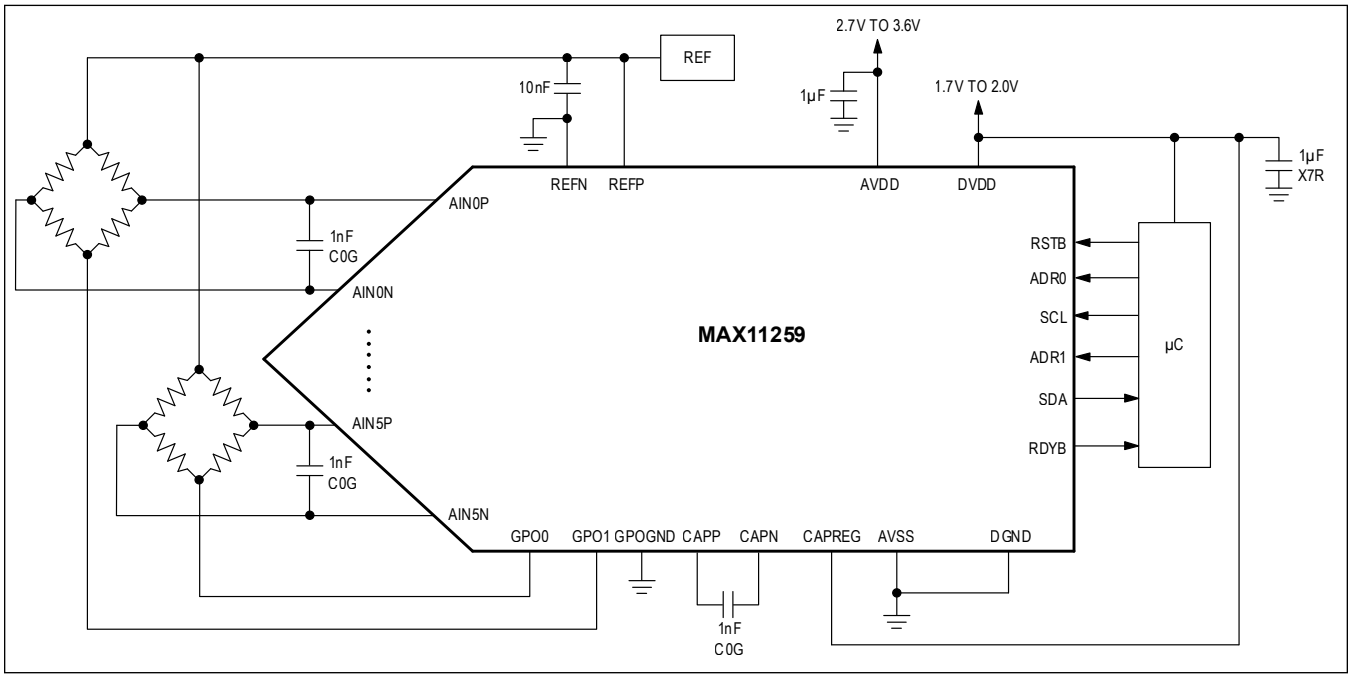


Figure 19. Application Diagram for 1.8V DVDD

Register Map

Legend: CNV IN PROGRESS column – behavior during conversion:

CNV – Normal read/write activities are available.
CS – Writes to these registers immediately abort conversion in progress and the MAX11259 enters STANDBY state.
IG – No changes, write is ignored.

RETENTION column – behavior during SLEEP mode:

R – The value of the register is retained.
M – Only bits in < > are retained. Others are cleared.

The address column shows the register address as used in the command byte definition (see Table 5).

Table 9. Register Map

NAME	R/W	CNV IN PROGRESS	RETENTION	ADDRESS(RS[4:0])	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
STAT	R	—	M	0	—	INRESET	<SRDY5>	<SRDY4>	<SRDY3>	<SRDY2>	<SRDY1>	<SRDY0>
					SCANERR	REFDET	ORDERR	GPOERR	ERROR	SYSGOR	DOR	AOR
					RATE3	RATE2	RATE1	RATE0	<PDSTAT1>	<PDSTAT0>	MSTAT	<RDY>
CTRL1	R/W	CS	R	1	CAL1	CAL0	PD1	PD0	U/$\overline{B}$	FORMAT	SCYCLE	CONTSC
CTRL2	R/W	CS	R	2	EXTCLK	CSSEN	LDOEN	LPMODE	PGAEN	PGAG2	PGAG1	PGAG0
CTRL3	R/W	CS	R	3	—	GPO_MODE	SYNC_MODE	CALREGSEL	NOSYSG	NOSYSO	NOSCG	NOSCO
GPIO_CTRL	R/W	CNV	R	4	GPIO1_EN	GPIO0_EN	DIR2	DIR1	DIR0	DIO2	DIO1	DIO0
DELAY	R/W	IG	R	5	MUX[7:0]							
					GPO[7:0]							
CHMAP1	R/W	IG	R	6	CG5_GPO2	CH5_GPO1	CH5_GPO0	CH5_ORD2	CH5_ORD1	CH5_ORD0	CH5_EN	CH5_GPOEN
					CG4_GPO2	CH4_GPO1	CH4_GPO0	CH4_ORD2	CH4_ORD1	CH4_ORD0	CH4_EN	CH4_GPOEN
					CG3_GPO2	CH3_GPO1	CH3_GPO0	CH3_ORD2	CH3_ORD1	CH3_ORD0	CH3_EN	CH3_GPOEN
CHMAP0	R/W	IG	R	7	CG2_GPO2	CH2_GPO1	CH2_GPO0	CH2_ORD2	CH2_ORD1	CH2_ORD0	CH2_EN	CH2_GPOEN
					CG1_GPO2	CH1_GPO1	CH1_GPO0	CH1_ORD2	CH1_ORD1	CH1_ORD0	CH1_EN	CH1_GPOEN
					CG0_GPO2	CH0_GPO1	CH0_GPO0	CH0_ORD2	CH0_ORD1	CH0_ORD0	CH0_EN	CH0_GPOEN
SEQ	R/W	CNV	R	8	MUX2	MUX1	MUX0	MODE1	MODE0	GPODREN	MDREN	RDYBEN
GPO_DIR	R/W	CNV	R	9	—	—	—	—	—	GPO2	GPO1	GPO0
SOC	R/W	IG	R	10	D[23:0]							
SGC	R/W	IG	R	11	D[23:0]							
SCOC	R/W	IG	R	12	D[23:0]							
SCGC	R/W	IG	R	13	D[23:0]							
DATA0	R	—	R	14	D[23:0]							
DATA1	R	—	R	15	D[23:0]							
DATA2	R	—	R	16	D[23:0]							

Table 9. Register Map (continued)

NAME	R/W	CNV IN PROGRESS	RETENTION	ADDRESS(RS[4:0])	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
DATA3	R	—	R	17	D[23:0]							
DATA4	R	—	R	18	D[23:0]							
DATA5	R	—	R	19	D[23:0]							

Register Definitions

STAT: Status Register (Read)

BIT NAME		INRESET	SRDY5	SRDY4	SRDY3	SRDY2	SRDY1	SRDY0
DEFAULT	0	0	0	0	0	0	0	0

BIT NAME	SCANERR	REFDET	ORDERR	GPOERR	ERROR	SYSGOR	DOR	AOR
DEFAULT	0	1	0	0	0	0	0	0

BIT NAME	RATE3	RATE2	RATE1	RATE0	PDSTAT1	PDSTAT0	MSTAT	RDY
DEFAULT	0	0	0	0	0	0	0	0

This register provides the functional status of the MAX11259.

BIT NAME	DESCRIPTION
INRESET	This bit is set to ‘1’ to indicate that the MAX11259 is in reset.
SRDY[5:0]	This bit is set to ‘1’ in sequencer modes 2 and 3 to indicate that a new conversion result is available from the channel indicated by the SRDY bit position. A complete read of the DATA register associated with the SRDY bit will reset the bit to ‘0’. At the start of a scan mode these bits are reset to ‘0’.
SCANERR	This bit is set to ‘1’ if sequencer mode 2 or 3 is selected and no channels or invalid channel numbers (‘000’ or ‘111’) are enabled in the CHMAP1 or CHMAP0 register. Until SCANERR is cleared, conversion commands are aborted.
REFDET	This bit is set to ‘1’ if a proper reference voltage is detected and ‘0’ if a proper reference voltage is missing. In SLEEP or STANDBY mode the value of this bit is ‘0’. The trigger level for this bit is VREF < 0.35V. This error does not inhibit normal operation and is intended for status only. The value of this status bit is valid within 30µs after a conversion start command and is invalid when not in conversion.
ORDERR	This bit is set to ‘1’ if two or more CHX_ORD bits decode to the same scan sequence order and are also enabled. This bit is also set to ‘1’ in the case when a channel is enabled for scan with CHX_EN=’1’ and CHX_ ORD[2:0] = ‘000’ or ‘111’. The CHX_ORD[2:0] values of ‘000’ and ‘111’ are not allowed as order of an enabled channel. The allowable orders are ‘001’, ‘010’, ‘011’, ‘100’, ‘101’, ‘110’. The MAX11259 remains in STANDBY state until this error is removed. The channel order must be strictly sequential and no missing numbers are allowed. For instance, if 4 channels are enabled then the order must be ‘001’, ‘010’, ‘011’, ‘100’. Any other order is flagged as ORDERR and the MAX11259 remains in STANDBY mode.
GPOERR	This bit is set to ‘1’ if more than one input channel is mapped to the same GPO/GPIO bump, and CHX_ GPOEN is enabled for more than one channel. The MAX11259 remains in STANDBY state until this error is removed.
ERROR	This bit is set to ‘1’ to indicate invalid configuration states. This bit is set if CAL[1:0] is programmed to ‘11’ which is an invalid state. This bit is set if CTRL1:SCYCLE = ‘0’ for scan modes 2 and 3. This error puts the MAX11259 into STANDBY mode.
SYSGOR	This bit is set to ‘1’ to indicate that a system gain calibration results in an overrange condition of the calibration coefficient. The SCGC calibration coefficient is set to the maximum value of 1.9999999.

BIT NAME	DESCRIPTION		
DOR	This bit is set to '1' to indicate that the conversion result has exceeded the maximum or minimum value of the converter and that the result has been clipped or limited to the maximum or minimum value. When set to '0' the conversion result is within the full-scale range of the inputs.		
AOR	This bit is set to '1' to indicate that the modulator detected an analog overrange condition by having the input signal level greater than the reference voltage. This check for overrange includes the PGA gain.		
RATE[3:0]	These bits indicate the conversion rate that corresponds to the result in the DATA registers or the rate that was used for calibration coefficient calculation. The corresponding RATE[3:0] is only valid until the DATA registers are read. The decoding of RATE[3:0] is shown in Table 1.		
PDSTAT[1:0]	These bits indicate the state of the MAX11259. See Table 7 for transition times		
	PDSTAT1	**PDSTAT0**	**DESCRIPTION**
	0	0	CONVERSION
	0	1	SLEEP
	1	0	STANDBY (default)
	1	1	RESET
MSTAT	This bit is set to '1' to indicate when a signal measurement is in progress. This indicates that a conversion, self-calibration, or system calibration is in progress and that the modulator is busy. When the modulator is not converting, this bit will be set to '0'.		
RDY	This bit is set to '1' to indicate that a new conversion result is available in sequencer mode 1. A complete read of the corresponding DATA register will reset this bit to '0'. This bit is invalid in sequencer mode 2 or 3. The function of this bit is redundant and is duplicated by the RDYB bump.		

CTRL1: Control Register 1 (Read/Write)

Default = 0x02I

BIT NAME	CAL1	CAL0	PD1	PD0	U/$\overline{B}$	FORMAT	SCYCLE	CONTSC
DEFAULT	0	0	0	0	0	0	1	0

This register controls the selection of operational modes and configurations.

BIT NAME	DESCRIPTION		
CAL[1:0]	The calibration bits control the type of calibration performed when a calibration command byte is issued:		
	CAL1	**CAL0**	**DESCRIPTION**
	0	0	Performs a self-calibration
	0	1	Performs a system-level offset calibration
	1	0	Performs a system-level full-scale calibration
	1	1	Reserved. Do not use.
PD[1:0]	Selects the power-down state to be executed. The MAX11259 enters the selected power-down state after a conversion command with MODE[1:0] set to '01' is written. The state is decoded as below:		
	PD1	**PD0**	**DESCRIPTION**
	0	0	NOP (default)
	0	1	SLEEP
	1	0	STANDBY
	1	1	RESET
U/B	The 'unipolar/bipolar' bit controls the input range. A '1' selects unipolar input range and a '0' selects bipolar input range.		
FORMAT	The 'format' bit controls the digital format of the bipolar range data. A '0' selects two's complement and a '1' selects offset binary format of the bipolar range. The data for unipolar range is always formatted in offset binary format.		

BIT NAME	DESCRIPTION
SCYCLE	The 'single-cycle' bit selects either no-latency single conversion mode or continuous conversion in sequencer mode 1. A '1' selects single-cycle mode where a no-latency conversion is followed by a power-down to SLEEP mode. A '0' selects continuous conversion mode with a latency of 5 conversion cycles for filtering. The RDYB bump goes low when valid/settled data is available. Only SCYCLE = '1' is valid in sequencer mode 2 and 3.
CONTSC	The 'continuous single-cycle' bit selects between single or continuous conversions while operating in single-cycle mode in sequencer mode 1. A '1' selects continuous conversions and a '0' selects a single conversion.

CTRL2: Control Register 2 (Read/Write)

Default = 0x20

BIT NAME	EXTCLK	CSSEN	LDOEN	LPMODE	PGAEN	PGAG2	PGAG1	PGAG0
DEFAULT	0	0	1	0	0	0	0	0

This register controls the selection and configuration of optional functions.

<table>
<tr><th>BIT NAME</th><th colspan="4">DESCRIPTION</th></tr>
<tr><td>EXTCLK</td><td colspan="4">External clock mode is enabled by setting this bit to '1'. In this mode, the internal oscillator is bypassed and the GPIO0/CLK bump is configured as external clock input.</td></tr>
<tr><td>CSSEN</td><td colspan="4">Setting this bit to '1' enables the current source and current sink on the analog inputs to detect sensor opens or shorts.</td></tr>
<tr><td>LDOEN</td><td colspan="4">Set this bit to '1' to enable the internal LDO. Set this bit to '0' when driving the CAPREG bump externally with a 1.8V supply. When driving the CAPREG bump with external supply, the user must ensure that the CAPREG bump is connected to the DVDD bump.</td></tr>
<tr><td>LPMODE</td><td colspan="4">PGA low-power mode is enabled by setting this bit to '1'. The PGA operates with reduced power consumption and reduced performance. The LPMODE does not affect power or performance when the PGA is not enabled.</td></tr>
<tr><td>PGAEN</td><td colspan="4">The PGA enable bit controls the operation of the PGA. A '1' enables and a '0' disables the PGA.</td></tr>
<tr><td rowspan="10">PGA[2:0]</td><td colspan="4">The 'PGA' bits control the PGA gain. The PGA gain is set by:</td></tr>
<tr><td>PGA2</td><td>PGA1</td><td>PGA0</td><td>DESCRIPTION</td></tr>
<tr><td>0</td><td>0</td><td>0</td><td>Gain = 1</td></tr>
<tr><td>0</td><td>0</td><td>1</td><td>Gain = 2</td></tr>
<tr><td>0</td><td>1</td><td>0</td><td>Gain = 4</td></tr>
<tr><td>0</td><td>1</td><td>1</td><td>Gain = 8</td></tr>
<tr><td>1</td><td>0</td><td>0</td><td>Gain = 16</td></tr>
<tr><td>1</td><td>0</td><td>1</td><td>Gain = 32</td></tr>
<tr><td>1</td><td>1</td><td>0</td><td>Gain = 64</td></tr>
<tr><td>1</td><td>1</td><td>1</td><td>Gain = 128</td></tr>
</table>

CTRL3: Control Register 3 (Read/Write)

Default = 0x1C

BIT NAME		GPO_MODE	SYNC_MODE	CALREGSEL	NOSYSG	NOSYSO	NOSCG	NOSCO
DEFAULT		0	0	1	1	1	0	0

This register is used to control the operation and calibration of the MAX11259.

BIT NAME	DESCRIPTION
GPO_MODE	The value of this bit controls the GPO mode for sequencer mode 3. When set to '1', the GPO and the GPIO bumps are sequenced based on the channel mapbumpg in the CHMAP1 and CHMAP0 registers. When set to '0', the GPO and GPIO bumps are directly controlled by the GPO_DIR and GPIO_CTRL registers, respectively, during conversion or STANDBY state. This bit has no effect in sequencer modes 1 and 2.
SYNC_MODE	This bit controls sync mode (see the Conversion Synchronization Using Sync Bump and External Clock section). When set to '1', the synchronization mode is enabled, when set to '0' it is disabled.

BIT NAME	DESCRIPTION
CALREGSEL	This bit controls which calibration value is read during a calibration register inquiry. Set this bit to '1' to read back the interface value. Set this bit to '0' to read back the internal register value.
NOSYSG	The 'no system gain' bit controls the use of the system gain calibration coefficient. Set this bit to '1' to disable the use of the system gain value when computing the final offset and gain corrected data value. Set this bit to '0' to enable the use of the system gain value when computing the final offset and gain corrected data value.
NOSYSO	The 'no system offset' bit controls the use of the system offset calibration coefficient. Set this bit to '1' to disable the use of the system offset value when computing the final offset and gain corrected data value. Set this bit to '0' to enable the use of the system offset value when computing the final offset and gain corrected data value.
NOSCG	The 'no self-calibration gain' bit controls the use of the self-calibration gain calibration coefficient. Set this bit to '1' to disable the use of the self-calibration gain value when computing the final offset and gain corrected data value. Set this bit to '0' to enable the use of the self-calibration gain value when computing the final offset and gain corrected data value.
NOSCO	The 'no self-calibration offset' bit controls the use of the self-calibration offset calibration coefficient. Set this bit to '1' to disable the use of the self-calibration offset value when computing the final offset and gain corrected data value. Set this bit to '0' to enable the use of the self-calibration offset value when computing the final offset and gain corrected data value.

GPIO_CTRL: GPIO Control Register (Read/Write)

Default = 0x4x

BIT NAME	GPIO1_EN	GPIO0_EN	DIR2	DIR1	DIR0	DIO2	DIO1	DIO0
DEFAULT	0	1	0	0	0	X	X	X

This register controls the direction and values of the general-purpose I/O (GPIO) bumps.

BIT NAME	DESCRIPTION
GPIO1_EN	This bit selects the functionality of the GPIO1/SYNC bump. Set this bit to '1' to use the bump as GPIO, or set the bit to '0' to use the bump as SYNC input.
GPIO0_EN	This bit selects the functionality of the GPIO0/CLK bump. Set this bit to '1' to use the bump as GPIO, or set the bit to '0' to use the bump as external clock input.
DIR[2:0]	The 'direction' bits configure the GPIO bumps either as input or output. DIR2 corresponds to GPIO2, DIR1 corresponds to GPIO1, while DIR0 controls GPIO0. Set the DIR bit to '1' to configure the GPIO bump as output. The output value of the GPIO bump is determined by the value of the DIO bit. Set the DIR bit to '0' to configure the associated GPIO bump as input. The logic input value of the GPIO bump can be read back from the DIO bit.
DIO[2:0]	The 'data input/output' bits reflect the status of the GPIO bumps. DIO2 corresponds to GPIO2, DIO1 corresponds to GPIO1, while DIO0 corresponds to GPIO0. If the GPIO bump is configured as output, the bump is driven to the logic value of DIO. If the GPIO bump is configured as input, DIO reflects the logic value seen at the bump.

DELAY: Delay Register (Read/Write)

Default = 0x0000

BIT NAME	MUX[7:0]	GPO[7:0]
DEFAULT	0x00	0x00

BIT NAME	DESCRIPTION
MUX[7:0]	Used to program the mux delay. The mux delay ranges from 4µs to 1.02ms. The default value of 0x00 corresponds to no delay. 1 LSB = 4µs of delay.
GPO[7:0]	Used to program the GPO/GPIO delay. The GPO/GPIO delay ranges from 20µs to 5.1ms. The default value of 0x00 corresponds to no delay. 1 LSB = 20µs of delay.

CHMAP1: Channel Map Register (Read/Write)

Default = 0x00_0000

BIT NAME	CH5_GPO2	CH5_GPO1	CH5_GPO0	CH5_ORD2	CH5_ORD1	CH5_ORD0	CH5_EN	CH5_GPOEN
DEFAULT	0	0	0	0	0	0	0	0
BIT NAME	CH4_GPO2	CH4_GPO1	CH4_GPO0	CH4_ORD2	CH4_ORD1	CH4_ORD0	CH4_EN	CH4_GPOEN
DEFAULT	0	0	0	0	0	0	0	0
BIT NAME	CH3_GPO2	CH3_GPO1	CH3_GPO0	CH3_ORD2	CH3_ORD1	CH3_ORD0	CH3_EN	CH3_GPOEN
DEFAULT	0	0	0	0	0	0	0	0

CHMAP0: Channel Map Register (Read/Write)

Default = 0x00_0000

BIT NAME	CH2_GPO2	CH2_GPO1	CH2_GPO0	CH2_ORD2	CH2_ORD1	CH2_ORD0	CH2_EN	CH2_GPOEN
DEFAULT	0	0	0	0	0	0	0	0
BIT NAME	CH1_GPO2	CH1_GPO1	CH1_GPO0	CH1_ORD2	CH1_ORD1	CH1_ORD0	CH1_EN	CH1_GPOEN
DEFAULT	0	0	0	0	0	0	0	0
BIT NAME	CH0_GPO2	CH0_GPO1	CH0_GPO0	CH0_ORD2	CH0_ORD1	CH0_ORD0	CH0_EN	CH0_GPOEN
DEFAULT	0	0	0	0	0	0	0	0

These registers are used to enable channels for scan, enable output controls for scan, program the channel scan order, and pair the GPO/GPIO bumps with its associated channel. These registers cannot be written during an active conversion.

<table>
<tr><th>BIT NAME</th><th colspan="4">DESCRIPTION</th></tr>
<tr><td rowspan="8">CHX_GPO[2:0]</td><td colspan="4">Used to map which GPO or GPIO bump is activated when this channel is selected. The STAT:GPOERR flag is set if more than one input channels is mapped to the same GPO/GPIO bump. The decoding is as follows:</td></tr>
<tr><td>CHX_GPO2</td><td>CHX_GPO1</td><td>CHX_GPO0</td><td>DESCRIPTION</td></tr>
<tr><td>0</td><td>0</td><td>0</td><td>GPO0</td></tr>
<tr><td>0</td><td>0</td><td>1</td><td>GPO1</td></tr>
<tr><td>0</td><td>1</td><td>0</td><td>GPO2</td></tr>
<tr><td>0</td><td>1</td><td>1</td><td>GPIO0</td></tr>
<tr><td>1</td><td>0</td><td>0</td><td>GPIO1</td></tr>
<tr><td>1</td><td>0</td><td>1</td><td>GPIO2</td></tr>
<tr><td>CHX_ORD[2:0]</td><td colspan="4">Defines the order during scan when the channel is enabled. The CHX_ORD[2:0] values of ‘000’ and ‘111’ are not allowed for the order of an enabled channel. The allowable orders are ‘001’, ‘010’, ‘011’, ‘100’, ‘101’, ‘110’ representing first, second, third channel to be scanned, and so on. The value of ‘000’ is a default value and the value of ‘111’ is greater than the number of scannable channels.
A value greater than the number of enabled channels is invalid and will set an error condition at STAT:ORDERR. Setting a channels order to ‘000’ or ‘111’ and enabling it will set the STAT:ORDERR flag in the STAT register. If sequencer mode 3 is selected, and more channels are enabled for sequencing than available GPO/GPIO bumps, then the sequence order of the channels for which a GPO/GPIO bump is enabled must be lower than for the channels which do not have a GPO/GPIO bump mapped to them.</td></tr>
<tr><td>CHX_EN</td><td colspan="4">Set this bit to ‘1’ to enable scanning of this channel. Set this bit to ‘0’ to disable scanning of this channel.</td></tr>
<tr><td>CHX_GPOEN</td><td colspan="4">Used to enable activation of the GPO/GPIO bumps when this channel is selected during scan. Set this bit to ‘1’ to enable. Set this bit to ‘0’ to disable.</td></tr>
</table>

SEQ: Sequencer Register (Read/Write)

Default = 0x00

BIT NAME	MUX2	MUX1	MUX0	MODE1	MODE0	GPODREN	MDREN	RDYBEN
DEFAULT	0	0	0	0	0	0	0	0

This register is used to control the operation of the sequencer when enabled.

BIT NAME	DESCRIPTION		
MUX[2:0]	Binary channel selection for sequencer mode 1. Valid channels are from 000 (channel 0) to 101 (channel 5).		
MODE[1:0]	Sequencer mode is decoded as shown in the following table:		
	MODE1	**MODE0**	**DESCRIPTION**
	0	0	Sequencer Mode 1
	0	1	Sequencer Mode 2
	1	0	Sequencer Mode 3
	1	1	Reserved. Do not use.
GPODREN	GPO/GPIO delay enable. Enables operation of the GPO/GPIO switch delay. When enabled, the channel selection is delayed. The value of the delay is set by the DELAY:GPO bits.		
MDREN	MUX delay enable. Enables the timer setting in the DELAY:MUX register to delay the conversion start of the selected channel.		
RDYBEN	Ready Bar enable. When this bit is ‘1’ the RDYB is inhibited from asserting in sequencer mode 2 and 3 until all channels are converted		

GPO_DIR: GPO Direct Access Register (Read/Write)

Default = 0x00

BIT NAME						GPO2	GPO1	GPO0
DEFAULT						0	0	0

This register is used to turn on and off the general-purpose outputs directly after an associated bit is written except when CTRL3:GPO_ MODE=’1’ during sequencer mode 3. When operating in sequencer mode 1 or 2, the activation of the GPOs is immediate upon setting a bit to ’1’, and the deactivation of the GPOs is immediate upon setting the bit to ‘0’. In SLEEP state, the values in this register do not control the state of the GPOs, as they all are deactivated. The register is writeable, but the values will not control the GPOs in SLEEP mode. In STANDBY state when CTRL3:GPO_MODE=’0’, this register accepts writes and updates the state of the GPOs immediately after the value of a bit changes. Writes to this register are ignored when operating in mode 3 when CTRL3:GPO_MODE=’1’. This register is enabled during system offset calibration, system gain calibration and self-calibration modes.

SOC: System Offset Calibration Register (Read/Write)

Default = 0x00_0000

BIT NAME	B23	B22	B21	….	B3	B2	B1	B0
DEFAULT	0	0	0	….	0	0	0	0

The system offset calibration register is a 24-bit read/write register. The data written/read to/from this register is clocked in/out MSB first. This register holds the system offset calibration value. The format is in two’s complement binary format. A system calibration does not overwrite the SOC register.

The readback value of this register depends on CTRL3:CALREGSEL. A ‘1’ reads back the user programmed value. A ‘0’ reads back the results of an internal register as described in CTRL3:CALREGSEL. The internal register can only be read during conversion.

The system offset calibration value is subtracted from each conversion result—provided the NOSYSO bit in the CTRL3 register is set to ‘0’. The system offset calibration value is subtracted from the conversion result after self-calibration but before system gain correction. It is also applied prior to the 1x or 2x scale factor associated with bipolar and unipolar modes. When a system offset calibration is in progress, this register is not writable by the user.

SGC: System Gain Calibration Register (Read/Write)

Default = 0x7F_FFFF

BIT NAME	B23	B22	B21	….	B3	B2	B1	B0
DEFAULT	0	1	1	….	1	1	1	1

The system gain calibration register is a 24-bit read/write register. The data written/read to/from this register is clocked

in/out MSB first. This register holds the system gain calibration value. The format is unsigned 24-bit binary. A system calibration does not overwrite the SGC register.

The readback value of this register depends on CTRL3:CALREGSEL. A ‘1’ reads back the user programmed value. A ‘0’ reads back the results of an internal register as described in CTRL3:CALREGSEL. The internal register can only be read during conversion.

The system gain calibration value is used to scale the offset corrected conversion result—provided the NOSYSG bit in the CTRL3 register is set to ‘0’. The system gain calibration value scales the offset corrected result by up to 2x or can correct a gain error of approximately -50%. The amount of positive gain error that can be corrected is determined by modulator overload characteristics, which may be as much as +25%. When a system gain calibration is in progress, this register is not writable by the user.

SCOC: Self-Calibration Offset Calibration Register (Read/Write)

Default = 0x00_0000

BIT NAME	B23	B22	B21	….	B3	B2	B1	B0
DEFAULT	0	0	0	….	0	0	0	0

The self-calibration offset register is a 24-bit read/write register. The data written/read to/from this register is clocked in/out MSB first. This register holds the self-calibration offset value. The format is always in two’s complement binary format. An internal self- calibration does not overwrite the SCOC register.

The readback value of this register depends on CTRL3:CALREGSEL. A ‘1’ reads back the user programmed value. A ‘0’ reads back the results of an internal register as described in CTRL3:CALREGSEL. The internal register can only be read during conversion.

The self-calibration offset value is subtracted from each conversion result—provided the NOSCO bit in the CTRL3 register is set to ‘0’. The self-calibration offset value is subtracted from the conversion result before the self-calibration gain correction and before the system offset and gain correction. It is also applied prior to the 2x scale factor associated with unipolar mode. When a self-calibration is in progress, this register is not writable by the user.

SCGC: Self-Calibration Gain Calibration Register (Read/Write)

Default = 0xBF_851B

BIT NAME	B23	B22	B21	….	B3	B2	B1	B0
DEFAULT	1	0	1	….	1	0	1	1

The self-calibration gain register is a 24-bit read/write register. The data written/read to/from this register is clocked in/out MSB first. This register holds the self-calibration gain value. The format is unsigned 24-bit binary. An internal self-calibration does not overwrite the SCGC register.

The readback value of this register depends on CTRL3:CALREGSEL. A ‘1’ reads back the user programmed value. A ‘0’ reads back the results of an internal register as described in CTRL3:CALREGSEL. The internal register can only be read during conversion.

The self-calibration gain calibration value is used to scale the self-calibration offset corrected conversion result before the system offset and gain calibration values have been applied – provided the NOSCG bit in the CTRL3 register is set to ‘0’. The self-calibration gain calibration value scales the self-calibration offset corrected conversion result by up to 2x or can correct a gain error of approximately

–50%. The gain will be corrected to within 2 LSB. When a self- calibration is in progress, this register is not writable by the user.

DATA[5:0]: Data Registers (Read Only)

Default = 0x00_0000

BIT NAME	D23	D22	D21	…	D3	D2	D1	D0
DEFAULT	0	0	0	…	0	0	0	0

Each data register holds the conversion result for the corresponding channel. DATA0 is the data register for channel 0, DATA1 is for channel 1, etc.

Each data register is a 24-bit read-only register. Any attempt to write data to this location will have no effect. The data read from these registers is clocked out MSB first. The result is stored in a format according to the FORMAT bit in the CTRL1 register. The data format while in unipolar mode is always offset binary. In offset binary format the most negative value is 0x000000, the midscale value is 0x800000 and the most positive value is 0xFFFFFF. In bipolar mode if the FORMAT bit = '1' then the data format is offset binary. If the FORMAT bit = '0', then the data format is two's complement. In two's complement the negative full-scale value is 0x800000, the midscale is 0x000000 and the positive full scale is 0x7FFFFF. Any input exceeding the available input range is limited to the minimum or maximum data value.

Ordering Information

PART	TEMP RANGE	BUMP-PACKAGE
MAX11259AWX+T	-40°C to +125°C	36 WLP

+Denotes a lead(Pb)-free/RoHS-compliant package.

T = Tape and reel.

Revision History

REVISION NUMBER	REVISION DATE	DESCRIPTION	PAGES CHANGED
0	9/15	Initial release	—
1	10/20	Updated *Detailed Description*	17, 38

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