General Description

The MAX1108/MAX1109 low-power, 8-bit, dual-channel, analog-to-digital converters (ADCs) feature an internal track/hold (T/H) voltage reference, clock, and serial interface. The MAX1108 is specified from +2.7V to +3.6V and consumes only 105 μ A. The MAX1109 is specified from +4.5V to +5.5V and consumes only 130 μ A. The analog inputs are software configurable, allowing unipolar/bipolar and single-ended/differential operation; battery monitoring capability is also included.

The full-scale analog input range is determined by the internal reference of +2.048V (MAX1108) or +4.096V (MAX1109), or by an externally applied reference ranging from 1V to VDD. The MAX1108/MAX1109 also feature a software power-down mode that reduces power consumption to 0.5µA when the device is not in use. The 4-wire serial interface directly connects to SPI™, QSPI™, and MICROWIRE™ devices without external logic. Conversions up to 50ksps are performed using either the internal clock or an external serial-interface clock.

The MAX1108 and MAX1109 are available in a 10-pin μ MAX package with a footprint that is just 20% of an 8-pin plastic DIP.

_ Applications

Portable Data Logging

Hand-Held Measurement Devices

Medical Instruments

System Diagnostics

Solar-Powered Remote Systems

4–20mA-Powered Remote Systems

Receive-Signal Strength Indicators



Pin Configuration

Features

- Single Supply: +2.7V to +3.6V (MAX1108) +4.5V to +5.5V (MAX1109)
- Low Power: 105µA at +3V and 50ksps 0.5µA in Power-Down Mode
- Software-Configurable Unipolar or Bipolar Inputs
- Input Voltage Range: 0 to VDD
- Internal Track/Hold
- Internal Reference: +2.048V (MAX1108) +4.096V (MAX1109)
- ♦ Reference Input Range: 1V to VDD
- SPI/QSPI/MICROWIRE-Compatible Serial Interface
- V_{DD} Monitoring Mode
- Small 10-Pin µMAX Package

Ordering Information

PART	TEMP RANGE	PIN-PACKAGE
MAX1108CUB	0°C to +70°C	10 µMAX
MAX1108EUB	-40°C to +85°C	10 µMAX
MAX1109CUB	0°C to +70°C	10 µMAX
MAX1109EUB	-40°C to +85°C	10 µMAX

Functional Diagram



SPI and QSPI are trademarks of Motorola, Inc. MICROWIRE is a trademark of National Semiconductor Corp.

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Maxim Integrated Products 1

For pricing, delivery, and ordering information, please contact Maxim/Dallas Direct! at 1-888-629-4642, or visit Maxim's website at www.maxim-ic.com.

ABSOLUTE MAXIMUM RATINGS

 Operating Temperature Ranges

MAX110_CUB	0°C to +70°C
MAX110_EUB	40°C to +85°C
Storage Temperature Range	65°C to +150°C
Lead Temperature (soldering, 10s)	+300°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS—MAX1108

 $(V_{DD} = +2.7V \text{ to } +3.6V; \text{ unipolar input mode; COM} = GND, f_{SCLK} = 500 \text{kHz}$, external clock mode (50% duty cycle); 10 clocks/conversion cycle (50ksps); 1µF capacitor at REF, external +2.048V reference at REF; T_A = T_{MIN} to T_{MAX}; unless otherwise noted. Typical values are at T_A = +25°C.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS					
DC ACCURACY											
Resolution			8			bits					
Polativo Acouroov (Noto 1)	INI	V _{DD} = 2.7V to 3.6V		±0.15	±0.5						
Relative Accuracy (Note T)		V _{DD} = 5.5V (Note 2)		±0.2		LOD					
Differential Nonlinearity	DNL	No missing codes over temperature			±1	LSB					
Offect Error		V _{DD} = 2.7V to 3.6V		±0.2	±1						
Oliset Error		V _{DD} = 5.5V (Note 2)		±0.5		LOD					
Gain Error (Note 3)					±1	LSB					
Gain Temperature Coefficient				±0.8		ppm/°C					
Total Lipsdiveted Error	THE	$T_A = +25^{\circ}C$			±1						
Total Onadjusted Error	IUE	$T_A = T_{MIN}$ to T_{MAX}		±0.5		LOD					
Channel-to-Channel Offset Matching				±0.1		LSB					
V _{DD} / 2 Sampling Accuracy				50		mV					
DYNAMIC PERFORMANCE (10)	kHz sine-wa	ve input, 2.048Vp-p, 50ksps, 500kHz external clc	ock)								
Signal-to-Noise Plus Distortion	SINAD			49		dB					
Total Harmonic Distortion (up to the 5th harmonic)	THD			-70		dB					
Spurious-Free Dynamic Range	SFDR			68		dB					
Small-Signal Bandwidth	BW-3dB	-3dB rolloff		1.5		MHz					
Full-Power Bandwidth				0.8		MHz					
ANALOG INPUTS											
		Unipolar input, V _{COM} = 0	0		VREF						
Input Voltage Range (Note 4)	V _{CH} _	Bipolar input, V_{COM} or $V_{CH1} = V_{REF} / 2$, referenced to COM or CH1		±	VREF / 2	V					
Multiplexer Leakage Current		On/off-leakage current, VCOM or VCH = 0 or VDD		±0.01	±1	μA					
Input Capacitance	CIN			18		pF					

ELECTRICAL CHARACTERISTICS—MAX1108 (continued)

 $(V_{DD} = +2.7V \text{ to } +3.6V; \text{ unipolar input mode; COM} = GND, f_{SCLK} = 500 \text{kHz}$, external clock mode (50% duty cycle); 10 clocks/conversion cycle (50ksps); 1µF capacitor at REF, external +2.048V reference at REF; T_A = T_{MIN} to T_{MAX}; unless otherwise noted. Typical values are at T_A = +25°C.)

PARAMETER	SYMBOL	CONE	ITIONS	MIN	ТҮР	MAX	UNITS
TRACK/HOLD							
		Internal clock				35	
Conversion Time (Note 5)	CONV	External clock, 500kHz	z, 10 sclks/conv	20			μs
Track/Hold Acquisition Time	tacq	External clock, 2MHz		1			μs
Aperture Delay					10		ns
Aperture Jitter					<50		ps
Internal Clock Frequency					400		kHz
External Clock Fraguency Panga				50		500	kHz
External Clock Frequency hange		For data transfer only				2	MHz
INTERNAL REFERENCE							
Output Voltage	VREF			1.968	2.048	2.128	V
REF Short-Circuit Current	IREFSC	(Note 6)			150		μA
REF Tempco					±50		ppm/°C
Load Regulation		0 to 0.5mA (Note 7)			2.5		mV
Capacitive Bypass at REF				1			μF
EXTERNAL REFERENCE							
Input Voltage Range				1.0	VD	D + 0.05	V
Input Current		+2.048V at REF, full sc 500kHz external clock	ale,		1	20	μA
POWER REQUIREMENTS							1
Supply Voltage	V _{DD}			2.7	3	5.5	V
		$V_{DD} = 2.7V$ to 3.6V,	Internal reference		105	250	
		$C_L = 10 pF$	External reference		70		
Supply Current (Notes 2, 8)	IDD	V _{DD} = 5.5V,	Internal reference		130		μA
		$C_L = 10 pF$	External reference		95		
		Power down, $V_{DD} = 2$.	7V to 3.6V (Note 9)		0.5	2.5	
Power-Supply Rejection (Note 10)	PSR	Full-scale input, V _{DD} =	2.7V to 3.6V		±0.4	±4	mV
DIGITAL INPUTS (DIN, SCLK, ar	nd <u>CS</u>)						
Threshold Voltage High	Vii i	$V_{DD} \le 3.6V$				2	V
Theshold voltage high	VIH	V _{DD} > 3.6V				3	V
Threshold Voltage Low	VIL			0.8			V
Input Hysteresis	VHYST				0.2		V
Input Current High	Ін					±1	μA
Input Current Low	١ _١ ٢					±1	μA
Input Capacitance	CIN				15		pF



ELECTRICAL CHARACTERISTICS—MAX1108 (continued)

 $(V_{DD} = +2.7V \text{ to } +3.6V; \text{ unipolar input mode; COM} = GND, f_{SCLK} = 500 \text{kHz}, external clock mode (50% duty cycle); 10 clocks/conversion cycle (50 ksps); 1µF capacitor at REF, external +2.048V reference at REF; T_A = T_{MIN} to T_{MAX}; unless otherwise noted. Typical values are at T_A = +25°C.)$

PARAMETER	SYMBOL	CONDITIONS	MIN	ΤΥΡ	MAX	UNITS			
DIGITAL OUTPUT (DOUT)									
Output High Voltage	Voh	I _{SOURCE} = 0.5mA	V _{DD} - 0.5			V			
	Voi	I _{SINK} = 5mA			0.4	V			
Output Low Voltage	VOL	ISINK = 16mA		0.8		V			
Three-State Leakage Current	١L	$\overline{\text{CS}} = \text{V}_{\text{DD}}$		±0.01	±10	μA			
Three-State Output Capacitance	Соит	$\overline{\text{CS}} = \text{V}_{\text{DD}}$		15		pF			
TIMING CHARACTERISTICS (Fig	gures 8, 9, a	and 10)							
Acquisition Time	tacq		1.0			μs			
DIN to SCLK Setup Time	tDS		100			ns			
DIN to SCLK Hold Time	tDH		0			ns			
SCLK Fall to Output Data Valid	tDO	Figure 1, C _{LOAD} = 100pF	20		200	ns			
CS Fall to Output Enable	tDV	Figure 1, C _{LOAD} = 100pF			240	ns			
CS Rise to Output Disable	t _{TR}	Figure 2, C _{LOAD} = 100pF			240	ns			
CS to SCLK Rise Setup	tcss		100			ns			
CS to SCLK Rise Hold	tCSH		0			ns			
SCLK Pulse Width High	tсн		200			ns			
SCLK Pulse Width Low	tCL		200			ns			
Waka Lip Tima	1 1111	External reference		20		μs			
Wake-Op Time	IVVAKE	Internal reference (Note 11)		12		ms			

ELECTRICAL CHARACTERISTICS—MAX1109

 $(V_{DD} = +4.5V \text{ to } +5.5V; \text{ unipolar input mode}; \text{COM} = \text{GND}, \text{f}_{SCLK} = 500\text{kHz}$, external clock (50% duty cycle); 10 clocks/conversion cycle (50ksps); 1µF capacitor at REF, external +4.096V reference at REF; TA = T_{MIN} to T_{MAX}; unless otherwise noted. Typical values are at T_A = +25^{\circ}\text{C}.)

PARAMETER	SYMBOL	CONDITIONS	MIN	ТҮР	MAX	UNITS
DC ACCURACY						
Resolution			8			bits
Relative Accuracy (Note 1)	INL	V _{DD} = 4.5V to 5.5V		±0.15	±0.5	LSB
Differential Nonlinearity	DNL	No missing codes over temperature			±1	LSB
Offset Error		V _{DD} = 4.5V to 5.5V		±0.2	±1	LSB
Gain Error (Note 3)					±1	LSB
Gain Temperature Coefficient				±0.8		ppm/°C
Total Lipadiustod Error	THE	$T_A = +25^{\circ}C$			±1	ICR
Total Orladjusted Error	TUL	TA = TMIN to TMAX		±0.5		LOD
Channel-to-Channel Offset Matching				±0.1		LSB
V _{DD} / 2 Sampling Accuracy				50		mV

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ELECTRICAL CHARACTERISTICS—MAX1109 (continued)

 $(V_{DD} = +4.5V \text{ to } +5.5V; \text{ unipolar input mode; COM} = GND, f_{SCLK} = 500\text{kHz}$, external clock (50% duty cycle); 10 clocks/conversion cycle (50ksps); 1µF capacitor at REF, external +4.096V reference at REF; T_A = T_{MIN} to T_{MAX}; unless otherwise noted. Typical values are at T_A = +25°C.)

PARAMETER	SYMBOL	CONDITIONS	MIN	ТҮР	MAX	UNITS
DYNAMIC PERFORMANCE (10k	Hz sine-wa	ve input, 4.096Vp-p, 50ksps, 500kHz external clo	ock)			
Signal-to-Noise Plus Distortion	SINAD			49		dB
Total Harmonic Distortion (up to the 5th harmonic)	THD			-70		dB
Spurious Free Dynamic Range	SFDR			68		dB
Small-Signal Bandwidth	BW-3dB	-3dB rolloff		1.5		MHz
Full-Power Bandwidth				0.8		MHz
ANALOG INPUTS		-	-1			
		Unipolar input, V _{COM} = 0	0		VREF	
Input Voltage Range (Note 4)	V _{CH} _	Bipolar input, V_{COM} or $V_{CH1} = V_{REF} / 2$, referenced to COM or CH1		:	±V _{REF} / 2	V
Multiplexer Leakage Current		On/off-leakage current, V _{CH} = 0 or V _{DD}		±0.01	±1	μA
Input Capacitance	CIN			18		рF
TRACK/HOLD						
	toouur	Internal clock			35	
Conversion Time (Note 5)	CONV	External clock, 500kHz, 10 sclks/conv	20			μs
Track/Hold Acquisition Time	tacq	External clock, 2MHz	1			μs
Aperture Delay				10		ns
Aperture Jitter				<50		ps
Internal Clock Frequency				400		kHz
External Clock Frequency Bange			50		500	kHz
External Clock Frequency hange		For data transfer only			2	MHz
INTERNAL REFERENCE						
Output Voltage	VREF		3.936	4.096	4.256	V
REF Short-Circuit Current	IREFSC			5		mA
REF Tempco		0 to 0.5mA (Note 7)		±50		ppm/°C
Load Regulation				2.5		mV
Capacitive Bypass at REF			1			μF
EXTERNAL REFERENCE						
Input Voltage Range			1.0	V	D + 0.05	V
Input Current		+4.096V at REF, full scale, 500kHz external clock		1	20	μA

ELECTRICAL CHARACTERISTICS—MAX1109 (continued)

 $(V_{DD} = +4.5V \text{ to } +5.5V; \text{ unipolar input mode; COM} = GND, f_{SCLK} = 500 \text{kHz}$, external clock (50% duty cycle); 10 clocks/conversion cycle (50ksps); 1µF capacitor at REF, external +4.096V reference at REF; T_A = T_{MIN} to T_{MAX}; unless otherwise noted. Typical values are at T_A = +25°C.)

PARAMETER	SYMBOL	COND	ITIONS	MIN	ТҮР	MAX	UNITS
POWER REQUIREMENTS	1						
Supply Voltage	V _{DD}			4.5	5	5.5	V
		$V_{DD} = 4.5V \text{ to } 5.5V,$	Internal reference		130	250	
Supply Current (Notes 2, 8)	IDD	full-scale input	External reference		95		μA
		Power down, $V_{DD} = 4.5$	5V to 5.5V (Note 9)		0.5	2.5	
Power-Supply Rejection (Note 10)	PSR	External reference = +4 full-scale input, V _{DD} = 4	4.096V, 4.5V to 5.5V		±0.4	±4	mV
DIGITAL INPUTS (DIN, SCLK, ar	nd CS)						
Threshold Voltage High	VIH					3	V
Threshold Voltage Low	VIL			0.8			V
Input Hysteresis	VHYST				0.2		V
Input Current High	Iн					±1	μA
Input Current Low	Ι _Ι Γ					±1	μA
Input Capacitance	CIN				15		pF
DIGITAL OUTPUT (DOUT)							
Output High Voltage	Voh	ISOURCE = 0.5mA		V _{DD} - 0.5			V
Output Low Voltage	Vo	ISINK = 5mA				0.4	V
Oulput Low Voltage	VOL	ISINK = 16mA			0.8		v
Three-State Leakage Current	١L	$\overline{\text{CS}} = \text{V}_{\text{DD}}$			±0.01	±10	μΑ
Three-State Output Capacitance	Cout	$\overline{\text{CS}} = \text{V}_{\text{DD}}$			15		рF
TIMING CHARACTERISTICS (Fig	gures 8, 9, a	and 10)					
Acquisition Time	tacq			1.0			μs
DIN to SCLK Setup Time	tDS			100			ns
DIN to SCLK Hold Time	tDH			0			ns
SCLK Fall to Output Data Valid	tDO	Figure 1, $C_{LOAD} = 100$	pF	20		200	ns
CS Fall to Output Enable	t _{DV}	Figure 1, $C_{LOAD} = 100$	pF			240	ns
CS Rise to Output Disable	t _{TR}	Figure 2, $C_{LOAD} = 100$	pF			240	ns

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ELECTRICAL CHARACTERISTICS—MAX1109 (continued)

 $(V_{DD} = +4.5V \text{ to } +5.5V; \text{ unipolar input mode}; COM = GND, f_{SCLK} = 500 \text{kHz}$, external clock (50% duty cycle); 10 clocks/conversion cycle (50ksps); 1µF capacitor at REF, external +4.096V reference at REF; T_A = T_{MIN} to T_{MAX}; unless otherwise noted. Typical values are at T_A = +25°C.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
CS to SCLK Rise Setup	tcss		100			ns
CS to SCLK Rise Hold	tCSH		0			ns
SCLK Pulse Width High	tСН		200			ns
SCLK Pulse Width Low	tCL		200			ns
Waka Up Timo	there is a	External reference		20		μs
Wake-op Time	WAKE	Internal reference (Note 11)		12		ms

Note 1: Relative accuracy is the deviation of the analog value at any code from its theoretical value after the full-scale range has been calibrated.

Note 2: See Typical Operating Characteristics.

Note 3: V_{REF} = +2.048V (MAX1108), V_{REF} = +4.096V (MAX1109), offset nulled.

Note 4: Common-mode range (CH0, CH1, COM) GND to VDD.

Note 5: Conversion time defined as the number of clock cycles times the clock period; clock has 50% duty cycle (Figures 6 and 8).

Note 6: REF supplies typically 2.5mA under normal operating conditions.

Note 7: External load should not change during the conversion for specified accuracy.

Note 8: Power consumption with CMOS levels.

Note 9: Power-down test performed using the following sequence 1) \overline{SHDN} 5bit = 0 in the configuration register; 2) Wait for 10 SCLK cycles to complete current conversion; 3) Measure shutdown current with \overline{CS} , SCLK, D_{IN} = V_{DD} or GND.

Note 10: Measured as | V_{FS}(2.7V) - V_{FS}(3.6V) | for MAX1108, and measured as | V_{FS}(4.5V) - V_{FS}(5.5V) | for MAX1109.

Note 11: 1µF at REF, internal reference settling to 0.5LSB.

Typical Operating Characteristics

 $(V_{DD} = +3.0V \text{ (MAX1108)}, V_{DD} = +5.0V \text{ (MAX1109)}; external conversion mode; f_{SCLK} = 500kHz; 50ksps; external reference; 1µF at REF; T_A = +25°C; unless otherwise noted.)$



Typical Operating Characteristics (continued)

(VDD = +3.0V (MAX1108), VDD = +5.0V (MAX1109); external conversion mode; $f_{SCLK} = 500$ kHz; 50ksps; external reference; 1µF at REF; $T_A = +25^{\circ}$ C; unless otherwise noted.)



MAX1108/MAX1109

Typical Operating Characteristics (continued)



$(V_{DD} = +3.0V (MAX1108), V_{DD} = +5.0V (MAX1109);$ external conversion mode; f_{SCLK} = 500kHz; 50ksps; external reference; 1µF at REF; T_A = +25°C; unless otherwise noted.)

PIN	NAME	FUNCTION
1	Vdd	Positive Supply Voltage
2, 3	CH0, CH1	Sampling Analog Inputs
4	GND	Ground
5	REF	Reference voltage for analog-to-digital conversion (internal or external reference). Reference input for external reference. Bypass internal reference with 1µF capacitor to GND.
6	СОМ	Common reference for analog inputs. Sets zero-code voltage in single-ended mode. Must be stable to ±0.5LSB during conversion.
7	CS	Active-Low Chip Select. Data is not clocked into DIN unless \overline{CS} is low. When \overline{CS} is high, DOUT is high impedance.
8	DIN	Serial Data Input. Data is clocked in at the rising edge of SCLK.
9	DOUT	Serial Data Output. Data is clocked out on the falling edge of SCLK. High impedance when $\overline{\text{CS}}$ is high.
10	SCLK	Serial Clock Input. Clocks data in and out of serial interface. In external clock mode, SCLK also sets the conversion speed.





Figure 1. Load Circuits for Enable Time

Detailed Description

The MAX1108/MAX1109 analog-to-digital converters (ADCs) use a successive-approximation conversion technique and input track/hold (T/H) circuitry to convert an analog signal to an 8-bit digital output. A flexible serial interface provides easy interface to microprocessors (μ Ps). No external hold capacitors are required. All of the MAX1108/MAX1109 operating modes are software-configurable: internal or external reference, internal or external conversion clock, single-ended unipolar or pseudo-differential unipolar/bipolar conversion, and power down (Table 1).

Analog Inputs

Track/Hold

The input architecture of the ADCs is illustrated in the equivalent-input circuit of Figure 4 and is composed of the T/H, the input multiplexer, the input comparator, the switched capacitor DAC, the reference, and the auto-zero rail.

The analog-inputs configuration is determined by the control-byte through the serial interface as shown in Table 2 (see *Modes of Operation* section and Table 1). The eight modes of operation include single-ended, pseudo-differential, unipolar/bipolar, and a VDD monitoring mode. During acquisition and conversion, only one of the switches in Figure 4 is closed at any time.

The T/H enters its tracking mode on the falling clock edge after bit 4 (SEL0) of the control byte has been shifted in. It enters its hold mode on the falling edge after the bit 2 (I/EREF) of the control byte has been shifted in.

For example, If CH0 and COM are chosen (SEL2 = SEL1 = SEL0 = 1) for conversion, CH0 is defined as the sampled input (SI), and COM is defined as the reference input (RI). During acquisition mode, the CH0 switch and the T/H switch are closed, charging the



Figure 2. Load Circuits for Disable Time



Figure 3. Typical Operating Circuit



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Figure 4. Equivalent Input Circuit

holding capacitor CHOLD through RIN. At the end of acquisition the T/H switch opens and CHOLD is connected to COM, retaining charge on CHOLD as a sample of the signal at CHO, and the difference between CHO and COM is the converted signal. Once conversion is complete, the T/H returns immediately to its tracking mode. This procedure holds for the different combinations summarized in Table 2.

The time available for the T/H to acquire an input signal (t_{ACQ}) is determined by the clock frequency, and is 1µs at the maximum clock frequency of 2MHz. The acquisition time is also the minimum time needed for the signal to be acquired. It is calculated by:

$t_{ACQ} = 6(R_S + R_{IN})18pF$

where $R_{IN} = 6.5 k\Omega$, $R_S =$ the source impedance of the input signal, and tACQ is never less than 1µs. Note that source impedances below 2.7k Ω do not significantly affect the AC performance of the ADC at the maximum clock speed. If the input-source impedance is higher than 3k Ω , the clock speed must be reduced accordingly.

Pseudo-Differential Input

The MAX1108/MAX1109 input configuration is pseudodifferential to the extent that only the signal at the sampled input (SI) is stored in the holding capacitor (C_{HOLD}). The reference input (RI) must remain stable within ± 0.5 LSB (± 0.1 LSB for best results) in relation to GND during a conversion. Sampled input and reference input configuration is determined by bit6-bit4 (SEL2-SEL0) of the control byte (Table 2).

If a varying signal is applied at the selected reference input, its amplitude and frequency need to be limited. The following equations determine the relationship between the maximum signal amplitude and its frequency to maintain ± 0.5 LSB accuracy:

Assuming a sinusoidal signal at the reference input

$$v_{\rm RI} = V_{\rm RI} \sin(2\pi ft)$$

the maximum voltage variation is determined by:

$$\max \frac{dv_{RI}}{dt} = 2\pi f \cdot v_{RI} \le \frac{1 \text{ LSB}}{t_{CONV}} = \frac{V_{REF}}{2^8 t_{CONV}}$$

a 60Hz signal at RI with an amplitude of 1.2V will generate a ± 0.5 LSB of error. This is with a 35µs conversion time (maximum t_{CONV} in internal conversion mode) and a reference voltage of ± 4.096 V. When a DC reference voltage is used at RI, connect a 0.1µF capacitor to GND to minimize noise at the input. The input configuration selection also determines unipolar or bipolar conversion mode. The commonmode input range of CH0, CH1, and COM is 0 to +V_{DD}. In unipolar mode, full scale is achieved when (SI - RI) = V_{REF}; in bipolar mode, full scale is achieved when $|(SI - RI)| = V_{REF} / 2$. In unipolar mode, SI must be higher than RI; in bipolar mode, SI can span above and below RI provided that it is within the common-mode range.

Conversion Process

The comparator negative input is connected to the autozero rail. Since the device requires only a single supply, the ZERO node at the input of the comparator equals V_{DD}/2. The capacitive DAC restores node ZERO to have 0V difference at the comparator inputs within the limits of 8-bit resolution. This action is equivalent to transferring a charge of 18pF(V_{IN+} - V_{IN-}) from C_{HOLD} to the binary-weighted capacitive DAC which, in turn, forms a digital representation of the analog-input signal.

Input Voltage Range

Internal protection diodes that clamp the analog input to V_{DD} and AGND allow the channel input pins (CH0, CH1, and COM) to swing from (AGND - 0.3V) to (V_{DD} + 0.3V) without damage. However, for accurate conversions, the inputs must not exceed (V_{DD} + 50mV) or be less than (GND - 50mV).

If the analog input voltage on an "off" channel exceeds 50mV beyond the supplies, the current should be limited to 2mA to maintain conversion accuracy on the "on" channel.

The MAX1108/MAX1109 input range is from 0 to V_{DD}; unipolar or bipolar conversion is available. In unipolar mode, the output code is invalid (code zero) when a negative input voltage (or a negative differential input voltage) is applied. The reference input-voltage range at REF is from 1V to (V_{DD} + 50mV.)

Input Bandwidth

The ADC's input tracking circuitry has a 1.5MHz smallsignal bandwidth, so it is possible to digitize highspeed transient events and measure periodic signals with bandwidths exceeding the ADC's sampling rate by using undersampling techniques. To avoid high-frequency signals being aliased into the frequency band of interest, anti-alias filtering is recommended.

Serial Interface

The MAX1108/MAX1109 have a 4-wire serial interface. The \overline{CS} , DIN, and SCLK inputs are used to control the device, while the three-state DOUT pin is used to access the result of conversion.

M/X/W

601 IXTURE 601 IXTURE 6

Single-Supply, Low-Power, 2-Channel, Serial 8-Bit ADCs

The serial interface provides easy connection to microcontrollers with SPI, QSPI and MICROWIRE serial interfaces at clock rates up to 2MHz. For SPI and QSPI, set CPOL = CPHA = 0 in the SPI control registers of the microcontroller. Figure 5 shows the MAX1108/MAX1109 common serial-interface connections.

Digital Inputs

The logic levels of the MAX1108/MAX1109 digital input are set to accept voltage levels from both +3V and +5V systems, regardless of the supply voltages. Input data (control byte) is clocked in at the DIN pin on the rising edge of serial clock (SCLK). CS is the standard chipselect signal which enables communication with the device. SCLK is used to clock data in and out of serial interface. In external clock mode, SCLK also sets the conversion speed.

Digital Output Output data is read on the rising edge of SCLK at DOUT, MSB first (D7). In unipolar input mode, the output is straight binary. For bipolar input mode, the output is twos-complement (see *Transfer Function* section).



Figure 5. Common Serial-Interface Connections

DOUT is active when \overline{CS} is low and high impedance when \overline{CS} is high. DOUT does not accept external voltages greater than V_{DD}. In external-clock mode, data is clocked out at the maximum clock rate of 500kHz while conversion is in progress. In internal-clock mode, data can be clocked out at up to 2MHz clock rate.

Modes of Operation

The MAX1108/MAX1109 feature single-ended or pseudo-differential operation in unipolar or bipolar configuration. The device is programmed through the input control-byte at the DIN pin of the serial interface (Table 1). Table 2 shows the analog-input configuration and Table 3 shows the input-voltage ranges in unipolar and bipolar configuration.

How to Start a Conversion

A conversion is started by clocking a control byte into DIN. With \overline{CS} low, each rising edge on SCLK clocks a bit from DIN into the MAX1108/MAX1109's internal shift register. After \overline{CS} falls, the first arriving logic "1" bit at DIN defines the MSB of the control byte. Until this first start bit arrives, any number of logic "0" bits can be clocked into DIN with no effect. Table 1 shows the control-byte format.

Using the *Typical Operating Circuit* (Figure 3), the simplest software interface requires two 8-bit transfers to perform a conversion (one 8-bit transfer to configure the ADC, and one 8-bit transfer to clock out the 8-bit conversion result). Figure 6 shows a single-conversion timing diagram using external clock mode.

Clock Modes

The MAX1108/MAX1109 can use either an external serial clock or the internal clock to perform the successiveapproximation conversion. In both clock modes, the external clock shifts data in and out of the devices. Bit 3 of control-byte (I/ECLK) programs the clock mode. Figure 8 shows the timing characteristics common to both modes.

External Clock

In external clock mode, the external clock not only shifts data in and out, it also drives the analog-to-digital conversion steps. In this mode the clock frequency must be between 50kHz and 500kHz. Single-conversion timing using an external clock begins with a falling edge on CS. When this occurs, DOUT leaves the high impedance state and goes low. The first "1" clocked into DIN by SCLK after CS is set low is considered as the start bit. The next seven clocks latch in the rest of the control byte. On the falling edge of the fourth clock, track mode is enabled, and on the falling edge of the sixth clock, acquisition is complete and conversion is



BIT 7 (MSB)	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0 (LSB)		
START	SEL2	SEL1	SEL0	I/ECLK	I/EREF	REFSHDN	SHDN		
BIT	NAME	IE DESCRIPTION							
7 (MSB)	START	The first logic "	1" bit after $\overline{\text{CS}}$ go	pes low defines th	e beginning of t	he control byte.			
6 5 4	SEL2 SEL1 SEL0	Selects the mo	Selects the mode of operation (Table 2).						
3	I/ECLK	1 = external clo SCLK signal.	ock, 0 = internal	clock. The SAR ca	an be driven by	the internal oscillat	or, or with the		
2	I/EREF	1 = internal refe +4.096V (MAX	erence, 0 = exte 1109), or an exte	rnal reference. Int rnal reference ca	ernal reference n be applied to t	selects +2.048V (N he REF pin.	1AX1108) or		
1	REFSHDN	1 = operational consumption ca REFSHDN mus	1 = operational (if I / EREF = 1), 0 = reference shutdown. When using an external reference, powe consumption can be minimized by powering down the internal reference separately (I / EREF = 0) $\overline{\text{REFSHDN}}$ must be set to 0 when $\overline{\text{SHDN}}$ = 0.						
0 (LSB)	SHDN	1 = operational, 0 = power down. For a full power down set $\overline{\text{REFSHDN}} = \overline{\text{SHDN}} = 0$. (See <i>Power-Down Mode</i> section.)							

Table 1. Control Byte Format

Table 2. Conversion Configuration

SEL2	SEL1	SEL0	SAMPLED INPUT (SI)	REFERENCE INPUT (RI)	CONVERSION MODE
1	1	1	CH0	COM	Unipolar
1	1	0	CH1	СОМ	Unipolar
1	0	1	CHO	GND	Unipolar
1	0	0	CH1	GND	Unipolar
0	1	1	CHO	СОМ	Bipolar
0	1	0	CH1	СОМ	Bipolar
0	0	1	CHO	CH1	Bipolar
0	0	0	V _{DD} / 2	GND	Unipolar

Table 3. Full- and Zero-Scale Voltages

UNIPOLAR MODE		BIPOLAR MODE		
Zero Scale	Full Scale	Negative Full Scale	Zero Scale	Positive Full Scale
RI*	RI + V _{REF}	RI - V _{REF} / 2	RI	RI + V _{REF} / 2

*RI = Reference Input (Table 2)

initiated. The MSB successive-approximation bit decision is made on the rising edge of the seventh SCLK. On the falling edge of the eighth SCLK, the MSB is clocked out on the DOUT pin; on each of the next seven SCLK falling edges, the remaining bits of conversion are clocked out. Zeros are clocked out on DOUT after the LSB has been clocked out, until $\overline{\text{CS}}$ is disabled. Then DOUT becomes high impedance and the part is ready for another conversion (Figure 6).

The conversion must complete in 1ms, or droop on the sample-and-hold capacitors may degrade conversion results. Use internal clock mode if the serial-clock frequency is less than 50kHz, or if serial-clock interruptions could cause the conversion interval to exceed 1ms.

Internal Clock

Internal clock mode frees the μ P from the burden of running the SAR conversion clock. This allows the conversion results to be read back at the processor's convenience, at any clock rate up to 2MHz.

An internal register stores data when the conversion is in progress. On the falling edge of the fourth SCLK, track mode is enabled, and on the falling edge of the eighth SCLK, acquisition is complete and internal conversion is initiated. The internal 400kHz clock completes the conversion in 20µs typically (35µs max), at which time the MSB of the conversion is present at the DOUT pin. The falling edge of SCLK clocks the remaining data out of this register at any time after the conversion is complete (Figure 8).



Figure 6. Single Conversion Timing, External Clock Mode



Figure 7. Detailed Serial-Interface Timing

 $\overline{\text{CS}}$ does not need to be held low once a conversion is started. Pulling $\overline{\text{CS}}$ high prevents data from being clocked into the MAX1108/MAX1109 and three-states DOUT, but it does not adversely affect an internal clock-mode conversion already in progress. In this mode, data can be shifted in and out of the MAX1108/MAX1109 at clock rates up to 2MHz, provided that the minimum acquisition time (t_{ACQ}) is kept above 1µs.

Quick Look

To quickly evaluate the MAX1108/MAX1109's analog performance, use the circuit of Figure 9. The device requires a control byte to be written to DIN before each conversion. Tying CS to GND and DIN to V_{DD} feeds in control bytes of FFH. In turn, this triggers single-ended, unipolar conversions on CH0 in relation to COM in external clock mode without powering down between conversions. Apply an external 50kHz to 500kHz clock



Figure 8. Single Conversion Timing, Internal Clock Mode



Figure 9. Quick-Look Schematic

to the SCLK pin; varying the analog input alters the result of conversion that is clocked out at the DOUT pin. A total of 10 clock cycles is required per conversion.

Data Framing

The falling edge of $\overline{\text{CS}}$ does not start a conversion. The first logic high clocked into DIN is interpreted as a start bit and defines the first bit of the control byte. Acquisition starts on the falling edge of the fourth SCLK and lasts for two SCLKs in external clock mode or four SCLKs in internal clock mode. Conversion starts immediately after acquisition is completed. The start bit is defined as:

The first high bit clocked into DIN with \overline{CS} low any time the converter is idle; e.g., after V_{DD} is applied.

OR

In external clock mode, the first high bit clocked into DIN after the bit 5 (D5) of a conversion in progress is clocked onto the DOUT pin.

OR

In internal clock mode, the first high bit clocked into DIN after the bit 4 (D4) is clocked onto the DOUT pin.

The MAX1108/MAX1109 can run at a maximum speed of 10 clocks per conversion. Figure 10 shows the serialinterface timing necessary to perform a conversion every 10 SCLK cycles in external clock mode.

Many microcontrollers require that conversions occur in multiples of 8 SCLK clocks; 16 clocks per conversion is typically the fastest that a microcontroller can drive the MAX1108/MAX1109. Figure 11 shows the serial-interface timing necessary to perform a conversion every 16 SCLK cycles in external clock mode.

///XI//



Figure 10. Continuous Conversion, External Clock Mode, 10 Clocks/Conversion Timing



Figure 11. Continuous Conversion, External Clock Mode, 16 Clocks/Conversion Timing

16

In external clock mode, if \overline{CS} is toggled before the current conversion is complete, the current conversion is terminated, and the next high bit clocked into DIN is recognized as a new start bit. This can be useful in extending acquisition time by selecting conversion on the same channel with the second control byte (doubleclocking mode), effectively extending acquisition to 6 SCLKs. This technique is ideal if the analog input source has high impedance, or if it requires more than 1µs to settle; it can also be used to allow the device and the reference to settle when using power downmodes (see *Power-Down Modes* section).

___Applications Information

Battery Monitoring Mode

This mode of operation samples and converts the midsupply voltage, V_{DD} / 2, which is internally generated. Set SEL2 = SEL1 = SEL0 = 0 in the control byte to select this configuration. This allows the user to monitor the condition of a battery providing V_{DD}. The reference voltage must be larger than V_{DD} / 2 for this mode of operation to work properly. From the result of conversion (CODE), V_{DD} is determined as follows: V_{DD} = CODE · V_{REF} / 128.

Power-On Configuration

When power is first applied, the MAX1108/MAX1109's reference is powered down and SHDN is not enabled. The device needs to be configured by setting \overline{CS} low and writing the control byte. Conversion can be started within 20µs if an external reference is used. When using the internal reference, allow 12ms for the reference to settle. This is done by first performing a configuration conversion to power up the reference and then performing a second conversion once the reference is settled. No conversions should be considered correct until the reference voltage (internal or external) has stabilized.

Power-Down Modes

To save power, place the converter into low-current power-down mode between conversions. Minimum power consumption is achieved by programming REFSHDN = 0 and $\overline{SHDN} = 0$ in the input control byte (Table 4). When software power-down is asserted, it becomes effective only after the conversion. If the control byte contains REFSHDN = 0, then the reference will turn off at the end of conversion. If $\overline{SHDN} = 0$, then the chip will power-down at the end of conversion (in this mode I/EREF or REFSHDN should also be set to zero). Table 4 lists the power-down modes of the MAX1108/MAX1109.

Table 4. Power-Down Modes of theMAX1108/MAX1109

BIT 2–BIT 0 OF CONTROL BYTE			OPERATING MODE	
I/EREF	REFSHDN	SHDN		
1	1	1	Device Active/Internal Reference Active	
1	0	1	Device Active; Internal refer- ence powered down after con- version, powered up at next start bit.	
0	Х	1	Device Active/External Reference Mode	
1	0	0	Device and internal reference powered down after conversion, powered up at next start bit.	
0	Х	0	Device powered down after each conversion, powered up at next start bit. External Reference Mode.	
1	1	0	Reserved. Do not use.	

X = Don't care

The first logical 1 clocked into DIN after \overline{CS} falls powers up the MAX1108/MAX1109 (20µs required for the device to power up). The reference is powered up only if internal reference was selected during the previous conversion. When the reference is powered up after being disabled, consider the settling time before using the result of conversion. Typically, 12ms are required for the reference to settle from a discharge state; less time may be considered if the external capacitor is not discharged completely when exiting shutdown. In all power-down modes, the interface remains active and conversion results may be read. Use the double clocking technique described in the *Data Framing* section to allow more time for the reference to settle before starting a conversion after short power-down.

Voltage Reference

The MAX1108/MAX1109 operate from a single supply and feature a software-controlled internal reference of +2.048V (MAX1108) and +4.096V (MAX1109). The device can operate with either the internal reference or an external reference applied at the REF pin. See the *Power-Down Modes* and *Modes of Operation* sections for detailed instructions on reference configuration.

The reference voltage determines the full-scale range: in unipolar mode, the input range is from 0 to V_{REF}; in bipolar mode, the input range spans RI \pm V_{REF} / 2 with RI = V_{REF} / 2.

External Reference

To use an external reference, set bit 2 (I/EREF) and bit 1 (REFSHDN) of control byte to 0 and connect the external reference (VREF between 1V and VDD) directly at the REF pin. The DC input impedance at REF is extremely high, consisting of leakage current only (typically 10nA). During a conversion, the reference must be able to deliver up to 20 μ A average load current and have an output impedance of 1k Ω or less at the conversion clock frequency. If the reference has higher output impedance or is noisy, bypass it close to the REF pin with a 0.1 μ F capacitor. MAX1109 has an internal reference of +4.096V. To use the device with supply voltages below 4.5V, external reference mode is required.

With an external reference voltage of less than +2.048V (MAX1108) or +4.096V (MAX1109) at REF, the increase in the ratio of the RMS noise to the LSB value (FS / 256) results in performance degradation and decreased dynamic range.

Internal Reference To use the internal reference, set bit 2 (I/EREF) and bit 1 (REFSHDN) of the control byte to 1 and bypass REF with a 1µF capacitor to ground. The internal reference can be powered down after a conversion by setting bit 1 (REF-SHDN) of the control byte to 0. When using the internal reference, use MAX1108 and MAX1109 with supply voltage below 4.5V and above 4.5V, respectively.

Transfer Function

Table 4 shows the full-scale voltage ranges for unipolar and bipolar modes. Figure 12a depicts the nominal, unipolar I/O transfer function, and Figure 12b shows the bipolar I/O transfer function. The zero scale is determined by the input selection setting and is either COM, GND, or CH1.

Code transitions occur at integer LSB values. Output coding is straight binary for unipolar operation and two's complement for bipolar operation. With a +2.048V reference, $1LSB = 8mV (V_{REF} / 256)$.

Layout, Grounding, and Bypassing

For best performance, use printed circuit boards. Wirewrap boards are not recommended. Board layout should ensure that digital and analog signal lines are separated from each other. Do not run analog and digital (especially clock) lines parallel to one another or run digital lines underneath the ADC package.

Figure 13 shows the recommended system-ground connections. A single-point analog ground (star-ground point) should be established at the A/D ground. Connect all analog grounds to the star ground. No digital-system ground should be connected to this point.



Figure 12a. Unipolar Transfer Function



Figure 12b. Bipolar Transfer Function

The ground return to the power supply for the star ground should be low impedance and as short as possible for noise-free operation.

High-frequency noise in the V_{DD} power supply may affect the comparator in the ADC. Bypass the supply to the star ground with 0.1µF and 1µF capacitors close to the V_{DD} pin of the MAX1108/MAX1109. Minimize capacitor lead lengths for best supply-noise rejection. If the power supply is very noisy, a 10 Ω resistor can be connected to form a lowpass filter.





Figure 13. Power-Supply Connections

Chip Information

TRANSISTOR COUNT: 2373

Package Information

10LUMAX.EPS

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information, go to **www.maxim-ic.com/packages**.

— 4X S MILLIMETERS INCHES DIM MIN MAX MIN MAX 0.043 1.10 А A1 0.002 0.006 0.05 0.15 A2 0.030 0.95 0.037 0.75 D1 0.116 0.120 2.95 3.05 0.114 2 89 D2 0.118 3 00 E1 0.116 0.120 2.95 3.05 0.50±0.1 E2 0.114 0.118 2.89 3.00 Н 0.187 0.199 4.75 5.05 0.6 ± 0.1 L 0.0157 0.0275 0.40 0.70 ł L1 0.037 REF 0.940 REF b 0.007 0.0106 0.177 0.270 е 0.0197 BSC 0.500 BSC 0.6+0.1 С 0.0035 0.0078 0.090 0.200 BOTTOM VIEW 0.498 REF S 0.0196 REF TOP VIEW α 0∞ 6∞ 0∞ 6∞ D2 E2 GAGE PLANE A2 -lb D1 FRONT VIEW SIDE VIEW NOTES: PROPRIETARY INFORMATION 1. D&E DO NOT INCLUDE MOLD FLASH. MOLD FLASH OR PROTRUSIONS NOT TO EXCEED 0.15mm (.006"). CONTROLLING DIMENSION: MILLIMETERS. 2. 3. PACKAGE OUTLINE, 10L uMAX/uSOP MEETS JEDEC MO-187C-BA. 4. 21-0061 Ι

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