High Power Prioritized PowerPath Controller

FEATURES

- **0V to 36V Wide Operating Range (60V Tolerant)**
- **Drives Large External N-Channel MOSFETs for High Output Current Applications**
- **Accurately Limits Inrush Current**
- **Connects Highest Priority Valid Supply to Output Load**
- **Changes Channel Priority in Real Time**
- **±2% OV, UV Input Comparators**
- Individually Adjustable Current Limit Time-Out for Each Channel
- Adjustable Input Validation Time
- Fast Switchover Minimizes V_{OUT} Droop
- 36-Lead 5mm × 6mm QFN and SSOP Packages

APPLICATIONS

- High Reliability Systems
- Server Based Back-Up Systems
- Industrial Handheld Instruments
- Battery Back-Up Systems

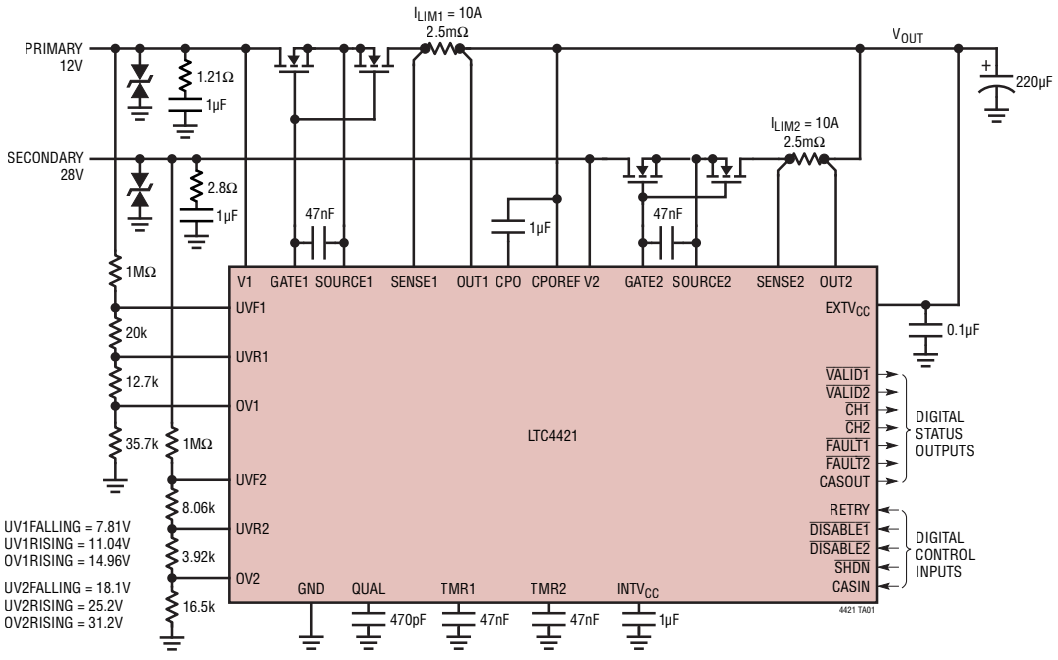
DESCRIPTION

The LTC®4421 connects one of two input supplies to a common output based on user-defined priority and validity. By definition, the supply connected to V1 is the higher priority supply, although this can be changed dynamically. External resistive dividers set the undervoltage and overvoltage thresholds that bound the valid voltage window.

Strong gate drivers switch the large external N-channel MOSFETs quickly. Fast switchover circuitry minimizes output droop when changing channels while preventing reverse and cross conduction. A fast comparator detects input short circuits and quickly turns off the N-channel MOSFETs to minimize disruption.

External sense resistors set the maximum inrush and current limit currents. During current limiting, the LTC4421 controls the N-channel MOSFET gate to regulate 25mV across the sense resistor. When the sense resistor voltage has been regulated to 25mV for a user-settable time, the channel is disconnected and a fault is set.

TYPICAL APPLICATION



Rev. 0

ABSOLUTE MAXIMUM RATINGS

(Notes 1, 2)

Supply Voltages
- V1, V2, $EXTV_{CC}$ ..... –10V to 60V
- OUT1, OUT2, CPOREF ..... –10V to 45V

Input Voltages
- $\overline{DISABLE1}$, $\overline{DISABLE2}$, $\overline{SHDN}$ ..... –0.3V to 60V
- CASIN ..... –0.3V to 6V
- SENSE1, SENSE2, SOURCE1, SOURCE2 .. –10V to 45V
- UVF1, UVF2, UVR1, UVR2, OV1, OV2 .... –0.3V to 60V
- RETRY, TMR1, TMR2, QUAL .... –0.3V to $INTV_{CC}$+0.3V

Output Voltages
- $\overline{VALID1}$, $\overline{VALID2}$, $\overline{CH1}$, $\overline{CH2}$, $\overline{FAULT1}$, $\overline{FAULT2}$, CPO ..... –0.3V to 60V
- $INTV_{CC}$ ..... –0.3V to 6V

GATE1, GATE2 (Note 3) ..... –0.3V to CPO

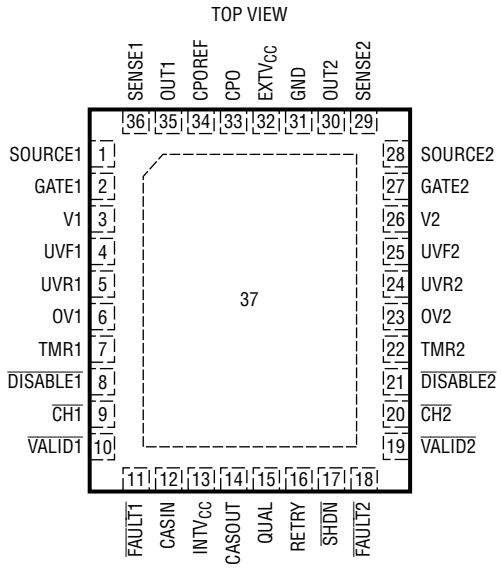
CASOUT ..... –0.3V to 6V

Output Currents
- $\overline{FAULT1}$, $\overline{FAULT2}$, $\overline{CH1}$, $\overline{CH2}$, $\overline{VALID1}$, $\overline{VALID2}$, CASOUT 5mA

Operating Ambient Temperature Range
- LTC4421C ..... 0°C to 70°C
- LTC4421I ..... –40°C to 85°C
- LTC4421H ..... –40°C to 125°C

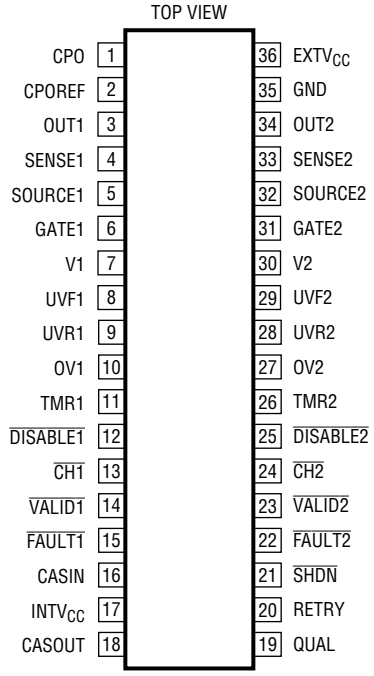
Storage Temperature Range ..... –65°C to 150°C

PIN CONFIGURATION



UHE PACKAGE
36-LEAD (5mm × 6mm) PLASTIC QFN

T_{JMAX} = 150°C, θ_{JA} = 43°C/W, θ_{JC} = 5°C/W
EXPOSED PAD (Pin 37), PCB GND CONNECTION OPTIONAL



G PACKAGE
36-LEAD PLASTIC SSOP

T_{JMAX} = 150°C, θ_{JA} = 70°C/W

ORDER INFORMATION

TUBE	TAPE AND REEL	PART MARKING	PACKAGE DESCRIPTION	TEMPERATURE RANGE
LTC4421CG#PBF	LTC4421CG#TRPBF	LTC4421G	36-Lead Plastic SSOP	0°C to 70°C
LTC4421IG#PBF	LTC4421IG#TRPBF	LTC4421G	36-Lead Plastic SSOP	–40°C to 85°C
LTC4421HG#PBF	LTC4421HG#TRPBF	LTC4421G	36-Lead Plastic SSOP	–40°C to 125°C
LTC4421CUHE#PBF	LTC4421CUHE#TRPBF	4421	36-Lead Plastic QFN	0°C to 70°C
LTC4421IUHE#PBF	LTC4421IUHE#TRPBF	4421	36-Lead Plastic QFN	–40°C to 85°C
LTC4421HUHE#PBF	LTC4421HUHE#TRPBF	4421	36-Lead Plastic QFN	–40°C to 125°C

Contact the factory for parts specified with wider operating temperature ranges.

Tape and reel specifications. Some packages are available in 500 unit reels through designated sales channels with #TRMPBF suffix.

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. See the LTC4421 Data Sheet Nomenclature section for more details on pin conditions. V1 = 12V, V2 = 13V, $EXTV_{CC}$ = CPOREF = OUT1 = OUT2 = SENSE1 = SENSE2 = 11V, OV1 = OV2 = TMR1 = TMR2 = OV, UVR1 = UVR2 = UVF1 = UVF2 = $\overline{DISABLE1}$ = $\overline{DISABLE2}$ = $\overline{SHDN}$ = RETRY = CASIN = 4V, CPO = 23.5V, QUAL = $INTV_{CC}$, unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
V_{IN}	V1, V2 Operating Voltage Range	(Note 4)	●	3.0		36	V
$V_{INT(UVL)}$	$INTV_{CC}$ Undervoltage Lockout Threshold Voltage		●	2	2.3	2.6	V
$\Delta V_{INT(HYS)}$	$INTV_{CC}$ Undervoltage Lockout Hysteresis				70		mV
V_{INTVCC}	$INTV_{CC}$ Output Voltage	I_{INTVCC} = 0µA	●	3.3	3.9	4.5	V
ΔV_{INTVCC}	$INTV_{CC}$ Voltage Change from Zero to Full Load	I_{INTVCC} = 0 to –500µA	●	–35	–85	–200	mV
$V_{CPO(UVL)}$	CPOGOOD Threshold Voltage	CPO–CPOREF	●	5.7	6.7	7.7	V
$V_{CPO(HYS)}$	CPOGOOD Hysteresis				1.4		V
$I_{CC(TOT)}$	Total Input Supply Current	V1, V2, OUT1, OUT2, $EXTV_{CC}$, CPOREF	●		0.53	1	mA
$I_{CC(SHDN)}$	Total Input Supply Current in Shutdown	V1, V2, $EXTV_{CC}$	●		5.4	12	µA
$I_{CC(PRIO)}$	Input Supply Current of Highest Priority Valid Supply	Measure I($EXTV_{CC}$)	●		360	750	µA
$I_{CC(VMAX)}$	Input Supply Current of Highest Voltage Input Supply	Measure I(V2)	●		25	50	µA
$I_{CC(CPOREF)}$	CPOREF Charge Pump Supply Current	CPOREF = 11V	●		160	300	µA
PRIORITIZER CONTROL (V1, V2, SENSE1, SENSE2, GATE1, GATE2, SOURCE1, SOURCE2, OUT1, OUT2)							
$\Delta V_{G(OFF)}$	External N-Channel MOSFET Off Threshold Voltage	(GATE1 – V1), (GATE2 – V2), GATE Falling	●	0	–0.6	–1.5	V
ΔV_{REV}	Input to Output Reverse Voltage Connect Threshold	(V1– OUT1), (V2–OUT2), OUT1, OUT2 Falling	●	0	40	80	mV
$\Delta V_{GATE(CL)}$	External N-Channel MOSFET Gate Drive, (GATE – CPOREF)	CPOREF = 3.2V, $EXTV_{CC}$ = 3.0V, I = 0, –1µA CPOREF = 12V, 36V, I = 0, –1µA	● ●	9 10	10.8 11.6	14 14	V V
$I_{SOURCE, HLD}$	SOURCE Hold Current	SOURCE = 12V, Channel Off	●	2.5	5	10	µA
$I_{SOURCE, OFF}$	SOURCE Fast Off Current	SOURCE = 12V, Channel Off	●	0.7	1.6	3.2	mA
$I_{GATE(ON)}$	GATE On Pull-Up Current	V(SENSE) – V(OUT) = 0V, GATE = 16V, OUT = 10V, V1 = V2 = 12V	●	–8	–16.5	–26	mA
$I_{GATE(OFF,FWD)}$	GATE Off Pull-Down Current, Large Forward Sense Voltage	V(SENSE)–V(OUT) = 100mV, GATE = 16V, OUT = 10V, V1 = V2 = 12V	●	30	54	124	mA

ELECTRICAL CHARACTERISTICS

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SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
$I_{GATE(OFF,REV)}$	GATE Off Pull-Down Current, Negative Sense Voltage	V(SENSE)–V(OUT) = –50mV, GATE = 16V, OUT = 10V, V1 = V2 = 12V	●	30	50	92	mA
ΔV_{SNS}	Current Limit Sense Voltage, ΔV_{SNS} = (SENSE – OUT) ΔV_{SNS} = (SENSE – OUT)	OUT = 1V, 12V, 32V $EXTV_{CC}$ = 3.0V, OUT = 1V	● ●	20 20	25 25	30 30	mV mV
$\Delta V_{SNS,FLD}$	Current Limit Sense Voltage in Foldback, $\Delta V_{SNS,FLD}$ = (SENSE – OUT)	OUT = 0V	●	7.5	12.5	17.5	mV
$V_{FLD,TH}$	Foldback Threshold Voltage	OUT1	●	380	480	580	mV
$V_{FLD,HYST}$	Foldback Hysteresis				50		mV
$V_{SNSDIS,FWD}$	Forward Overcurrent Disconnect Voltage	SENSE – OUT, Rising			50		mV
$V_{SNSDIS,REV}$	Reverse Current Disconnect Voltage	SENSE – OUT, Falling			–30		mV
I_{SNS}	SENSE Input Current	SENSE = OUT = 12V	●			±1	µA
$t_{G(SWITCH)}$	Gate Break-Before-Make Time	C_{GATE} = 47nF	●		10.3	15	µs
$t_{PG(DIS, OFF)}$	Gate Turn-Off Delay from $\overline{DISABLE}$	Falling $\overline{DISABLE}$ to Gate < 12V	●		1.4	2.7	µs
$t_{PG(DIS, ON)}$	Gate Turn-On Delay from $\overline{DISABLE}$	Rising $\overline{DISABLE}$ to Gate > 12V	●		1.3	2.1	µs
$t_{PG(CAS)}$	CASIN to CASOUT Propagation Delay	High-to-Low			1		µs
$t_{PG(DIS, CAS)}$	$\overline{DISABLE}$ to CASOUT Propagation Delay	$\overline{DISABLE}$ High-to-Low			2.8		µs
CURRENT LIMIT TIMER (TMR1, TMR2)							
$I_{TMR(UP)}$	TMR Pull-Up Current		●	–3	–6	–9	µA
$I_{TMR(DN)}$	TMR Pull-Down Current		●	1	2	3	µA
$t_{TMR,FLT}$	TMR Fault Time	C_{TMR} = 10nF	●	550	830	1250	µs
%TMR(COOL)	TMR Cool Down Ratio to Fault Time				0.1		%
OV, UV PROTECTION CIRCUITRY (OV1, OV2, UVF1, UVF2, UVR1, UVR2, QUAL)							
$V_{TH,OVUV}$	OV, UV Threshold Voltage	OV Rising, UVF Falling, UVR Rising	●	490	500	510	mV
$V_{HYST, OV}$	OV Hysteresis		●	40	50	60	mV
$I_{LK,OVUV}$	UVR, UVF, OV Input Leakage Current	V = 0.5V	●			±10	nA
$I_{QUAL,SRC}$	QUAL Source Current		●	–1	–2	–3	µA
$I_{QUAL,SNK}$	QUAL Sink Current		●	1	2	3	µA
t_{VALID}	OV, UV Validation Time	QUAL = $INTV_{CC}$ C_{QUAL} = 470pF	● ●	1.75 5	5 7.5	8 11	µs ms
$t_{INVALID}$	OV, UV Invalidation Filter Time	Overdrive = 50mV	●	1.75	5	8	µs
DIGITAL INPUTS ($\overline{DISABLE1}$, $\overline{DISABLE2}$, $\overline{SHDN}$, CASIN, RETRY)							
V_{TH}	Rising Threshold Voltage		●	0.5	1.0	1.5	V
V_{HYST}	Hysteresis Voltage				150		mV
$I_{LK,HV}$	Input Leakage Current	V = 36V, $\overline{DISABLE}$, $\overline{SHDN}$	●		±0.1	±1	µA
$I_{LK,LV}$	Input Leakage Current	V = 5.5V, CASIN Retry = $INTV_{CC}$	● ●		±0.1 ±0.1	±1 ±1	µA µA
I_{CASIN}	CASIN Pull-Up Current	CASIN = 0V	●	2.5	5	10	µA

ELECTRICAL CHARACTERISTICS

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SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
DIGITAL OUTPUTS ($\overline{CH1}$, $\overline{CH2}$, $\overline{VALID1}$, $\overline{VALID2}$, $\overline{FAULT1}$, $\overline{FAULT2}$, CASOUT)							
$V_{OL,HV}$	Output Voltage Low, $\overline{CH}$, $\overline{VALID}$, $\overline{FAULT}$	I = 1mA, V1 = V2 = $EXTV_{CC}$ = 3.0V I = 3mA, V1 = V2 = $EXTV_{CC}$ = 3.0V	● ●		185 0.58	450 1.35	mV V
$I_{OH,HV}$	Open Drain, Output High Leakage Current	V = 36V, $\overline{CH}$, $\overline{VALID}$, $\overline{FAULT}$	●			±1	µA
$V_{CASO,OH}$	CASOUT Output High Voltage	I = –1µA , $\overline{SHDN}$ = 0V	●	2	3.4	4.5	V
$V_{CASO,OL}$	CASOUT Output Low Voltage	I = 1mA	●		85	200	mV
I_{CASO}	CASOUT Pull-Up Current	CASOUT = 1V	●	–11	–22	–40	µA
$I_{LK,CASO}$	CASOUT Leakage Current	CASOUT = 5.5V	●			±1	µA

Note 1. Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

Note 2. All currents into pins are positive; all voltages are referenced to GND unless otherwise noted.

Note 3. Do not drive GATE1 and GATE2 above CPO. Doing so can cause excessive voltage on CPO.

Note 4. V1 can operate down to 0V, provided V2 ≥ 3.0V or $EXTV_{CC}$ ≥ 3.0V. Likewise, V2 can operate down to 0V, provided V1 ≥ 3.0V or $EXTV_{CC}$ ≥ 3.0V.

LTC4421 DATA SHEET NOMENCLATURE

The LTC4421 dedicates 13 pins per channel for the purposes of monitoring each input supply and controlling its connection to the output. Pin names having suffix “1” apply to Channel 1, while those having suffix “2” apply to Channel 2. When no suffix is used when referencing one of these pins, it means that the text applies to the pins on both channels. For example, “Connect a capacitor C_{TMR} from TMR to ground” means “Connect a capacitor C_{TMR1} between the TMR1 pin and ground” and “Connect a capacitor C_{TMR2} between the TMR2 pin and ground”.

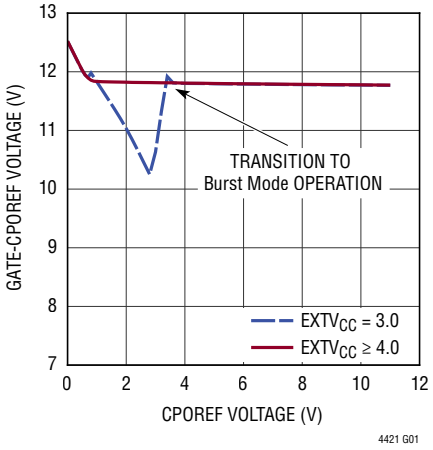
References to multiple pin names with no suffix are meant to describe functionality within a channel but apply to both channels. These references occur for the following cases:

1. Connecting two pins together: “Tie $\overline{FAULT}$ to $\overline{DISABLE}$” means “Tie $\overline{FAULT1}$ to $\overline{DISABLE1}$” and “Tie $\overline{FAULT2}$ to $\overline{DISABLE2}$”.
2. Referring to differential voltages: “SENSE to OUT” means “SENSE1 to OUT1” and “SENSE2 to OUT2”.
3. Causation: “The $\overline{VALID}$ pins pull low when their V1-V2 supplies have been validated” means “The $\overline{VALID1}$ pin pulls low when the V1 supply has been validated” and “The $\overline{VALID2}$ pin pulls low when the V2 supply has been validated”.

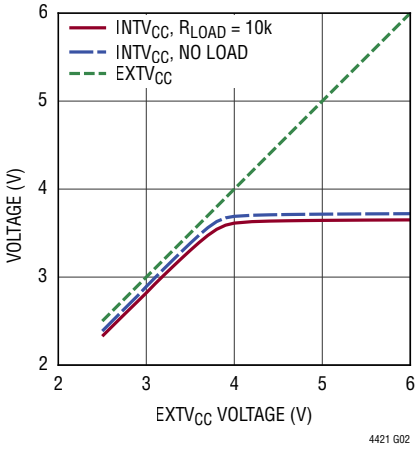
TYPICAL PERFORMANCE CHARACTERISTICS

T_A = 25°C, $EXTV_{CC}$ = 11V, unless otherwise noted.

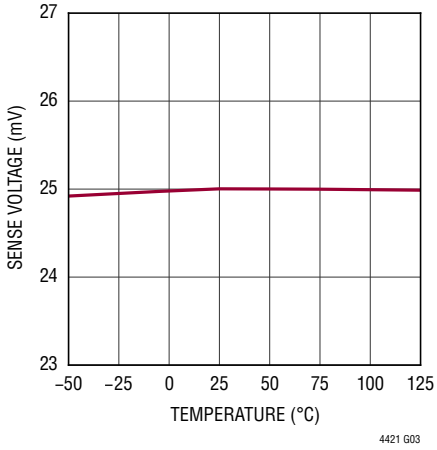
GATE Drive Voltage vs CPOREF Voltage



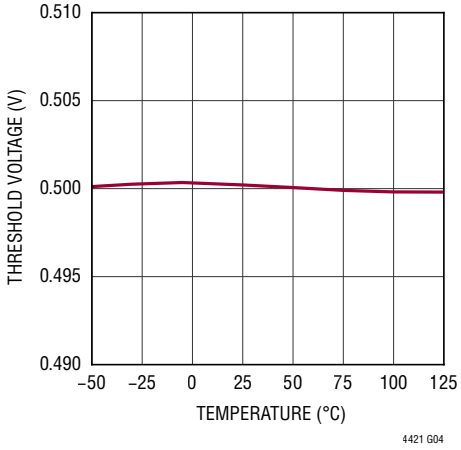
$INTV_{CC}$ Voltage vs $EXTV_{CC}$ Voltage



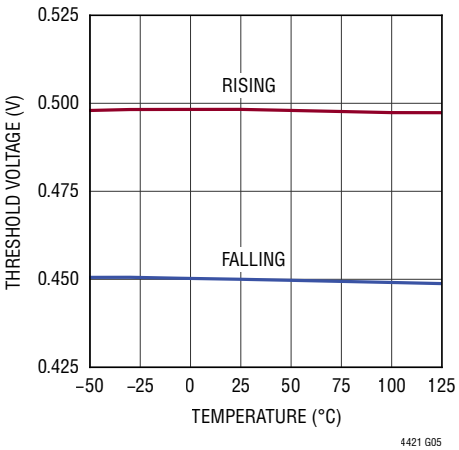
SENSE Voltage vs Temperature



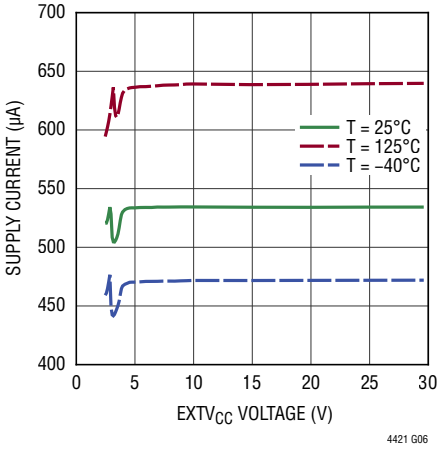
Undervoltage Threshold vs Temperature



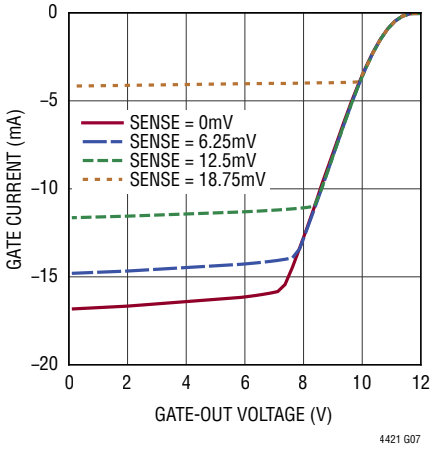
Overvoltage Thresholds vs Temperature



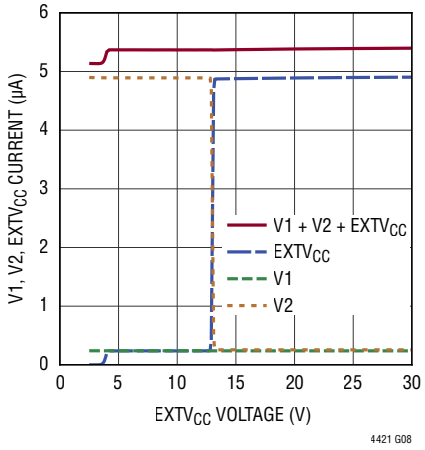
Total Supply Current vs $EXTV_{CC}$ Voltage



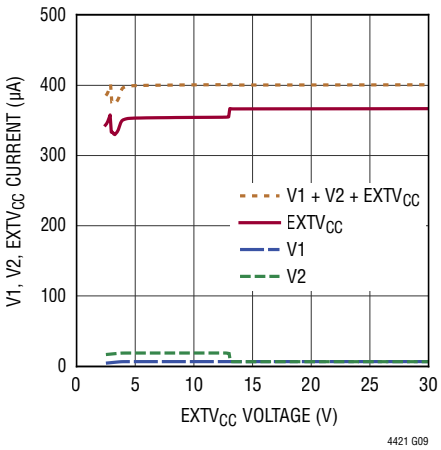
GATE On Pull-Up Current vs GATE Voltage



Shutdown Current vs $EXTV_{CC}$ Voltage (V1 = 12V, V2 = 13V)



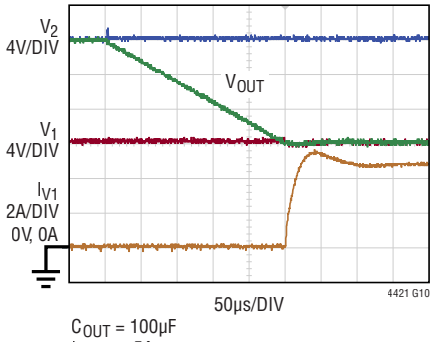
Supply Current vs $EXTV_{CC}$ Voltage (V1 = 12V, V2 = 13V)



TYPICAL PERFORMANCE CHARACTERISTICS

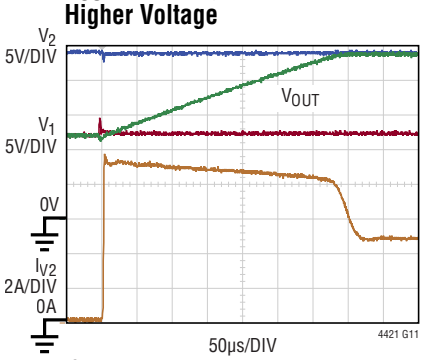
T_A = 25°C, $EXTV_{CC}$ = 11V, unless otherwise noted.

V_{OUT} Switching from Higher to Lower Voltage



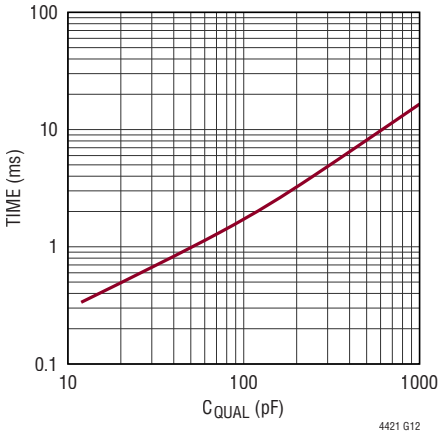
C_{OUT} = 100µF
I_{LOAD} = 5A
30V NCH SiR158DP

V_{OUT} Switching from Lower to Higher Voltage

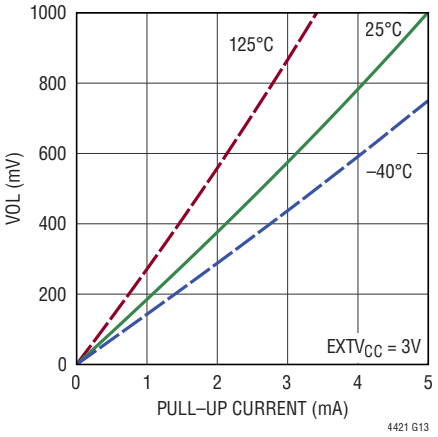


C_{OUT} = 100µF
I_{LOAD} = 5A
30V NCH SiR158DP

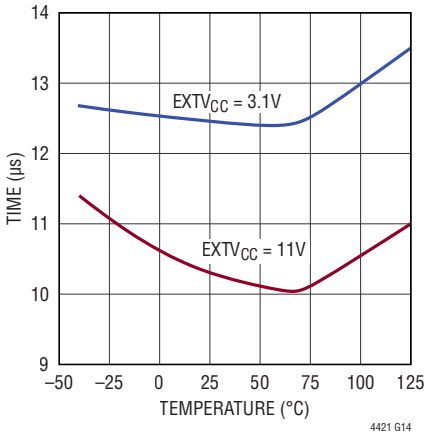
OV, UV Validation Time vs QUAL Capacitance



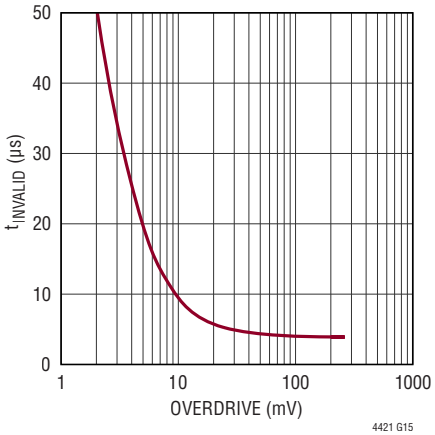
$\overline{VALID}$, $\overline{CH}$, $\overline{FAULT}$ Output Low Voltage vs Pull-Up Current



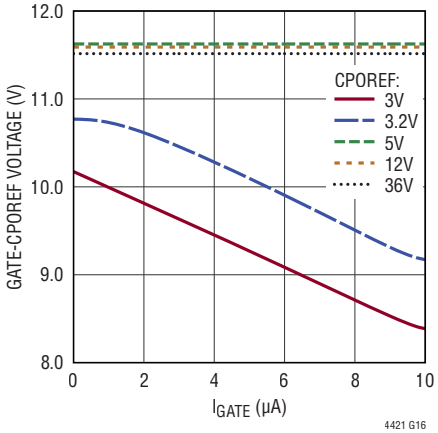
GATE Break-Before-Make Time vs Temperature



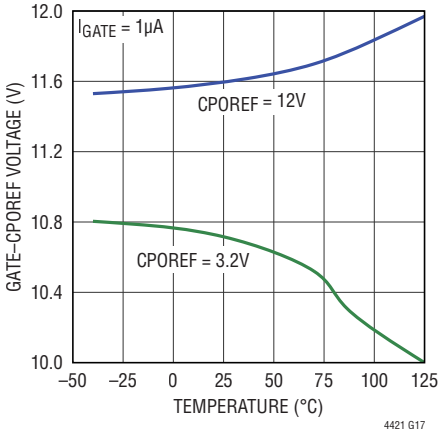
OV, UV Propagation Delay vs Overdrive



GATE Drive vs GATE Current



GATE Drive vs Temperature



PIN FUNCTIONS

CASIN: Digital Input for Cascading. Connect to CASOUT of another, higher priority LTC4421 when cascading. Connect to $INTV_{CC}$ or drive to a supply voltage above 1V if not used.

CASOUT: Digital Output for Cascading. Connect to the CASIN of another, lower priority LTC4421 when cascading. Leave open if not used.

$\overline{CH1}$: Voltage Power Source Indicator Output. This open-drain output pulls low when V1 is powering the output voltage and releases high otherwise. Connect a pull-up resistor to a supply less than or equal to 36V to provide the pull-up. Connect to ground or leave open if unused.

$\overline{CH2}$: Voltage Power Source Indicator Output. This open-drain output pulls low when V2 is powering the output voltage and releases high otherwise. Connect a pull-up resistor to a supply less than or equal to 36V to provide the pull-up. Connect to ground or leave open if unused.

CPO: Charge Pump Output. This is the output of the charge pump, which is used to provide overdrive to the GATE pins. Connect a ceramic capacitor between CPO and CPOREF whose value must be at least 10 times the combined capacitance of the GATE compensation capacitor plus the gate capacitance of the back-to-back external N-Channel MOSFETs of one channel. When the (CPO–CPOREF) voltage is lower than the CPOGOOD threshold voltage $V_{CPO(UVL)}$, the input supplies are prevented from powering the output. See the Operation section for details of the initial start-up delay due to the time required to charge the CPO capacitor.

CPOREF: Charge Pump Reference Output. This is the reference point for the charge pump, which is used to provide overdrive to the GATE pins. Connect to the system output voltage using a short PCB trace. Do not connect to the OUT1 or OUT2 sense resistor Kelvin connections.

$\overline{DISABLE1}$, $\overline{DISABLE2}$: Digital Inputs for Input Disconnect and Current Limit Fault Reset. Voltages below 1V prevent the corresponding input V1, V2 supply from powering the output voltage. Driving $\overline{DISABLE}$ low, then high after a current limit fault resets the current limit timer circuitry and releases the corresponding $\overline{FAULT}$ pin high. Connecting $\overline{DISABLE}$ to the corresponding $\overline{FAULT}$ pin configures the device in auto-retry mode, with a cool-down period between retries that is 1024 times longer than the current limit fault time. See Applications Information for more details. Tie to $INTV_{CC}$ or drive to a supply voltage above 1V if not used.

$EXTV_{CC}$: External High Priority Supply Input. When $EXTV_{CC}$ exceeds 2.45V, an internal LDO generates a low voltage supply rail from $EXTV_{CC}$ to power the low voltage internal circuitry. Most of the LTC4421's I_{CC} is drawn from $EXTV_{CC}$. Connect $EXTV_{CC}$ to a supply voltage ranging from 3.0V to 36V. Connect $EXTV_{CC}$ to the output voltage (OUT1 or OUT2) to make the output voltage provide the internal bias current to the LTC4421. If unused, connect to ground, and the LDO will be powered from another supply.

$\overline{FAULT1}$, $\overline{FAULT2}$: Current Limit Fault Indicators. These open-drain outputs pull low when an overcurrent fault occurs on their corresponding inputs and remain low during the cool down cycle. Connect pull-up resistors to a supply voltage less than or equal to 36V to provide the pull-up. Tie to ground or leave open if unused.

GATE1, GATE2: Gate Drives for External N-Channel MOSFETs. Connect these pins to the gates of the external back-to-back N-Channel MOSFETs. The charge pump drives these pins with up to 12V of enhancement. Connect a capacitor between each GATE pin and the sources of the corresponding MOSFETs to compensate the current limit regulation loop.

GND: Device Ground.

$INTV_{CC}$: Internal Low Voltage Supply Decoupling Output. An internal LDO generates a low voltage rail to power the low voltage internal circuitry. It is capable of supplying up to 500µA of external current. Connect a 1µF or larger capacitor between this pin and ground to provide bypassing. This pin has an undervoltage lockout threshold voltage of 2.3V.

OUT1, OUT2: Output Voltage Sense. The LTC4421 prevents input supplies from connecting to the corresponding OUT until OUT is at least 35mV below the connecting supply. These pins are also used in conjunction with the SENSE pins to set the current limit values for the input supplies. Connect OUT directly to the output side of the sense resistor with Kelvin connection.

OV1, OV2: Overvoltage Comparator Inputs. Rising input voltages that cross above 0.5V cause an overvoltage

PIN FUNCTIONS

event. Connect OV1 and OV2 to a resistive divider between the respective V1, V2 and ground to set the overvoltage threshold. See Applications Information section for connecting unused OV1 and OV2 pins.

QUAL: OV, UV Qualification Timer. Connect a capacitor C_{QUAL} from this pin to ground to set an OV, UV qualification time of 16ms/nF. Alternatively, connect this pin to $INTV_{CC}$ to set a default time of 3.5µs. Do not leave open.

RETRY: Digital Input for Retry after Current Limit Fault. When this pin is above 1V, after a current limit fault disconnect occurs, the LTC4421 reconnects the input to the output up to 6 additional times, waiting for a cool down period between each reconnection. If current limit faults occur in each of 6 additional reconnections, the LTC4421 keeps the input disconnected until the input's $\overline{\text{DISABLE}}$ pin is toggled. See the Applications section for more details. Connect to ground if unused. Do not leave open.

SENSE1, SENSE2: Current Sense Non-Inverting Inputs. The current limit regulation circuits control the GATE pins to limit the sense voltages between SENSE and OUT to 25mV. If the OUT1 voltage drops below 0.45V, the regulation voltage is reduced from 25mV to 12.5mV. Connect SENSE1, SENSE2 directly to the input sides of the sense resistors with Kelvin connections.

$\overline{\text{SHDN}}$: Digital Input Shutdown to Disconnect Output and Set Low Current Mode. Voltages below 1V turn off all external MOSFETs, invalidate both channels and cause the LTC4421 to enter a low current mode. CASOUT is pulled high to allow a lower priority LTC4421 in a cascaded system to provide power to the output. All circuitry is debiased, except for the shutdown comparator and low voltage rail generators, and total device current is reduced to 6µA. When $\overline{\text{SHDN}}$ is driven back above 1V, the external MOSFETs are held off until the OV and UV comparators revalidate. Connect to $INTV_{CC}$ if unused.

SOURCE1, SOURCE2: Connections to Common Sources of External Back-to-Back N-Channel MOSFETs. Leave open or connect to the sources of the external MOSFETs. To minimize channel switchover time, a 5µA pull-down current biases the MOSFETs on the edge of conduction when their input supply is not connected to the output. Add resistors from the MOSFET sources to ground to increase the MOSFET V_{GS} bias voltage and reduce switchover time.

TMR1, TMR2: Current Limit Fault Timers. Connect a capacitor between each TMR pin and ground to set a 83ms/µF duration for current limit before an overcurrent fault occurs. When a fault occurs, the external N-Channel MOSFETs are turned off and the corresponding $\overline{\text{FAULT}}$ pin is pulled low. The LTC4421 can be configured to latch-off, auto-retry indefinitely or auto-retry 6 additional times after an overcurrent fault. See the Applications Information for more details.

UVR1, UVR2: Undervoltage Comparator Inputs for Rising Voltages. Rising input voltages that cross above 0.5V are considered valid, provided that the OV pin voltage is below 0.5V. Connect UVR1 and UVR2 to a resistive divider between the respective V1, V2 and ground to set the rising undervoltage threshold. Set the UVR threshold voltage above the corresponding UVF threshold voltage to ensure proper operation. See Applications Information section for connecting unused UVR1 and UVR2 pins.

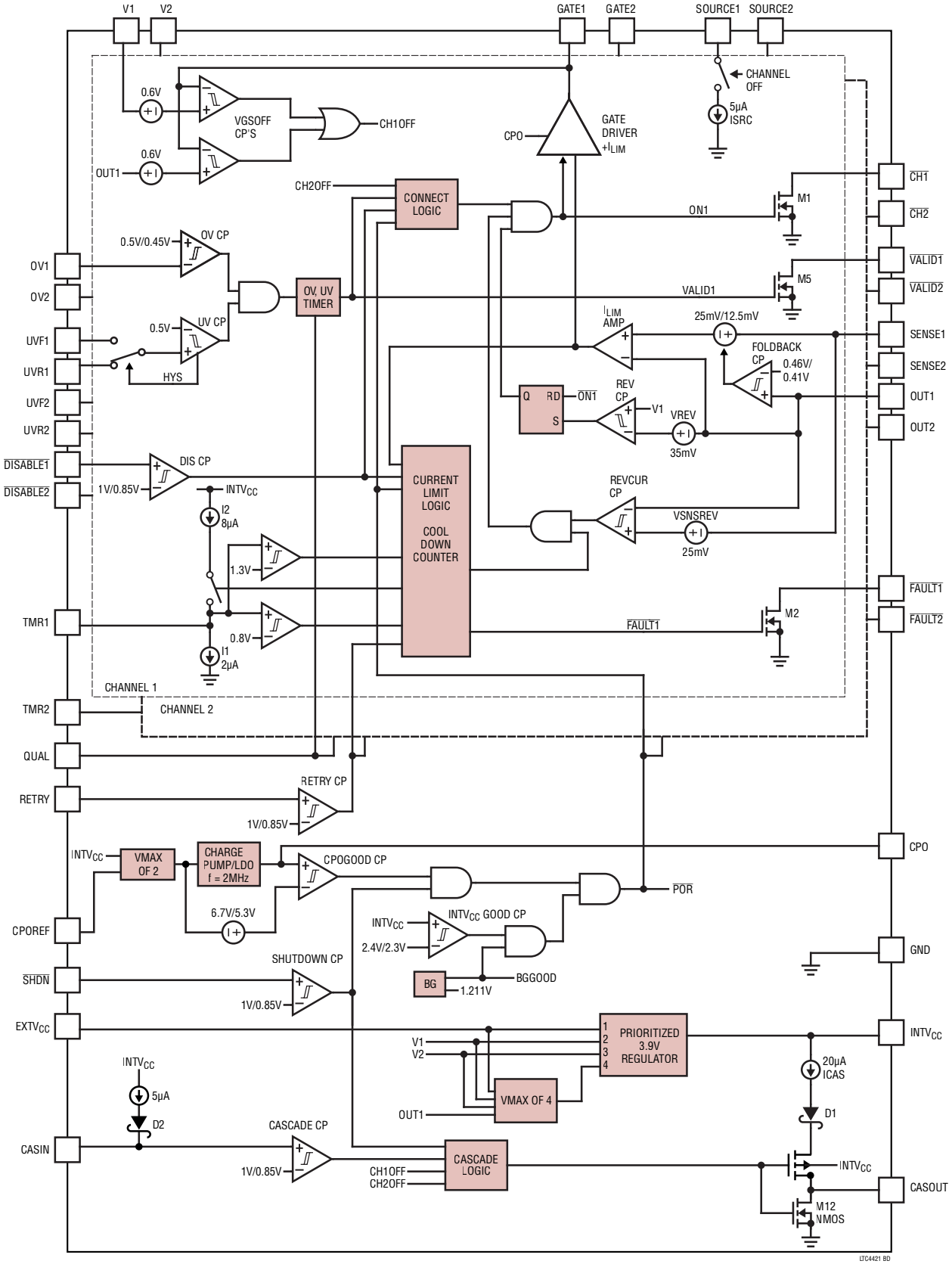
UVF1, UVF2: Undervoltage Comparator Inputs for Falling Voltages. Falling input voltages that cross below 0.5V cause an undervoltage event. Connect UVF1 and UVF2 to a resistive divider between the respective V1, V2 and ground to set the falling undervoltage threshold. Set the UVR threshold voltage above the corresponding UVF threshold voltage to ensure proper operation. See Applications Information section for connecting unused UVF1 and UVF2 pins.

V1, V2: Input Power Supply Voltages. Typically V1 and V2 are connected to input supply voltages ranging from 3.0V to 36V, but each supply can operate down to 0V, provided another supply voltage ≥3.0V powers the LTC4421. In normal operation, V1 is the higher priority supply and V2 is the lower priority supply.

$\overline{\text{VALID1}}$, $\overline{\text{VALID2}}$: Voltage Valid Indicator Outputs. These open-drain outputs pull low when their corresponding V1, V2 inputs are within their OV, UV window for the required qualification time. Connect pull-up resistors to a supply voltage less than or equal to 36V to provide the pull-up. Connect to ground or leave open if unused.

Exposed Pad (Pin 37, UHE Package only): Exposed Pad may be left open or connected to device ground.

BLOCK DIAGRAM



OPERATION

The LTC4421 is a Prioritized PowerPath™ Controller that drives external N-Channel MOSFETs to connect one of two input supplies to a common output based on user-defined priority and validity. By definition, the supply connected to V1 is the higher priority supply, and the supply connected to V2 is lower priority, although this can be changed dynamically. The V1 voltage can be lower than, equal to or higher than the V2 voltage.

At initial power-up, the LTC4421 prevents the input supplies from validating and connecting to the output until it has enough bias voltage to function properly. Referring to the Block Diagram, the LTC4421 prevents OV, UV validation and connection to the output until the $INTV_{CC}$ voltage exceeds 2.3V ($V_{INT(UVL)}$) as detected by comparator $INTV_{CC}$ GOOD CP, the bandgap reference voltage has reached its final regulated value as indicated by the BGGOOD signal, and the CPO voltage exceeds the higher of the CPOREF and $INTV_{CC}$ voltages by 6.7V ($V_{CPO(UVL)}$) as detected by comparator CPOGOOD CP. With a 1µF capacitor connected between CPO and CPOREF, the Charge Pump/LDO circuit can take several hundred milliseconds to charge to 6.7V. See the Applications Information for methods to reduce the charging time.

After initial power-up is complete, the LTC4421 monitors the V1 and V2 voltages via resistive dividers to precision overvoltage (OV CP) and undervoltage (UV CP) comparators. The UVR and UVF pins set the rising and falling undervoltage thresholds for the UV comparators. When an input voltage has been inside its OV, UV voltage window for a time (t_{VALID}) set by the QUAL pin, it is considered valid and is eligible to power the output. If the input supply voltage falls out of the OV, UV window and remains outside for at least 3.5µs ($t_{INVALID}$), the supply is disconnected from the output. Open drain output status pins provide information regarding a channel's validity and connection status to the output. $\overline{VALID1}$ and $\overline{VALID2}$ are pulled low when V1 and V2, respectively, are valid. $\overline{CH1}$ and $\overline{CH2}$ are pulled low when V1 and V2, respectively, are powering V_{OUT}.

The GATE DRIVER circuit provides strong sourcing and sinking currents to external N-Channel MOSFETs to connect and disconnect the input supplies to and from the output. When turning on the MOSFETs, GATE DRIVER sources current from the CPO pin to pull the GATE voltage up to the CPO voltage. A charge pump regulates the CPO voltage 12V ($V_{GATE(CL)}$) above the CPOREF voltage to provide 12V of V_{GS} enhancement to the MOSFETs. Strong sinking currents ensure rapid turnoff of the external MOSFETs when a channel is no longer valid, a higher priority channel takes precedence or when comparator REVCUR CP detects a reverse voltage of –25mV ($V_{SNSDIS,REV}$) across the external sense resistor. Such a reverse voltage occurs when an input supply powering the output is shorted. Fast charge and discharge of the external NMOS gates ensure fast switching between supplies, minimizing droop at the output.

During channel transitions, monitoring circuitry prevents cross conduction between input supplies and reverse current from the output using a break-before-make architecture. Two V_{GS} comparators (VGSOFF CPs) monitor the disconnecting channel's gate pin voltage (GATE1 or GATE2). When the GATE voltage is 600mV ($V_{GS(OFF)}$) lower than either the input or output voltage of the channel turning off, the V_{GS} comparators determine the external N-channel MOSFETs to be off and allow the other channel to connect to the output. The V_{GS} comparator outputs are latched in the off state; the latch is reset when the channel is commanded to turn back on.

To prevent reverse conduction from the output to the inputs during channel switchover, the reverse comparator (REV CP) monitors the connecting V1, V2 supply and the corresponding OUT1, OUT2 output. The REV comparator prevents connection until the output droops 35mV (V_{REV}) below the connecting supply. The connection is latched, resetting when the channel is commanded to disconnect.

OPERATION

The current limit amplifier (I_{LIM} AMP) monitors the load current using the difference between the SENSE and OUT pin voltages. The amplifier and gate driver work together to limit the current in the load by reducing the GATE-to-SOURCE voltage in an active control loop. The SENSE-to-OUT differential voltage is regulated to 25mV (ΔV_{SNS}). An external sense resistor placed between SENSE and OUT sets the current limit value for each channel. Foldback comparator (FOLDBACK CP) reduces the SENSE-to-OUT differential voltage from 25mV (ΔV_{SNS}) to 12.5mV ($\Delta V_{SNS,FLD}$) to conserve power when the OUT1 voltage is low. The foldback comparator's rising and falling threshold voltages are 460mV and 410mV, respectively. If the SENSE–OUT voltage on a channel remains in current limit for the time programmed by the TMR pin, the LTC4421 registers a current limit fault. Additionally, pulsed output load currents exceeding current limit and occurring at duty cycles of 25% or higher will integrate over time and cause a current limit fault.

When a current limit fault occurs, the LTC4421 disconnects the channel and drives the $\overline{FAULT}$ pin low to indicate that a current limit fault has occurred. After a current fault occurs, driving $\overline{DISABLE}$ low initiates a cool down period that is 1024 times longer than the time-out period. Driving $\overline{DISABLE}$ back high terminates the cool-down period, resets $\overline{FAULT}$ high and allows reconnection to the output. Alternatively, if RETRY and $\overline{DISABLE}$ are both high when a current limit fault occurs, the LTC4421 will try to reconnect up to 6 additional times after the first fault, with a cool-down period between attempted connections that is 1024 times longer than the current limit fault time.

Driving $\overline{DISABLE1}$ and $\overline{DISABLE2}$ low disconnects V1 and V2, respectively, from powering the output. The CASIN and CASOUT pins of multiple LTC4421's can be configured to prioritize as many input supplies as desired. The $\overline{DISABLE1}$, $\overline{DISABLE2}$ and CASIN inputs are connected to comparators having 1V (V_{TH}) threshold and 150mV ($V_{TH,HYST}$) hysteresis. See the Applications Information section for circuits that use the $\overline{DISABLE}$, $\overline{FAULT2}$ and $\overline{VALID2}$ pins to redefine input supply priorities in real time and to prevent the primary input from powering the output until a valid back-up supply is available.

Driving $\overline{SHDN}$ low causes the device to turn off the external N-Channel MOSFETs, enter a low current state and invalidate V1 and V2. All circuitry is debiased except the $INTV_{CC}$ rail generator and shutdown comparator. The total internal bias current is reduced dramatically to 6µA to conserve power. The $INTV_{CC}$ voltage is reduced to 3V and is powered from the highest of the V1, V2, $EXTV_{CC}$ and OUT1 voltages. The CASOUT pin is driven high to allow a lower priority LTC4421 in a cascading application to power V_{OUT}.

When $\overline{SHDN}$ is driven high, the LTC4421 reactivates all circuits. It may take several hundred milliseconds for a valid input to connect to the output, because the external charge pump capacitor C_{CPO} must charge to 6.7V before connection is allowed.

The LTC4421 includes its own internally generated low voltage rail ($INTV_{CC}$) that provides power to the low voltage sections of the device. Because most of the device's quiescent current is provided by $INTV_{CC}$, the $INTV_{CC}$ power source is prioritized to minimize current draw from lower priority sources. The $INTV_{CC}$ rail is powered from one of 4 prioritized sources. These sources in order of priority are $EXTV_{CC}$, V1 and V2. If none of these three inputs is valid, $INTV_{CC}$ is powered by the highest of the V1, V2, $EXTV_{CC}$ and OUT1 voltages.

APPLICATIONS INFORMATION

Introduction

High availability systems employ multiple input supplies to power a single common output. When individual supplies such as wall adapters and batteries are unplugged at various points in time, output power must not brown out as control of the output power is transferred to the other supply. Power ORing diodes are often used in these systems, but the highest input supply voltage always powers the output. The LTC4421 powers the output from the highest priority supply available, even if it is lower in voltage than the lower priority supplies. When switching between supplies, output voltage droop is minimized, and backfeeding current is prevented. A typical LTC4421 application circuit is shown in Figure 1, where the primary input supply is 12V and the secondary is 28V. External component selection is discussed in detail in the following sections.

Setting Valid Operating Voltage Range

The LTC4421 requires an input supply remain inside a user-defined voltage window for a user-defined amount of time to be considered valid. The valid voltage window is set by a resistive divider from the input supply to ground that allows three thresholds voltages to be configured: the UV rising threshold (V_{UVRISE}), the UV falling threshold (V_{UVFALL}) and the OV rising threshold (V_{OVRISE}). The OV falling threshold is set by internal hysteresis to be 10% below the OV rising threshold. Using the 500mV

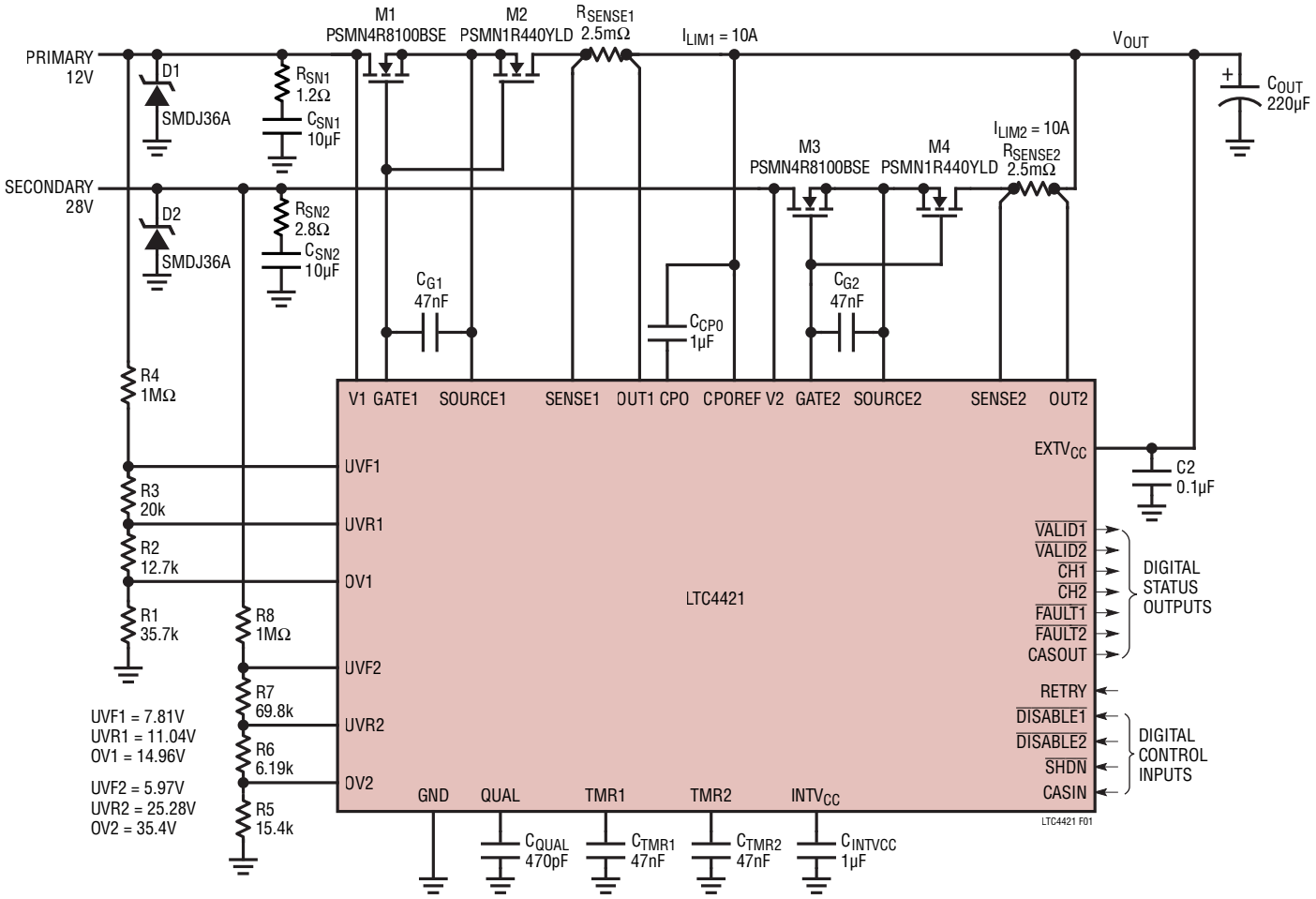


Figure 1. Typical LTC4421 Application Circuit

APPLICATIONS INFORMATION

comparator threshold, the resistor values can be calculated as shown in Equation 1 through Equation 5.

$$R_{TOTAL} = R1 + R2 + R3 + R4 \quad (1)$$

$$R1 = \frac{(0.5 \bullet R_{TOTAL})}{V_{OVRISE}} \quad (2)$$

$$R2 = \left(\frac{V_{OVRISE}}{V_{UVRISE}} - 1\right) \bullet R1 \quad (3)$$

$$R3 = \left(\frac{V_{UVRISE}}{V_{UVFALL}} - 1\right) \bullet \left(\frac{V_{OVRISE}}{V_{UVRISE}}\right) \bullet R1 \quad (4)$$

$$R4 = R1 \bullet \left(\frac{V_{OVRISE}}{0.5} - 1\right) - R3 - R2 \quad (5)$$

When setting the resistor values, take into account the tolerance of the input supply voltage, the tolerance of the resistors, the ±2% error in the 500mV reference and the ±10nA maximum leakage of the UVR, UVF and OV pins. To permanently invalidate a channel, connect OV, UVR and UVF to ground.

During channel turn-on, the relatively large inrush current causes a voltage drop across the input supply source resistance and the parasitic resistances of PCB traces and any cable. This voltage drop can cause UV faults that trigger a phenomenon called UV motorboating, where the input supply repeatedly connects and disconnects from the output. UV motorboating can lead to component damage and undesirable/erratic behavior. To prevent UV motorboating, set the V_{UVRISE} and V_{UVFALL} as far apart as possible to maximize hysteresis and prevent channel disconnect during the inrush. Ideally, quantify the worst-case input resistance $R_{SRC,MAX}$, and set (V_{UVRISE}-V_{UVFALL}) larger than ($I_{LIM} \bullet R_{SRC,MAX}$), where I_{LIM} is the current limit. The OV hysteresis is fixed at 10% above the OV threshold voltage.

For better accuracy, use one resistive divider per channel to set the UVF and UVR thresholds, and a second, separate resistive divider to set the OV threshold. For ease of calculation, use three individual resistive divider strings per channel – one for OV, one for UVF and one for UVR. **However, to ensure the UVR threshold is always higher than the UVF threshold on a given channel, do not use separate strings for UVR and UVF when setting their thresholds close together in voltage.** Figure 2 shows these various resistive divider possibilities, using Channel 1 as an example.

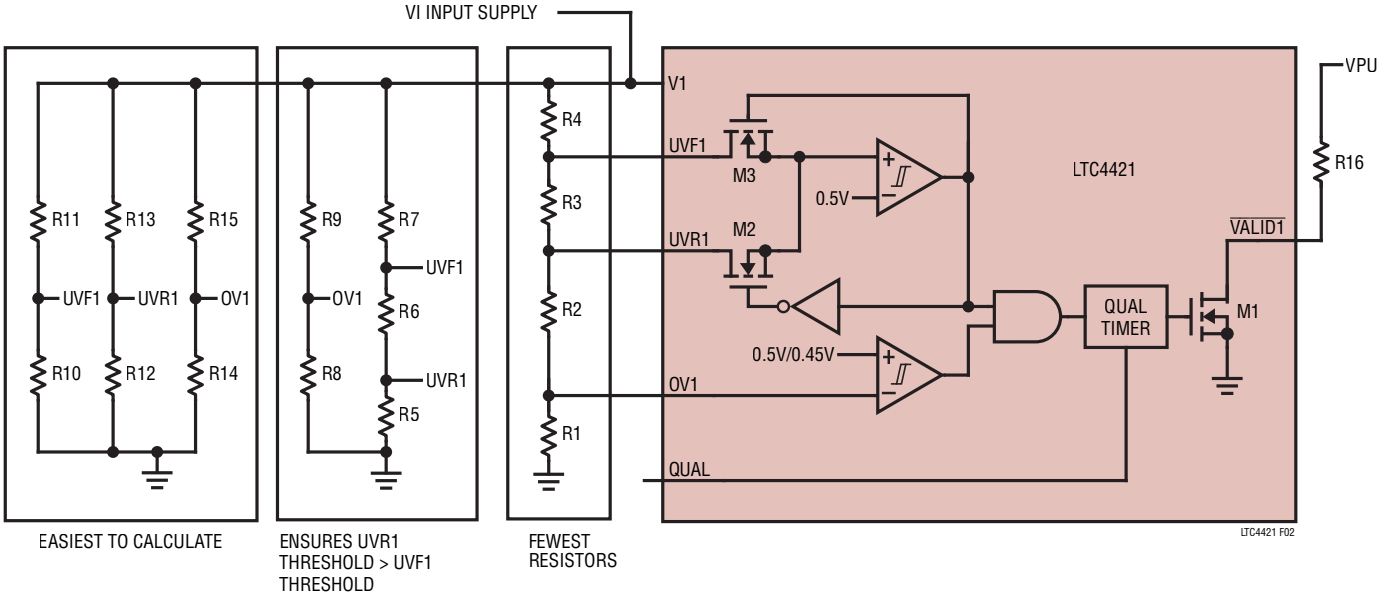


Figure 2. Three Resistive Divider Options For Setting the OV, UVR and UVF Threshold Voltages

APPLICATIONS INFORMATION

Current Limit Regulation and Setting the Current Limit

The LTC4421 provides independently settable current limit values for each input. On a given channel, the LTC4421 regulates the maximum voltage across the SENSE and OUT pins to 25mV (ΔV_{SNS}). Connect a sense resistor R_{SENSE} between SENSE and OUT to set the current limit value I_{LIM}, is given by Equation 6.

$$I_{LIM} = \frac{25mV}{R_{SENSE}} \quad (6)$$

Ensure the input supply is capable of sourcing more current than I_{LIM}, so that the input supply does not drop out and cause UV motorboating. Use standard 1% resistor values and choose R_{SENSE} to set I_{LIM} at least 25% higher than the maximum output load current $I_{LOAD(MAX)}$ to account for tolerances in the current limit and to provide sufficient charging current to the output capacitor when charging the output.

I_{LIM} and C_{OUT} set the rate at which the output voltage will rise.

The minimum output rise rate is shown by Equation 7.

$$\frac{dV_{OUT}}{dt}(min) = \frac{\left(I_{LIM} - I_{LOAD(MAX)}\right)}{C_{OUT}} \quad (7)$$

Equation 7 assumes that the output voltage is charging under maximum output load current conditions, so that only the difference between the programmed current limit current and the maximum DC load current is available to charge C_{OUT}. **It is essential to set I_{LIM} to ensure that the output is fully charged before an overcurrent fault timeout occurs.**

The LTC4421 implements a stepped current limit foldback feature. A foldback comparator monitors the voltage on the OUT1 pin and reduces the current limit regulation voltage from 25mV (ΔV_{SNS}) to 12.5mV ($\Delta V_{SNS,FLD}$) for low OUT1 voltages, thereby cutting the current limit in half to reduce power consumption. The comparator rising and falling threshold voltages are 460mV ($V_{FLD,TH}$) and 410mV, respectively. When the OUT1 voltage is initially being powered up from 0V, the current limit regulation voltage is 12.5mV until OUT1 rises above 460mV, at which point it is increased to 25mV. **For output voltages below 460mV, ensure the maximum output load current is lower than the foldback current limit to ensure the output powers up.** When the OUT1 voltage is initially powered and then discharges, for example due to an input or output short circuit, the current limit regulation voltage will be 25mV until OUT1 drops below 410mV, at which point it is reduced to 12.5mV.

Use Kelvin connections from the R_{SENSE} terminals to the LTC4421's SENSE and OUT pins for best accuracy. Choose sense resistors having low inductance to minimize the sense resistor's impact on the current limit regulation loop stability. A single sense resistor can be used if the current limit is the same on both channels, as shown in Figure 3.

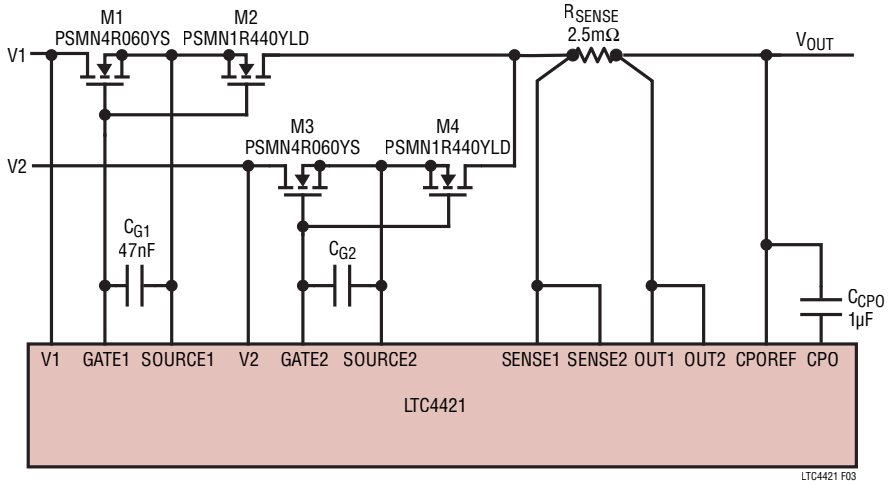


Figure 3. Using a Single Sense Resistor R_{SENSE} to Set the Same Current Limit for Both Channels

APPLICATIONS INFORMATION

Selecting the Output Capacitor

When switching connection to the output between the two input supplies, the LTC4421 utilizes break-before-make circuitry to ensure the first channel has completely disconnected from the output before the second turns on. This prevents current from flowing from one input to the other via the output, a phenomenon known as cross-conduction. As a result, there is a dead time during switchover when neither supply is powering the output.

Users must choose an output capacitance C_{OUT} to support the output load current and minimize the output voltage step and droop during switchover. When the first channel disconnects, a voltage step occurs at the output due to the load current flowing through C_{OUT}'s equivalent series resistance R_{ESR}. The magnitude of the voltage step is given by Equation 8.

$$V_{STEP} = (I_{LOAD} \bullet R_{ESR}) \quad (8)$$

For the duration of the dead time, the output voltage droops as the load current discharges C_{OUT}. The maximum magnitude of the droop is given by Equation 9.

$$V_{DROOP} = \frac{\left(I_{LOAD(MAX)} \bullet t_{G(SWITCH),MAX}\right)}{C_{OUT}} \quad (9)$$

Set C_{OUT} to optimize the trade-off between minimizing output voltage droop and minimizing the time required to fully charge the output from 0V. Set $V_{DROOP(MAX)}$ as high as possible; usually, $V_{DROOP(MAX)} \leq 0.1 \bullet V_{OUT}$ is acceptable. Typically, using 10µF to 50µF of output capacitance per Ampere of maximum load current achieves a reasonable trade-off.

Figure 4 shows an output voltage waveform during switchover for a system having 5A output load current and a 220µF output capacitor with 100mΩ R_{ESR}. When the first channel is turned off, the 5A load is provided by the 220µF capacitor. With 5A flowing through the 100mΩ R_{ESR}, V_{STEP} = 500mV. Following the ESR step, the output discharges at a rate dV/dt = 5A/220µF until the second channel is switched in.

Because of the high output currents, it is imperative to choose capacitors having very low ESR to minimize V_{STEP}. Also, consult the capacitor vendor's curves of capacitance versus DC bias voltage and capacitance versus temperature, and account for temperature and voltage coefficients of C_{OUT}.

Determining the Maximum Time to Charge the Output Voltage

Whenever the output is being charged from a lower voltage to a higher voltage, it charges in current limit. As a result, the overcurrent fault timer is running during charging. It is imperative to determine the maximum time $t_{(CHG,MAX)}$ required to charge the output and set the overcurrent fault time $t_{TMR,FLT} > t_{(CHG,MAX)}$. The maximum charge time is given by Equation 10.

$$t_{(CHG,MAX)} = \frac{\left(C_{OUT} \bullet V_{IN,MAX}\right)}{\left(I_{LIM} - I_{LOAD,CHG}\right)} \quad (10)$$

where $V_{IN,MAX}$ is the highest input voltage and $I_{LOAD,CHG}$ is the maximum DC load current present when C_{OUT} is being charged. The worst case occurs when $I_{LOAD,CHG}$ = $I_{LOAD,MAX}$. If possible, disable the output load current

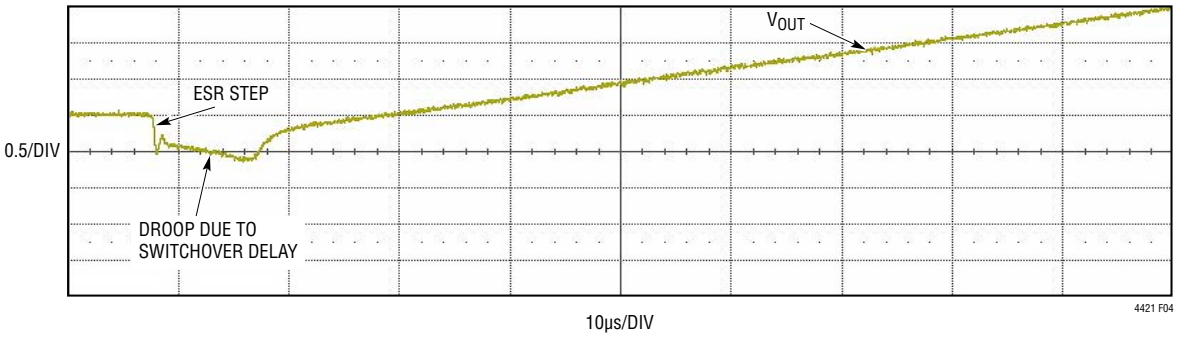


Figure 4. Output Voltage ESR Step and Linear Discharge During Channel Switchover

APPLICATIONS INFORMATION

when initially charging the output from 0V, so that $I_{LOAD,CHG}$ = 0. The application circuit in Figure 5 utilizes an LTC2965 voltage monitor on the output to disable the output DC/DC converter until V_{OUT} rises above 9V. Once V_{OUT} rises above 9V, the DC/DC remains enabled until V_{OUT} drops below 1V.

N-Channel MOSFET Selection

The LTC4421 drives N-Channel MOSFETs to conduct or block current from an input supply voltage and an output load current. The important features of the MOSFETs are:

1. BV_{DSS}, the absolute maximum drain-source voltage
2. $V_{GS,MAX}$, the absolute maximum V_{GS} voltage
3. $V_{GS(TH)}$, the threshold voltage
4. $R_{DS(ON)}$, the on-resistance
5. SOA, the safe operating area

The maximum allowable drain-source voltage, BV_{DSS}, must be higher than all supply voltages, as there are various scenarios where the output voltage can be at the highest supply voltage when the input is at 0V, and vice versa. Additionally, it must be higher than the clamping voltage of Transient Voltage Suppressor (TVS) diodes D1 and D2. Supplies with high input parasitic inductance may require additional precautions. See the Input and Output Short Circuits and Supply Transient Protection section for more information. Choose MOSFETs having $V_{GS,MAX}$ = ±20V, to handle the LTC4421's 14V maximum gate drive voltage.

When the back-to-back MOSFETs turn on and conduct current to the output, large drain-source voltages can occur on the input side MOSFET as the output is charging. However, the drain-source voltage of the output side MOSFET is limited to about 1V due to the body diode turning on, so the output side MOSFET is always in triode. As a result, the input side MOSFET has much more stringent SOA requirements. A MOSFET with lower SOA and lower $V_{GS(TH)}$ can be used on the output side to minimize power loss in that MOSFET.

The chosen MOSFET must be able to withstand an output short circuit for longer than $t_{TMR,FLT}$. During output shorts, the LTC4421 regulates the short-circuit current using its current limit regulation circuitry and runs the overcurrent fault timer. When the short persists longer than the programmed $t_{TMR,FLT}$ time, the LTC4421 turns off the MOSFETs. The worst-case occurs when the output is resistively shorted and the output voltage, V_{SHORT}, remains above the foldback comparator falling threshold voltage, which is 410mV. In this case, the power during the short circuit is given in Equation 11.

$$POWER \approx V_{IN} \bullet I_{LIM} = \frac{(V_{IN} \bullet 25mV)}{R_{SENSE}} \quad (11)$$

where V_{IN} is in the input voltage and $V_{IN} >> V_{SHORT}$.

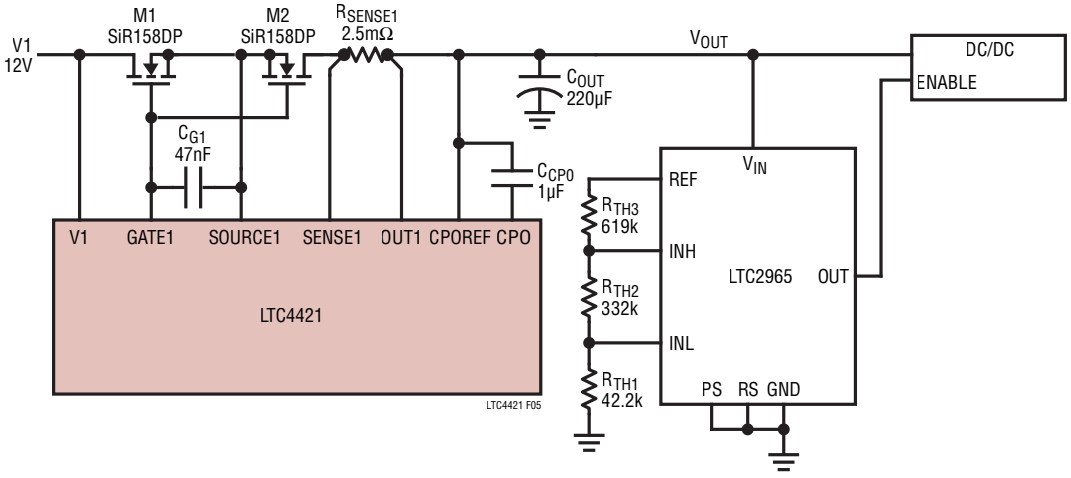


Figure 5. Load Current Hold Off. The LTC2965 Voltage Monitor Disables the DC/DC Output Load Current Until V_{OUT} > 9V

APPLICATIONS INFORMATION

After calculating the power, refer to the SOA curves in the MOSFET manufacturer's data sheet. The SOA curves are usually specified at 25°C and must be adjusted to account for the highest operating ambient temperature T_A as given by Equation 12.

$$SOA(T_A) = SOA(25°C) \bullet \frac{(T_{JMAX} - T_A)}{(T_{JMAX} - 25°C)} \quad (12)$$

Where T_{JMAX} is the maximum allowed junction temperature of the MOSFET. Most of the recommended MOSFETs have T_{JMAX} =175°C. As a result, multiply the y-axis values of the SOA curves by 0.6 for T_A = 85°C, and multiply by 0.333 for T_A = 125°C.

Note that MOSFET data sheets usually show a family of 5-6 SOA curves, with each curve separated from the next by a factor of 10 in time (e.g., 100µs, 1ms, 10ms, etc.). To be conservative, choose the time curve closest to and higher than $t_{TMR,FLT}$ and make sure the MOSFET can handle the power in Equation 11.

When the output is hard-shorted to ground, such that the output voltage is below 410mV, the LTC4421 implements a stepped foldback feature, reducing the short circuit current, and hence the power, by a factor of two. As a result, the LTC4421 provides more SOA margin for the MOSFET for hard shorts than resistive shorts. See procedures outlined in this section and the SOA curves in the chosen MOSFET manufacturer's data sheet to verify suitability for the application.

Overcurrent Faults and Retry

The LTC4421 features an adjustable current limit that protects against output short circuits and excessive load current. An overcurrent fault occurs when the current limit circuitry has been engaged for longer than the time set by the TMR pin. When the output load current is less than I_{LIM}, the LTC4421 pre-biases the TMR pin voltage to its DC TMR Parking Voltage. When the LTC4421 is regulating the output current to I_{LIM}, it sources 6µA out of the TMR pin to charge the external TMR capacitor. When the TMR pin voltages increases by 500mV from the TMR Parking Voltage, an overcurrent fault occurs. The $\overline{FAULT}$ open-drain output pull-down pin is latched low, and the input is disconnected from the output. Connect a capacitor C_{TMR} between TMR and ground and use Equation 13 to set the overcurrent fault time $t_{TMR,FLT}$.

$$t_{TMR,FLT} = C_{TMR} \bullet 83[\mu s/nF] \quad (13)$$

Note that pulsed current loads exceeding the programmed current limit and having duty cycle > 25% will integrate over time and cause a current limit fault.

After an overcurrent fault occurs, the subsequent functionality depends on the configuration of the $\overline{DISABLE}$, $\overline{FAULT}$ and RETRY pins. Figure 6 shows a timing diagram for an overcurrent fault occurring on Channel 1 where the RETRY pin is set low, $\overline{FAULT1}$ is pulled up to a supply voltage with a 100k resistor and the user drives $\overline{DISABLE1}$ with a digital signal. For simplicity, there is no input supply connected to V2.

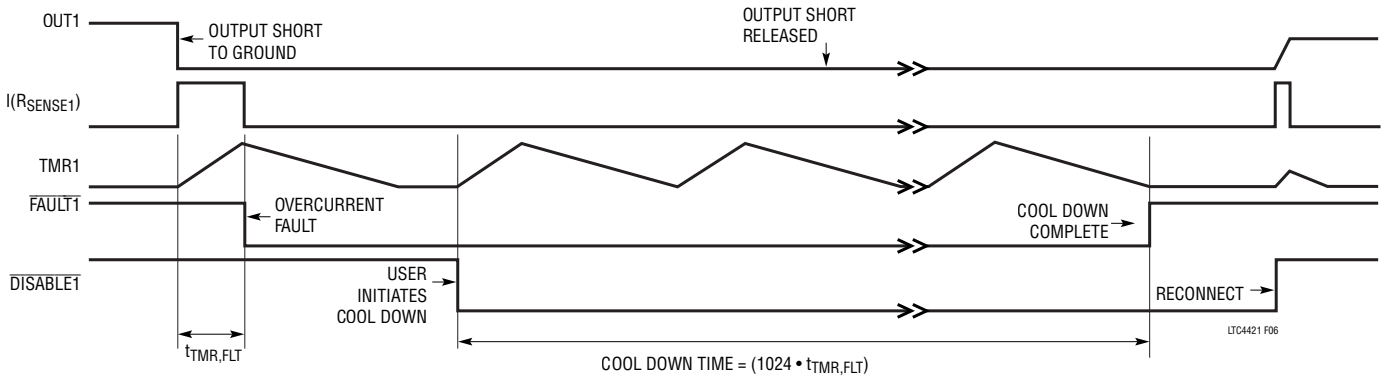


Figure 6. Manual Retry after Overcurrent Fault on Channel 1. Conditions: RETRY = 0V, User Driven $\overline{DISABLE1}$ and Output Short Released During Cool Down Time

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When output voltage OUT1 is shorted to ground, the LTC4421 limits the current $I(R_{SENSE1})$ flowing in the sense resistor and simultaneously sources 6µA out the TMR1 pin to charge the C_{TMR1} capacitor. At time $t_{TMR,FLT}$ after the short, an overcurrent fault occurs as described above, and the LTC4421 drives $\overline{FAULT1}$ low. The user detects $\overline{FAULT1}$ being low and drives $\overline{DISABLE1}$ low to initiate the cool down cycle.

In this example, the short circuit is released during the cool down cycle, as indicated in the waveforms. Because V1 is disconnected from the output, the output voltage remains low when the short is released. At the end of cool-down, $\overline{FAULT1}$ releases high and the input is allowed to reconnect to the output. Driving $\overline{DISABLE1}$ high reconnects Channel 1's input to the output. With the output short removed, the output successfully powers up, and no further faults occur. **Note: driving $\overline{DISABLE1}$ low-to-high at any point in the cool down cycle asynchronously terminates the cool down cycle and allows reconnection to the output. It is strongly recommended not to terminate the cool down cycle early, as the MOSFETs may not have sufficient time to cool down, and the subsequent overcurrent fault time may be significantly shorter than the time set by the TMR pin.**

Figure 7 shows the functionality with RETRY = 0V, but with the $\overline{FAULT1}$ pin connected to $\overline{DISABLE1}$. In this case the user does not drive $\overline{DISABLE1}$. When the overcurrent fault occurs, the $\overline{FAULT1}$ pin is driven low. Because $\overline{FAULT1}$ is connected to $\overline{DISABLE1}$, $\overline{DISABLE1}$ also pulls low, initiating the cool down cycle. At the end of the cool down cycle, the LTC4421 releases $\overline{FAULT1}$ high, which drives $\overline{DISABLE1}$ high, causing the V1 input supply to reconnect to the output, a process called "auto-retry". This process repeats indefinitely until the output short is removed. In this example, the output short is released during the second cool down cycle, so the output voltage successfully powers up on the third connection.

Figure 8 shows the functionality with $\overline{DISABLE1}$ pulled high, $\overline{FAULT1}$ pulled up to a supply voltage with a 100k resistor but not connected to $\overline{DISABLE1}$, and RETRY set high. In this example, we are leaving the output shorted permanently. In this case, the LTC4421 reconnects the V1 supply 6 additional times after the first overcurrent fault occurs. Each reconnection results in an overcurrent fault, followed by a cool down cycle. After a total of 7 faults, the LTC4421 keeps the inputs disconnected from the output until the $\overline{DISABLE1}$ is toggled low, then high.

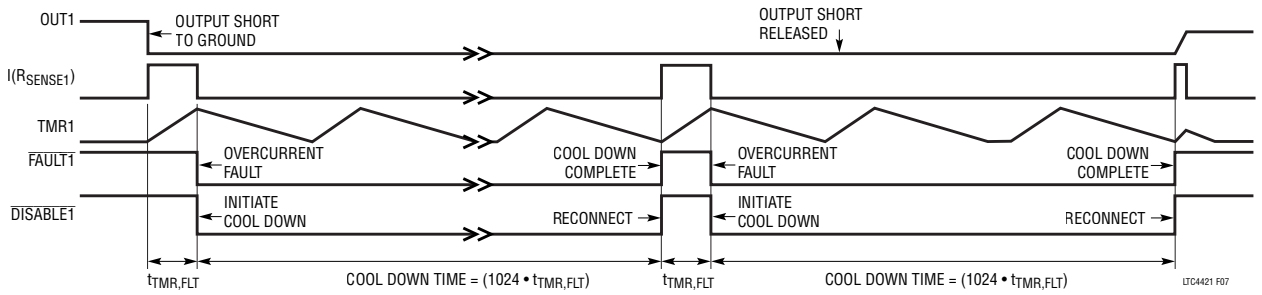

Figure 7. Auto-Retry After Overcurrent Fault on Channel 1. Conditions: RETRY = 0V, $\overline{FAULT1}$ Connected to $\overline{DISABLE1}$ and Output Short Released During Second Cool Down Time

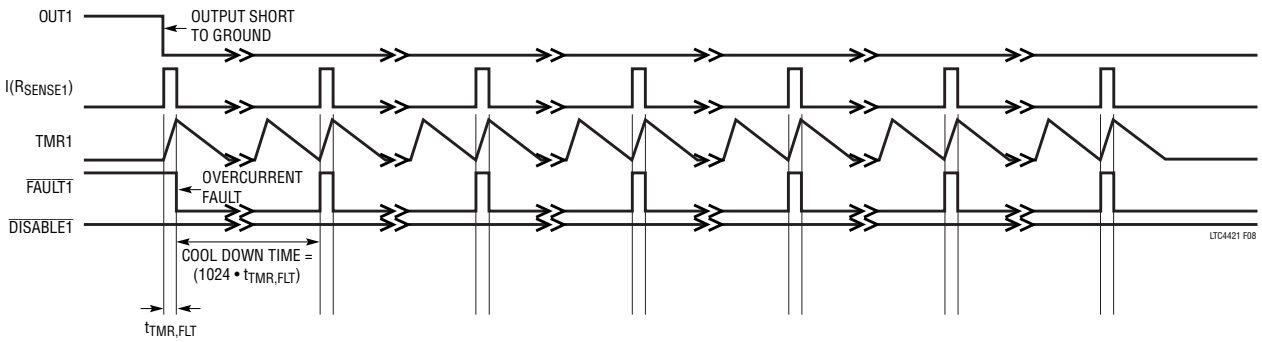

Figure 8. 6 Retries After Overcurrent Fault on Channel 1. Conditions: RETRY = 3V, $\overline{DISABLE1}$ = 4V and Output Short Never Released

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The overcurrent fault times are independently settable for each channel. Set the time to ensure the output can charge from 0V to the maximum input voltage, as described above. Whenever Channel 1 experiences a current limit fault, Channel 2 is allowed to power the output, presuming Channel 2 is valid. Channel 2 powers the output until the fault on Channel 1 is cleared.

The RETRY count of 6 counter on a channel is reset whenever its input supply is invalid, its $\overline{DISABLE}$ is driven low, or a higher priority supply becomes valid. It is also reset when $INTV_{CC}$ is below the $INTV_{CC}$ GOOD Threshold Voltage and CPO is below the CPOGOOD Threshold Voltage. Toggling the RETRY pin low, then high also resets the counter.

Iterating the Application Circuit Solution for MOSFET SOA

If the selected MOSFET does not meet the SOA requirements imposed by the initial current limit and output capacitor values, take one or more of the following steps:

1. Reduce $t_{TMR,FLT}$ to meet the MOSFET SOA requirements. This requires reducing $t_{(CHG,MAX)}$ from Equation 10 to ensure $t_{TMR,FLT} > t_{(CHG,MAX)}$. One way to do this is to reduce C_{OUT}. The trade-off is an increase in output voltage droop during channel switchover.
2. Reduce $t_{TMR,FLT}$ and $t_{(CHG,MAX)}$ by increasing the current limit I_{LIM}. This is only helpful if the reduction in $t_{(CHG,MAX)}$ provides a larger SOA benefit than the SOA loss caused by the increased power dissipated in the MOSFET. For example, assume I_{LIM} = 11A and $I_{LOAD,CHG}$ = 10A. Using Equation 14.

$$t_{(CHG,MAX)} = \frac{(C_{OUT} \bullet V_{IN,MAX})}{11A - 10A} = \frac{(C_{OUT} \bullet V_{IN,MAX})}{1A} \quad (14)$$

If I_{LIM} is then increased from 11A to 20A, the new result is given by Equation 15.

$$t_{(CHG,MAX)} = \frac{(C_{OUT} \bullet V_{IN,MAX})}{20A - 10A} = \frac{(C_{OUT} \bullet V_{IN,MAX})}{10A} \quad (15)$$

With $t_{(CHG,MAX)}$ reduced by a factor of 10, we can reduce $t_{TMR,FLT}$ by a factor of 10. By doubling I_{LIM}, the maximum power during output short circuits has doubled, but $t_{(CHG,MAX)}$ has decreased by a factor of 10, so there is a net reduction in the SOA stress. Be sure the input power supply is capable of sourcing more current than the new, higher value of I_{LIM}. Also, ensure the new I_{LIM} does not cause UV motorboating.

3. Choose a MOSFET with higher SOA. Look for MOSFET's having high BV_{DSS}, as they usually have better SOA performance.

Charge Pump and Gate Driver Circuitry

The gate drive is provided by a charge pump circuit that powers CPO. A curve of GATE pin voltage versus output voltage is shown in the Typical Performance Characteristics curves. For output voltages less than 4V, the minimum gate drive voltage is 9V. When the output voltage is higher than 5V, the gate drive is at least 10V. A burst mode comparator ensures the gate drive never exceeds 14V.

When an input supply is invalid, the LTC4421 drives the GATE pin voltage close to ground using a 50mA pull-down current. When a supply is valid but turned off, gate driver parking circuitry regulates the GATE voltage to 1V below the lower of the channel input voltage and the output voltage. This is called the GATE Parking Voltage. The LTC4421 also sinks 5µA from the SOURCE pin to bias the external MOSFETs at their threshold voltages, to minimize the ΔV_{GS} and hence the turn-on time during channel switchover when the MOSFETs are turned back on. If possible, choose a lower threshold MOSFET for the output MOSFET to preferentially draw the SOURCE current from V_{OUT} instead of the input supply of the off channel, and add a resistor from SOURCE to ground to increase current and hence the V_{GS}.

CPO Charge Pump Capacitor Selection

Connect a reservoir capacitor C_{CPO} between CPO and CPOREF to provide the charge necessary to turn on the MOSFETs quickly. The recommended value is approximately 10× the combined input C_{ISS} capacitances of the two back-to-back MOSFETs on one channel, plus any discrete GATE-to-SOURCE capacitor C_G that has been added to stabilize the current limit loop. A larger C_{CPO} capacitor

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takes a correspondingly longer time to charge up by the internal charge pump, resulting in longer delays from initial power-up of the first input supply to first connection to the output. A smaller capacitor suffers more voltage drop during a channel turn-on event as it shares charge with C_G and the MOSFET C_{ISS} capacitances. Given the limited charging capability of the charge pump, continuously changing channels at rates higher than 80Hz (typical) eventually depletes the C_{CPO} capacitor, causing disconnection of both inputs from the output. At that point, the charge pump charges the C_{CPO} capacitor above 6.7V, the inputs are then allowed to reconnect to the output, and the process repeats.

Analog Current Limit Loop Stability

The active current limit loop is compensated by adding a capacitor C_G between the gate and source of the external MOSFETs. Choosing 47nF for C_G ensures stability for all recommended MOSFETs. In addition, add a snubber from the input supply to ground consisting of resistor R_{SN} in series with capacitor C_{SN}. Choose R_{SN} using Equation 16.

$$R_{SN} = \frac{V_{IN}}{I_{LIM}} \quad (16)$$

where V_{IN} is the maximum input supply voltage and I_{LIM} is the current limit being set by R_{SENSE}. Setting C_{SN} to 10µF works well for all applications. Applications having small input inductance and low output load current may use values as low as 1µF for C_{SN}.

Setting Qualification Time for Validity

The QUAL pin sets the amount of time a supply must be inside the OV, UV voltage window to be valid. Connect a capacitor C_{QUAL} from QUAL to ground and use Equation 17 to set the validation time:

$$t_{VALID} = C_{QUAL} \bullet 16[ms/nF] \quad (17)$$

where t_{VALID} is the validation time. Note that the validation time is the same for both channels. To set a fixed qualification time of 3.5µs, connect QUAL to $INTV_{CC}$ instead of connecting a capacitor to ground.

If possible, set a qualification time on the order of 10ms or longer. This allows the LTC4421's gate driver parking circuitry to pre-bias the GATE1 voltage to its GATE Parking Voltage when hot-plugging the V1 input supply. This will reduce switchover time and hence output voltage droop when switching from Channel 2 to Channel 1.

Optional Charge Pump Pre-Charge Circuit

The LTC4421 prevents the input supplies from being validated and powering the output until the external C_{CPO} capacitor voltage is charged to 6.7V ($V_{CPO(UVL)}$) above the higher of the CPOREF and $INTV_{CC}$ voltages. With a typical C_{CPO} capacitor of 1µF, the charge pump voltage may take several hundred milliseconds to charge to 6.7V. For input supplies ≥ 12V, this time can be shortened by pre-charging the CPO pin with the circuit shown in Figure 9. The 12V Zener diode Z1 and NPN transistor Q1 are used to quickly charge the CPO voltage to about 10.8V above ground. For V1, V2 voltages below 12V, the circuit pre-charges CPO to a voltage approximately 1.8V below the higher of the V1 and V2 voltages. Diode D3 prevents reverse current conduction when an input supply is connected to V_{OUT} and causes the CPO voltage to rise above 9V. Diodes D1 and D2 form a diode-OR circuit that powers the Z1 and Q1 from the higher of the V1 and V2 input supply voltages.

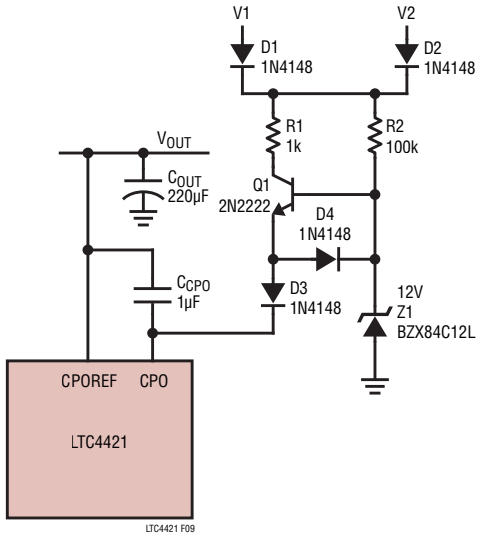

Figure 9. Optional CPO Pre-Charge. The Higher Voltage of Input Supplies V1 and V2 Pre-Charges the CPO Voltage to Reduce System Power-Up Time

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Minimizing Bias Current Draw from Lower Priority Supplies

In order to minimize current draw from lower priority power sources, the LTC4421 draws the vast majority of its supply current from the highest priority available supply. When $\overline{SHDN}$ is high and $EXTV_{CC}$ is connected to the system output voltage, the LTC4421 consumes 600µA from the supply powering the output and only 10µA to 26µA from the other supplies. When $\overline{SHDN}$ is low, the 6µA (typical) is drawn from the highest of the V1, V2, $EXTV_{CC}$ and OUT1 voltages, and the supply current in each of the other, lower voltage pins is a miniscule 250nA.

Digital Status Outputs $\overline{VALID1}$, $\overline{VALID2}$, $\overline{CH1}$, $\overline{CH2}$

The LTC4421 provides open-drain pull-down digital outputs to provide system status information. The $\overline{VALID1}$ and $\overline{VALID2}$ pins pull low when their respective V1 and V2 input supplies have been validated. The $\overline{CH1}$ and $\overline{CH2}$ pins pull low when their input supply is connected to the output voltage. Connect large value pull-up resistors between these pins and $INTV_{CC}$ to provide the logic high, taking care not to exceed the 500µA maximum current draw from $INTV_{CC}$. The pull-downs are capable of driving low power LED's, but they cannot be pulled up to $INTV_{CC}$ in that case due to the LED current required. When using LED's, power the pull-up from a supply voltage up to 36V.

These outputs can be used in conjunction with the $\overline{DISABLE}$ pins in a variety of application circuits to change V1, V2 priority over time. For example, consider what happens when $\overline{CH2}$ is connected to $\overline{DISABLE1}$. Once V2 is connected to the output, it will continue to power the output regardless of V1's validity. In effect, V2 became the higher priority supply, but only after it connected to the output. This configuration can be used in systems where, after switching to the secondary supply, it is desirable to run the secondary supply to full discharge before re-connecting to the primary. For proper operation at power up, it is essential that Channel 1 becomes valid before Channel 2.

In Figure 10, logic gates U1 and U2 disable channel 1 whenever V2 is valid, enabled and does not have a latched overcurrent fault. Disabling channel 1 disconnects V1 from the output and allows V2 to connect to the output. This configuration permanently flips V1 and V2 priority, so that V2 is always the higher priority input.

In Figure 11, inverter U1 is used to connect the logically inverted $\overline{VALID2}$ signal to $\overline{DISABLE1}$. This configuration prevents Channel 1 from connecting to the output whenever Channel 2 is invalid. This prevents the primary input from powering the output unless a valid secondary supply is available to power the output when the primary fails.

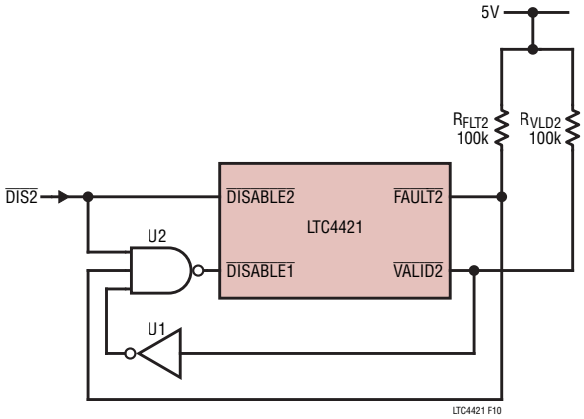

Figure 10. Flip Priority. Two External Logic Gates Are Used to Flip Priorities of Channel 1 and Channel 2

Input and Output Short Circuits and Supply Transient Protection

When an input supply powering the output is shorted to ground, the LTC4421 senses reverse current through the sense resistor. When the reverse voltage developed

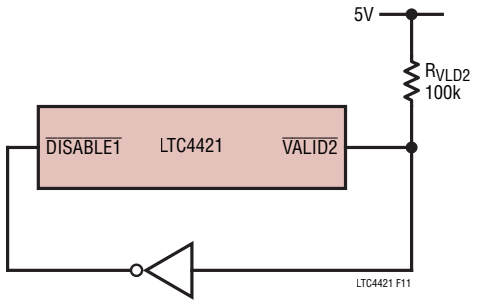

Figure 11. Valid Secondary Required. Preventing the Primary Input Supply from Powering the Output Unless a Valid Secondary Supply Is Present

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across the sense resistor exceeds 30mV, the LTC4421 sinks 50mA from the GATE pin of the shorted channel to turn off the N-Channel MOSFETs, thereby disconnecting the input from the output. Assuming the input is still valid, reconnection occurs when the output voltage drops 35mV below the input.

When the output is shorted to ground, the voltage across the sense resistor may exceed 25mV until the current limit loop enters regulation. When the forward voltage across the sense resistors exceeds 50mV, the LTC4421 sinks 50mA from the GATE pin to quickly reduce the V_{GS} of the N-Channel MOSFETs. The 50mA sink current is turned off when the voltage across the sense resistor falls below 25mV.

When the output is shorted to ground, the current limit circuitry will regulate the current to I_{LIM}. When the current limit circuitry has been engaged for longer than the time set by the TMR pin, a current limit fault is registered. The input is disconnected from the output, and $\overline{FAULT}$ is driven low.

For large input and output inductances, rapid changes in current during short circuit events and channel turn-off can cause transient voltages that exceed the Absolute Maximum ratings of the input and output pins and/or violate the BV_{DSS} limits of the external MOSFETs. To minimize such transients, use wider PCB traces and heavier trace plating to reduce power trace inductance. External to the PCB, twist the power and ground wires together to minimize inductance. Although the input snubber helps dissipate the input inductive energy at channel turn-off, transient voltage suppressor (TVS) D1 is still needed to clamp the peak input voltage, as shown in Figure 12. When selecting transient voltage suppressors, ensure the reverse standoff voltage (V_R) is equal to or greater than the application operating voltage, the peak pulse current (I_{PP}) is higher than the peak transient voltage divided by the source impedance, and the maximum clamping voltage (V_{CLAMP}) at the rated I_{PP} is less than the Absolute Maximum ratings of the LTC4421 and the BV_{DSS} of the external MOSFETs. The LTC4421's Absolute Maximum Voltage Ratings of V1 and V2 allow it to withstand supply side inductive voltage spikes up to 60V. A range of TVS's can be used accommodating V_R ratings up to 36V and V_{CLAMP} ratings up to 60V.

Cascading

Multiple LTC4421's can be cascaded to prioritize more than two input supplies. To prioritize three or four supplies, use two LTC4421's with their OUT pins connected together, and connect CASOUT of the higher priority

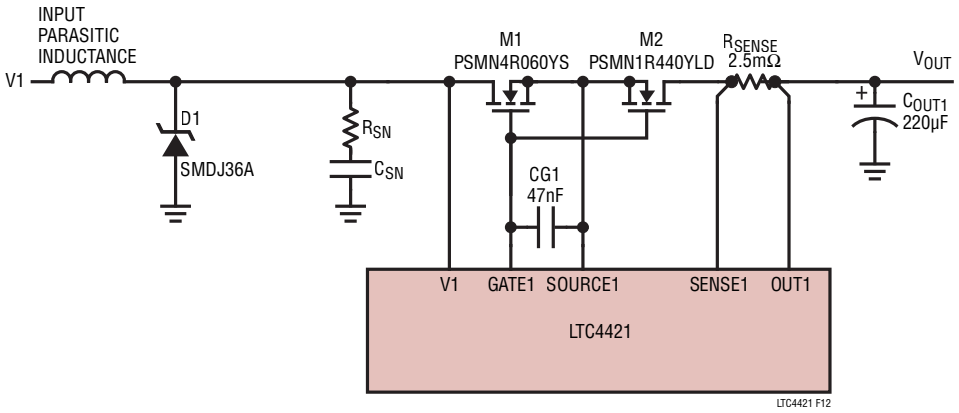

Figure 12. Supply Voltage Transient Suppression Circuitry

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master LTC4421 to CASIN of the lower priority slave LTC4421, as shown in Figure 13.

When both master input supplies are invalid, the master verifies that it has disconnected both supplies from the output before driving its CASOUT pin high. This ensures the reverse conduction paths from the output back to the master inputs are blocked before the slave is allowed to power the output. The master LTC4421 pulls CASOUT up to $INTV_{CC}$ using a 20µA current source, allowing the slave LTC4421 to connect its highest priority valid supply to the output.

When the slave is powering the output and one of the master's inputs becomes valid, the master simultaneously connects its valid channel to the output and drives its CASOUT pin low to force the slave to disconnect its inputs. To prevent cross conduction, make the connection between the master's CASOUT and slave's CASIN as short as possible. This minimizes the capacitance of the connection and hence the turn-off delay of the slave channel.

This scheme can be extended to prioritize as many input supplies as necessary. Connect each additional lower priority LTC4421's OUT pins to the common output voltage and connect its CASIN pin to the CASOUT pin of the next higher priority LTC4421. Note that driving the master LTC4421's CASIN pin low disconnects all input supplies in the system. Driving the master's $\overline{DISABLE1}$ and $\overline{DISABLE2}$ pins low disconnects the master's inputs from the output and allows the slave LTC4421's to connect to the output.

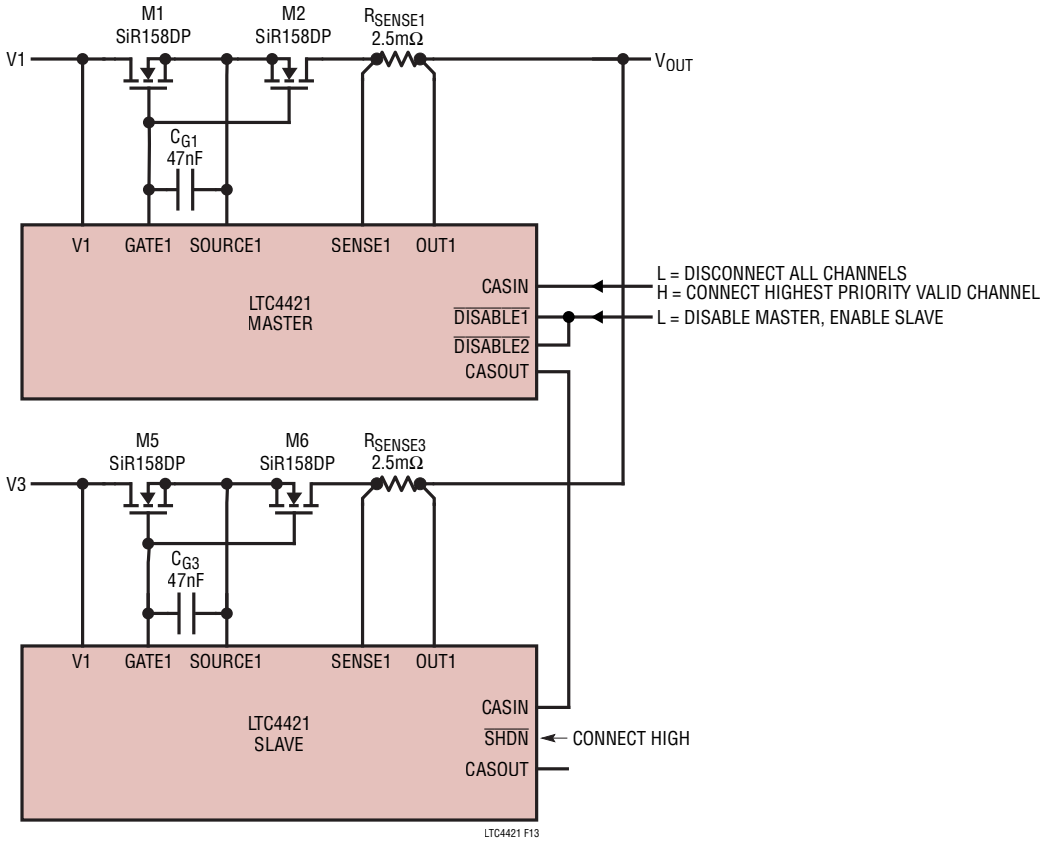

Figure 13. Using Two LTC4421's in a Cascading Application to Prioritize Four Input Supplies. (The Master and Slave V2 Power Paths are Omitted for Clarity)

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Design Example

As a design example, take the following specifications for the circuit in Figure 14. For simplicity, the same specifications and hence the same component values are used for each channel. The application is rated for an input voltage of 12V, maximum output load current of 8A, UV rising = 11V, UV falling = 8V, OV Rising = 15V and maximum output voltage drop during switchover = 1.2V (10% of the input supply voltages). The minimum and maximum operating ambient temperatures are –40°C and 85°C, respectively.

Start by setting the current limit to 16A, so that the output voltage can be charged at full DC load conditions in a reasonable amount of time as shown by Equation 18 (from Equation 6).

$$R_{SENSE} = \frac{25mV}{16A} = 1.5625m\Omega \quad (18)$$

The nearest standard value sense resistor is 1.5mΩ, which results in a current limit of 16.7A.

Choose an electrolytic output capacitor having R_{ESR} = 50mΩ. During switchover is given by Equation 19 (from Equation 8).

$$V_{STEP} = (8A \bullet 50m\Omega) = 400mV \quad (19)$$

To keep the total output voltage drop during switchover to less than 1.2V, the maximum droop must be ≤ 800mV. Therefore is given by Equation 20 (from Equation 9).

$$C_{OUT} \geq \frac{(8A \bullet 15\mu s)}{800mV} = 150\mu F \quad (20)$$

so we choose C_{OUT} = 220µF for margin.

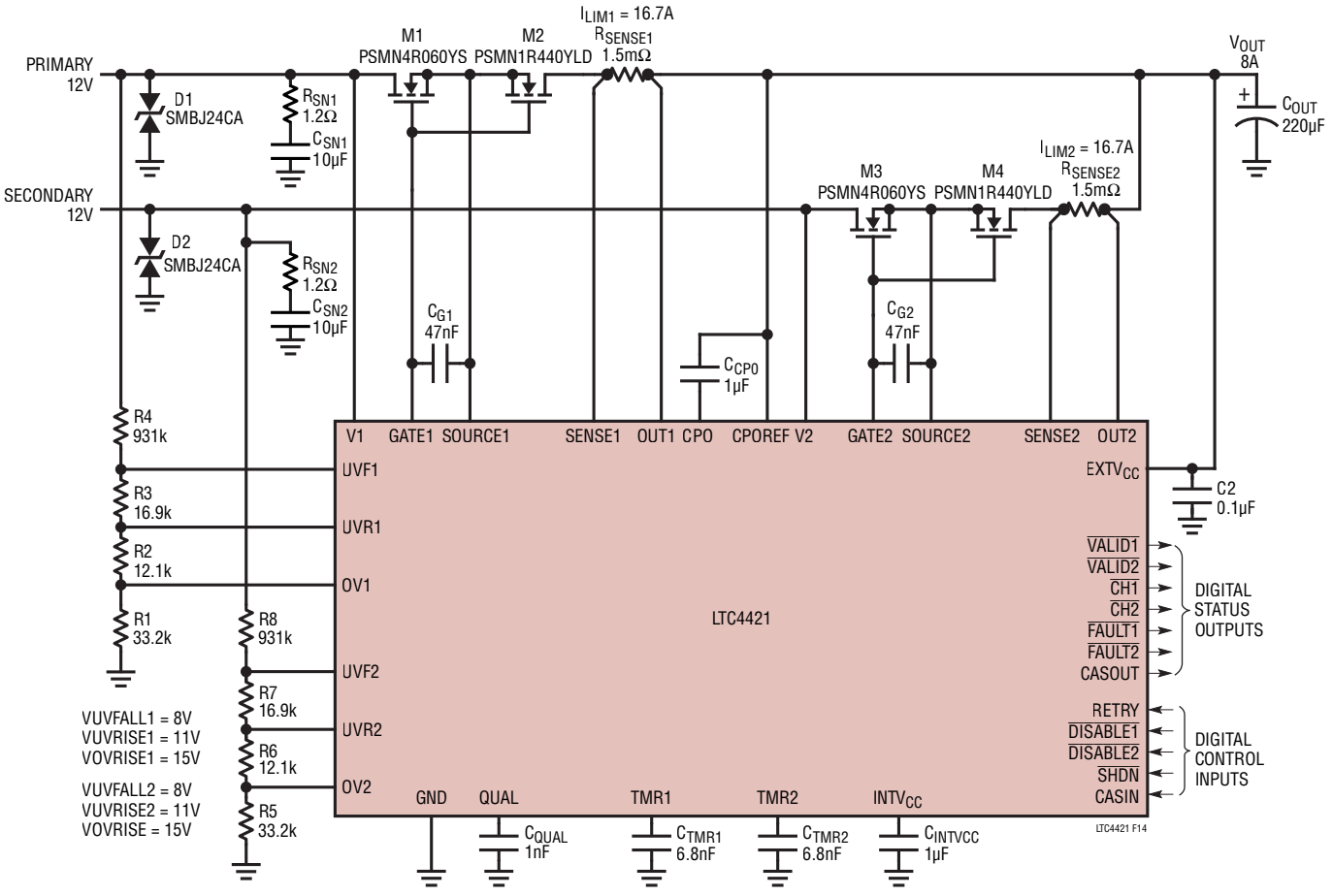

Figure 14. Dual 12V, 8A Application Circuit for Design Example

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Next, calculate the time it takes to charge the output voltage from 0V to 12V at the maximum DC load current as shown in Equation 21 (from Equation 10).

$$t_{CHG(MAX)} = \frac{(220\mu F \bullet 12V)}{(16.7A - 8A)} = 303\mu s \quad (21)$$

To ensure the output will fully charge before triggering an overcurrent fault time-out, choose C_{TMR1} to set $t_{TMR,FLT}$ = 450µs. See Equation 22 (from Equation 13).

$$C_{TMR1} = \left(\frac{450\mu s}{83[\mu s/nF]}\right) = 5.4nF \quad (22)$$

Using the nearest standard value and accounting for tolerance, we choose 6.8nF, which yields $t_{TMR,FLT}$ = 564µs.

The power dissipation during short circuits is given by Equation 23 (from Equation 11).

$$Power = (12V \bullet 16.7A) = 200W \quad (23)$$

Referring to the SOA curves in the PSMN4R060YS data sheet, the MOSFET can withstand 720W for 1ms at 25°C and 12V. Derating the SOA for the maximum operating temperature is given by Equation 24 (from Equation 12).

$$SOA(85°C) = 720W \bullet \frac{(175-85)}{(175-25)} = 432W \text{ at } 1ms \quad (24)$$

Our overcurrent fault time-out will occur for 200W at 564µs, so the requirement is satisfied.

Next, select 47nF capacitors C_{G1} and C_{G2} to compensate the current limit regulation loops of channels 1 and 2, respectively. D1 and D2 are bidirectional Transient Voltage Suppression (TVS) diodes that clamp the input voltages below 40V at channel turn-off, thereby protecting the LTC4421 and the N-Channel MOSFETs.

The OV, UV monitoring resistors should be chosen to yield a total divider resistance of between 1MΩ and 2MΩ for both low power and good transient response time. Using Equation 1 through Equation 4 and rounding up to the nearest 1% accurate standard resistor values, R1-R4 are calculated by Equation 25.

$$Choose\ R1 + R2 + R3 + R4 = 1000k\Omega \quad (25)$$

From Equation 2, R1 = (0.5/15) • 1000kΩ = 33.3kΩ. The nearest standard resistor value is 33.2kΩ.

From Equation 3, R2 = (15/11 – 1) • 33.2kΩ = 12.07kΩ. The nearest standard value is 12.1kΩ.

From Equation 4, R3 = (11/8 – 1) • (15/11) • 33.2kΩ = 16.98kΩ. The nearest standard value is 16.9kΩ.

From Equation 5, R4 = (15/0.5 – 1) • 33.2kΩ – 12.1kΩ – 16.9kΩ = 933.8kΩ. The nearest standard value is 931kΩ.

From Equation 17, C_{QUAL} is set to 1nF to set an OV, UV validation time of 16ms. This gives the LTC4421 time to pre-charge the GATE1 voltage to minimize turn-on time when V2 is powering the output and the V1 input supply is plugged in.

PCB Layout Considerations

To achieve accurate current sensing, Kelvin connections are recommended for the sense resistors. The PCB layout for the sense resistors should be balanced and symmetrical to minimize wiring errors. In addition, the PCB layout for the sense resistors and power MOSFETs should include good thermal management techniques for optimal device power dissipation. Small resistances add up quickly in high current applications. Note that 1oz copper exhibits a sheet resistance of about 530µΩ/square. The minimum trace width for 1oz copper is 0.02" per amp (0.5mm per amp) to make sure the trace stays at a reasonable temperature. Using 0.03” per amp (0.8mm per amp) is recommended.

To improve noise immunity, put the OV, UVR, UVF resistive dividers close to the LTC4421 and keep traces to GND pin and the input supply pin short. It is also important to put C_{INTVCC}, the bypass capacitor for the $INTV_{CC}$ pin, as close as possible between $INTV_{CC}$ and GND. Place C_{CPO}, the charge pump reservoir capacitor, as close as possible between the CPO and CPOREF pins. Transient voltage suppressors D1 and D2 are located close to the LTC4421 and are connected between the input supply and ground using wide traces. Figure 15 shows a recommended PCB layout for a 2-layer board.

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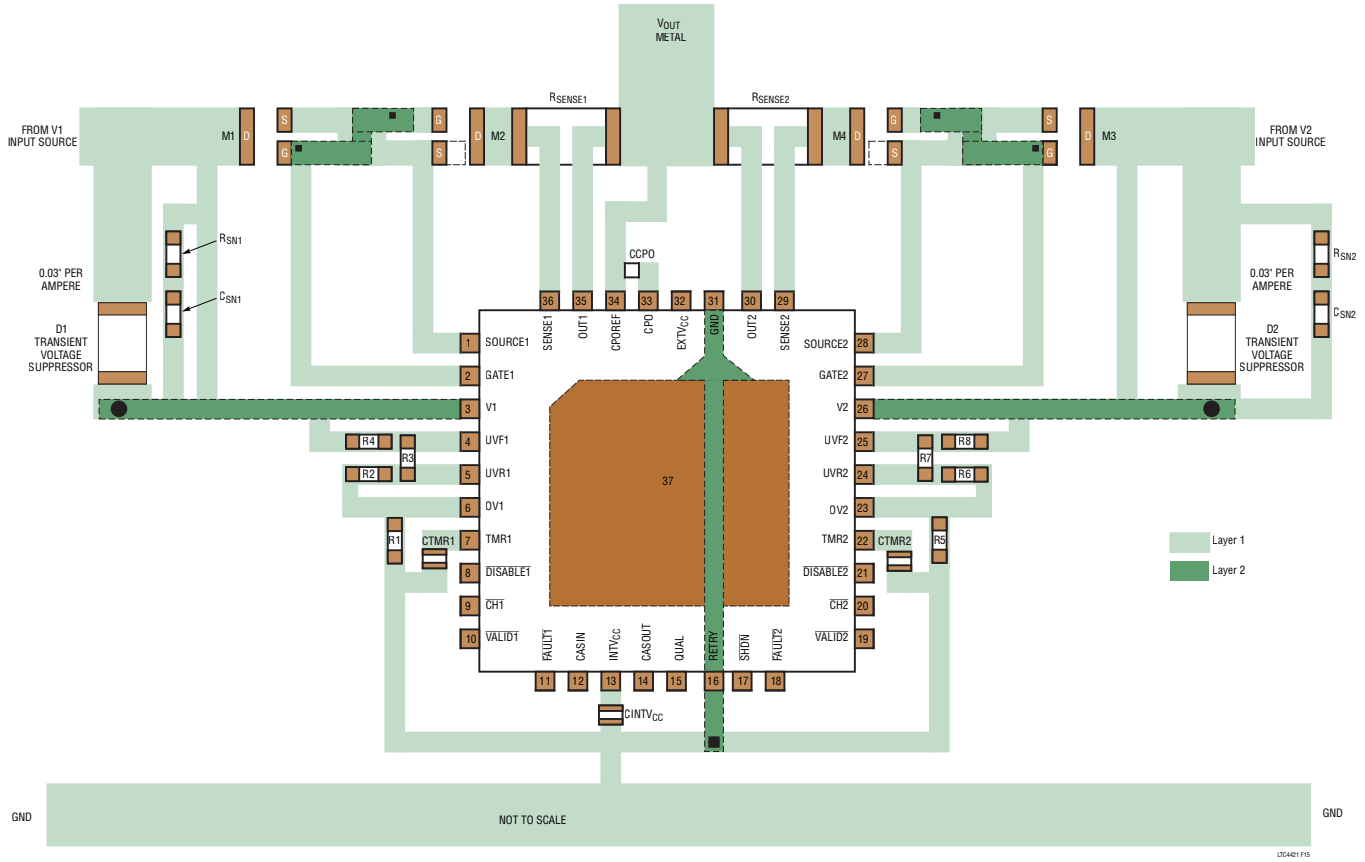


Figure 15. Recommended 2-Layer PCB Layout

Preventing Input Hold-Up During Unplug Events

Figure 16 includes a backplane connector with a kelvin sense. The resistive divider network that sets the OV and UV thresholds is connected to the kelvin sense. Disconnecting the supply powering V1 causes a nearly immediate UV fault, because there is no hold-up capacitance on the OV1, UVF1 or UVR1 pins. The output voltage discharges minimally before the UV fault occurs, as the output discharge rate is very slow compared to the UV fault time. Without a kelvin sense connection, upon input supply disconnection the resistive divider would stay connected to the drain of M1. The output, OV1, UVF1 and UVR1 pin voltages would all fall at the rate dictated by the output discharge, and the channel would not be disconnected until the output voltage dropped below the UVF1 threshold voltage.

SOA Doubler

Multiple LTC4421's can be used to control parallel MOSFET pathways from each input to the output, as shown in Figure 17. This is valuable in very high current applications to cut the SOA and load current carrying burdens of each MOSFET in half. LTC4421 #1 acts as a master and performs all monitoring functions, including OV, UV, fault and reverse current. After LTC4421 #2 drives the $\overline{\text{VALID12}}$ and $\overline{\text{VALID22}}$ signals low to indicate that it has successfully powered up, it acts as a slave to LTC4421 #1, turning its external MOSFETs on and off at LTC4421 #1's command. Connecting LTC4421 #1's $\overline{\text{CH1}}$ and $\overline{\text{CH2}}$ outputs through inverters U3 and U4 to LTC4421 #2's $\overline{\text{DISABLE1}}$ and $\overline{\text{DISABLE2}}$ inputs, respectively, synchronizes channel turn-on and turn-off of the two LTC4421's. NOR gates U1 and U2 prevent LTC4421 #1 from turning on its MOSFETs until LTC4421 #2's inputs are validated. This ensures that LTC4421 #1 never turns on its MOSFETs when LTC4421 #2 is unable to turn on its MOSFETs.

APPLICATIONS INFORMATION

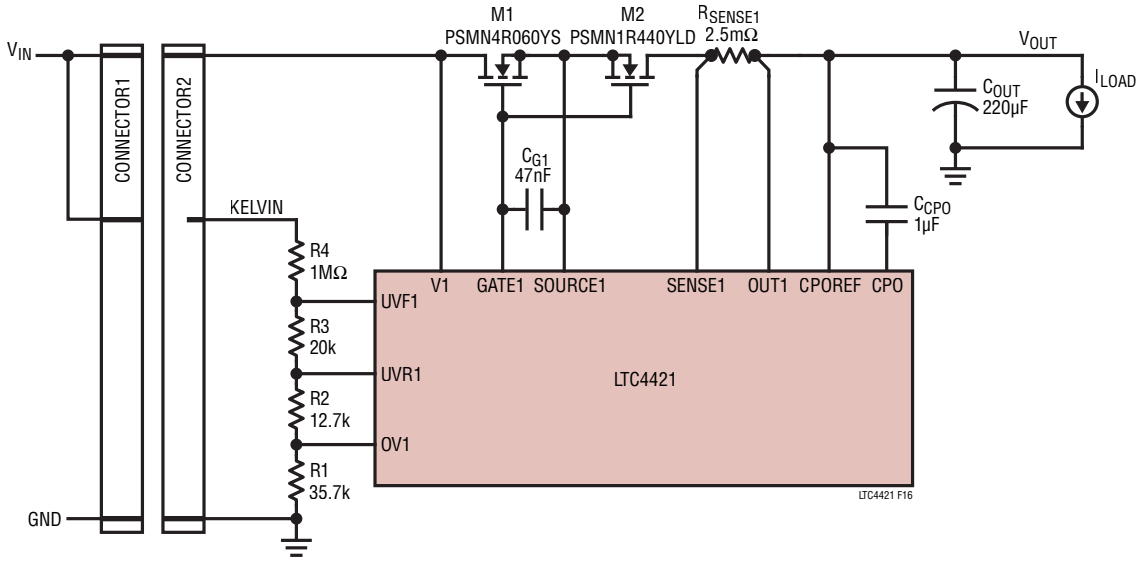


Figure 16. Preventing Input Hold-Up During Unplug Events with a Staggered Connector to Decouple OV and UV Pins from V_{OUT}

APPLICATIONS INFORMATION

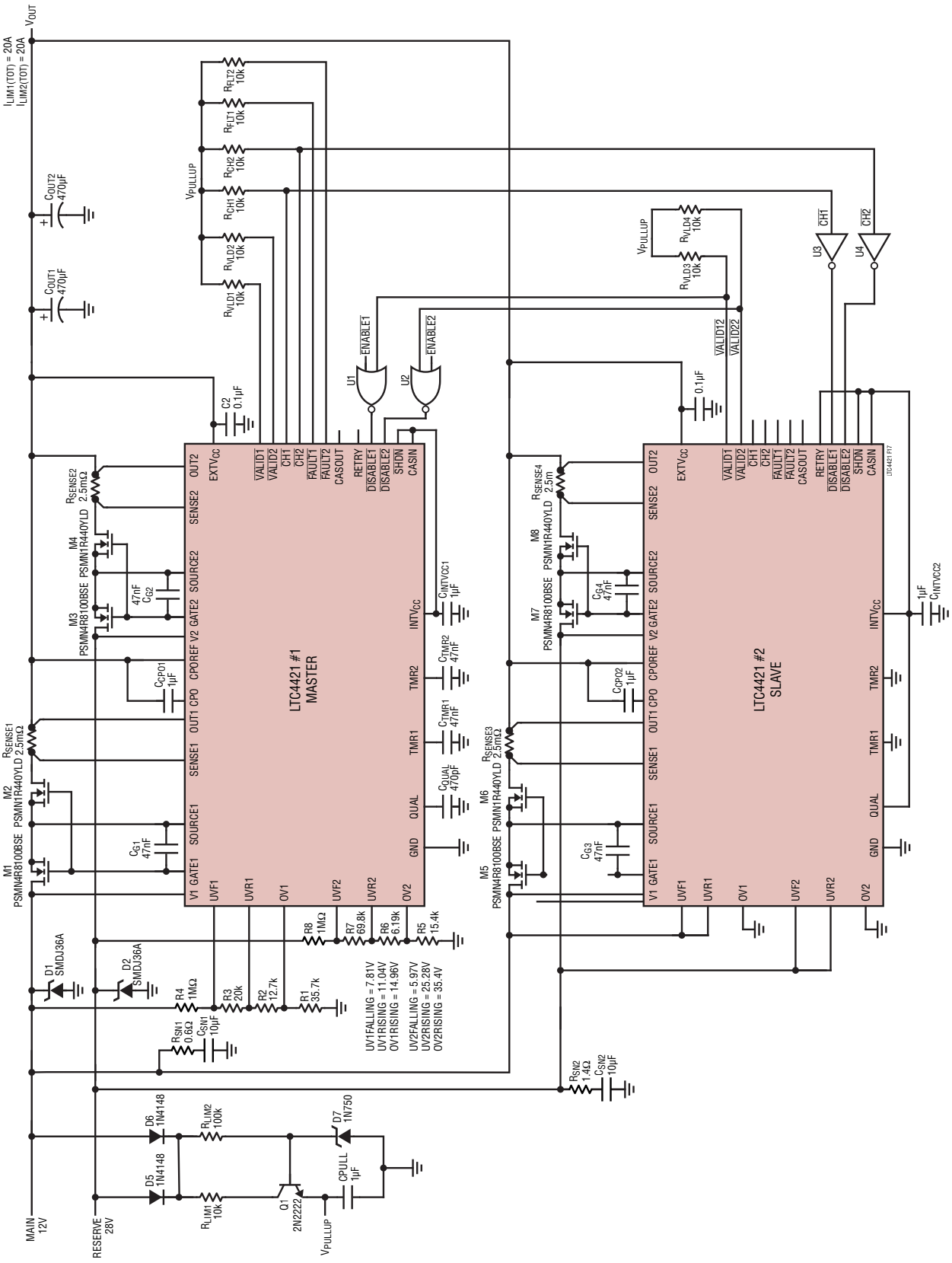
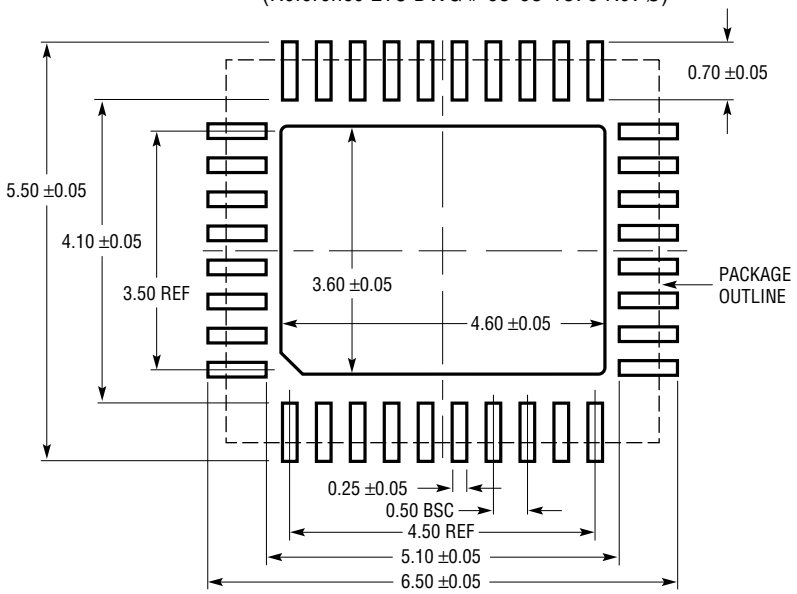


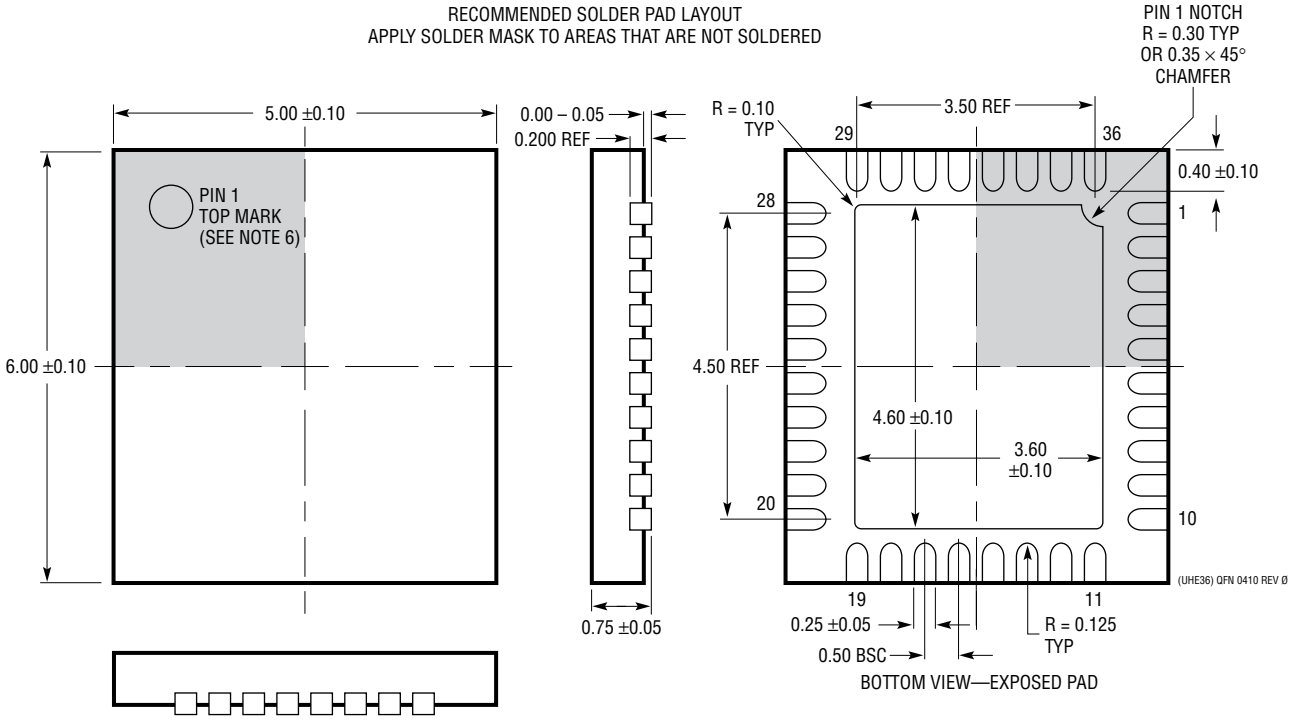
Figure 17. SOA Doubler. Using Two LTC4421's in a Master–Slave Configuration to Split Current and SOA Burden Between Parallel Pairs of MOSFETs in High Current Applications

PACKAGE DESCRIPTION

UHE Package
36-Lead Plastic QFN (5mm × 6mm)
(Reference LTC DWG # 05-08-1876 Rev Ø)



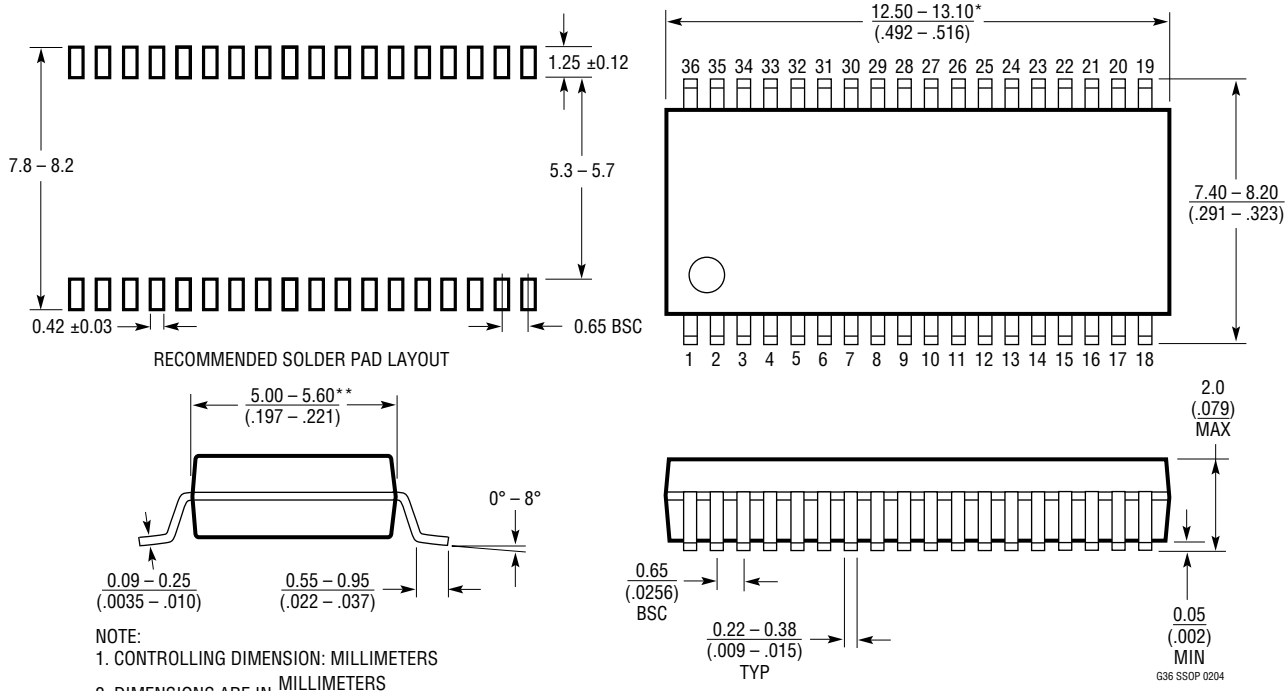
RECOMMENDED SOLDER PAD LAYOUT
APPLY SOLDER MASK TO AREAS THAT ARE NOT SOLDERED



NOTE:
1. DRAWING IS NOT A JEDEC PACKAGE OUTLINE
2. DRAWING NOT TO SCALE
3. ALL DIMENSIONS ARE IN MILLIMETERS
4. DIMENSIONS OF EXPOSED PAD ON BOTTOM OF PACKAGE DO NOT INCLUDE MOLD FLASH. MOLD FLASH, IF PRESENT, SHALL NOT EXCEED 0.20mm ON ANY SIDE
5. EXPOSED PAD SHALL BE SOLDER PLATED
6. SHADED AREA IS ONLY A REFERENCE FOR PIN 1 LOCATION ON THE TOP AND BOTTOM OF PACKAGE

PACKAGE DESCRIPTION

G Package
36-Lead Plastic SSOP (5.3mm)
(Reference LTC DWG # 05-08-1640)



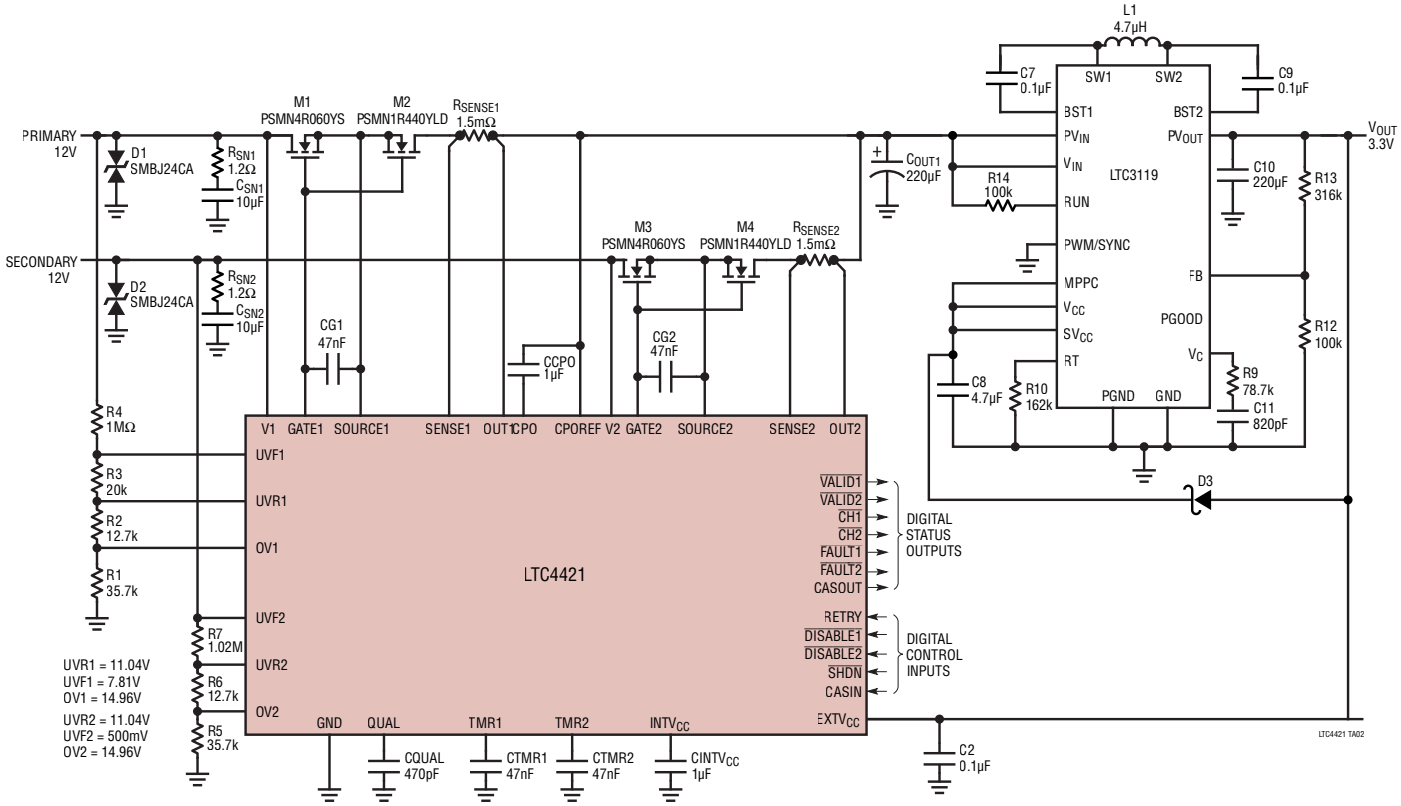
NOTE:
1. CONTROLLING DIMENSION: MILLIMETERS
2. DIMENSIONS ARE IN $\frac{\text{MILLIMETERS}}{(\text{INCHES})}$
3. DRAWING NOT TO SCALE

*DIMENSIONS DO NOT INCLUDE MOLD FLASH. MOLD FLASH SHALL NOT EXCEED .152mm (.006") PER SIDE

**DIMENSIONS DO NOT INCLUDE INTERLEAD FLASH. INTERLEAD FLASH SHALL NOT EXCEED .254mm (.010") PER SIDE

TYPICAL APPLICATION

Secondary Supply Run Down to 500mV Using LTC3119 to Power EXTV$_{CC}$



RELATED PARTS

PART NUMBER	DESCRIPTION	COMMENTS
LTC4417	Triple Prioritized PowerPath Controller	2.5V to 36V Operation; Ext P-Channel MOSFET; –42V Reverse Protection
LTC4418	Dual Prioritized PowerPath Controller	2.5V to 40V Operation; Ext P-Channel MOSFET; –42V Reverse Protection
LTC4419	Dual Prioritized PowerPath Controller	1.8V to 18V Operation; 0.5A Switches; Freshness Seal
LTC4420	Dual Prioritized PowerPath Controller	1.8V to 18V Operation; 0.5A Switches; Freshness Seal; Backup Disconnect
LTC4411	Single 2.6A Ideal Diode	2.6V to 5.5V Operation; 140mΩ R_{ON}; 40µA I_Q
LTC4358	Single 5A Ideal Diode	9V to 26.5V Operation; 20mΩ R_{ON}; 780µA I_Q
LTC4413	Dual 2.6A Ideal Diode	2.5V to 5.5V Operation; 140mΩ R_{ON}; 25µA I_Q
LTC4415	Dual 4A Ideal Diode	1.7V to 5.5V Operation; 50mΩ R_{ON}; 44µA I_Q

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LTC4421CG#PBF LTC4421HUHE#PBF LTC4421IG#PBF LTC4421IUHE#TRPBF LTC4421CUHE#PBF LTC4421HUHE#TRPBF LTC4421CUHE#TRPBF LTC4421HG#PBF LTC4421HG#TRPBF LTC4421CG#TRPBF LTC4421IUHE#PBF LTC4421IG#TRPBF DC2866A