45V V_{IN}, 500mA Low Noise, Linear Regulator with Programmable Current Limit and Active Output Discharge

FEATURES

- **Input Voltage Range: 1.6V to 45V**
- **Output Current: 500mA**
- **Active Output Discharge**
- **Dropout Voltage: 300mV**
- **Programmable Precision Current Limit: ±10%**
- **Power Good Flag**
- **Input Filtering for High PSRR**
- **Low Noise: 25µV_{RMS} (10Hz to 100kHz)**
- Adjustable Output (V_{REF} = $V_{OUT(MIN)}$ = 600mV)
- Output Tolerance: ±2% Over Line, Load and Temperature
- Stable with Low ESR, Ceramic Output Capacitors (3.3µF Minimum)
- Single Capacitor Soft-Starts Reference and Lowers Output Noise
- Current Limit Foldback Protection
- Shutdown Current: <3µA
- Reverse Battery and Thermal Limit Protection
- 12-Lead 4mm × 3mm DFN and 12-lead MSOP Packages

APPLICATIONS

- Battery-Powered Systems
- Automotive Power Supplies
- Industrial Power Supplies
- Avionic Power Supplies
- Portable Instruments

DESCRIPTION

The LT®3066 series are micropower, low noise, low dropout voltage (LDO) linear regulators that operate over a 1.6V to 45V input voltage range. The devices supply 500mA of output current with a typical dropout voltage of 300mV. A single external capacitor provides programmable low noise reference performance and output soft-start functionality.

A single external resistor programs the LT3066's current limit, accurate to ±10% over a wide input voltage and temperature range. A PWRGD flag indicates output regulation.

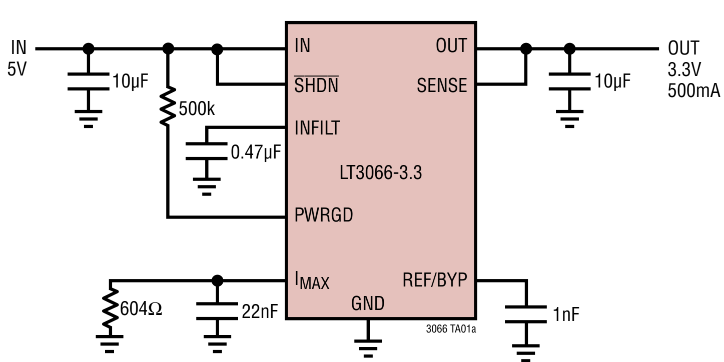
The LT3066 features an NMOS pull-down that discharges the output if $\overline{SHDN}$ or IN is driven low.

The LT3066 optimizes stability and transient response with low ESR ceramic capacitors, requiring a minimum of 3.3µF. Internal protection circuitry includes current limiting with foldback, thermal limiting, reverse battery protection, reverse current protection and reverse output protection.

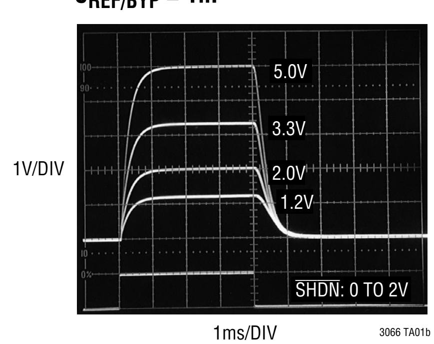
The LT3066 is available in fixed output voltages of 3.3V and 5V, and as an adjustable device with an output voltage range from 0.6V to 19V. The device is offered in the thermally-enhanced 12-lead 4mm × 3mm DFN and MSOP packages.

TYPICAL APPLICATION

3.3V Supply with 497mA Precision Current Limit



Output Discharge vs V_{OUT}
$C_{REF/BYP}$ = 1nF



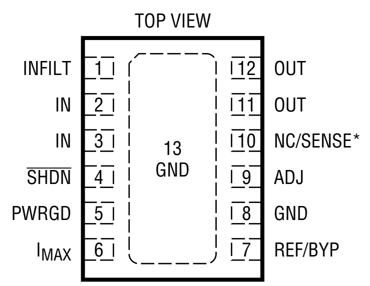
V_{IN} = V_{OUT} +1V
C_{OUT} = 10µF
$I_{FB\text{-}DIVIDER}$ = 10µA

Rev. B

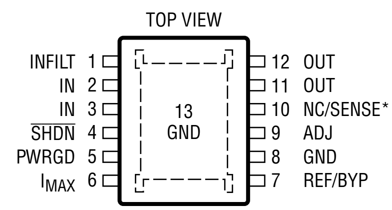
ABSOLUTE MAXIMUM RATINGS (Note 1)

IN Pin Voltage .... ±50V
OUT Pin Voltage .... +20V, –1V
Input-to-Output Differential Voltage (Note 2) .... ±50V
ADJ Pin Voltage .... ±50V
SHDN Pin Voltage .... ±50V
PWRGD Pin Voltage .... –0.3V, 50V
INFILT Pin Voltage (Note 15) .... ±50V
SENSE Pin Voltage .... ±50V
Output Short-Circuit Duration .... Indefinite
Operating Junction Temperature Range (Notes 3, 5, 14)
  E-, I-Grades .... –40°C to 125°C
Storage Temperature Range .... –65°C to 150°C
Lead Temperature (Soldering, 10 sec)
  MSOP Package Only .... 300°C

PIN CONFIGURATION



DE PACKAGE
12-LEAD (4mm × 3mm) PLASTIC DFN
T_{JMAX} = 150°C, θ_{JA} = 34°C/W, θ_{JC} = 5°C/W
EXPOSED PAD (PIN 13) IS GND, MUST BE SOLDERED TO PCB



MSE PACKAGE
12-LEAD PLASTIC MSOP
T_{JMAX} = 150°C, θ_{JA} = 34°C/W, θ_{JC} = 6°C/W
EXPOSED PAD (PIN 13) IS GND, MUST BE SOLDERED TO PCB

*Pin 10: NC for LT3066, SENSE for LT3066-3.3, LT3066-5

ORDER INFORMATION

LEAD FREE FINISH	TAPE AND REEL	PART MARKING*	PACKAGE DESCRIPTION	TEMPERATURE RANGE
LT3066EDE#PBF	LT3066EDE#TRPBF	3066	12-Lead (4mm x 3mm) Plastic DFN	–40°C to 125°C
LT3066IDE#PBF	LT3066IDE#TRPBF	3066	12-Lead (4mm x 3mm) Plastic DFN	–40°C to 125°C
LT3066EDE-3.3#PBF	LT3066EDE-3.3#TRPBF	06633	12-Lead (4mm x 3mm) Plastic DFN	–40°C to 125°C
LT3066IDE-3.3#PBF	LT3066IDE-3.3#TRPBF	06633	12-Lead (4mm x 3mm) Plastic DFN	–40°C to 125°C
LT3066EDE-5#PBF	LT3066EDE-5#TRPBF	30665	12-Lead (4mm x 3mm) Plastic DFN	–40°C to 125°C
LT3066IDE-5#PBF	LT3066IDE-5#TRPBF	30665	12-Lead (4mm x 3mm) Plastic DFN	–40°C to 125°C
LT3066EMSE#PBF	LT3066EMSE#TRPBF	3066	12-Lead Plastic MSOP	–40°C to 125°C
LT3066IMSE#PBF	LT3066IMSE#TRPBF	3066	12-Lead Plastic MSOP	–40°C to 125°C
LT3066EMSE-3.3#PBF	LT3066EMSE-3.3#TRPBF	306633	12-Lead Plastic MSOP	–40°C to 125°C
LT3066IMSE-3.3#PBF	LT3066IMSE-3.3#TRPBF	306633	12-Lead Plastic MSOP	–40°C to 125°C
LT3066EMSE-5#PBF	LT3066EMSE-5#TRPBF	30665	12-Lead Plastic MSOP	–40°C to 125°C
LT3066IMSE-5#PBF	LT3066IMSE-5#TRPBF	30665	12-Lead Plastic MSOP	–40°C to 125°C

Contact the factory for parts specified with wider operating temperature ranges. *The temperature grade is identified by a label on the shipping container.

Tape and reel specifications. Some packages are available in 500 unit reels through designated sales channels with #TRMPBF suffix.

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C (Note 3).

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Minimum Input Voltage (Notes 4, 9)	I_{LOAD} = 500mA	●		1.6	2.2	V
Regulated Output Voltage (Note 5)	LT3066-3.3: V_{IN} = 3.9V, I_{LOAD} = 1mA LT3066-3.3: 3.9V < V_{IN} < 45V, 1mA < I_{LOAD} < 500mA LT3066-5: V_{IN} = 5.6V, I_{LOAD} = 1mA LT3066-5: 5.6V < V_{IN} < 45V, 1mA < I_{LOAD} < 500mA	 ● ●	3.267 3.234 4.950 4.900	3.3 5 	3.333 3.366 5.050 5.100	V V V V
ADJ Pin Voltage (Notes 4, 5)	V_{IN} = 2.2V, I_{LOAD} = 1mA 2.2V < V_{IN} < 45V, 1mA < I_{LOAD} < 500mA	 ●	594 588	600 	606 612	mV mV
Line Regulation I_{LOAD} = 1mA	LT3066-3.3: ΔV_{IN} = 3.9V to 45V LT3066-5: ΔV_{IN} = 5.6V to 45V LT3066: ΔV_{IN} = 2.2V to 45V (Note 4)	● ● ●		1.6 2.6 0.1	19.5 30 3	mV mV mV
Load Regulation ΔI_{LOAD} = 1mA to 500mA	LT3066-3.3: V_{IN} = 3.9V LT3066-5: V_{IN} = 5.6V LT3066: V_{IN} = 2.2V (Note 4)	● ● ●		1.6 2.4 0.1	22 33 4	mV mV mV
Dropout Voltage, V_{IN} = $V_{OUT(NOMINAL)}$ (Notes 6, 7)	I_{LOAD} = 10mA	 ●		110	150 210	mV mV
	I_{LOAD} = 50mA	 ●		145	200 310	mV mV
	I_{LOAD} = 100mA	 ●		175	220 330	mV mV
	I_{LOAD} = 500mA	 ●		300	350 510	mV mV
GND Pin Current, V_{IN} = $V_{OUT(NOMINAL)}$ + 0.6V (Notes 7, 8)	I_{LOAD} = 0mA I_{LOAD} = 1mA I_{LOAD} = 10mA I_{LOAD} = 100mA I_{LOAD} = 500mA	● ● ● ● ●		64 100 270 1.8 11	125 200 550 4.5 25	μA μA μA mA mA
Quiescent Current in Shutdown	V_{IN} = 45V, $V_{\overline{SHDN}}$ = 0V			1.25	3	μA
ADJ Pin Bias Current (Notes 4, 10)	V_{IN} = 2.2V	●		16	60	nA
Output Voltage Noise	C_{OUT} = 10μF, I_{LOAD} = 500mA, V_{OUT} = 600mV, BW = 10Hz to 100kHz			90		μV_{RMS}
	C_{OUT} = 10μF, C_{BYP} = 10nF, I_{LOAD} = 500mA, V_{OUT} = 600mV, BW = 10Hz to 100kHz			25		μV_{RMS}
Shutdown Threshold (Notes 4, 9)	V_{OUT} = Off to On V_{OUT} = On to Off	● ●	 0.9	1. 3 1.1	1.42 	V V
Output Discharge Time (Notes 7, 9)	V_{OUT} Discharged to 10% of Nominal, C_{OUT} = 4.7μF	●		0.4	1	ms
Output Discharge Switch Resistance	V_{IN} = 3.6V, V_{OUT} = 1V, $\overline{SHDN}$ = 0V			30		Ω
Shutdown Pin Output Discharge Threshold	V_{IN} = 3.6V			0.56		V
$\overline{SHDN}$ Pin Current (Note 11)	$V_{\overline{SHDN}}$ = 0V, V_{IN} = 45V $V_{\overline{SHDN}}$ = 45V, V_{IN} = 45V	● ●		 1.2	±1 3	μA μA
Ripple Rejection $V_{IN} - V_{OUT}$ = 2V, V_{RIPPLE} = 0.5V_{P-P}, f_{RIPPLE} = 120Hz, I_{LOAD} = 500mA	LT3066-3.3 LT3066-5 LT3066 (Note 4)		56 55 70	71 70 85		dB dB dB
Input Reverse Leakage Current	V_{IN} = –45V, V_{OUT} = 0	●			1	mA
Reverse Output Current (Note 12)	V_{OUT} = 3.4V, V_{IN} = $V_{\overline{SHDN}}$ = 2.2V			2.5	15	μA
Internal Current Limit (Notes 4, 9)	V_{IN} = 2.2V or V_{IN} = $V_{OUT(NOMINAL)}$ + 1V, V_{OUT} = 0V, V_{IMAX} = 0V V_{IN} = 2.2V or V_{IN} = $V_{OUT(NOMINAL)}$ + 1V, ΔV_{OUT} = –5%	 ●	 520	900 		mA mA

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C (Note 3).

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
External Programmed Current Limit (Notes 7, 13)	R_{IMAX} = 1.5k, V_{OUT} = 95% of $V_{OUT(NOMINAL)}$ $V_{OUT(NOMINAL)}$ + 0.6V < V_{IN} < $V_{OUT(NOMINAL)}$+ 5V	●	180	200	220	mA
	R_{IMAX} = 604Ω, V_{OUT} = 95% of $V_{OUT(NOMINAL)}$ $V_{OUT(NOMINAL)}$ + 0.6V < V_{IN} < $V_{OUT(NOMINAL)}$ + 2V	●	445	495	545	mA
PWRGD Logic Low Voltage	Pull-Up Current = 50μA	●		0.07	0.25	V
PWRGD Leakage Current	V_{PWRGD} = 5V			0.01	1	μA
PWRGD Trip Point	% of Nominal Output Voltage, Output Rising	●	86	90	94	%
PWRGD Trip Point Hysteresis	% of Nominal Output Voltage			1.6		%

Note 1: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

Note 2: Absolute maximum input-to-output differential voltage is not achievable with all combinations of rated IN pin and OUT pin voltages. With IN at 50V, do not pull OUT below 0V. If OUT is pulled above IN and GND, the OUT to IN differential voltage must not exceed 40V.

Note 3: The LT3066 regulator is tested and specified under pulse load conditions such that $T_J \cong T_A$. The LT3066E regulators are 100% tested at T_A = 25°C and performance is guaranteed from 0°C to 125°C. Performance at –40°C to 125°C is assured by design, characterization and correlation with statistical process controls. The LT3066I regulators are guaranteed over the full –40°C to 125°C operating junction temperature range. High junction temperatures degrade operating lifetimes. Operating lifetime is derated at junction temperatures greater than 125°C.

Note 4: The LT3066 adjustable version is tested and specified for these conditions with the ADJ pin connected to the OUT pin.

Note 5: Maximum junction temperature limits operating conditions. Regulated output voltage specifications do not apply for all possible combinations of input voltage and output current. If operating at the maximum input voltage, limit the output current range. If operating at the maximum output current, limit the input voltage range. Current limit foldback limits the maximum output current as a function of input-to-output voltage. See Current Limit vs $V_{IN} – V_{OUT}$ in the Typical Performance Characteristics section.

Note 6: Dropout voltage is the minimum IN-to-OUT differential voltage needed to maintain regulation at a specified output current. In dropout, the output voltage equals ($V_{IN} – V_{DROPOUT}$). For some output voltages, minimum input voltage requirements limit dropout voltage.

Note 7: To satisfy minimum input voltage requirements, the LT3066 adjustable version is tested and specified for these conditions with an external resistor divider (60.4k bottom, 442k top) which sets V_{OUT} to 5V. The divider adds 10uA of output DC load. This external current is not factored into GND pin current. For fixed voltage options, an internal resistor divider will add 5μA to the GND pin current. See the GND Pin Current curves in the Typical Performance Characteristics section

Note 8: GND pin current is tested with V_{IN} = $V_{OUT(NOMINAL)}$ + 0.6V and a current source load. GND pin current increases in dropout. See GND pin current curves in the Typical Performance Characteristics section.

Note 9: To satisfy requirements for minimum input voltage, the LT3066 is tested at V_{IN} = $V_{OUT(NOMINAL)}$ + 1V or V_{IN} = 2.2V, whichever is greater.

Note 10: ADJ pin bias current flows out of the ADJ pin.

Note 11: $\overline{SHDN}$ pin current flows into the $\overline{SHDN}$ pin.

Note 12: This current flows into the OUT pin and out of the GND pin.

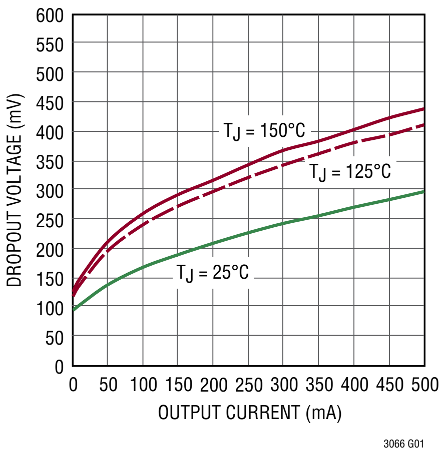
Note 13: Current limit varies inversely with the external resistor value tied from the IMAX pin to GND. If the externally programmed current limit feature is unused, tie the IMAX pin to GND. The internal current limit circuitry implements short-circuit protection as specified.

Note 14: This IC includes over temperature protection that protects the device during overload conditions. Junction temperature exceeds 125°C (LT3066E, LT3066I) when the over temperature circuitry is active. Continuous operation above the specified maximum junction temperature may impair device reliability.

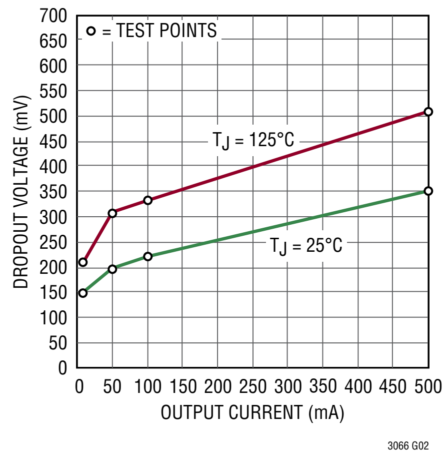
Note 15: Tie INFILT directly to IN or to a decoupling capacitor.

TYPICAL PERFORMANCE CHARACTERISTICS T_J = 25°C, unless otherwise noted.

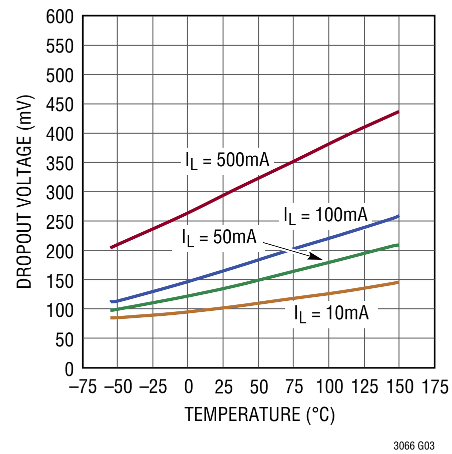
Typical Dropout Voltage



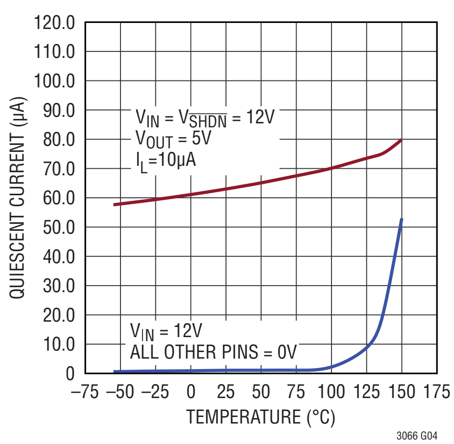
Guaranteed Dropout Voltage



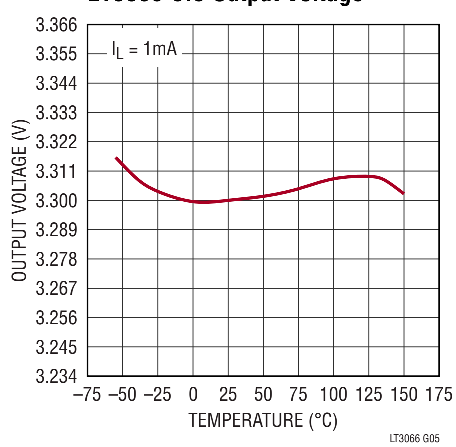
Dropout Voltage



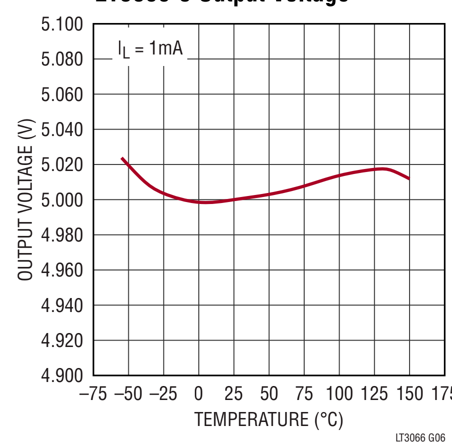
Quiescent Current



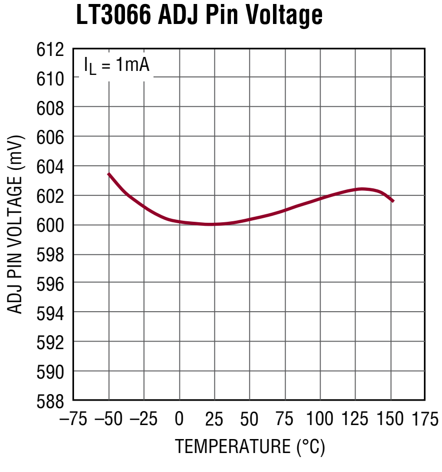
LT3066-3.3 Output Voltage



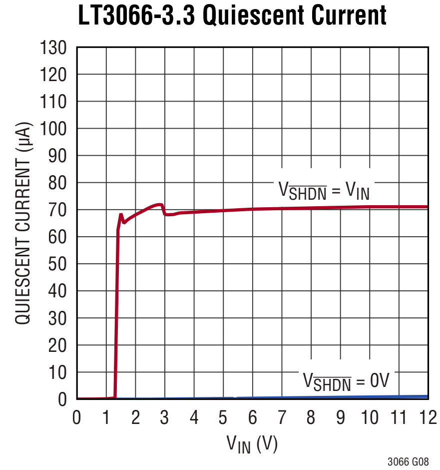
LT3066-5 Output Voltage



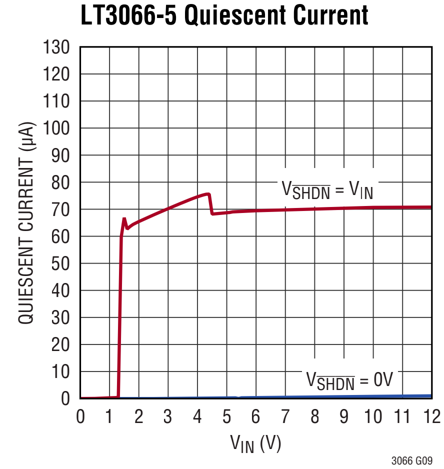
LT3066 ADJ Pin Voltage



LT3066-3.3 Quiescent Current

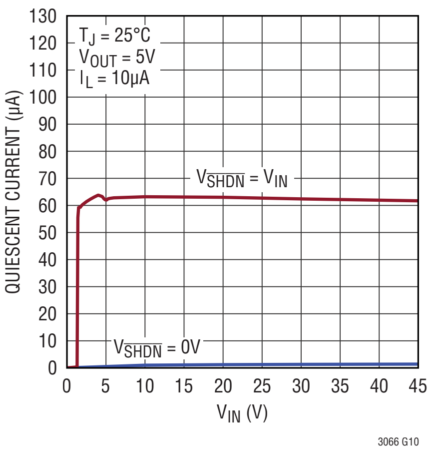


LT3066-5 Quiescent Current

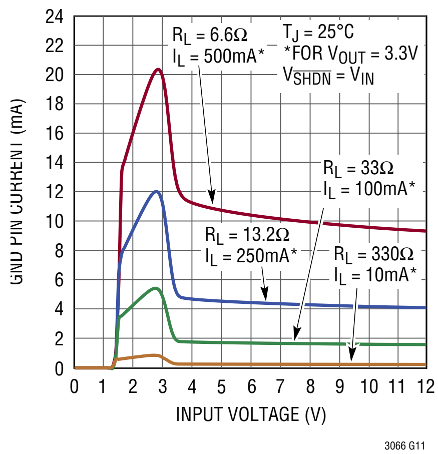


TYPICAL PERFORMANCE CHARACTERISTICS T_J = 25°C, unless otherwise noted.

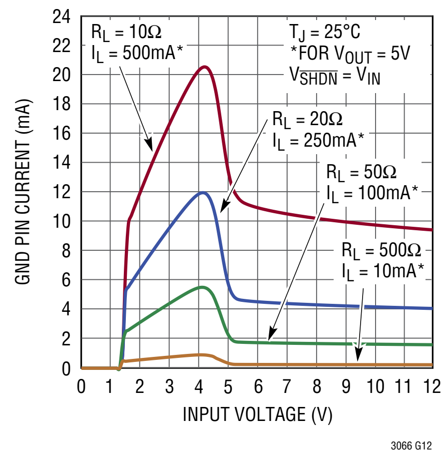
Quiescent Current



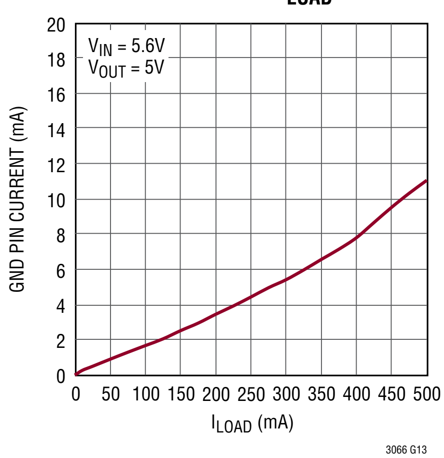
LT3066-3.3 GND Pin Current



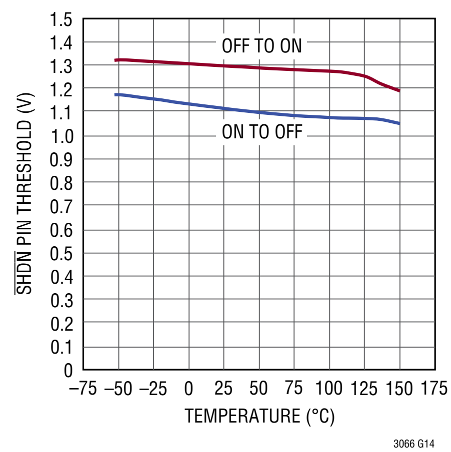
LT3066-5 GND Pin Current



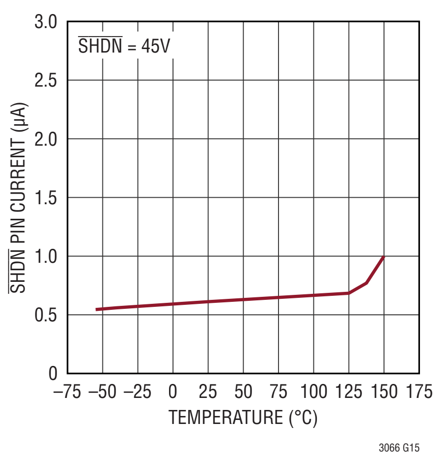
GND Pin Current vs I_{LOAD}



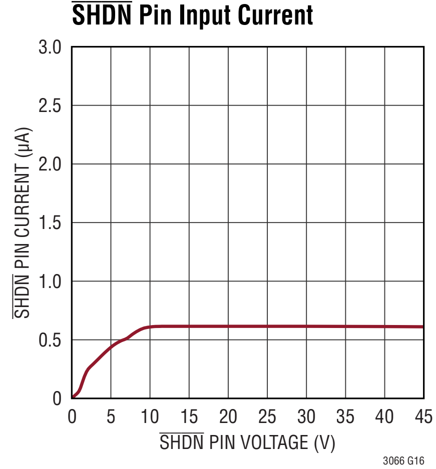
SHDN Pin Threshold



SHDN Pin Current



SHDN Pin Input Current



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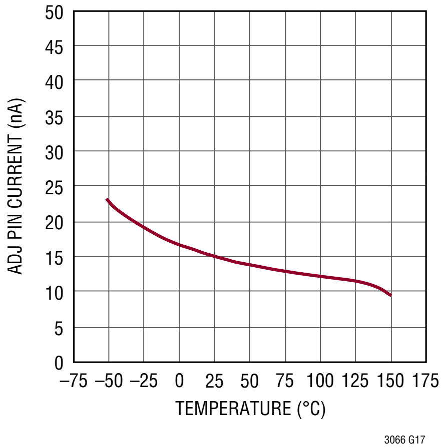
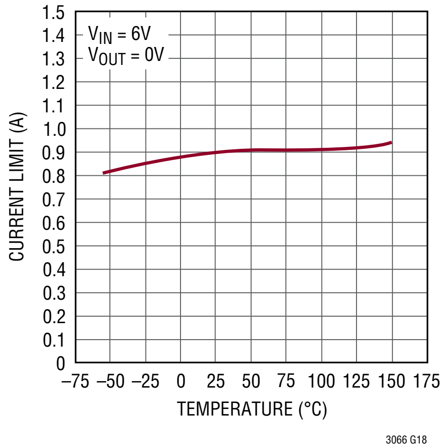
TYPICAL PERFORMANCE CHARACTERISTICS T_J = 25°C, unless otherwise noted.

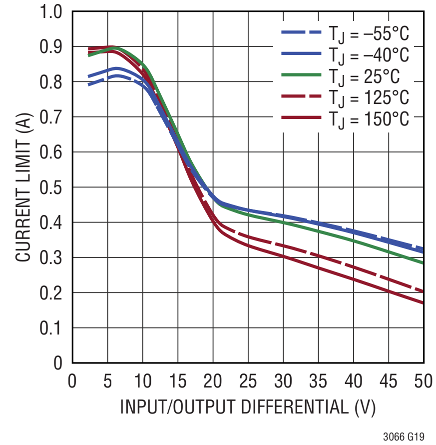
ADJ Pin Bias Current



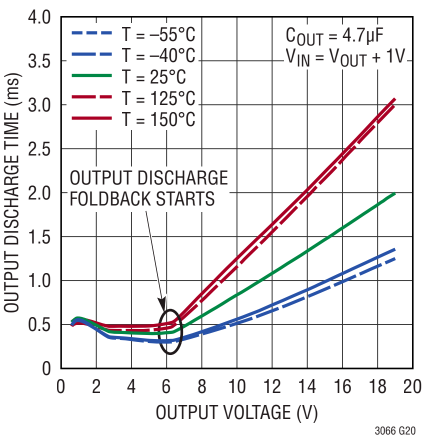
Internal Current Limit



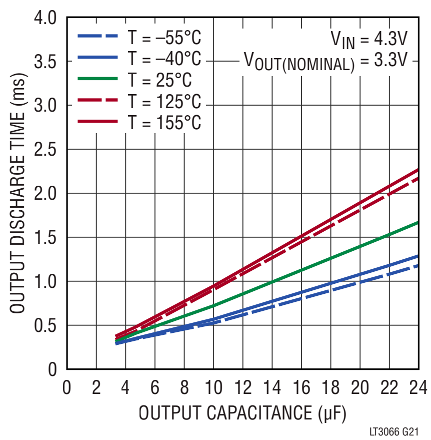
Internal Current Limit



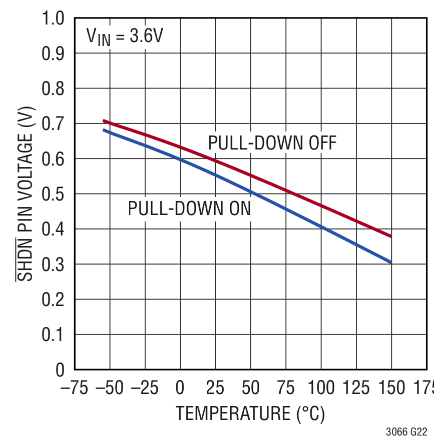
Output Discharge Time



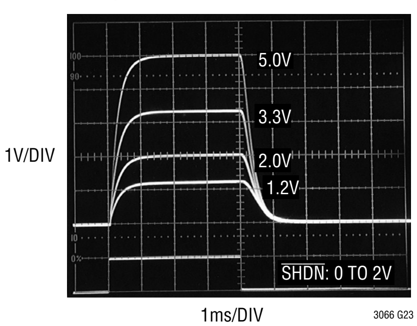
Output Discharge Time



Output Discharge Pull-Down Threshold

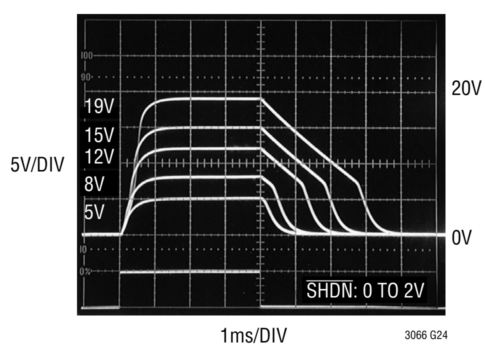


Output Discharge vs V_{OUT} $C_{REF/BYP}$ = 1nF



$V_{IN} = V_{OUT}$ +1V
C_{OUT} = 10µF
$I_{FB\text{-}DIVIDER}$ = 10µA

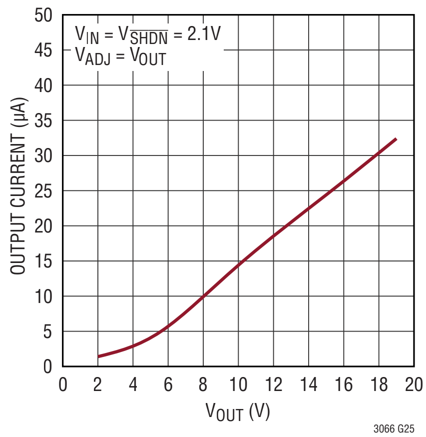
Output Discharge vs V_{OUT} $C_{REF/BYP}$ = 1nF



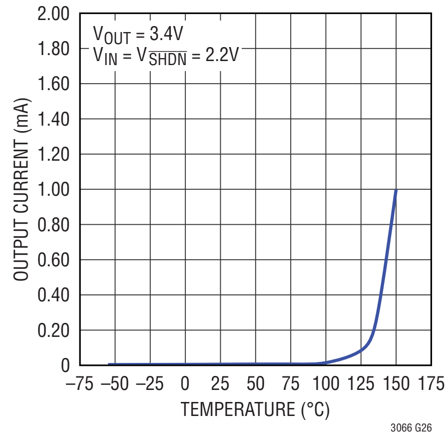
$V_{IN} = V_{OUT}$ +1V
C_{OUT} = 10µF
$I_{FB\text{-}DIVIDER}$ = 10µA

TYPICAL PERFORMANCE CHARACTERISTICS
$T_J = 25°C$, unless otherwise noted.

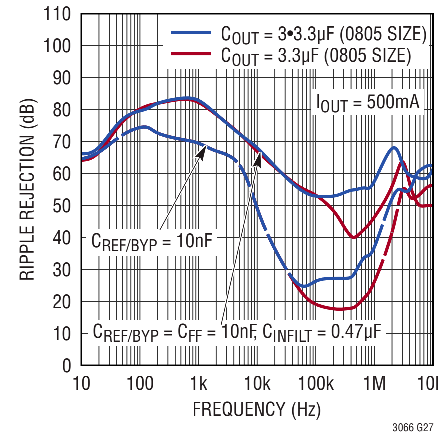
Reverse Output Current



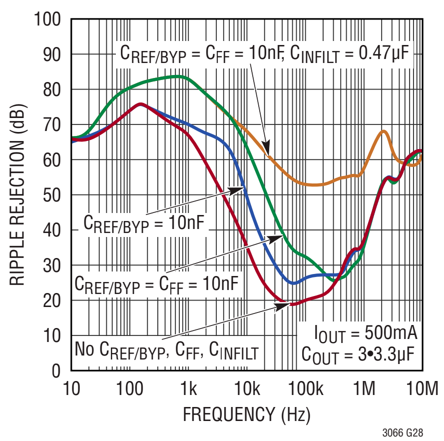
Reverse Output Current



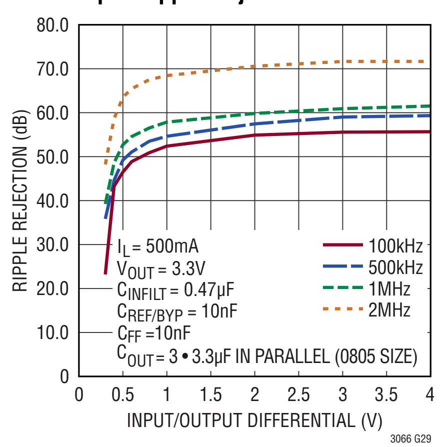
Input Ripple Rejection
V_{IN} = 4.3V + 50mV_{RMS}, V_{OUT} = 3.3V



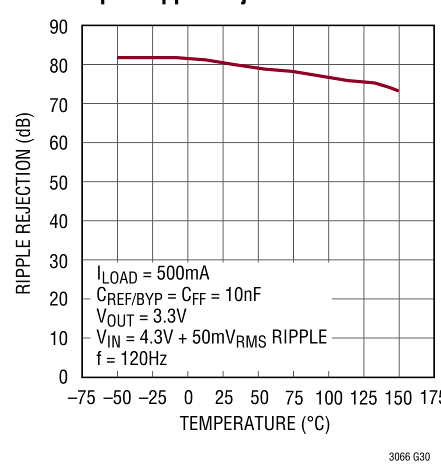
Input Ripple Rejection
V_{IN} = 4.3V + 50mV_{RMS}, V_{OUT} = 3.3V



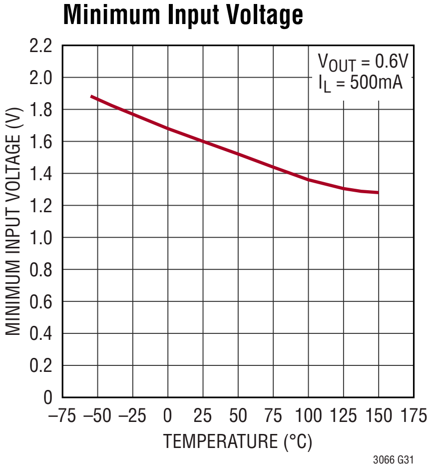
Input Ripple Rejection



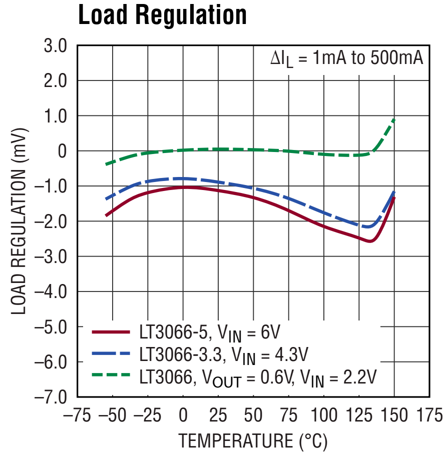
Input Ripple Rejection



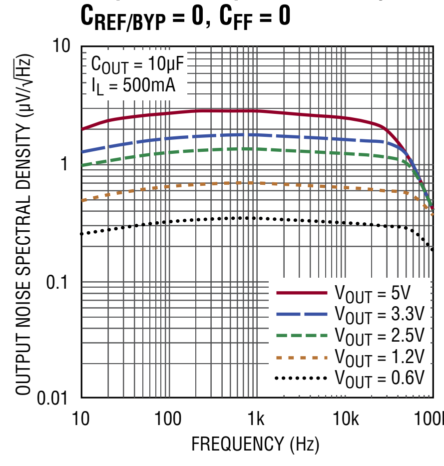
Minimum Input Voltage



Load Regulation



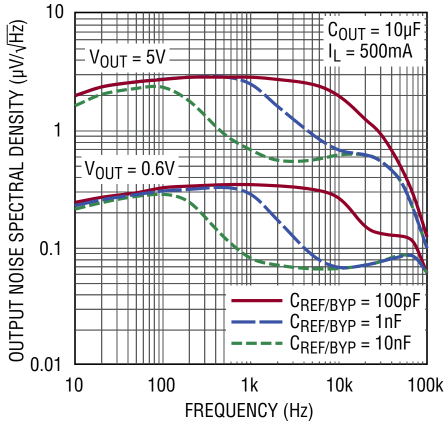
Output Noise Spectral Density
$C_{REF/BYP}$ = 0, C_{FF} = 0



Rev. B

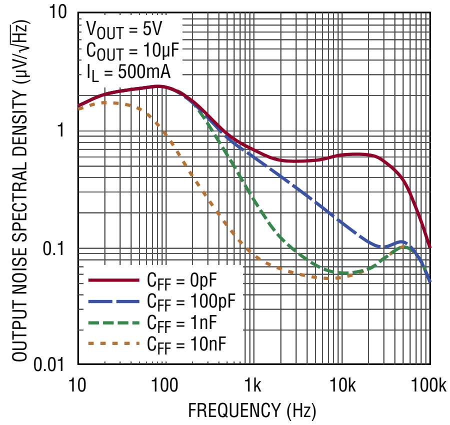
TYPICAL PERFORMANCE CHARACTERISTICS $T_J = 25°C$, unless otherwise noted.

Output Noise Spectral Density vs $C_{REF/BYP}$, $C_{FF} = 0$



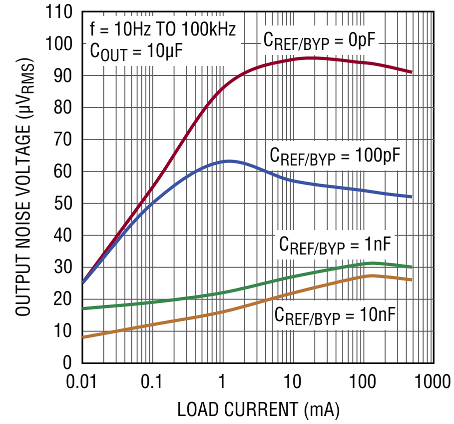
3066 G34

Output Noise Spectral Density vs C_{FF}, $C_{REF/BYP} = 10nF$



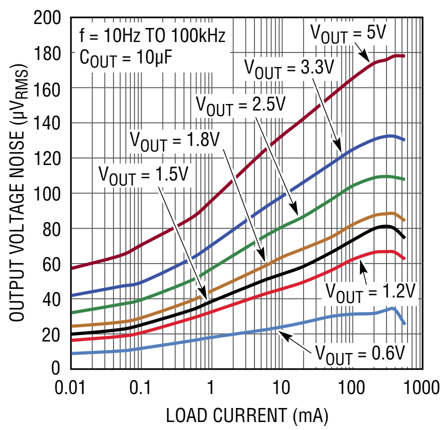
3066 G35

RMS Output Noise, $V_{OUT} = 0.6V$, $C_{FF} = 0$



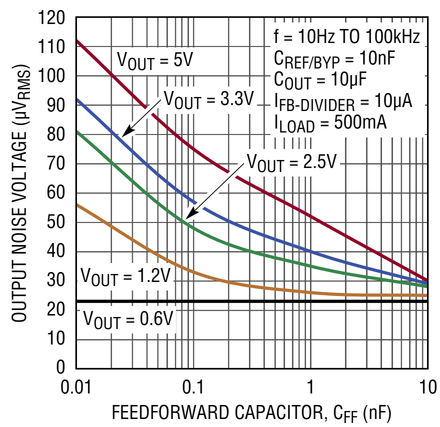
3066 G36

RMS Output Noise vs Load Current vs $C_{REF/BYP} = 10nF$, $C_{FF} = 0$



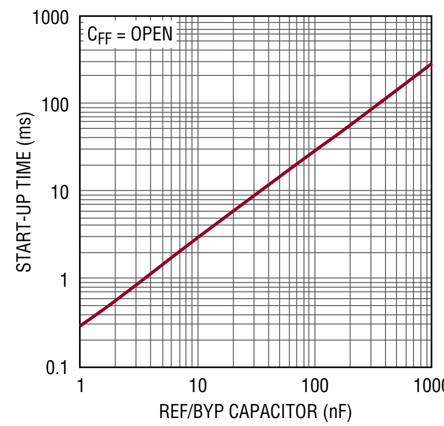
3066 G37

RMS Output Noise, vs Feedforward Capacitor (C_{FF})



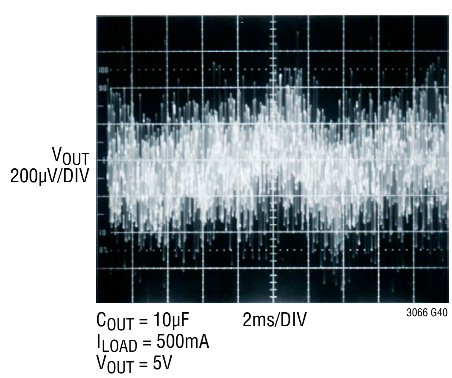
3066 G38

Start-Up Time vs REF/BYP Capacitor



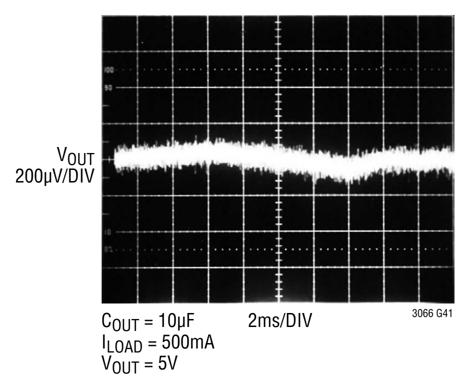
3066 G39

10Hz to 100kHz Output Noise $C_{REF/BYP} = 10nF$, $C_{FF} = 0$



3066 G40

10Hz to 100kHz Output Noise $C_{REF/BYP} = 10nF$, $C_{FF} = 10nF$

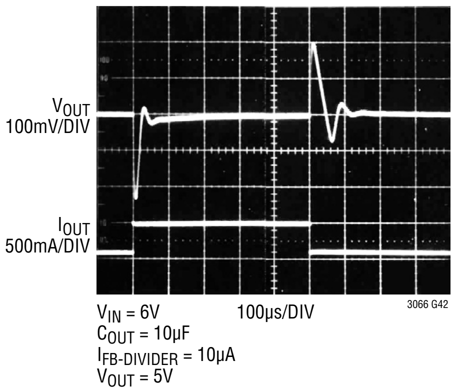


3066 G41

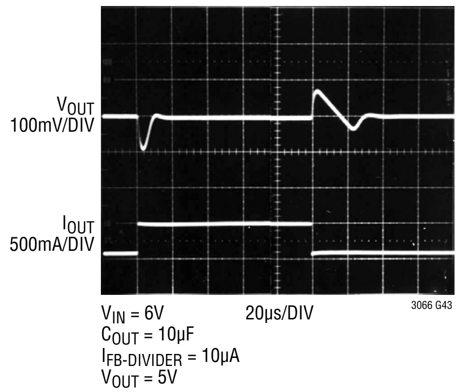
Rev. B

TYPICAL PERFORMANCE CHARACTERISTICS T_J = 25°C, unless otherwise noted.

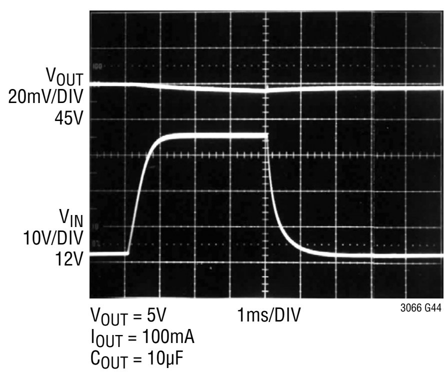
5V Transient Response C_{FF} = 0, I_{OUT} = 50mA to 500mA



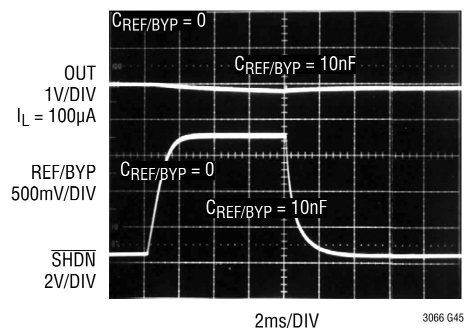
5V Transient Response C_{FF} = 10nF, I_{OUT} = 50mA to 500mA



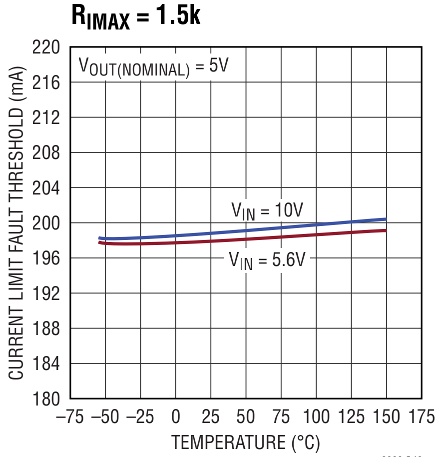
Transient Response (Load Dump)



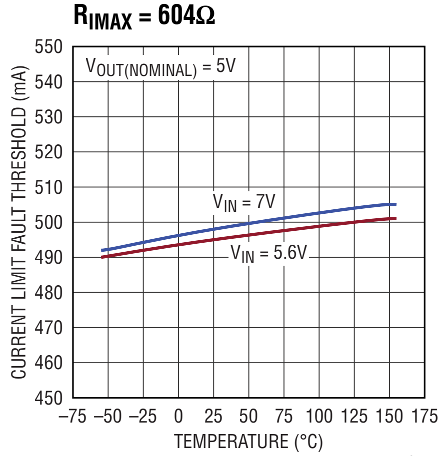
SHDN Transient Response $C_{REF/BYP}$ = 10nF



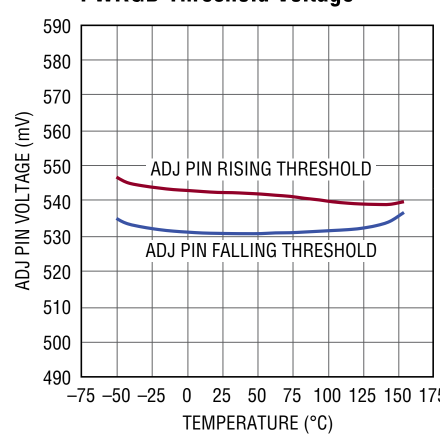
Precision Current Limit, R_{IMAX} = 1.5k



Precision Current Limit, R_{IMAX} = 604Ω



PWRGD Threshold Voltage



PIN FUNCTIONS (DFN/MSOP)

INFILT (Pin 1): Filtered Input. This pin is connected to IN through a ~140Ω on-chip resistor. To improve PSRR, at frequencies greater than 10kHz connect up to a 0.47µF capacitor from INFILT to GND (see Figure 1). If improved PSRR is not needed, connect the INFILT pin to IN.

IN (Pins 2, 3): Input. These pin(s) supply power to the device. The LT3066 requires a local IN bypass capacitor if it is located more than six inches from the main input filter capacitor. In general, battery output impedance rises with frequency, so adding a bypass capacitor in battery-powered circuits is advisable. An input bypass capacitor in the range of 1µF to 10µF generally suffices. See Input Capacitance and Stability in the Applications Information section for more information.

The LT3066 withstands reverse voltages on the IN pin with respect to its GND and OUT pins. In such case, such as a battery plugged in backwards, the LT3066 behaves as if a diode is in series with its input. No reverse current flows into the LT3066 and no reverse voltage appears at the load. The device protects itself and the load.

$\overline{\text{SHDN}}$ (Pin 4): Shutdown. Pulling the $\overline{\text{SHDN}}$ pin low puts the LT3066 into a low power state and turns the output off. Drive the $\overline{\text{SHDN}}$ pin with either logic or an open collector/drain with a pull-up resistor. The resistor supplies the pull-up current to the open collector/drain logic, normally several microamperes, and the $\overline{\text{SHDN}}$ pin current, typically less than 2µA. If unused, connect the $\overline{\text{SHDN}}$ pin to IN. The LT3066 does not function if the $\overline{\text{SHDN}}$ pin is not connected.

PWRGD (Pin 5): Power Good. The PWRGD pin is an open-drain output that actively pulls low if the output is less than 90% of the nominal output value. The PWRGD pin is capable of sinking 50µA. There is no internal pull-up resistor; an external pull-up resistor must be used.

I_{MAX} (Pin 6): Precision Current Limit Programming. This pin is the collector of a current mirror PNP that is 1/500th the size of the output power PNP. This pin is also the input to the current limit amplifier. The current limit threshold is set by connecting a resistor between the I_{MAX} pin and GND.

For detailed information on how to set the I_{MAX} pin resistor value, see the Applications Information section. The I_{MAX} pin requires a 22nF de-coupling capacitor to ground. If not used, tie I_{MAX} to GND. Do not drive this pin with any active circuitry.

REF/BYP (Pin 7): Bypass/Soft-Start. Connecting a capacitor from this pin to GND bypasses the LT3066's reference noise and soft-starts the reference. A 10nF bypass capacitor typically reduces output voltage noise to 25µV_{RMS} in a 10Hz to 100kHz bandwidth. Soft-start time is directly proportional to the BYP capacitor value. If the LT3066 is placed in shutdown, BYP is actively pulled low by an internal device to reset soft-start. If low noise or soft-start performance is not required, this pin must be left floating (unconnected). Do not drive this pin with any active circuitry.

Because the REF/BYP pin is the reference input to the error amplifier, stray capacitance at this point should be minimized. Special attention should be given to any stray capacitances that can couple external signals onto the REF/BYP pin producing undesirable output transients or ripple. A minimum capacitance of 100pF from REF/BYP to GND is recommended.

GND (Pin 8, Exposed Pad Pin 13): Ground. The exposed pad of the DFN and MSOP packages is an electrical connection to GND. To ensure proper electrical and thermal performance, solder Pin 8 to the PCB GND and tie it directly to Pin 13. For the adjustable LT3066, connect the bottom of the external resistor divider that sets output voltage directly to GND (Pin 8)for optimum load regulation.

ADJ (Pin 9): Adjust. This pin is the error amplifier's inverting terminal. It's typical bias current of 16nA flows out of the pin (see curve of ADJ Pin Bias Current vs Temperature in the Typical Performance Characteristics section). The ADJ pin voltage is 600mV referenced to GND.

PIN FUNCTIONS (DFN/MSOP)

NC (LT3066: Pin 10): No Connect. This pin has no connection to internal circuitry. This pin may be floated or connected to GND.

SENSE (LT3066-3.3, LT3066-5: Pin 10): Sense. This pin is the top of the internal resistor divider network and should be connected directly to the load, as a Kelvin sense, for optimum load regulation and transient performance. Connecting this pin to the output pin at the package, rather than directly to the load, can result in load regulation errors due to the current across the parasitic resistance of the PCB trace.

OUT (Pins 11, 12): Output. These pins supply power to the load. Stability requirements demand a minimum 3.3µF ceramic output capacitor with an ESR < 1Ω to prevent oscillations. Applications with output voltages less than 1.2V require a minimum 4.7µF ceramic output capacitor. Large load transient applications require larger output capacitors to limit peak voltage transients. See the Applications Information section for details on transient response and reverse output characteristics. Permissible output voltage range is 600mV to 19V.

Connecting a capacitor from OUT to ADJ reduces output noise and improves transient response for output voltages greater than 600mV. See the Applications Information section for calculating the value of the feedforward capacitor.

At output voltages above 0.6V, the resistor divider connected to the ADJ pin is used to regulate voltage at the load. Parasitic resistances of PCB traces or cables can therefore result in load regulation errors at high output currents. To eliminate these, connect the resistor divider directly to the load for a Kelvin sense connection, as shown in Figure 1.

If the LT3066 is placed in shutdown, OUT is actively discharged by an internal NMOS device. Gate drive is controlled to insure that a 10µF capacitor is discharged 90% in 2ms or less. If IN is driven low, OUT is actively discharged to ~800mV. For OUT voltages greater than 6V, current limit foldback is implemented to protect the NMOS device and discharge rates increase. See the Applications Information section for more information.

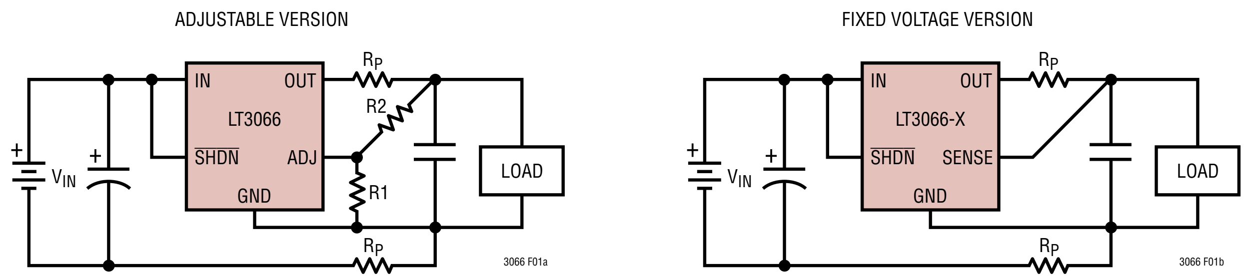


Figure 1. Kelvin Sense Connection

Rev. B

BLOCK DIAGRAM

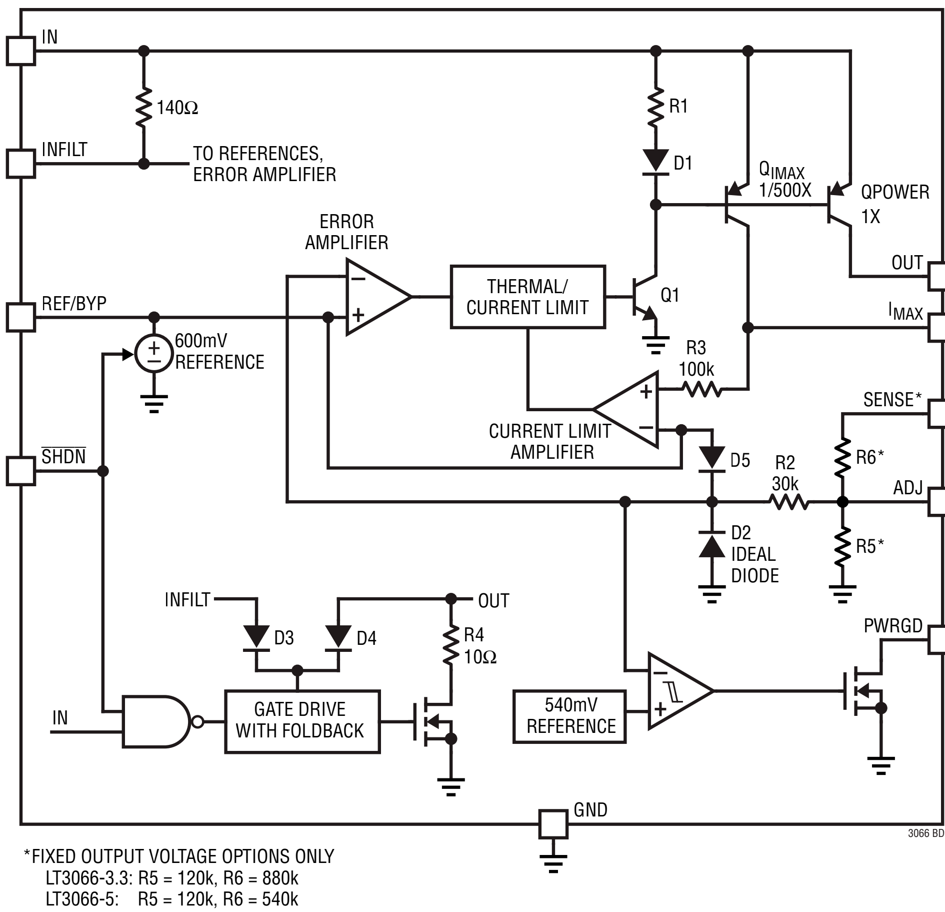


Figure 2. System Block Diagram

APPLICATIONS INFORMATION

The LT3066 series are micropower, low noise and low drop-out voltage, 500mA linear regulators with micropower shutdown, programmable current limit, and a Power-good flag. The devices supply up to 500mA at a typical dropout voltage of 300mV and operate over a 1.6V to 45V input range.

A single external capacitor provides low noise reference performance and output soft-start functionality. For example, connecting a 10nF capacitor from the REF/BYP pin to GND lowers output noise to $25\mu V_{RMS}$ over a 10Hz to 100kHz bandwidth. This capacitor also soft-starts the reference and prevents output voltage overshoot at turn-on.

The LT3066's quiescent current is merely 64µA but provides fast transient response with a low ESR, minimum value 3.3µF ceramic output capacitor. In shutdown, quiescent current is less than 3µA and the reference soft-start capacitor is reset.

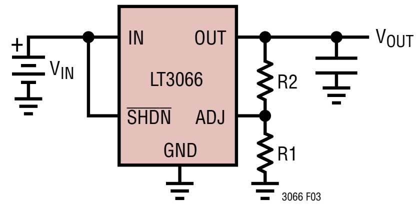
The LT3066 optimizes stability and transient response with low ESR, ceramic output capacitors. The regulator does not require the addition of ESR as is common with other regulators. The LT3066 typically provides better than 0.1% line regulation and 0.1% load regulation. Internal protection circuitry includes reverse battery protection, reverse output protection, reverse current protection, current limit with foldback and thermal shutdown.

This "bullet-proof" protection set makes it ideal for use in battery-powered, automotive and industrial systems.In battery backup applications where the output is held up by a backup battery and the input is pulled to ground, the LT3066 acts like it has a diode in series with its output and prevents reverse current.

Adjustable Operation

The adjustable LT3066 has an output voltage range of 0.6V to 19V. Output voltage is set by the ratio of two external resistors, as shown in Figure 3. The device regulates the output to maintain the ADJ pin voltage at 0.6V referenced to ground. The current in R1 equals 0.6V/R1, and R2's current is R1's current minus the ADJ pin bias current.

The ADJ pin bias current, 16nA at 25°C, flows from the ADJ pin through R1 to GND. Calculate the output voltage using the formula in Figure 3. R1's value should not be greater than 62k to provide a minimum 10µA load current so that output voltage errors, caused by the ADJ pin bias current, are minimized. Note that in shutdown, the output is turned off and the divider current is zero. Curves of ADJ Pin Voltage vs Temperature and ADJ Pin Bias Current vs Temperature appear in the Typical Performance Characteristics section.



$$V_{OUT} = 0.6V\left(1+\frac{R2}{R1}\right) - (I_{ADJ} \bullet R2)$$

$$V_{ADJ} = 0.6V$$

$$I_{ADJ} = 16nA\ AT\ 25°C$$

OUTPUT RANGE = 0.6V TO 19V

Figure 3. Adjustable Operation

The LT3066 is tested and specified with the ADJ pin tied to the OUT pin, yielding V_{OUT} = 0.6V. Specifications for output voltages greater than 0.6V are proportional to the ratio of the desired output voltage to 0.6V: V_{OUT}/0.6V. For example, load regulation for an output current change of 1mA to 500mA is 0.1mV (typical) at V_{OUT} = 0.6V. At V_{OUT} = 12V, load regulation is:

$$\frac{12V}{0.6V} \bullet (0.1mV) = 2mV$$

Table 1 shows 1% resistor divider values for some common output voltages with a resistor divider current of 10µA.

Table 1. Output Voltage Resistor Divider Values

V_{OUT} (V)	R1 (kΩ)	R2 (kΩ)
1.2	60.4	60.4
1.5	59	88.7
1.8	59	118
2.5	60.4	191
3	59	237
3.3	61.9	280
5	59	432

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APPLICATIONS INFORMATION

Bypass Capacitance and Output Voltage Noise

The LT3066 regulator provides low output voltage noise over a 10Hz to 100kHz bandwidth while operating at full load with the addition of a bypass capacitor ($C_{REF/BYP}$) from the REF/BYP pin to GND. A high quality low leakage capacitor is recommended. This capacitor bypasses the internal reference of the regulator, providing a low frequency noise pole for the internal reference. With the use of 10nF for $C_{REF/BYP}$, output voltage noise decreases to as low as 25µV_{RMS} when the output voltage is set for 0.6V. For higher output voltages (generated by using a feedback resistor divider), the output voltage noise gains up proportionately when using $C_{REF/BYP}$.

To lower the higher output voltage noise, connect a feedforward capacitor (C_{FF}) from V_{OUT} to the ADJ pin. A high quality, low leakage capacitor is recommended. This capacitor bypasses the error amplifier of the regulator, providing an additional low frequency noise pole. With the use of 10nF for both C_{FF} and $C_{REF/BYP}$, output voltage noise decreases to 25µV_{RMS} when the output voltage is set to 5V by a 10µA feedback resistor divider. If the current in the feedback resistor divider is doubled, C_{FF} must also be doubled to achieve equivalent noise performance.

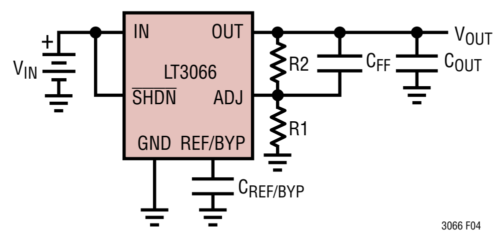
Feedforward capacitance can also be used in fixed-voltage parts; the feedforward capacitor is connected from OUT to ADJ in the same manner. In this case, the current in the internal feedback resistor divider is 5µA.

Higher values of output voltage noise can occur if care is not exercised with regard to circuit layout and testing. Crosstalk from nearby traces induces unwanted noise onto the LT3066's output. Power supply ripple rejection must also be considered. The LT3066 regulator does not have unlimited power supply rejection and passes a small portion of the input noise through to the output.

Using a feedforward capacitor (C_{FF}) connected between V_{OUT} and ADJ has the added benefit of improving transient response for output voltages greater than 0.6V. With no feedforward capacitor, the settling time increases as the output voltage increases above 0.6V. Use the equation in Figure 4 to determine the minimum value of C_{FF} to achieve a transient response that is similar to the 0.6V output voltage performance regardless of the chosen output voltage (See Figure 5 and Transient Response in the Typical Performance Characteristics section).

During start-up, the internal reference soft-starts when a REF/BYP capacitor is used. Regulator start-up time is directly proportional to the size of the bypass capacitor (see Start-Up Time vs REF/BYP Capacitor in the Typical Performance Characteristics section). The reference bypass capacitor is actively pulled low during shutdown to reset the internal reference.

Using a feedforward capacitor also affects start-up time. Start-up time is directly proportional to the size of the feedforward capacitor and the output voltage, and is inversely proportional to the feedback resistor divider current, slowing to 15ms with a 10nF feedforward capacitor and a 10µF output capacitor for an output voltage set to 5V by a 10µA feedback resistor divider.



$$C_{FF} \geq \frac{10nF}{10\mu A} \bullet \left(I_{FB\_DIVIDER}\right)$$

$$I_{FB\_DIVIDER} = \frac{V_{OUT}}{R1+R2}$$

Figure 4. Feedforward Capacitor for Fast Transient Response

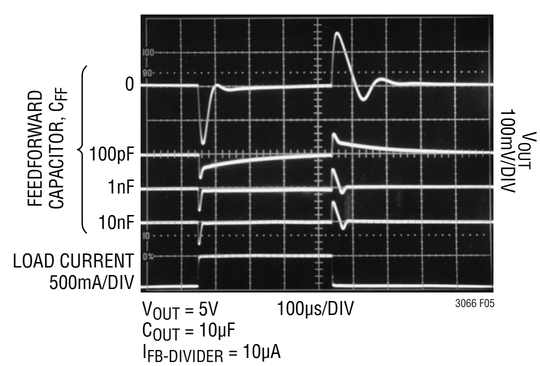


Figure 5. Transient Response vs Feedforward Capacitor

APPLICATIONS INFORMATION

Output Capacitance and Transient Response

The LT3066 regulator is stable with a wide range of output capacitors. The ESR of the output capacitor affects stability, most notably with small capacitors. Use a minimum output capacitor of 3.3µF with an ESR of 1Ω or less to prevent oscillations. For V_{OUT} less than 1.2V, use a minimum C_{OUT} of 4.7µF. The LT3066 is a micropower device and output load transient response is a function of output capacitance. Larger values of output capacitance decrease the peak deviations and provide improved transient response for larger load current changes. Bypass capacitors, used to decouple individual components powered by the LT3066, increase the effective output capacitor value. For applications with large load current transients, a low ESR ceramic capacitor in parallel with a bulk tantalum capacitor often provides an optimally damped response.

Give extra consideration to the use of ceramic capacitors. Manufacturers make ceramic capacitors with a variety of dielectrics, each with different behavior across temperature and applied voltage. The most common dielectrics are specified with EIA temperature characteristic codes of Z5U, Y5V, X5R and X7R. The Z5U and Y5V dielectrics provide high C-V products in a small package at low cost, but exhibit strong voltage and temperature coefficients, as shown in Figures 6 and 7. When used with a 5V regulator, a 16V 10µF Y5V capacitor can exhibit an effective value as low as 1µF to 2µF for the DC bias voltage applied, and over the operating temperature range. The X5R and X7R dielectrics yield much more stable characteristics and are more suitable for use as the output capacitor.

The X7R type works over a wider temperature range and has better temperature stability, while the X5R is less expensive and is available in higher values. Care still must be exercised when using X5R and X7R capacitors; the X5R and X7R codes only specify operating temperature range and maximum capacitance change over temperature. Capacitance change due to DC bias with X5R and X7R capacitors is better than Y5V and Z5U capacitors, but can still be significant enough to drop capacitor values below appropriate levels. Capacitor DC bias characteristics tend to improve as component case size increases, but expected capacitance at operating voltage should be verified.

Voltage and temperature coefficients are not the only sources of problems. Some ceramic capacitors have a piezoelectric response. A piezoelectric device generates voltage across its terminals due to mechanical stress, similar to the way a piezoelectric accelerometer or microphone works. For a ceramic capacitor, the stress is induced by vibrations in the system or thermal transients. The resulting voltages produced cause appreciable amounts of noise. A ceramic capacitor produced the trace in Figure 8 in response to light tapping from a pencil. Similar vibration induced behavior can masquerade as increased output voltage noise.

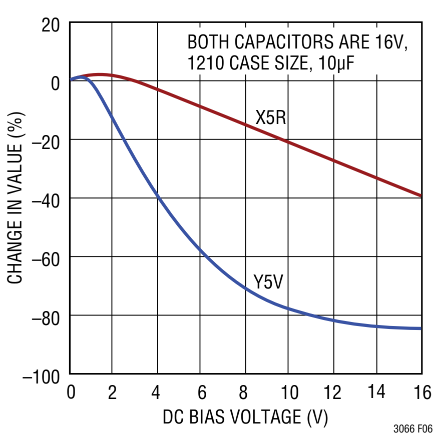


Figure 6. Ceramic Capacitor DC Bias Characteristics

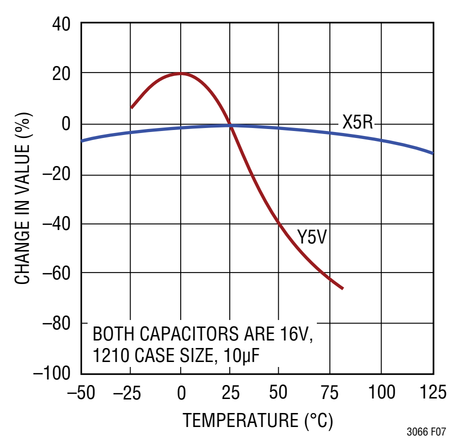


Figure 7. Ceramic Capacitor Temperature Characteristics

APPLICATIONS INFORMATION

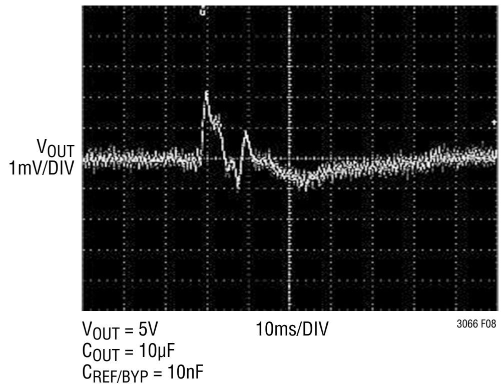


Figure 8. Noise Resulting from Tapping On a Ceramic Capacitor

Stability and Input Capacitance

Low ESR, ceramic input bypass capacitors are acceptable for applications without long input leads. However, applications connecting a power supply to an LT3066 circuit's IN and GND pins with long input wires combined with a low ESR, ceramic input capacitors are prone to voltage spikes, reliability concerns and application-specific board oscillations.

The input wire inductance found in many battery-powered applications, combined with the low ESR ceramic input capacitor, forms a high Q LC resonant tank circuit. In some instances this resonant frequency beats against the output current dependent LDO bandwidth and interferes with proper operation. Simple circuit modifications/solutions are then required. This behavior is not indicative of LT3066 instability, but is a common ceramic input bypass capacitor application issue.

The self-inductance, or isolated inductance, of a wire is directly proportional to its length. Wire diameter is not a major factor on its self-inductance. For example, the self-inductance of a 2-AWG isolated wire (diameter = 0.26") is about half the self-inductance of a 30-AWG wire (diameter = 0.01"). One foot of 30-AWG wire has approximately 465nH of self-inductance.

Two methods can reduce wire self-inductance. One method divides the current flowing towards the LT3066 between two parallel conductors. In this case, the farther apart the wires are from each other, the more the self-inductance is reduced; up to a 50% reduction when placed a few inches apart. Splitting the wires connects two equal inductors in parallel, but placing them in close proximity creates mutual inductance adding to the self-inductance. The second and most effective way to reduce overall inductance is to place both forward and return current conductors (the input and GND wires) in very close proximity. Two 30-AWG wires separated by only 0.02", used as forward and return current conductors, reduce the overall self-inductance to approximately one-fifth that of a single isolated wire.

If a battery, mounted in close proximity, powers the LT3066, a 10µF input capacitor suffices for stability. However, if a distant supply powers the LT3066, use a larger value input capacitor. Use a rough guideline of 1µF (in addition to the 10µF minimum) per 8 inches of wire length. The minimum input capacitance needed to stabilize the application also varies with power supply output impedance variations. Placing additional capacitance on the LT3066's output also helps. However, this requires an order of magnitude more capacitance in comparison with additional LT3066 input bypassing. Series resistance between the supply and the LT3066 input also helps stabilize the application; as little as 0.1Ω to 0.5Ω suffices. This impedance dampens the LC tank circuit at the expense of dropout voltage. A better alternative is to use higher ESR tantalum or electrolytic capacitors at the LT3066 input in place of ceramic capacitors.

Input Filtering

The INFILT pin is a separate input pin which supplies power to the error amplifier and reference. It is connected to the IN pin by a 140Ω resistor. Placing a decoupling capacitor from INFILT to ground creates an RC filter which reduces input supply ripple at the error amplifier and reference. Placing a 0.47µF decoupling capacitor on INFILT improves PSRR by as much as 30dB at frequencies greater than 10kHz. If input filtering is not required, connect the INFILT pin to the IN pins.

APPLICATIONS INFORMATION

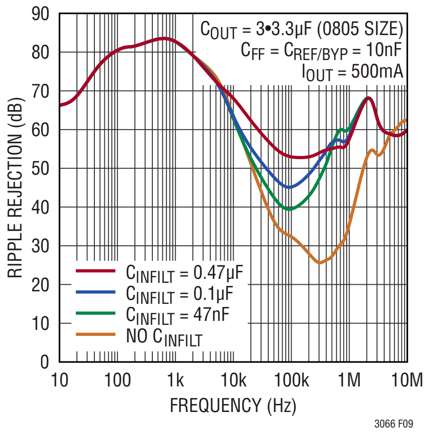


Figure 9. Input Ripple Rejection. V_{IN} = 4.3V + 50mV$_{RMS}$. V_{OUT} = 3.3

I_{MAX} Pin Operation

The I_{MAX} pin is the collector of a PNP that sources a current equal to 1/500th of output load current (see Block Diagram). The I_{MAX} pin is also the input to the precision current limit amplifier. Connecting a resistor (R_{IMAX}) from I_{MAX} to GND sets the current limit threshold. If the output load increases to a level such that the I_{MAX} pin voltage reaches 0.6V, the current limit amplifier takes control and regulates the I_{MAX} voltage to 0.6V, regardless of the output voltage. Calculate the required R_{IMAX} value for a given current limit from the following formula:

$$R_{IMAX} = 500 \bullet \frac{0.6V}{I_{LIMIT}}$$

In cases where the IN to OUT differential voltage exceeds 10V, current limit foldback lowers the internal current limit level, possibly causing it to override the external programmable current limit. See the Internal Current Limit vs V_{IN} – V_{OUT} graph in the Typical Performance Characteristics section.

The I_{MAX} pin requires a 22nF decoupling capacitor. If the external programmable current limit is not used, connect the I_{MAX} pin directly to GND. LT3066 power dissipation increases the I_{MAX} threshold at a rate of approximately 0.5 percent per watt.

PWRGD Pin Operation

The PWRGD pin is an open-drain high voltage NMOS digital output capable of sinking 50µA. The PWRGD pin de-asserts and becomes high impedance if the output rises above 90% of its nominal value. If the output falls below 88.4% of its nominal value for more than 25µs, the PWRGD pin asserts low. The PWRGD comparator has 1.6% hysteresis and about 25µs of deglitching. The PWRGD comparator has a dedicated reference that does not soft-start if a capacitor is used on the REF/BYP pin.

The use of a feed-forward capacitor, C_{FF}, as shown in Figure 4, can result in the ADJ pin being pulled artificially high during startup transients, which causes the PWRGD flag to assert early. To avoid this problem, ensure that the REF/BYP capacitor is significantly larger than the feed-forward capacitor, causing REF/BYP time constant to dominate over the time constant of the resistor divider network.

Operation in Dropout

Some degradation of the I_{MAX} current mirror accuracy occurs for output currents less than 50mA when operating in dropout.

Overload Recovery

Like many IC power regulators, the LT3066 has safe operating area protection. The safe area protection decreases current limit as input-to-output voltage increases, and keeps the power transistor inside a safe operating region for all values of input-to-output voltage. The LT3066 provides some output current at all values of input-to-output voltage up to the device's Absolute Maximum Rating.

When power is first applied, the input voltage rises and the output follows the input; allowing the regulator to start-up into very heavy loads. During start-up, as the input voltage is rising, the input-to-output voltage differential is small, allowing the regulator to supply large output currents. With a high input voltage, a problem can occur wherein the removal of an output short will not allow the output to recover. Other regulators, such as the LT1083/LT1084/LT1085 family and LT1764A also exhibit this phenomenon, so it is not unique to the LT3066. The problem occurs with a heavy output load when the input voltage is high and the output voltage is low. Common situations are immediately after the removal of a short circuit or if the shutdown pin is pulled high after the input voltage is already turned on.

APPLICATIONS INFORMATION

The load line intersects the output current curve at two points. If this happens, there are two stable output operating points for the regulator. With this double intersection, the input power supply needs to be cycled down to zero and back up again to recover the output.

Active Output Discharge

The LT3066 includes a low resistance NMOS device which rapidly discharges the output voltage if the part is put in shutdown mode. For a 2.9V output with a 10µF decoupling capacitor, the NMOS discharges the output to 290mV in 750µs if $\overline{SHDN}$ is driven low.

Control circuitry drives the gate of the NMOS high if either the $\overline{SHDN}$ pin or the IN pin are driven low. In the case where the IN pin is driven to ground, the NMOS rapidly discharges the OUT pin to the threshold voltage of the NMOS, approximately 800mV. From 800mV, the external load discharges the OUT pin at a reduced rate.

The $\overline{SHDN}$ pin threshold to turn on the output discharge NMOS is nominally 560mV at room temperature (see Typical Performance curves). In order to ensure rapid discharge at high temperature, drive $\overline{SHDN}$ below 200mV.

The control circuitry implements protection features which allow the OUT pin to be driven from –1V to 20V without damaging the LT3066. Current limit foldback for output voltages greater than 6V protects the NMOS pull-down, but increases discharge times for higher output voltages.

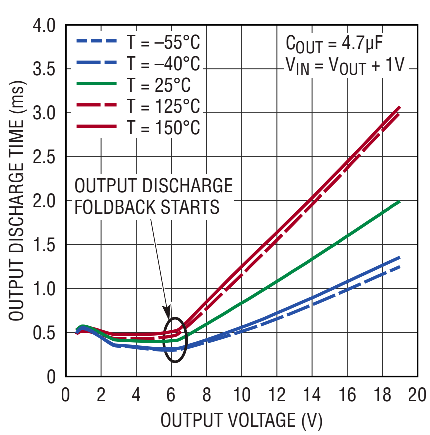


Figure 10. Discharge Time vs Output Voltage

Thermal Considerations

The LT3066's maximum rated junction temperature of 125°C (E-, I-grades) limits its power handling capability. Two components comprise the power dissipated by the device:

1. Output current multiplied by the input/output voltage differential:

   $I_{OUT} \bullet (V_{IN} - V_{OUT})$,

   and

2. GND pin current multiplied by the input voltage:

   $I_{GND} \bullet V_{IN}$

GND pin current is determined using the GND Pin Current curves in the Typical Performance Characteristics section. Power dissipation equals the sum of the two components listed above.

The LT3066 regulator has internal thermal limiting that protects the device during overload conditions. For continuous normal conditions, do not exceed the maximum junction temperature of 125°C (E-, I-grades). Carefully consider all sources of thermal resistance from junction-to-ambient including other heat sources mounted in proximity to the LT3066.

The undersides of the LT3066 DFN and MSE packages have exposed metal from the lead frame to the die attachment. These packages allow heat to directly transfer from the die junction to the printed circuit board metal to control maximum operating junction temperature. The dual-in line pin arrangement allows metal to extend beyond the ends of the package on the topside (component side) of a PCB. Connect this metal to GND on the PCB. The multiple IN and OUT pins of the LT3066 also assist in spreading heat to the PCB.

For surface mount devices, heat sinking is accomplished by using the heat spreading capabilities of the PC board and its copper traces. Copper board stiffeners and plated through-holes also can spread the heat generated by power devices.

APPLICATIONS INFORMATION

Tables 2 and 3 list thermal resistance as a function of copper area in a fixed board size. All measurements were taken in still air on a 4-layer FR-4 board with 1oz solid internal planes, and 2oz external trace planes with a total board thickness of 1.6mm. For further information on thermal resistance and using thermal information, refer to JEDEC standard JESD51, notably JESD51-12.

Table 2. MSOP Measured Thermal Resistance

COPPER AREA			
TOPSIDE (sq mm)	BACKSIDE (sq mm)	BOARD AREA	THERMAL RESISTANCE (JUNCTION-TO-AMBIENT)
2500	2500	2500	34°C/W
1000	2500	2500	34°C/W
225	2500	2500	37°C/W
100	2500	2500	44°C/W

Table 3. DFN Measured Thermal Resistance

COPPER AREA TOPSIDE (sq mm)	BOARD AREA (sq mm)	THERMAL RESISTANCE (JUNCTION-TO-AMBIENT)
2500	2500	34°C/W
1000	2500	36°C/W
225	2500	39°C/W
100	2500	42°C/W

Calculating Junction Temperature

Example: Given an output voltage of 5V, an input voltage range of 12V ±5%, a maximum output current range of 75mA and a maximum ambient temperature of 85°C, what is the maximum junction temperature?

The power dissipated by the device equals:

$$I_{OUT(MAX)} \bullet (V_{IN(MAX)} - V_{OUT}) + I_{GND} \bullet V_{IN(MAX)}$$

where:

$I_{OUT(MAX)} = 75mA$

$V_{IN(MAX)} = 12.6V$

I_{GND} at ($I_{OUT} = 75mA$, $V_{IN} = 12V$) = 3.5mA

So:

$$P = 75mA \bullet (12.6V - 5V) + 3.5mA \bullet 12.6V = 0.614W$$

Using a DFN package, the thermal resistance ranges from 31°C/W to 35°C/W depending on the copper area. So the junction temperature rise above ambient approximately equals:

$$0.614W \bullet 34°C/W = 20.9°C$$

The maximum junction temperature equals the maxi-mum ambient temperature plus the maximum junction temperature rise above ambient or:

$$T_{JMAX} = 85°C + 20.9°C = 105.9°C$$

Protection Features

The LT3066 incorporates several protection features that make it ideal for use in battery-powered circuits. In addition to the normal protection features associated with monolithic regulators, such as current limiting and thermal limiting, the device also protects against reverse input voltages, reverse output voltages and reverse output-to-input voltages.

Current limit protection and thermal overload protection protect the device against current overload conditions at the LT3066's output. The typical thermal shutdown temperature is 165°C with about 7°C of hysteresis. For normal operation, do not exceed a junction temperature of 125°C (E-, I-grades).

The LT3066 IN pin withstands reverse voltages of 50V. The device limits current flow to less than 1mA and no negative voltage appears at OUT. The device protects both itself and the load against batteries that are plugged in backwards.

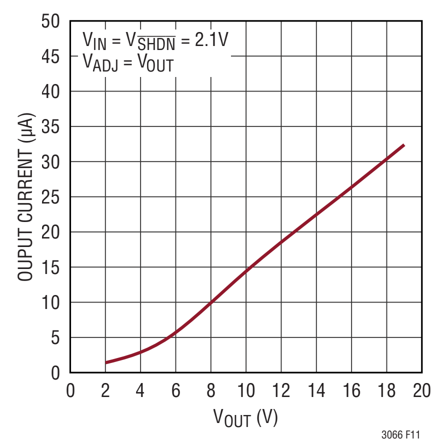


Figure 11. Reverse Output Current

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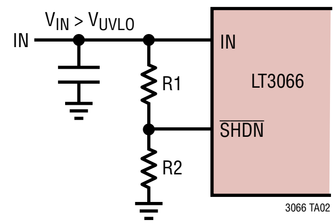
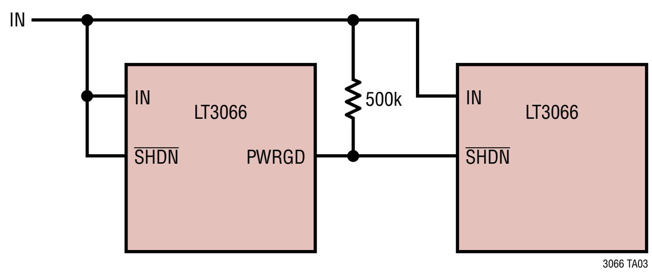
TYPICAL APPLICATIONS

Programming Undervoltage Lockout

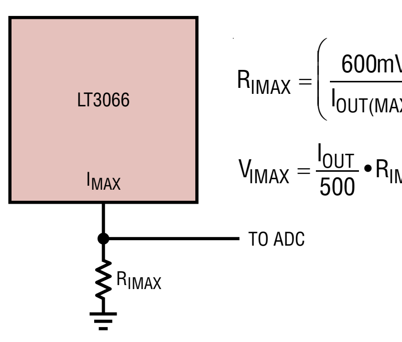


$$V_{UVLO} = \frac{R1 + R2}{R2} \bullet 1.1V$$

Power Supply Sequencing Using PWRGD



Current Monitor

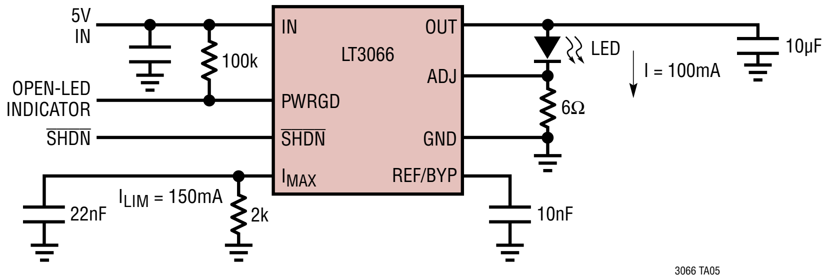


$$R_{IMAX} = \left(\frac{600mV}{I_{OUT(MAX)}}\right) \bullet 500$$

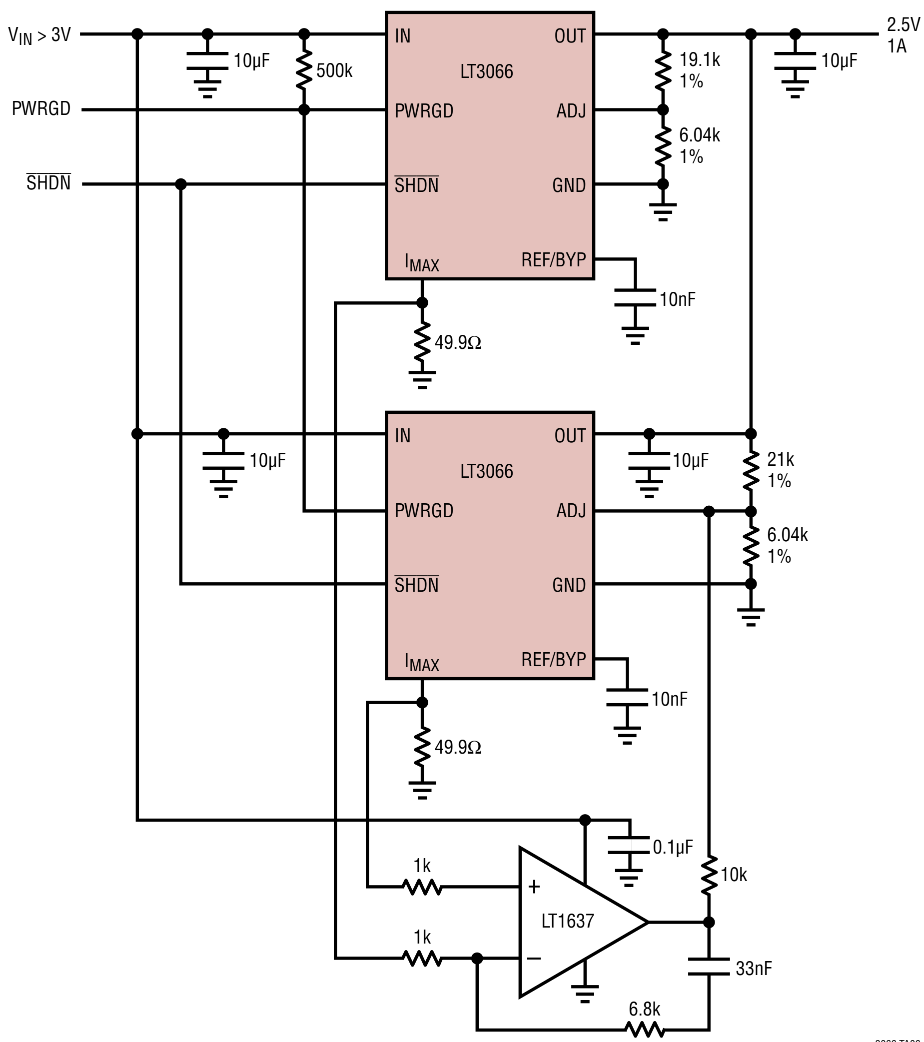
$$V_{IMAX} = \frac{I_{OUT}}{500} \bullet R_{IMAX}$$

TYPICAL APPLICATIONS

LED Driver/Current Source



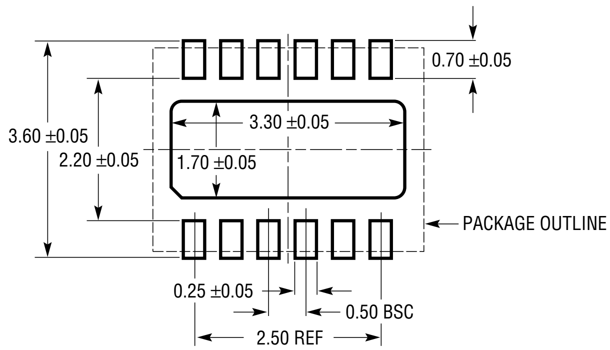
Paralleling Regulators for Higher Output Current



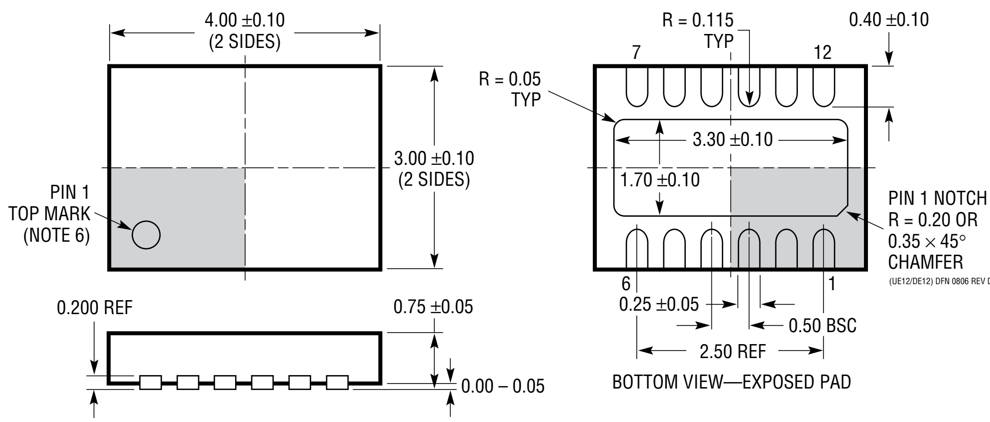
Rev. B

PACKAGE DESCRIPTION

DE/UE Package
12-Lead Plastic DFN (4mm × 3mm)
(Reference LTC DWG # 05-08-1695 Rev D)



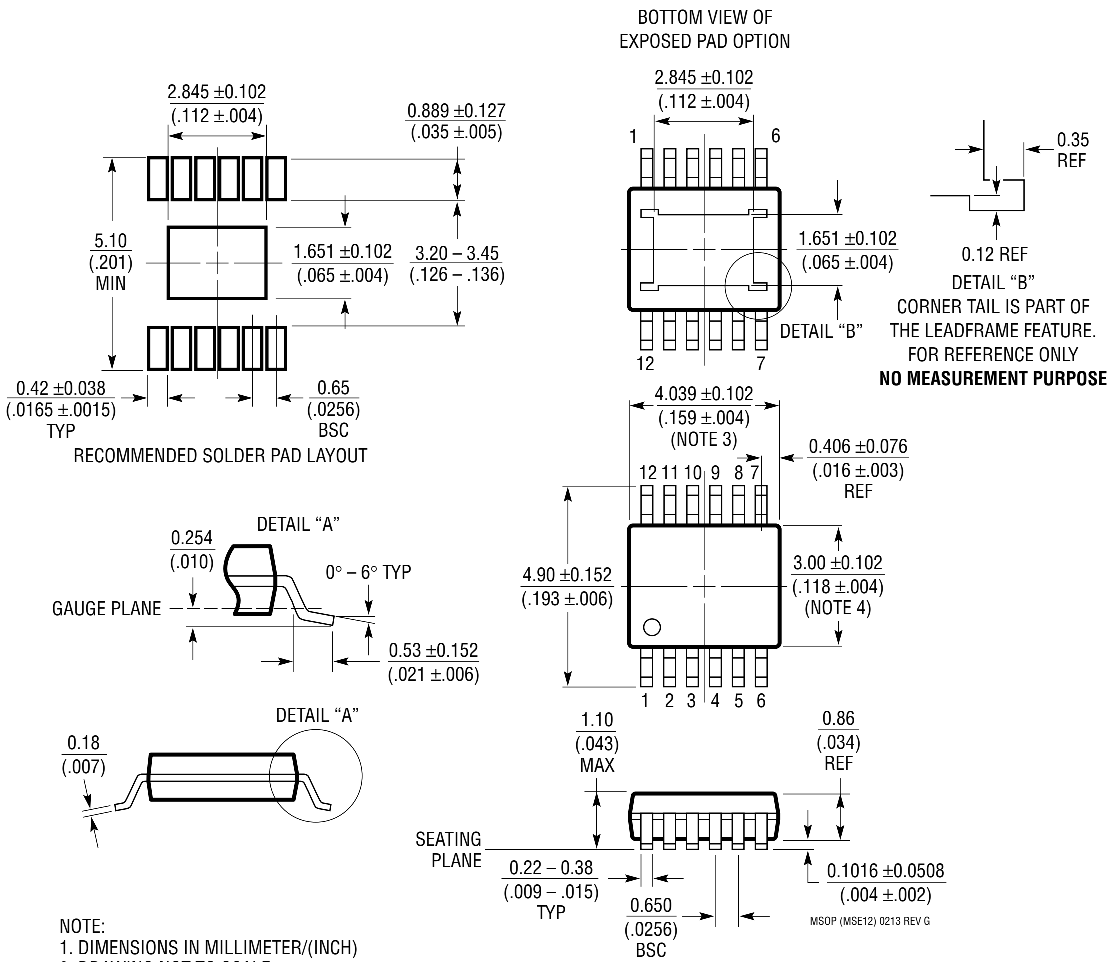
RECOMMENDED SOLDER PAD PITCH AND DIMENSIONS
APPLY SOLDER MASK TO AREAS THAT ARE NOT SOLDERED



NOTE:
1. DRAWING PROPOSED TO BE A VARIATION OF VERSION (WGED) IN JEDEC PACKAGE OUTLINE M0-229
2. DRAWING NOT TO SCALE
3. ALL DIMENSIONS ARE IN MILLIMETERS
4. DIMENSIONS OF EXPOSED PAD ON BOTTOM OF PACKAGE DO NOT INCLUDE MOLD FLASH. MOLD FLASH, IF PRESENT, SHALL NOT EXCEED 0.15mm ON ANY SIDE
5. EXPOSED PAD SHALL BE SOLDER PLATED
6. SHADED AREA IS ONLY A REFERENCE FOR PIN 1 LOCATION ON THE TOP AND BOTTOM OF PACKAGE

PACKAGE DESCRIPTION

MSE Package
12-Lead Plastic MSOP, Exposed Die Pad
(Reference LTC DWG # 05-08-1666 Rev G)



NOTE:
1. DIMENSIONS IN MILLIMETER/(INCH)
2. DRAWING NOT TO SCALE
3. DIMENSION DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH, PROTRUSIONS OR GATE BURRS SHALL NOT EXCEED 0.152mm (.006") PER SIDE
4. DIMENSION DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSIONS. INTERLEAD FLASH OR PROTRUSIONS SHALL NOT EXCEED 0.152mm (.006") PER SIDE
5. LEAD COPLANARITY (BOTTOM OF LEADS AFTER FORMING) SHALL BE 0.102mm (.004") MAX
6. EXPOSED PAD DIMENSION DOES INCLUDE MOLD FLASH. MOLD FLASH ON E-PAD SHALL NOT EXCEED 0.254mm (.010") PER SIDE.

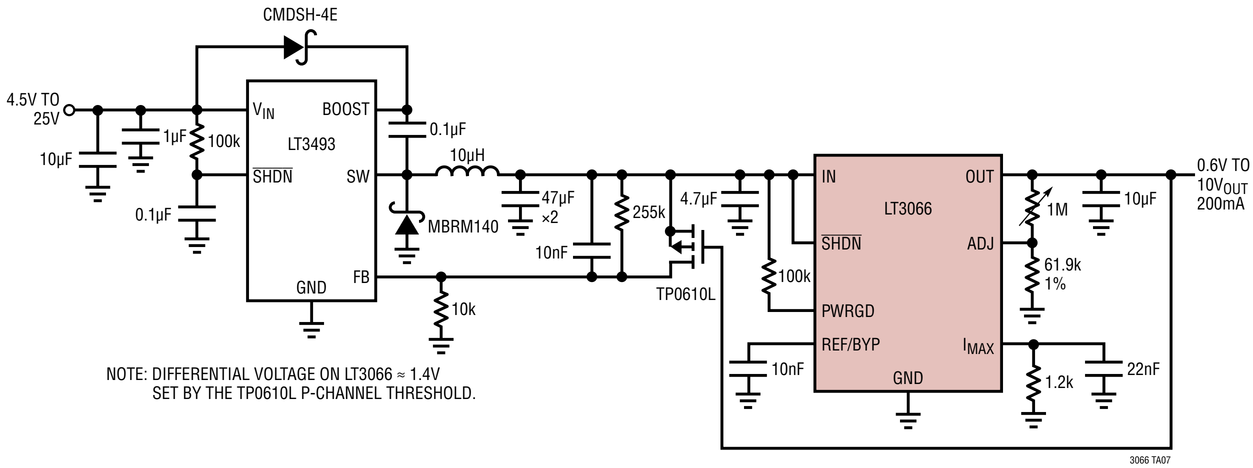
Rev. B

REVISION HISTORY

REV	DATE	DESCRIPTION	PAGE NUMBER
A	05/16	Add –3.3V, –5V fixed voltage options.	1–26
B	10/18	Change typical minimum input voltage from 1.8V to 1.6V	1, 3, 14
		Update Minimum Input Voltage graph in Typical Performance Section	8
		Add 10μF output capacitor to figure TA05	22
		Update Related Parts section with new 1.6V minimum V_{IN} (LT3050/LT3055/LT3060/LT3065)	26

TYPICAL APPLICATION

Adjustable High Efficiency Regulator



RELATED PARTS

PART NUMBER	DESCRIPTION	COMMENTS
LT1761	100mA, Low Noise LDO	300mV Dropout Voltage, Low Noise: 20µV_{RMS}, V_{IN} = 1.8V to 20V, ThinSOT™ Package
LT1762	150mA, Low Noise LDO	300mV Dropout Voltage, Low Noise: 20µV_{RMS}, V_{IN} = 1.8V to 20V, MS8 Package
LT1763	500mA, Low Noise LDO	300mV Dropout Voltage, Low Noise: 20µV_{RMS}, V_{IN} = 1.8V to 20V, SO-8 and 3mm × 4mm DFN Packages
LT1962	300mA, Low Noise LDO	270mV Dropout Voltage, Low Noise: 20µV_{RMS}, V_{IN} = 1.8V to 20V, MS8 Package
LT1964	200mA, Low Noise Negative LDO	V_{IN} = –2.2V to –20V, $V_{OUT(MIN)}$ = –1.21V, V_{DO} = 0.34V, I_Q = 30µA, I_{SD} = 3µA, Low Noise <30µV_{RMS}, Stable with Ceramic Capacitors, ThinSOT and 3mm × 3mm DFN Packages
LT1965	1.1A, Low Noise LDO	290mV Dropout Voltage, Low Noise: 40µV_{RMS}, V_{IN} = 1.8V to 20V, V_{OUT} = 1.2V to 19.5V, Stable with Ceramic Capacitors, TO-220, DD-Pak, MSOP and 3mm × 3mm DFN Packages
LT3050	100mA LDO with Diagnostics and Precision Current Limit	340mV Dropout Voltage, Low Noise: 30µV_{RMS}, V_{IN} = 1.6V to 45V, 3mm × 2mm DFN and MSOP Packages
LT3055	500mA LDO with Diagnostics and Precision Current Limit	350mV Dropout Voltage, Low Noise: 25µV_{RMS}, V_{IN} = 1.6V to 45V, 4mm × 3mm DFN and MSOP Packages
LT3060	100mA Low Noise LDO with Soft-Start	300mV Dropout Voltage, Low Noise: 30µV_{RMS}, V_{IN} = 1.6V to 45V, 2mm × 2mm DFN and ThinSOT Packages
LT3061	45V V_{IN}, Micropower, Low Noise, 100mA LDO with Output Discharge	250mV Dropout Voltage, Low Noise: 30µV_{RMS}, V_{IN} = 1.6V to 45V, 8-Lead 2mm × 3mm DFN and MSOP Packages
LT3063	45V V_{IN}, Micropower, Low Noise, 200mA LDO with Output Discharge	300mV Dropout Voltage, Low Noise: 30µV_{RMS}, V_{IN} = 1.6V to 45V, 8-Lead 2mm × 3mm DFN and MSOP Packages
LT3065	45V V_{IN}, 500mA Low Noise, Linear Regulator with Programmable Current Limit and Power Good	300mV Dropout Voltage, Low Noise: 25µV_{RMS}, V_{IN} = 1.6V to 45V, 10-Lead 3mm × 3mm DFN and 12-lead MSOP Packages
LT3080/ LT3080-1	1.1A, Parallelable, Low Noise LDO	300mV Dropout Voltage (2-Supply Operation), Low Noise 40µV_{RMS}, V_{IN} = 1.2V to 36V, V_{OUT} = 0V to 35.7V, Current-Based Reference with 1-Resistor V_{OUT} Set, Directly Parallelable, Stable with Ceramic Capacitors, TO-220, SOT-223, MSOP and 3mm × 3mm DFN
LT3082	200mA, Parallelable, Low Noise LDO	Outputs may be Paralleled for Higher Output Current or Heat Spreading, Wide Input Voltage Range: 1.2V to 40V, Low Value Input/Output Capacitors Required: 2.2µF, Single Resistor Sets Output Voltage, 8-Lead SOT-23, 3-Lead SOT-223 and 8-Lead 3mm × 3mm DFN Packages
LT3085	500mA, Parallelable, Low Noise LDO	275mV Dropout Voltage (2-Supply Operation), Low Noise 40µV_{RMS}, V_{IN} = 1.2V to 36V, V_{OUT} = 0V to 35.7V, Current-Based Reference with 1-Resistor V_{OUT} Set, Directly Parallelable, Stable with Ceramic Capacitors, MS8E and 2mm × 3mm DFN-6 Packages

10/18
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