

# 800MHz Low Distortion, Low Noise Differential Amplifier/ADC Driver ( $A_V = 2V/V$ )

## FEATURES

- 800MHz –3dB Bandwidth
- Fixed Gain of 2V/V (6dB)
- Low Distortion:
  - 38dBm OIP3, –70dBc HD3 (70MHz, 2V<sub>P-P</sub>)
  - 51dBm OIP3, –94dBc HD3 (10MHz, 2V<sub>P-P</sub>)
- Low Noise: 12.3dB NF,  $e_n = 3.8nV/\sqrt{Hz}$  (70MHz)
- Differential Inputs and Outputs
- Additional Filtered Outputs
- Adjustable Output Common Mode Voltage
- DC- or AC-Coupled Operation
- Minimal Support Circuitry Required
- Small 0.75mm Tall 16-Lead 3 × 3 QFN Package

## APPLICATIONS

- Differential ADC Driver for:
  - Imaging
  - Communications
- Differential Driver/Receiver
- Single Ended to Differential Conversion
- Differential to Single Ended Conversion
- Level Shifting
- IF Sampling Receivers
- SAW Filter Interfacing/Buffering

All registered trademarks and trademarks are the property of their respective owners.

## DESCRIPTION

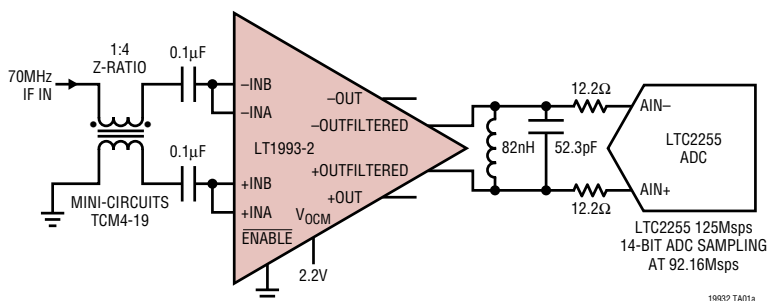
The **LT<sup>®</sup>1993-2** is a low distortion, low noise Differential Amplifier/ADC driver for use in applications from DC to 800MHz. The LT1993-2 has been designed for ease of use, with minimal support circuitry required. Exceptionally low input-referred noise and low distortion products (with either single-ended or differential inputs) make the LT1993-2 an excellent solution for driving high speed 12-bit and 14-bit ADCs. In addition to the normal unfiltered outputs (+OUT and –OUT), the LT1993-2 has a built-in 175MHz differential low pass filter and an additional pair of filtered outputs (+OUTFILTERED, –OUTFILTERED) to reduce external filtering components when driving high speed ADCs. The output common mode voltage is easily set via the V<sub>OCM</sub> pin, eliminating either an output transformer or AC-coupling capacitors in many applications.

The LT1993-2 is designed to meet the demanding requirements of communications transceiver applications. It can be used as a differential ADC driver, a general-purpose differential gain block, or in any other application requiring differential drive. The LT1993-2 can be used in data acquisition systems required to function at frequencies down to DC.

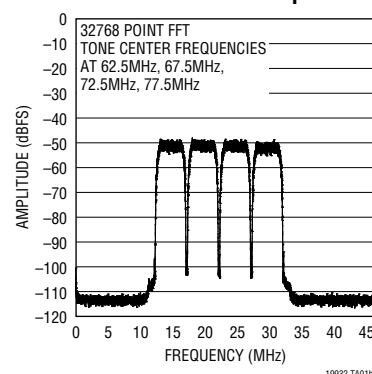
The LT1993-2 operates on a 5V supply and consumes 100mA. It comes in a compact 16-lead 3 × 3 QFN package and operates over a –40°C to 85°C temperature range.

## TYPICAL APPLICATION

**4-Channel WCDMA Receive Channel**



**4-Tone WCDMA Waveform,  
LT1993-2 Driving LTC2255 14-Bit  
ADC at 92.16Msps**

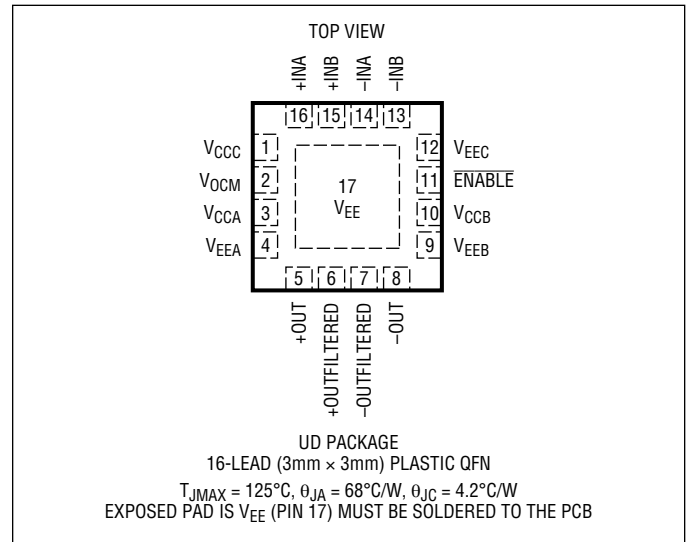


## ABSOLUTE MAXIMUM RATINGS

(Note 1)

|   |  |
|---|--|
| Total Supply Voltage ( $V_{CCA}/V_{CCB}/V_{CCC}$ to $V_{EEA}/V_{EEB}/V_{EEC}$ ) | 5.5V   |
| Input Current (+INA, -INA, +INB, -INB, $V_{OCM}$ , $\overline{\text{ENABLE}}$ ) | $\pm 10\text{mA}$                              |
| Output Current (Continuous) (Note 6)  |  |
| +OUT, -OUT (DC)   | $\pm 100\text{mA}$                             |
| (AC)  | $\pm 100\text{mA}$                             |
| +OUTFILTERED, -OUTFILTERED (DC)   | $\pm 15\text{mA}$                              |
| (AC)  | $\pm 45\text{mA}$                              |
| Output Short Circuit Duration (Note 2)  | Indefinite                                     |
| Operating Temperature Range (Note 3)  | $-40^{\circ}\text{C}$ to $85^{\circ}\text{C}$  |
| Specified Temperature Range (Note 4)  | $-40^{\circ}\text{C}$ to $85^{\circ}\text{C}$  |
| Storage Temperature Range   | $-65^{\circ}\text{C}$ to $125^{\circ}\text{C}$ |
| Junction Temperature  | $125^{\circ}\text{C}$                          |
| Lead Temperature Range (Soldering 10 sec)                                       | $300^{\circ}\text{C}$                          |

## PIN CONFIGURATION



## ORDER INFORMATION

| LEAD FREE FINISH | TAPE AND REEL     | PART MARKING* | PACKAGE DESCRIPTION             | TEMPERATURE RANGE                             |
|------------------|-------------------|---------------|---------------------------------|---|
| LT1993CUD-2#PBF  | LT1993CUD-2#TRPBF | LBJG          | 16-LEAD (3mm x 3mm) PLASTIC QFN | $-40^{\circ}\text{C}$ to $85^{\circ}\text{C}$ |
| LT1993IUD-2#PBF  | LT1993IUD-2#TRPBF | LBJG          | 16-LEAD (3mm x 3mm) PLASTIC QFN | $-40^{\circ}\text{C}$ to $85^{\circ}\text{C}$ |

Consult ADI Marketing for parts specified with wider operating temperature ranges. \*The temperature grade is identified by a label on the shipping container.

[Tape and reel specifications](#). Some packages are available in 500 unit reels through designated sales channels with #TRMPBF suffix.

## DC ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at  $T_A = 25^{\circ}\text{C}$ .  $V_{CCA} = V_{CCB} = V_{CCC} = 5\text{V}$ ,  $V_{EEA} = V_{EEB} = V_{EEC} = 0\text{V}$ ,  $\overline{\text{ENABLE}} = 0.8\text{V}$ , +INA shorted to +INB (+IN), -INA shorted to -INB (-IN),  $V_{OCM} = 2.2\text{V}$ , Input common mode voltage =  $2.2\text{V}$ , no  $R_{LOAD}$  unless otherwise noted.

| SYMBOL  | PARAMETER                     | CONDITIONS  |   | MIN         | TYP      | MAX         | UNITS                  |
|---|-------------------------------|---|---|-------------|----------|-------------|------------------------|
| Input/Output Characteristics (+INA, +INB, -INA, -INB, +OUT, -OUT, +OUTFILTERED, -OUTFILTERED) |                               |   |   |             |          |             |                        |
| GDIF  | Gain                          | Differential (+OUT, -OUT), $V_{IN} = \pm 0.8V$ Differential                           | ● | 5.8         | 6.08     | 6.3         | dB                     |
| $V_{SWINGMIN}$  |                               | Single-Ended +OUT, -OUT, +OUTFILTERED, -OUTFILTERED. $V_{IN} = \pm 2.2V$ Differential | ● |             | 0.25     | 0.35<br>0.5 | V<br>V                 |
| $V_{SWINGMAX}$  |                               | Single-Ended +OUT, -OUT, +OUTFILTERED, -OUTFILTERED. $V_{IN} = \pm 2.2V$ Differential | ● | 3.6<br>3.5  | 3.75     |             | V<br>V                 |
| $V_{SWINGDIFF}$   | Output Voltage Swing          | Differential (+OUT, -OUT), $V_{IN} = \pm 2.2V$ Differential                           | ● | 6.5<br>6    | 7        |             | $V_{P-P}$<br>$V_{P-P}$ |
| $I_{OUT}$   | Output Current Drive          | (Note 5)  | ● | $\pm 40$    | $\pm 45$ |             | mA                     |
| $V_{OS}$  | Input Offset Voltage          |   | ● | -6.5<br>-10 | 1        | 6.5<br>10   | mV<br>mV               |
| $TCV_{OS}$  | Input Offset Voltage Drift    | $T_{MIN}$ to $T_{MAX}$  | ● |             | 2.5      |             | $\mu V/^{\circ}C$      |
| $I_{VRMIN}$   | Input Voltage Range, MIN      | Single-Ended  | ● |             |          | -0.1        | V                      |
| $I_{VRMAX}$   | Input Voltage Range, MAX      | Single-Ended  | ● | 5.1         |          |             | V                      |
| $R_{INDIFF}$  | Differential Input Resistance |   | ● | 170         | 200      | 240         | $\Omega$               |

Rev B

## DC ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at  $T_A = 25^\circ\text{C}$ .  $V_{CCA} = V_{CCB} = V_{CCC} = 5\text{V}$ ,  $V_{EEA} = V_{EEB} = V_{EEC} = 0\text{V}$ ,  $\text{ENABLE} = 0.8\text{V}$ ,  $+INA$  shorted to  $+INB$  ( $+IN$ ),  $-INA$  shorted to  $-INB$  ( $-IN$ ),  $V_{OCM} = 2.2\text{V}$ , Input common mode voltage =  $2.2\text{V}$ , no  $R_{LOAD}$  unless otherwise noted.

| SYMBOL        | PARAMETER                      | CONDITIONS  | MIN  | TYP | MAX | UNITS    |
|---------------|--------------------------------|---|------|-----|-----|----------|
| $C_{INDIFF}$  | Differential Input Capacitance |   |      | 1   |     | pF       |
| CMRR          | Common Mode Rejection Ratio    | Input Common Mode $-0.1\text{V}$ to $5.1\text{V}$ | ● 45 | 70  |     | dB       |
| $R_{OUTDIFF}$ | Output Resistance              |   |      | 0.3 |     | $\Omega$ |
| $C_{OUTDIFF}$ | Output Capacitance             |   |      | 0.8 |     | pF       |

### Common Mode Voltage Control ( $V_{OCM}$ Pin)

|                     |  |  |   |            |          |            |            |
|---------------------|--|--|---|------------|----------|------------|------------|
| GCM                 | Common Mode Gain                                 | Differential (+OUT, −OUT), V <sub>OCM</sub> = 1.1V to 3.6V<br>Differential (+OUT, −OUT), V <sub>OCM</sub> = 1.3V to 3.4V | ● | 0.9<br>0.9 | 1<br>1.1 | 1.1<br>1.1 | V/V<br>V/V |
| V <sub>OCMMIN</sub> | Output Common Mode Voltage Adjustment Range, MIN | Measured Single-Ended at +OUT and −OUT   | ● |            |          | 1.1<br>1.3 | V<br>V     |
| V <sub>OCMMAX</sub> | Output Common Mode Voltage Adjustment Range, MAX | Measured Single-Ended at +OUT and −OUT   | ● | 3.6<br>3.4 |          |            | V<br>V     |
| V <sub>OSCM</sub>   | Output Common Mode Offset Voltage                | Measured from V <sub>OCM</sub> to Average of +OUT and −OUT   | ● | −30        | 4        | 30         | mV         |
| I <sub>BIASCM</sub> | V <sub>OCM</sub> Input Bias Current              |  | ● |            | 5        | 15         | μA         |
| R <sub>INCM</sub>   | V <sub>OCM</sub> Input Resistance                |  | ● | 0.8        | 3        |            | MΩ         |
| C <sub>INCM</sub>   | V <sub>OCM</sub> Input Capacitance               |  |   |            | 1        |            | pF         |

### ENABLE Pin

|          |                           |                        |   |   |     |               |
|----------|---------------------------|------------------------|---|---|-----|---------------|
| $V_{IL}$ | ENABLE Input Low Voltage  |                        | ● |   | 0.8 | V             |
| $V_{IH}$ | ENABLE Input High Voltage |                        | ● | 2 |     | V             |
| $I_{IL}$ | ENABLE Input Low Current  | ENABLE = $0.8\text{V}$ | ● |   | 0.5 | $\mu\text{A}$ |
| $I_{IH}$ | ENABLE Input High Current | ENABLE = $2\text{V}$   | ● | 1 | 3   | $\mu\text{A}$ |

### Power Supply

|                 |                              |                              |   |    |     |     |               |
|-----------------|------------------------------|------------------------------|---|----|-----|-----|---------------|
| $V_S$           | Operating Range              |                              | ● | 4  | 5   | 5.5 | V             |
| $I_S$           | Supply Current               | ENABLE = $0.8\text{V}$       | ● | 88 | 100 | 112 | mA            |
| $I_{SDISABLED}$ | Supply Current (Disabled)    | ENABLE = $2\text{V}$         | ● |    | 250 | 500 | $\mu\text{A}$ |
| PSRR            | Power Supply Rejection Ratio | $4\text{V}$ to $5.5\text{V}$ | ● | 55 | 90  |     | dB            |

## AC ELECTRICAL CHARACTERISTICS

$T_A = 25^\circ\text{C}$ ,  $V_{CCA} = V_{CCB} = V_{CCC} = 5\text{V}$ ,  $V_{EEA} = V_{EEB} = V_{EEC} = 0\text{V}$ ,  $\text{ENABLE} = 0.8\text{V}$ ,  $+INA$  shorted to  $+INB$  ( $+IN$ ),  $-INA$  shorted to  $-INB$  ( $-IN$ ),  $V_{OCM} = 2.2\text{V}$ , Input common mode voltage =  $2.2\text{V}$ , no  $R_{LOAD}$  unless otherwise noted.

| SYMBOL                              | PARAMETER                    | CONDITIONS   | MIN | TYP  | MAX | UNITS            |
|-------------------------------------|------------------------------|--|-----|------|-----|------------------|
| <b>Input/Output Characteristics</b> |                              |  |     |      |     |                  |
| -3dB BW                             | -3dB Bandwidth               | $200\text{mV}_{p-p}$ Differential (+OUT, -OUT)                     | 500 | 800  |     | MHz              |
| 0.1dB BW                            | Bandwidth for 0.1dB Flatness | $200\text{mV}_{p-p}$ Differential (+OUT, -OUT)                     |     | 50   |     | MHz              |
| 0.5dB BW                            | Bandwidth for 0.5dB Flatness | $200\text{mV}_{p-p}$ Differential (+OUT, -OUT)                     |     | 100  |     | MHz              |
| SR                                  | Slew Rate                    | $3.2\text{V}_{p-p}$ Differential (+OUT, -OUT)                      |     | 1100 |     | V/ $\mu\text{s}$ |
| $t_{s1\%}$                          | 1% Settling Time             | 1% Settling for a $1\text{V}_{p-p}$ Differential Step (+OUT, -OUT) |     | 4    |     | ns               |
| $t_{ON}$                            | Turn-On Time                 |  |     | 40   |     | ns               |
| $t_{OFF}$                           | Turn-Off Time                |  |     | 250  |     | ns               |

## AC ELECTRICAL CHARACTERISTICS

$T_A = 25^\circ\text{C}$ ,  $V_{CCA} = V_{CCB} = V_{CCC} = 5\text{V}$ ,  $V_{EEA} = V_{EEB} = V_{EEC} = 0\text{V}$ ,  $\text{ENABLE} = 0.8\text{V}$ , +INA shorted to +INB (+IN), -INA shorted to -INB (-IN),  $V_{OCM} = 2.2\text{V}$ , Input common mode voltage =  $2.2\text{V}$ , no  $R_{LOAD}$  unless otherwise noted.

| SYMBOL   | PARAMETER  | CONDITIONS   | MIN | TYP  | MAX | UNITS                        |
|--|--|--|-----|------|-----|------------------------------|
| <b>Common Mode Voltage Control (<math>V_{OCM}</math> Pin)</b>  |  |  |     |      |     |                              |
| $-3\text{dB BW}_{CM}$  | Common Mode Small-Signal $-3\text{dB}$ Bandwidth | $0.1\text{V}_{P-P}$ at $V_{OCM}$ , Measured Single-Ended at +OUT and -OUT  |     | 300  |     | MHz                          |
| $SR_{CM}$  | Common Mode Slew Rate                            | $1.3\text{V}$ to $3.4\text{V}$ Step at $V_{OCM}$   |     | 500  |     | $\text{V}/\mu\text{s}$       |
| <b>Noise/Harmonic Performance Input/output Characteristics</b> |  |  |     |      |     |                              |
| <b>1kHz Signal</b>   |  |  |     |      |     |                              |
|  | Second/Third Harmonic Distortion                 | $2\text{V}_{P-P}$ Differential (+OUTFILTERED, -OUTFILTERED)  |     | -100 |     | dBc                          |
|  |  | $2\text{V}_{P-P}$ Differential (+OUT, -OUT)  |     | -100 |     | dBc                          |
|  |  | $2\text{V}_{P-P}$ Differential (+OUT, -OUT), $R_L = 100\Omega$   |     | -100 |     | dBc                          |
|  |  | $3.2\text{V}_{P-P}$ Differential (+OUTFILTERED, -OUTFILTERED)  |     | -91  |     | dBc                          |
|  |  | $3.2\text{V}_{P-P}$ Differential (+OUT, -OUT)  |     | -91  |     | dBc                          |
|  |  | $3.2\text{V}_{P-P}$ Differential (+OUT, -OUT), $R_L = 100\Omega$   |     | -91  |     | dBc                          |
|  | Third-Order IMD                                  | $2\text{V}_{P-P}$ Differential Composite (+OUTFILTERED, -OUTFILTERED), $f_1 = 0.95\text{kHz}$ , $f_2 = 1.05\text{kHz}$     |     | -102 |     | dBc                          |
|  |  | $2\text{V}_{P-P}$ Differential Composite (+OUT, -OUT), $R_L = 100\Omega$ , $f_1 = 0.95\text{kHz}$ , $f_2 = 1.05\text{kHz}$ |     | -102 |     | dBc                          |
|  |  | $3.2\text{V}_{P-P}$ Differential Composite (+OUTFILTERED, -OUTFILTERED), $f_1 = 0.95\text{kHz}$ , $f_2 = 1.05\text{kHz}$   |     | -93  |     | dBc                          |
| $OIP3_{1k}$  | Output Third-Order Intercept                     | Differential (+OUTFILTERED, -OUTFILTERED), $f_1 = 0.95\text{kHz}$ , $f_2 = 1.05\text{kHz}$                                 |     | 54   |     | dBm                          |
| $e_{n1k}$  | Input Referred Noise Voltage Density             |  |     | 3.5  |     | $\text{nV}/\sqrt{\text{Hz}}$ |
|  | 1dB Compression Point                            | $R_L = 100\Omega$  |     | 22.7 |     | dBm                          |
| <b>10MHz Signal</b>  |  |  |     |      |     |                              |
|  | Second/Third Harmonic Distortion                 | $2\text{V}_{P-P}$ Differential (+OUTFILTERED, -OUTFILTERED)  |     | -94  |     | dBc                          |
|  |  | $2\text{V}_{P-P}$ Differential (+OUT, -OUT)  |     | -94  |     | dBc                          |
|  |  | $2\text{V}_{P-P}$ Differential (+OUT, -OUT), $R_L = 100\Omega$   |     | -86  |     | dBc                          |
|  |  | $3.2\text{V}_{P-P}$ Differential (+OUTFILTERED, -OUTFILTERED)  |     | -85  |     | dBc                          |
|  |  | $3.2\text{V}_{P-P}$ Differential (+OUT, -OUT)  |     | -85  |     | dBc                          |
|  |  | $3.2\text{V}_{P-P}$ Differential (+OUT, -OUT), $R_L = 100\Omega$   |     | -77  |     | dBc                          |
|  | Third-Order IMD                                  | $2\text{V}_{P-P}$ Differential Composite (+OUTFILTERED, -OUTFILTERED), $f_1 = 9.5\text{MHz}$ , $f_2 = 10.5\text{MHz}$      |     | -96  |     | dBc                          |
|  |  | $2\text{V}_{P-P}$ Differential Composite (+OUT, -OUT), $R_L = 100\Omega$ , $f_1 = 9.5\text{MHz}$ , $f_2 = 10.5\text{MHz}$  |     | -96  |     | dBc                          |
|  |  | $3.2\text{V}_{P-P}$ Differential Composite (+OUTFILTERED, -OUTFILTERED), $f_1 = 9.5\text{MHz}$ , $f_2 = 10.5\text{MHz}$    |     | -87  |     | dBc                          |
| $OIP3_{10M}$   | Output Third-Order Intercept                     | Differential (+OUTFILTERED, -OUTFILTERED), $f_1 = 9.5\text{MHz}$ , $f_2 = 10.5\text{MHz}$                                  |     | 51   |     | dBm                          |
| NF   | Noise Figure                                     | Measured Using DC800A Demo Board   |     | 11.3 |     | dB                           |
| $e_{n10M}$   | Input Referred Noise Voltage Density             |  |     | 3.5  |     | $\text{nV}/\sqrt{\text{Hz}}$ |
|  | 1dB Compression Point                            | $R_L = 100\Omega$  |     | 22.6 |     | dBm                          |

# AC ELECTRICAL CHARACTERISTICS

$T_A = 25^\circ\text{C}$ ,  $V_{CCA} = V_{CCB} = V_{CCC} = 5\text{V}$ ,  $V_{EEA} = V_{EEB} = V_{EEC} = 0\text{V}$ ,  $\text{ENABLE} = 0.8\text{V}$ , +INA shorted to +INB (+IN), -INA shorted to -INB (-IN),  $V_{OCM} = 2.2\text{V}$ , Input common mode voltage =  $2.2\text{V}$ , no  $R_{LOAD}$  unless otherwise noted.

| SYMBOL               | PARAMETER                            | CONDITIONS  | MIN | TYP  | MAX | UNITS                  |
|----------------------|--------------------------------------|---|-----|------|-----|------------------------|
| <b>50MHz Signal</b>  |                                      |   |     |      |     |                        |
|                      | Second/Third Harmonic Distortion     | 2V <sub>p-p</sub> Differential (+OUTFILTERED, -OUTFILTERED)   |     | -77  |     | dBc                    |
|                      |                                      | 2V <sub>p-p</sub> Differential (+OUT, -OUT)   |     | -77  |     | dBc                    |
|                      |                                      | 2V <sub>p-p</sub> Differential (+OUT, -OUT), $R_L = 100\Omega$  |     | -74  |     | dBc                    |
|                      |                                      | 3.2V <sub>p-p</sub> Differential (+OUTFILTERED, -OUTFILTERED)   |     | -68  |     | dBc                    |
|                      |                                      | 3.2V <sub>p-p</sub> Differential (+OUT, -OUT)   |     | -65  |     | dBc                    |
|                      |                                      | 3.2V <sub>p-p</sub> Differential (+OUT, -OUT), $R_L = 100\Omega$  |     | -65  |     | dBc                    |
|                      | Third-Order IMD                      | 2V <sub>p-p</sub> Differential Composite (+OUTFILTERED, -OUTFILTERED), $f_1 = 49.5\text{MHz}$ , $f_2 = 50.5\text{MHz}$      |     | -84  |     | dBc                    |
|                      |                                      | 2V <sub>p-p</sub> Differential Composite (+OUT, -OUT), $R_L = 100\Omega$ , $f_1 = 49.5\text{MHz}$ , $f_2 = 50.5\text{MHz}$  |     | -88  |     | dBc                    |
|                      |                                      | 3.2V <sub>p-p</sub> Differential Composite (+OUTFILTERED, -OUTFILTERED), $f_1 = 49.5\text{MHz}$ , $f_2 = 50.5\text{MHz}$    |     | -75  |     | dBc                    |
| OIP <sub>30M</sub>   | Output Third-Order Intercept         | Differential (+OUTFILTERED, -OUTFILTERED), $f_1 = 49.5\text{MHz}$ , $f_2 = 50.5\text{MHz}$                                  |     | 45   |     | dBm                    |
| NF                   | Noise Figure                         | Measured Using DC800A Demo Board  |     | 11.8 |     | dB                     |
| e <sub>n50M</sub>    | Input Referred Noise Voltage Density |   |     | 3.65 |     | nV/ $\sqrt{\text{Hz}}$ |
|                      | 1dB Compression Point                | $R_L = 100\Omega$   |     | 19.7 |     | dBm                    |
| <b>70MHz Signal</b>  |                                      |   |     |      |     |                        |
|                      | Second/Third Harmonic Distortion     | 2V <sub>p-p</sub> Differential (+OUTFILTERED, -OUTFILTERED)   |     | -70  |     | dBc                    |
|                      |                                      | 2V <sub>p-p</sub> Differential (+OUT, -OUT)   |     | -61  |     | dBc                    |
|                      |                                      | 2V <sub>p-p</sub> Differential (+OUT, -OUT), $R_L = 100\Omega$  |     | -61  |     | dBc                    |
|                      | Third-Order IMD                      | 2V <sub>p-p</sub> Differential Composite (+OUTFILTERED, -OUTFILTERED), $f_1 = 69.5\text{MHz}$ , $f_2 = 70.5\text{MHz}$      |     | -70  |     | dBc                    |
|                      |                                      | 2V <sub>p-p</sub> Differential Composite (+OUT, -OUT), $R_L = 100\Omega$ , $f_1 = 69.5\text{MHz}$ , $f_2 = 70.5\text{MHz}$  |     | -72  |     | dBc                    |
| OIP <sub>370M</sub>  | Output Third-Order Intercept         | Differential (+OUTFILTERED, -OUTFILTERED), $f_1 = 69.5\text{MHz}$ , $f_2 = 70.5\text{MHz}$                                  |     | 38   |     | dBm                    |
| NF                   | Noise Figure                         | Measured Using DC800A Demo Board  |     | 12.3 |     | dB                     |
| e <sub>n70M</sub>    | Input Referred Noise Voltage Density |   |     | 3.8  |     | nV/ $\sqrt{\text{Hz}}$ |
|                      | 1dB Compression Point                | $R_L = 100\Omega$   |     | 18.5 |     | dBm                    |
| <b>100MHz Signal</b> |                                      |   |     |      |     |                        |
|                      | Second/Third Harmonic Distortion     | 2V <sub>p-p</sub> Differential (+OUTFILTERED, -OUTFILTERED)   |     | -56  |     | dBc                    |
|                      |                                      | 2V <sub>p-p</sub> Differential (+OUT, -OUT)   |     | -54  |     | dBc                    |
|                      |                                      | 2V <sub>p-p</sub> Differential (+OUT, -OUT), $R_L = 100\Omega$  |     | -51  |     | dBc                    |
|                      | Third-Order IMD                      | 2V <sub>p-p</sub> Differential Composite (+OUTFILTERED, -OUTFILTERED), $f_1 = 99.5\text{MHz}$ , $f_2 = 100.5\text{MHz}$     |     | -58  |     | dBc                    |
|                      |                                      | 2V <sub>p-p</sub> Differential Composite (+OUT, -OUT), $R_L = 100\Omega$ , $f_1 = 99.5\text{MHz}$ , $f_2 = 100.5\text{MHz}$ |     | -59  |     | dBc                    |
| OIP <sub>3100M</sub> | Output Third-Order Intercept         | Differential (+OUTFILTERED, -OUTFILTERED), $f_1 = 99.5\text{MHz}$ , $f_2 = 100.5\text{MHz}$                                 |     | 32   |     | dBm                    |
| NF                   | Noise Figure                         | Measured Using DC800A Demo Board  |     | 12.8 |     | dB                     |

AC ELECTRICAL CHARACTERISTICS  $T_A = 25^{\circ}\text{C}$ ,  $V_{CCA} = V_{CCB} = V_{CCC} = 5\text{V}$ ,  $V_{EEA} = V_{EEB} = V_{EEC} = 0\text{V}$ ,  $\text{ENABLE} = 0.8\text{V}$ , +INA shorted to +INB (+IN), -INA shorted to -INB (-IN),  $V_{OCM} = 2.2\text{V}$ , Input common mode voltage =  $2.2\text{V}$ , no  $R_{LOAD}$  unless otherwise noted.

| SYMBOL      | PARAMETER                            | CONDITIONS        | MIN | TYP  | MAX | UNITS                        |
|-------------|--------------------------------------|-------------------|-----|------|-----|------------------------------|
| $e_{n100M}$ | Input Referred Noise Voltage Density |                   |     | 4.1  |     | $\text{nV}/\sqrt{\text{Hz}}$ |
|             | 1dB Compression Point                | $R_L = 100\Omega$ |     | 17.8 |     | $\text{dBm}$                 |

- Note 1:** Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

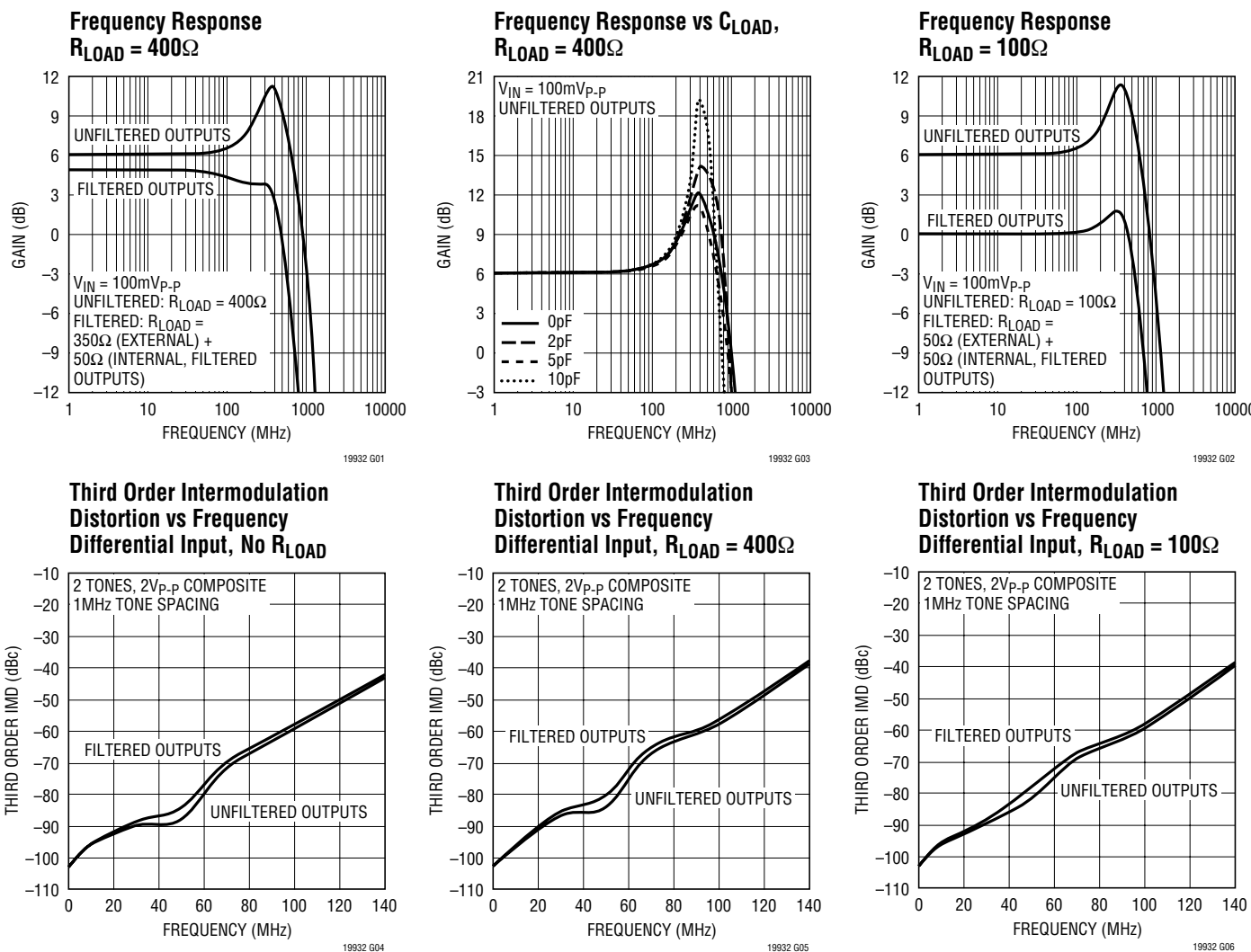
**Note 2:** As long as output current and junction temperature are kept below the Absolute Maximum Ratings, no damage to the part will occur.

**Note 3:** The LT1993C-2 is guaranteed functional over the operating temperature range of  $-40^{\circ}\text{C}$  to  $85^{\circ}\text{C}$ .
- Note 4:** The LT1993C-2 is guaranteed to meet specified performance from  $0^{\circ}\text{C}$  to  $70^{\circ}\text{C}$ . It is designed, characterized and expected to meet specified performance from  $-40^{\circ}\text{C}$  and  $85^{\circ}\text{C}$  but is not tested or QA sampled at these temperatures. The LT1993I-2 is guaranteed to meet specified performance from  $-40^{\circ}\text{C}$  to  $85^{\circ}\text{C}$ .

**Note 5:** This parameter is pulse tested.

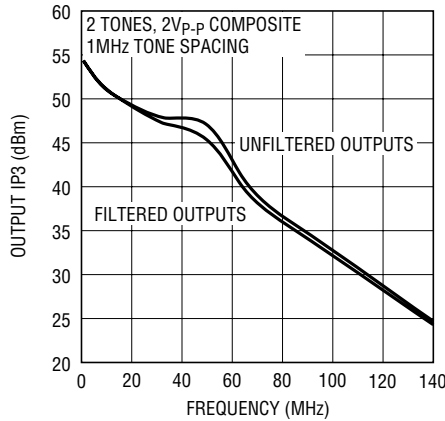
**Note 6:** This parameter is guaranteed to meet specified performance through design and characterization. It has not been tested.

TYPICAL PERFORMANCE CHARACTERISTICS

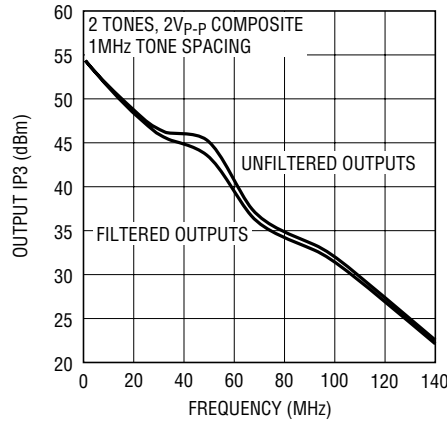


# TYPICAL PERFORMANCE CHARACTERISTICS

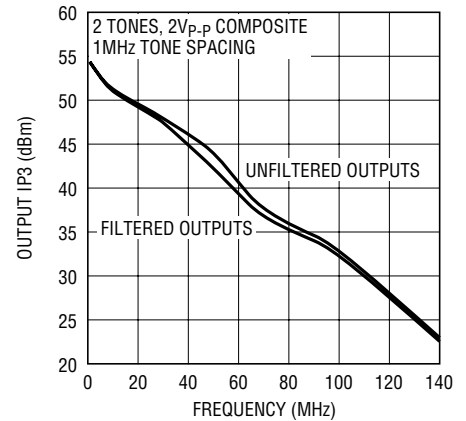
**Output Third Order Intercept vs Frequency, Differential Input, No  $R_{LOAD}$**



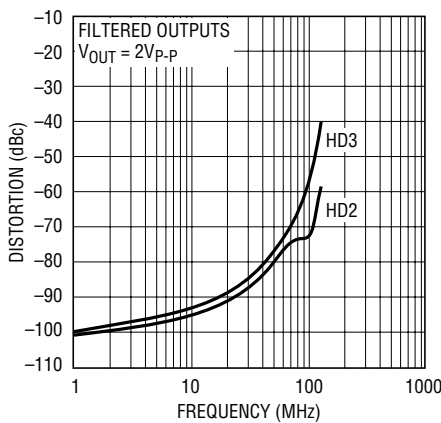
**Output Third Order Intercept vs Frequency, Differential Input,  $R_{LOAD} = 400\Omega$**



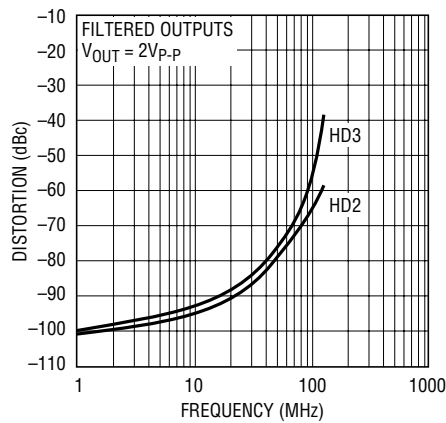
**Output Third Order Intercept vs Frequency, Differential Input,  $R_{LOAD} = 100\Omega$**



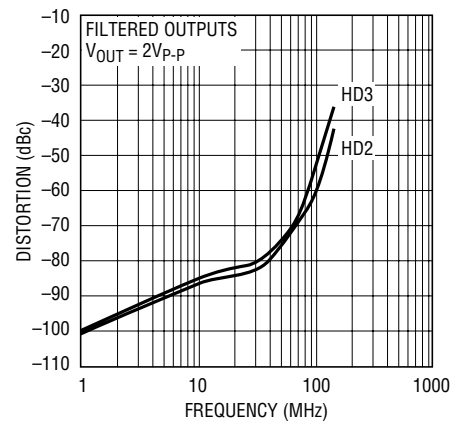
**Distortion (Filtered) vs Frequency Differential Input, No  $R_{LOAD}$**



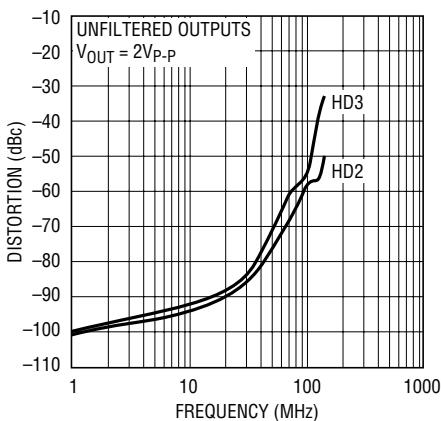
**Distortion (Filtered) vs Frequency Differential Input,  $R_{LOAD} = 400\Omega$**



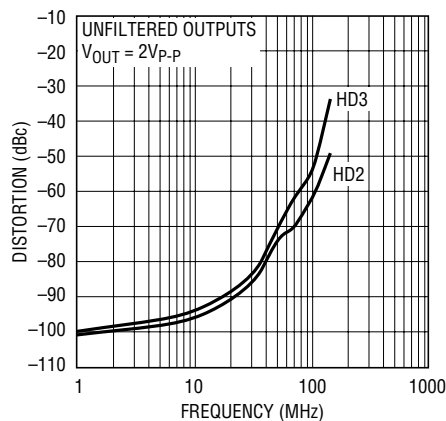
**Distortion (Filtered) vs Frequency Differential Input,  $R_{LOAD} = 100\Omega$**



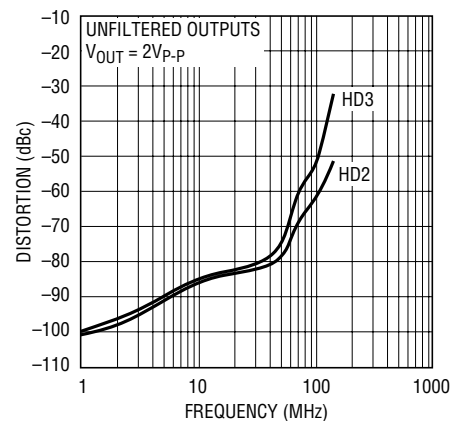
**Distortion (Unfiltered) vs Frequency, Differential Input, No  $R_{LOAD}$**



**Distortion (Unfiltered) vs Frequency, Differential Input,  $R_{LOAD} = 400\Omega$**

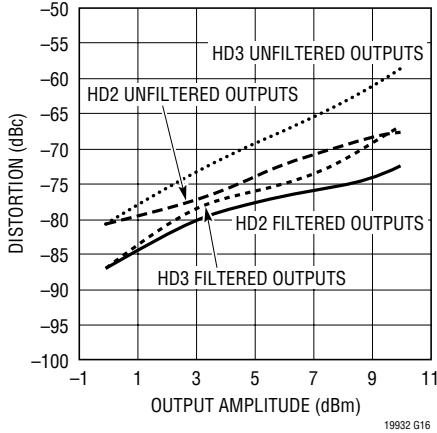


**Distortion (Unfiltered) vs Frequency, Differential Input,  $R_{LOAD} = 100\Omega$**

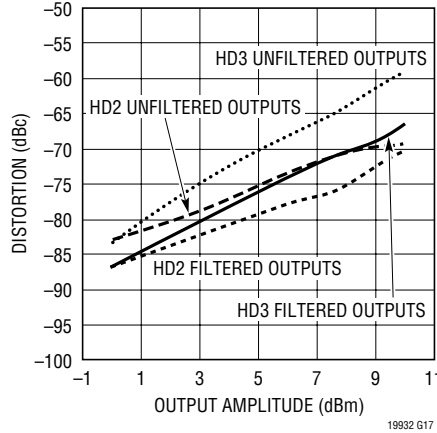


# TYPICAL PERFORMANCE CHARACTERISTICS

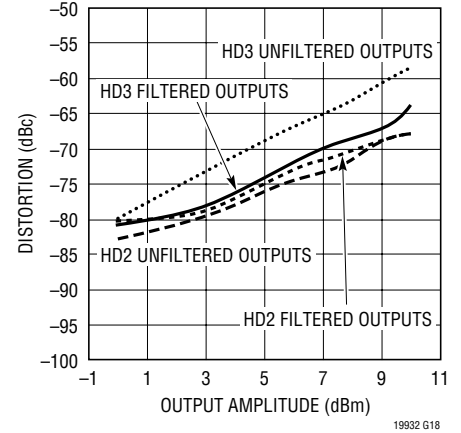
**Distortion vs Output Amplitude**  
70MHz Differential Input,  
No  $R_{LOAD}$



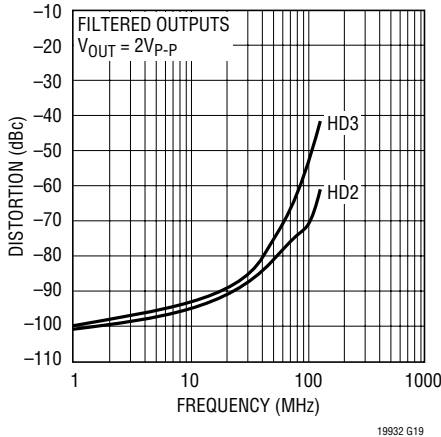
**Distortion vs Output Amplitude**  
70MHz Differential Input,  
 $R_{LOAD} = 400\Omega$



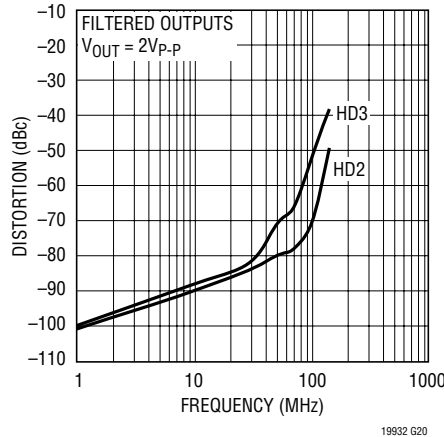
**Distortion vs Output Amplitude**  
70MHz Differential Input,  
 $R_{LOAD} = 100\Omega$



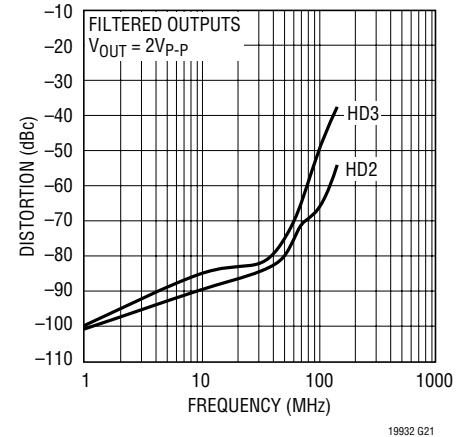
**Distortion (Filtered) vs Frequency**  
Single-Ended Input, No  $R_{LOAD}$



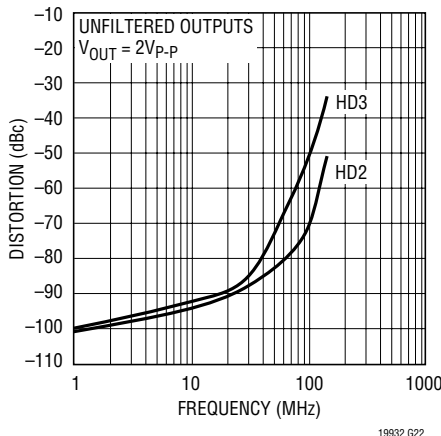
**Distortion (Filtered) vs Frequency**  
Single-Ended Input,  $R_{LOAD} = 400\Omega$



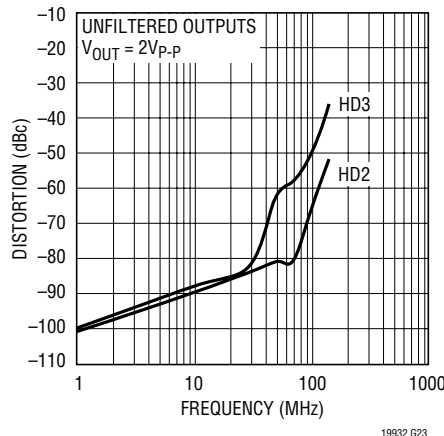
**Distortion (Filtered) vs Frequency**  
Single-Ended Input,  $R_{LOAD} = 100\Omega$



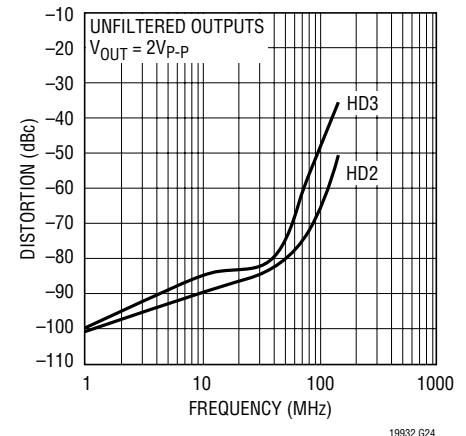
**Distortion (Unfiltered) vs Frequency, Single-Ended Input, No  $R_{LOAD}$**



**Distortion (Unfiltered) vs Frequency, Single-Ended Input,  $R_{LOAD} = 400\Omega$**



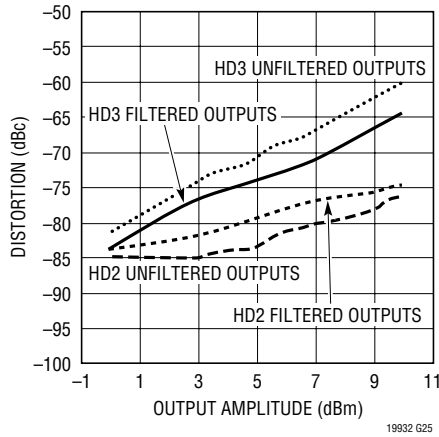
**Distortion (Unfiltered) vs Frequency, Single-Ended Input,  $R_{LOAD} = 100\Omega$**



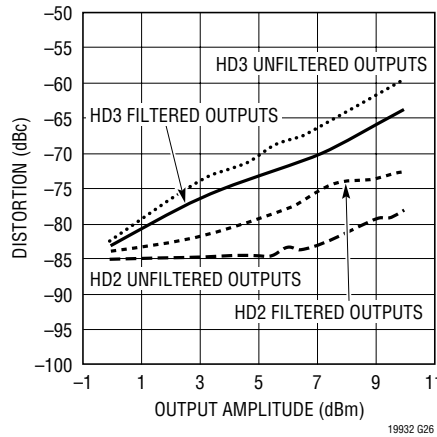


# TYPICAL PERFORMANCE CHARACTERISTICS

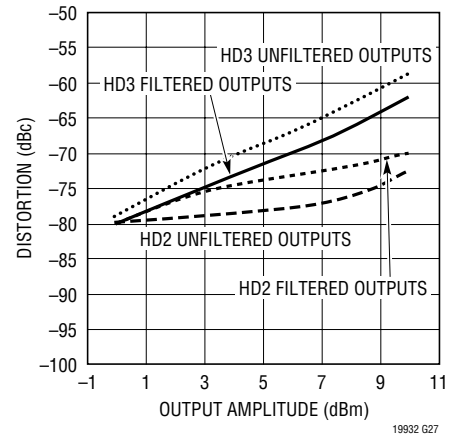
**Distortion vs Output Amplitude**  
70MHz Single-Ended Input,  
No  $R_{LOAD}$



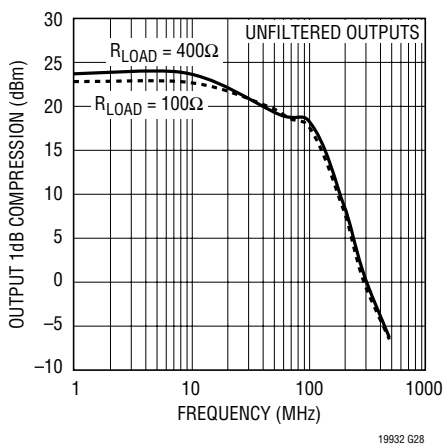
**Distortion vs Output Amplitude**  
70MHz Single-Ended Input,  
 $R_{LOAD} = 400\Omega$



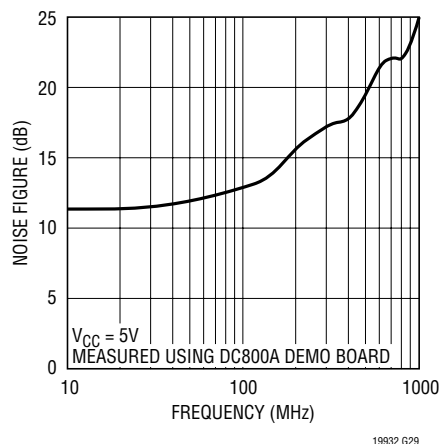
**Distortion vs Output Amplitude**  
70MHz Single-Ended Input,  
 $R_{LOAD} = 100\Omega$



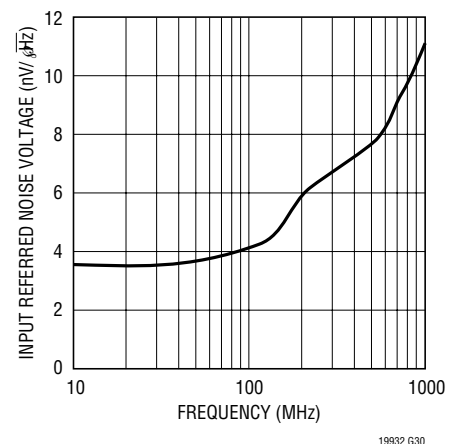
**Output 1dB Compression**  
**vs Frequency**



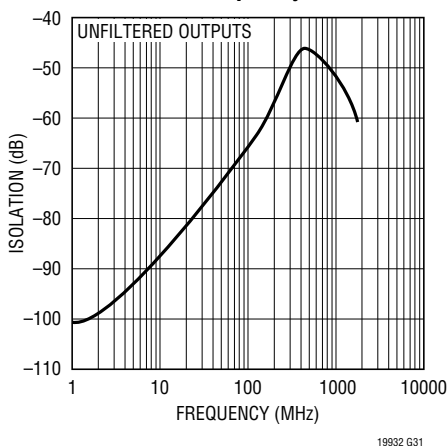
**Noise Figure vs Frequency**



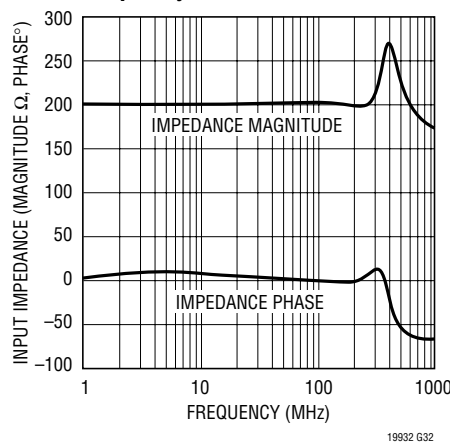
**Input Referred Noise Voltage vs**  
**Frequency**



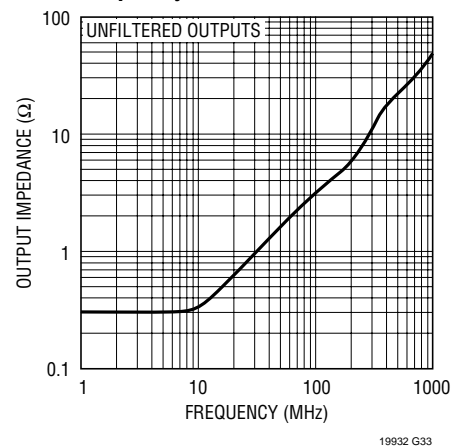
**Isolation vs Frequency**



**Differential Input Impedance vs**  
**Frequency**

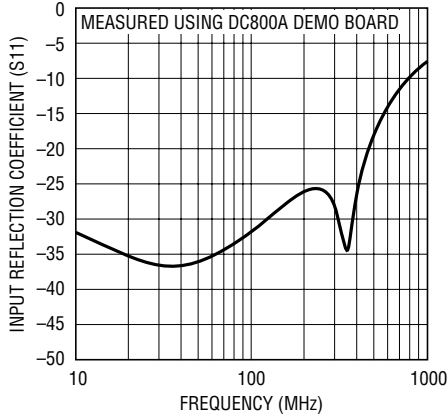


**Differential Output Impedance vs**  
**Frequency**



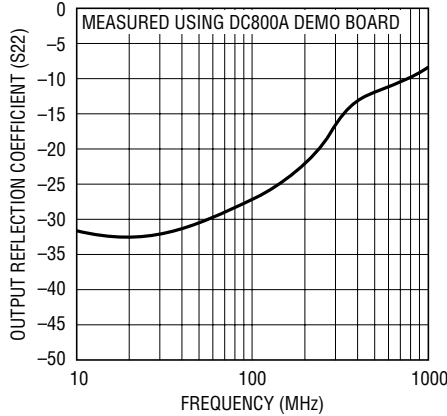
# TYPICAL PERFORMANCE CHARACTERISTICS

**Input Reflection Coefficient vs Frequency**



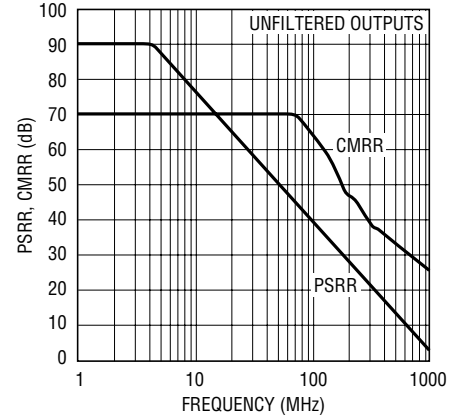
19932 G34

**Output Reflection Coefficient vs Frequency**



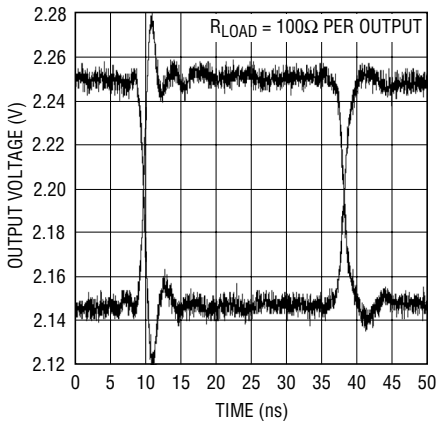
19932 G35

**PSRR, CMRR vs Frequency**



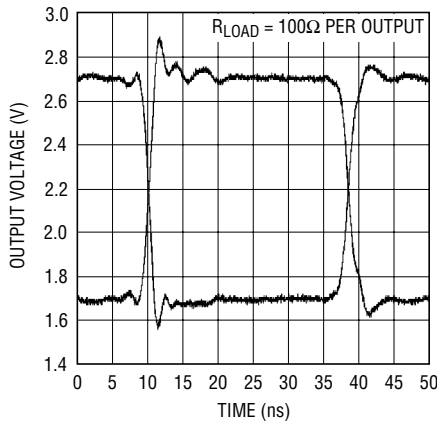
19932 G36

**Small-Signal Transient Response**



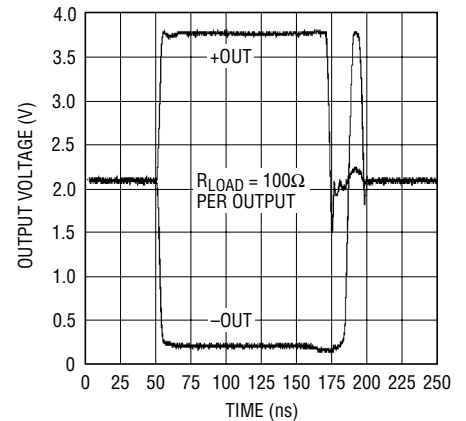
19932 G37

**Large-Signal Transient Response**



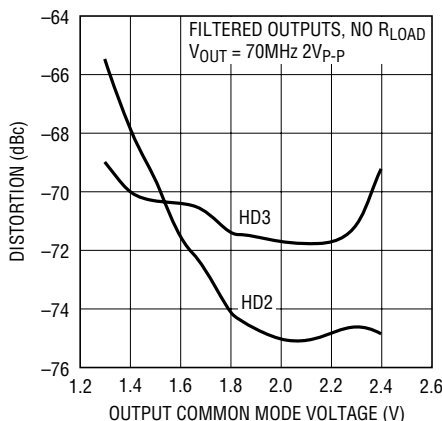
19932 G38

**Overdrive Recovery Time**



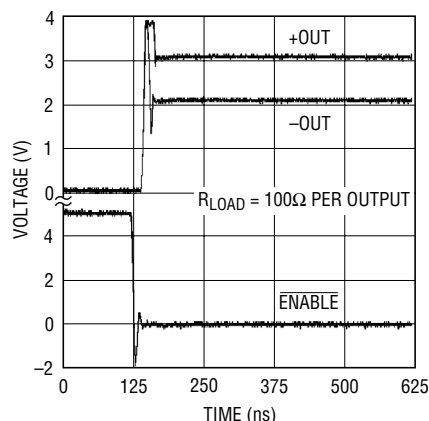
19932 G39

**Distortion vs Output Common Mode Voltage LT1993-2 Driving LTC2249 14-Bit ADC**



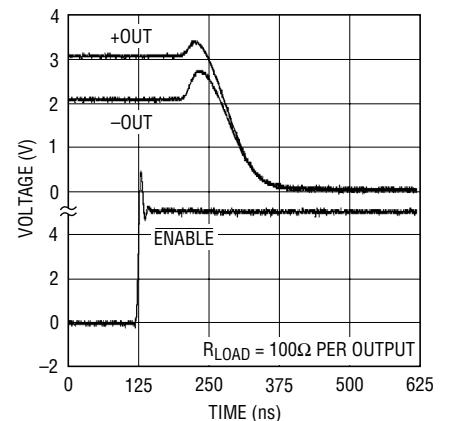
19932 G40

**Turn-On Time**



19932 G41

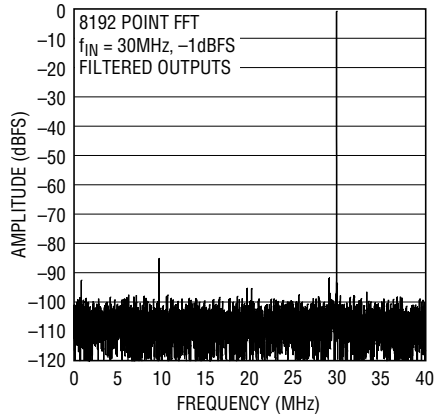
**Turn-Off Time**



19932 G42

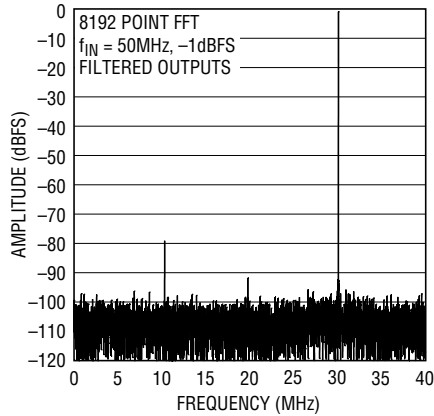
# TYPICAL PERFORMANCE CHARACTERISTICS

**30MHz 8192 Point FFT, LT1993-2  
Driving LTC2249 14-Bit ADC**



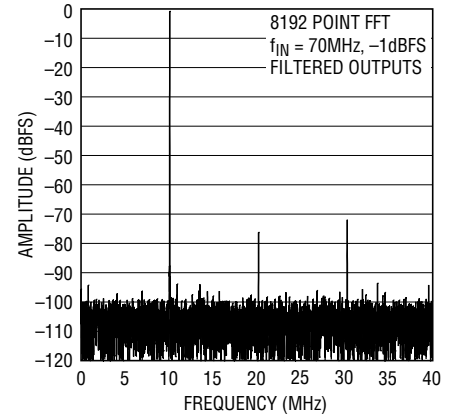
19932 G46

**50MHz 8192 Point FFT, LT1993-2  
Driving LTC2249 14-Bit ADC**



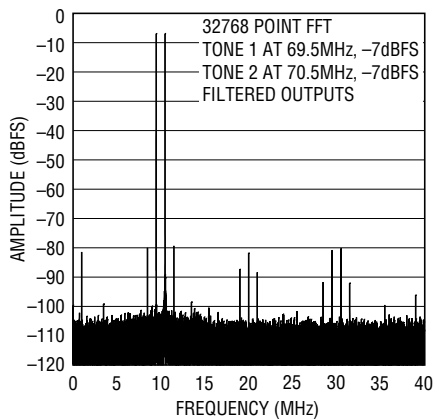
19932 G47

**70MHz 8192 Point FFT, LT1993-2  
Driving LTC2249 14-Bit ADC**



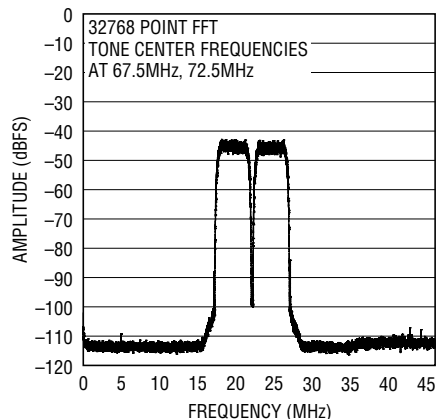
19932 G48

**70MHz 2-Tone 32768 Point FFT,  
LT1993-2 Driving LTC2249  
14-Bit ADC**



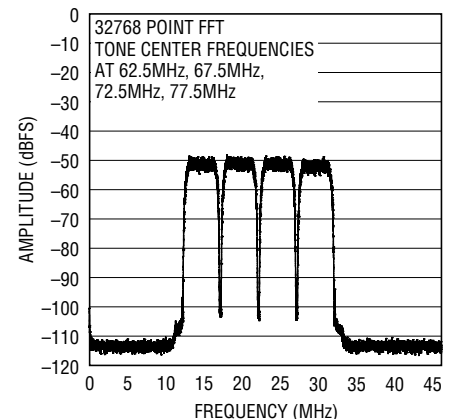
19932 G49

**2-Tone WCDMA Waveform,  
LT1993-2 Driving LTC2255 14-Bit  
ADC at 92.16Msps**



19932 G50

**4-Tone WCDMA Waveform,  
LT1993-2 Driving LTC2255 14-Bit  
ADC at 92.16Msps**



19932 G51

## PIN FUNCTIONS

**V<sub>OCM</sub> (Pin 2):** This pin sets the output common mode voltage. Without additional biasing, both inputs bias to this voltage as well. This input is high impedance.

**V<sub>CCA</sub>, V<sub>CCB</sub>, V<sub>CCC</sub> (Pins 3, 10, 1):** Positive Power Supply (Normally Tied to 5V). All three pins must be tied to the same voltage. Bypass each pin with 1000pF and 0.1μF capacitors as close to the package as possible. Split supplies are possible as long as the voltage between V<sub>CC</sub> and V<sub>EE</sub> is 5V.

**V<sub>EEA</sub>, V<sub>EEB</sub>, V<sub>EEC</sub> (Pins 4, 9, 12):** Negative Power Supply (Normally Tied to Ground). All three pins must be tied to the same voltage. Split supplies are possible as long as the voltage between V<sub>CC</sub> and V<sub>EE</sub> is 5V. If these pins are not tied to ground, bypass each pin with 1000pF and 0.1μF capacitors as close to the package as possible.

**+OUT, -OUT (Pins 5, 8):** Outputs (Unfiltered). These pins are high bandwidth, low-impedance outputs. The DC output voltage at these pins is set to the voltage applied at V<sub>OCM</sub>.

**+OUTFILTERED, -OUTFILTERED (Pins 6, 7):** Filtered Outputs. These pins add a series 25Ω resistor from the unfiltered outputs and three 12pF capacitors. Each output has 12pF to V<sub>EE</sub>, plus an additional 12pF between each pin (See the Block Diagram). This filter has a -3dB bandwidth of 175MHz.

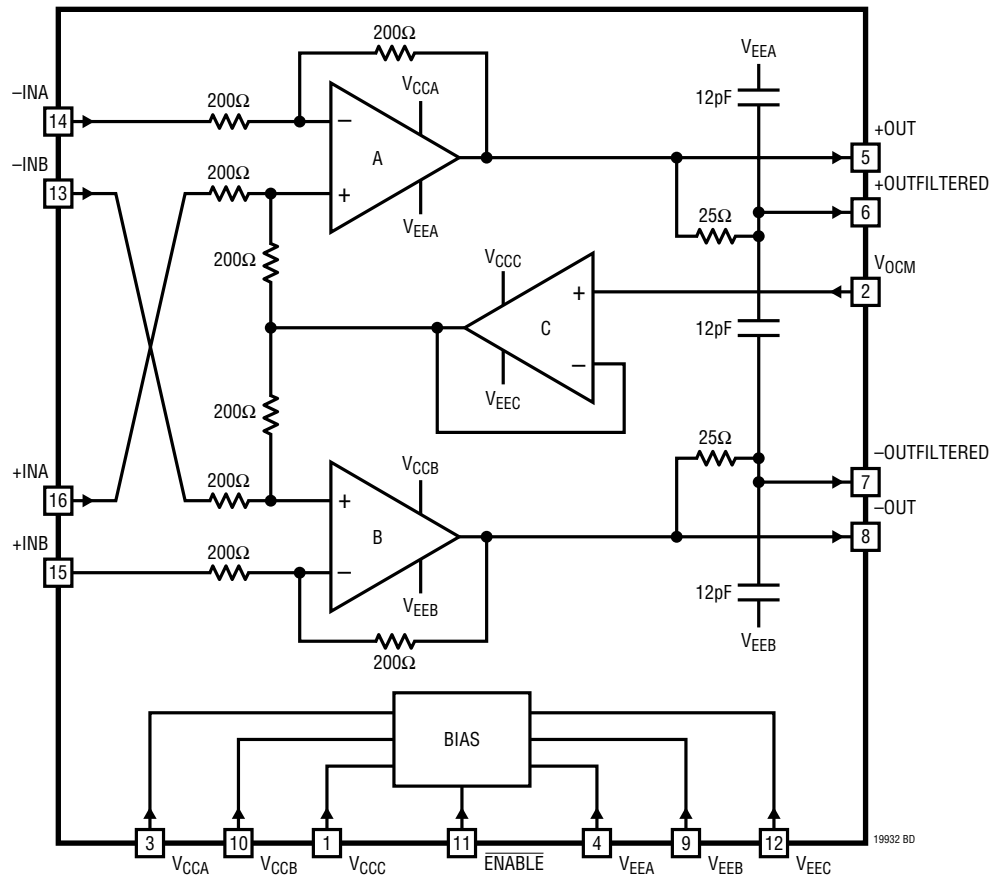
**ENABLE (Pin 11):** This pin is a TTL logic input referenced to the V<sub>EEC</sub> pin. If low, the LT1993-2 is enabled and draws typically 100mA of supply current. If high, the LT1993-2 is disabled and draws typically 250μA.

**+INA, +INB (Pins 15, 16):** Positive Inputs. These pins are normally tied together. These inputs may be DC- or AC-coupled. If the inputs are AC-coupled, they will self-bias to the voltage applied to the V<sub>OCM</sub> pin.

**-INA, -INB (Pins 14, 13):** Negative Inputs. These pins are normally tied together. These inputs may be DC- or AC-coupled. If the inputs are AC-coupled, they will self-bias to the voltage applied to the V<sub>OCM</sub> pin.

**Exposed Pad (Pin 17):** Tie the pad to V<sub>EEC</sub> (Pin 12). If split supplies are used, DO NOT tie the pad to ground.

# BLOCK DIAGRAM



## APPLICATIONS INFORMATION

### Circuit Description

The LT1993-2 is a low-noise, low-distortion differential amplifier/ADC driver with:

- DC to 800MHz –3dB bandwidth
- Fixed gain of 2V/V (6dB) independent of  $R_{LOAD}$
- 200 $\Omega$  differential input impedance
- Low output impedance
- Built-in, user adjustable output filtering
- Requires minimal support circuitry

Referring to the block diagram, the LT1993-2 uses a closed-loop topology which incorporates 3 internal amplifiers. Two of the amplifiers (A and B) are identical and drive the differential outputs. The third amplifier (C) is used to set the output common mode voltage. Gain and input impedance are set by the 200 $\Omega$  resistors in the internal feedback network. Output impedance is low, determined by the inherent output impedance of amplifiers A and B, and further reduced by internal feedback.

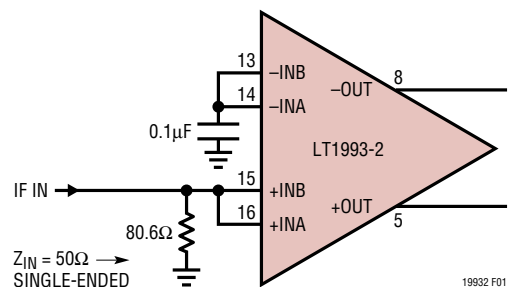
The LT1993-2 also includes built-in single-pole output filtering. The user has the choice of using the unfiltered outputs, the filtered outputs (175MHz –3dB lowpass), or modifying the filtered outputs to alter frequency response by adding additional components. Many lowpass and bandpass filters are easily implemented with just one or two additional components.

The LT1993-2 has been designed to minimize the need for external support components such as transformers or AC-coupling capacitors. As an ADC driver, the LT1993-2 requires no external components except for power-supply bypass capacitors. This allows DC-coupled operation for applications that have frequency ranges including DC. At the outputs, the common mode voltage is set via the  $V_{OCM}$  pin, allowing the LT1993-2 to drive ADCs directly. No output AC-coupling capacitors or transformers are needed. At the inputs, signals can be differential or single-ended with virtually no difference in performance. Furthermore, DC levels at the inputs can be set independently of the output common mode voltage. These input characteristics often eliminate the need for an input transformer and/or AC-coupling capacitors.

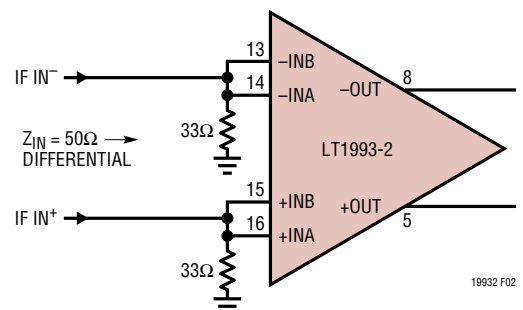
### Input Impedance and Matching Networks

Because of the internal feedback network, calculation of the LT1993-2's input impedance is not straightforward from examination of the block diagram. Furthermore, the input impedance when driven differentially is different than when driven single-ended. When driven differentially, the LT1993-2's input impedance is 200 $\Omega$  (differential); when driven single-ended, the input impedance is 133 $\Omega$ .

For single-ended 50 $\Omega$  applications, an 80.6 $\Omega$  shunt matching resistor to ground will result in the proper input termination (Figure 1). For differential inputs there are several termination options. If the input source is 50 $\Omega$  differential, then input matching can be accomplished by either a 67 $\Omega$  shunt resistor across the inputs (Figure 3), or a 33 $\Omega$  shunt resistor on each of the inputs to ground (Figure 2). If additional AC gain is desired, a 1:4 impedance ratio transformer (like the Mini-Circuits TCM4-19) can also be used to better match impedances and to provide an additional 6dB of gain (Figure 4). With a 1:4 impedance ratio transformer, ideal matching impedance at the transformer output is 200 $\Omega$ , so no termination resistors are required to match the LT1993-2's 200 $\Omega$  input impedance.



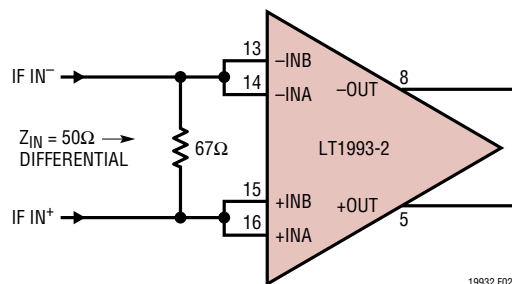
**Figure 1. Input Termination for Single-Ended 50 $\Omega$  Input Impedance**



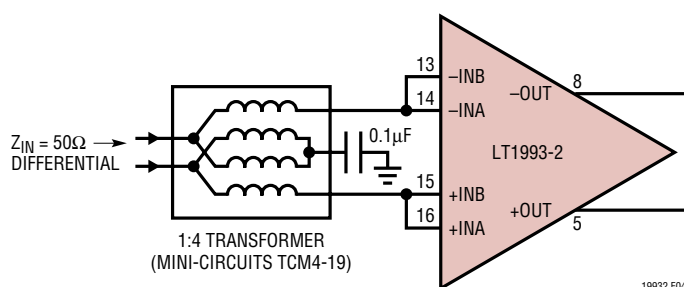
**Figure 2. Input Termination for Differential 50 $\Omega$  Input Impedance**

Rev B

# APPLICATIONS INFORMATION



**Figure 3. Alternate Input Termination for Differential 50Ω Input Impedance**



**Figure 4. Input Termination for Differential 50Ω Input Impedance with 6dB Additional Gain**

## Single-Ended to Differential Operation

The LT1993-2's performance with single-ended inputs is comparable to its performance with differential inputs. This excellent single-ended performance is largely due to the internal topology of the LT1993-2. Referring to the block diagram, if the +INA and +INB pins are driven with a single-ended signal (while -INA and -INB are tied to AC ground), then the +OUT and -OUT pins are driven differentially without any voltage swing needed from amplifier C. Single-ended to differential conversion using more conventional topologies suffers from performance limitations due to the common mode amplifier.

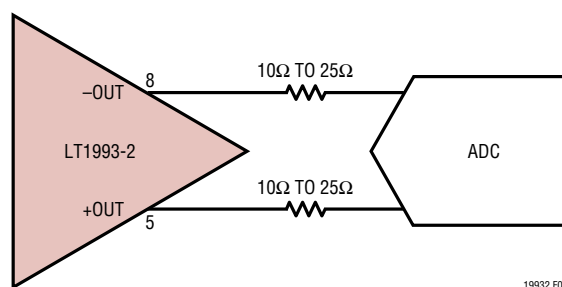
## Driving ADCs

The LT1993-2 has been specifically designed to interface directly with high speed Analog to Digital Converters (ADCs). In general, these ADCs have differential inputs, with an input impedance of 1k or higher. In addition, there is generally some form of lowpass or bandpass filtering just prior to the ADC to limit input noise at the ADC, thereby improving system signal to noise ratio. Both the unfiltered and filtered outputs of the LT1993-2 can

easily drive the high impedance inputs of these differential ADCs. If the filtered outputs are used, then cutoff frequency and the type of filter can be tailored for the specific application if needed.

## Wideband Applications (Using the +OUT and -OUT Pins)

In applications where the full bandwidth of the LT1993-2 is desired, the unfiltered output pins (+OUT and -OUT) should be used. They have a low output impedance; therefore, gain is unaffected by output load. Capacitance in excess of 5pF placed directly on the unfiltered outputs results in additional peaking and reduced performance. When driving an ADC directly, a small series resistance is recommended between the LT1993-2's outputs and the ADC inputs (Figure 5). This resistance helps eliminate any resonances associated with bond wire inductances of either the ADC inputs or the LT1993-2's outputs. A value between 10Ω and 25Ω gives excellent results.



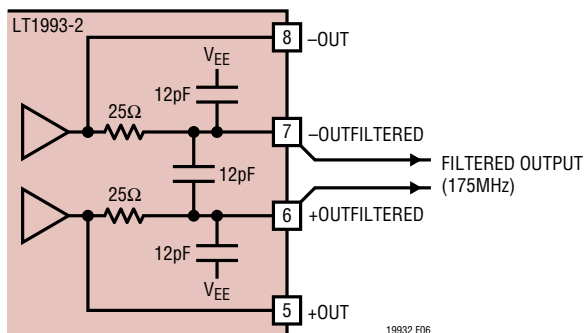
**Figure 5. Adding Small Series R at LT1993-2 Output**

## Filtered Applications (Using the +OUTFILTERED and -OUTFILTERED Pins)

Filtering at the output of the LT1993-2 is often desired to provide either anti-aliasing or improved signal to noise ratio. To simplify this filtering, the LT1993-2 includes an additional pair of differential outputs (+OUTFILTERED and -OUTFILTERED) which incorporate an internal low-pass filter network with a -3dB bandwidth of 175MHz (Figure 6). These pins each have an output impedance of 25Ω. Internal capacitances are 12pF to V<sub>EE</sub> on each filtered output, plus an additional 12pF capacitor connected differentially between the two filtered outputs. This resistor/capacitor combination creates filtered outputs

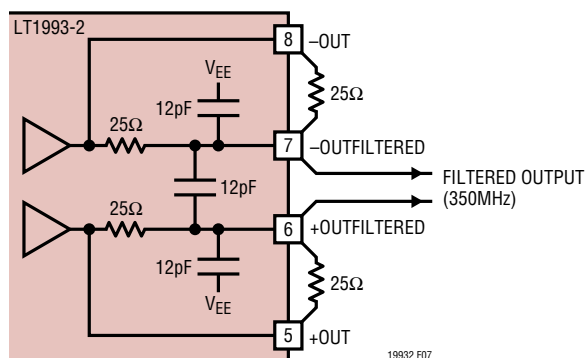
# APPLICATIONS INFORMATION

that look like a series  $25\Omega$  resistor with a  $36\text{pF}$  capacitor shunting each filtered output to AC ground, giving a  $-3\text{dB}$  bandwidth of  $175\text{MHz}$ .



**Figure 6. LT1993-2 Internal Filter Topology  $-3\text{dB BW} \approx 175\text{MHz}$**

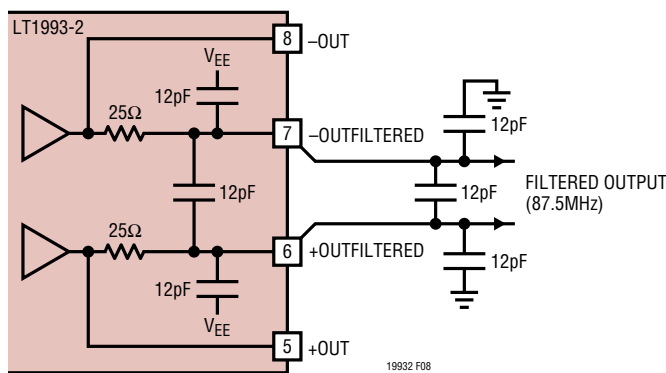
The filter cutoff frequency is easily modified with just a few external components. To increase the cutoff frequency, simply add 2 equal value resistors, one between +OUT and +OUTFILTERED and the other between -OUT and -OUTFILTERED (Figure 7). These resistors are in parallel with the internal  $25\Omega$  resistor, lowering the overall resistance and increasing filter bandwidth. To double the filter bandwidth, for example, add two external  $25\Omega$  resistors to lower the series resistance to  $12.5\Omega$ . The  $36\text{pF}$  of capacitance remains unchanged, so filter bandwidth doubles.



**Figure 7. LT1993-2 Internal Filter Topology Modified for 2x Filter Bandwidth (2 External Resistors)**

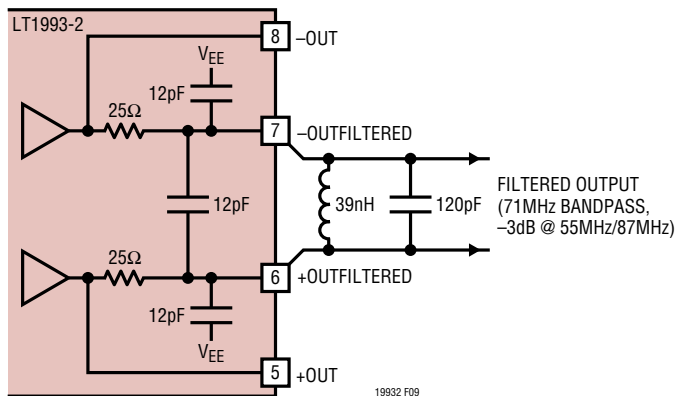
To decrease filter bandwidth, add two external capacitors, one from +OUTFILTERED to ground, and the other from -OUTFILTERED to ground. A single differential capacitor connected between +OUTFILTERED and -OUTFILTERED can also be used, but since it is being driven differentially

it will appear at each filtered output as a single-ended capacitance of twice the value. To halve the filter bandwidth, for example, two  $36\text{pF}$  capacitors could be added (one from each filtered output to ground). Alternatively one  $18\text{pF}$  capacitor could be added between the filtered outputs, again halving the filter bandwidth. Combinations of capacitors could be used as well; a three capacitor solution of  $12\text{pF}$  from each filtered output to ground plus a  $12\text{pF}$  capacitor between the filtered outputs would also halve the filter bandwidth (Figure 8).



**Figure 8. LT1993-2 Internal Filter Topology Modified for 1/2x Filter Bandwidth (3 External Capacitors)**

Bandpass filtering is also easily implemented with just a few external components. An additional  $120\text{pF}$  and  $39\text{nH}$ , each added differentially between +OUTFILTERED and -OUTFILTERED creates a bandpass filter with a  $71\text{MHz}$  center frequency,  $-3\text{dB}$  points of  $55\text{MHz}$  and  $87\text{MHz}$ , and  $1.6\text{dB}$  of insertion loss (Figure 9).



**Figure 9. LT1993-2 Output Filter Topology Modified for Bandpass Filtering (1 External Inductor, 1 External Capacitor)**

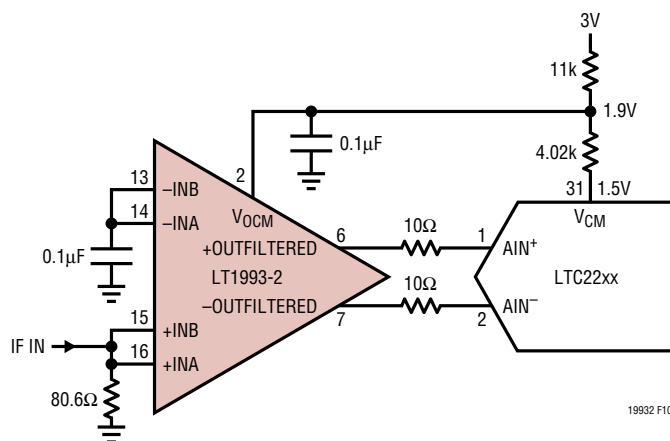


## APPLICATIONS INFORMATION

### Output Common Mode Adjustment

The LT1993-2's output common mode voltage is set by the  $V_{OCM}$  pin. It is a high-impedance input, capable of setting the output common mode voltage anywhere in a range from 1.1V to 3.6V. Bandwidth of the  $V_{OCM}$  pin is typically 300MHz, so for applications where the  $V_{OCM}$  pin is tied to a DC bias voltage, a 0.1 $\mu$ F capacitor at this pin is recommended. For best distortion performance, the voltage at the  $V_{OCM}$  pin should be between 1.8V and 2.6V.

When interfacing with most ADCs, there is generally a  $V_{OCM}$  output pin that is at about half of the supply voltage of the ADC. For 5V ADCs such as the LTC17XX family, this  $V_{OCM}$  output pin should be connected directly (with the addition of a 0.1 $\mu$ F capacitor) to the input  $V_{OCM}$  pin of the LT1993-2. For 3V ADCs such as the LTC22XX families, the LT1993-2 will function properly using the 1.65V from the ADC's  $V_{CM}$  reference pin, but improved Spurious Free Dynamic Range (SFDR) and distortion performance can be achieved by level-shifting the LTC22XX's  $V_{CM}$  reference voltage up to at least 1.8V. This can be accomplished as shown in Figure 10 by using a resistor divider between the LTC22XX's  $V_{CM}$  output pin and  $V_{CC}$  and then bypassing the LT1993-2's  $V_{OCM}$  pin with a 0.1 $\mu$ F capacitor. For a common mode voltage above 1.9V, AC coupling capacitors are recommended between the LT1993-2 and LTC22XX ADCs because of the input voltage range constraints of the ADC.



**Figure 10. Level Shifting 3V ADC  $V_{CM}$  Voltage for Improved SFDR**

### Large Output Voltage Swings

The LT1993-2 has been designed to provide the 3.2V<sub>P-P</sub> output swing needed by the LTC1748 family of 14-bit low-noise ADCs. This additional output swing improves system SNR by up to 4dB. Typical performance curves and AC specifications have been included for these applications.

### Input Bias Voltage and Bias Current

The input pins of the LT1993-2 are internally biased to the voltage applied to the  $V_{OCM}$  pin. No external biasing resistors are needed, even for AC-coupled operation. The input bias current is determined by the voltage difference between the input common mode voltage and the  $V_{OCM}$  pin (which sets the output common mode voltage). At both the positive and negative inputs, any voltage difference is imposed across 200 $\Omega$ , generating an input bias current. For example, if the inputs are tied to 2.5V with the  $V_{OCM}$  pin at 2.2V, then a total input bias current of 1.5mA will flow into the LT1993-2's +INA and +INB pins. Furthermore, an additional input bias current totaling 1.5mA will flow into the -INA and -INB inputs.

### $V_{OCM}$ and Output Voltages for Proper Operation

The electrical tables suggest 1.3V  $V_{OCM}$  minimum to ensure proper operation over temperature. The electrical tables also guarantee  $V_{SWINGMIN}$  to be 0.5V over temperature. It would appear that operation is okay so long as the low output voltage on either pin is 0.5V or higher, and  $V_{OCM}$  is 1.3V or higher. The values in the table are correct. However, the  $V_{SWINGMIN}$  value is tested with the input difference overdriven. Overdriven input is a static condition during which the overdrive forces transistors well into their saturated state.

### Amplifier Inputs

Dynamically, the situation is more complicated. Referring to the Block Diagram, an NPN differential pair with tail current forms the input stage of both amplifiers A and B. Appropriate biasing of these inputs requires 1.3V, or in other words the same value as the minimum  $V_{OCM}$ .

## APPLICATIONS INFORMATION

Specifically, the minimum voltage at amplifiers A and B should be 1.3V.

The calculation for the voltage at the A and B inputs is as follows.

$$\text{Amp A CM} = \frac{+INA \cdot R_R}{1 + R_R} + V_{OCM} \cdot \frac{1}{1 + R_R}$$

$$\text{Amp B CM} = \frac{-INB \cdot R_R}{1 + R_R} + V_{OCM} \cdot \frac{1}{1 + R_R}$$

$$R_R = \frac{R_F}{R_G} = \frac{\text{Gain}}{2}$$

### Amplifier Outputs

The Amplifiers A and B output from the collectors of pull-down NPNs in combination with high-side current boosting NPN emitters. The pull-down NPN circuit includes degeneration resistors. Fully linear, non-saturated operation requires that the NPN collector voltage be 0.8V or higher. *As a result, operation without compromised stability must be to 0.8V output voltages or higher.* This requirement is at variance with the electrical table  $V_{SWINGMIN}$ ; again,  $V_{SWINGMIN}$  uses input overdrive in a static condition, whereas full-speed operation demands non-saturated, full Beta transistors.

The following table shows examples of operating condition voltages. The boldface numbers indicate examples that do one or more of the following:

- Amplifier input voltage is at the minimum suggested as noted above.

- Output voltage low level is 0.8V as noted above.
- Output voltage high level is at 3.5V (data sheet  $V_{SWINGMAX}$ ).

**Table 1.**

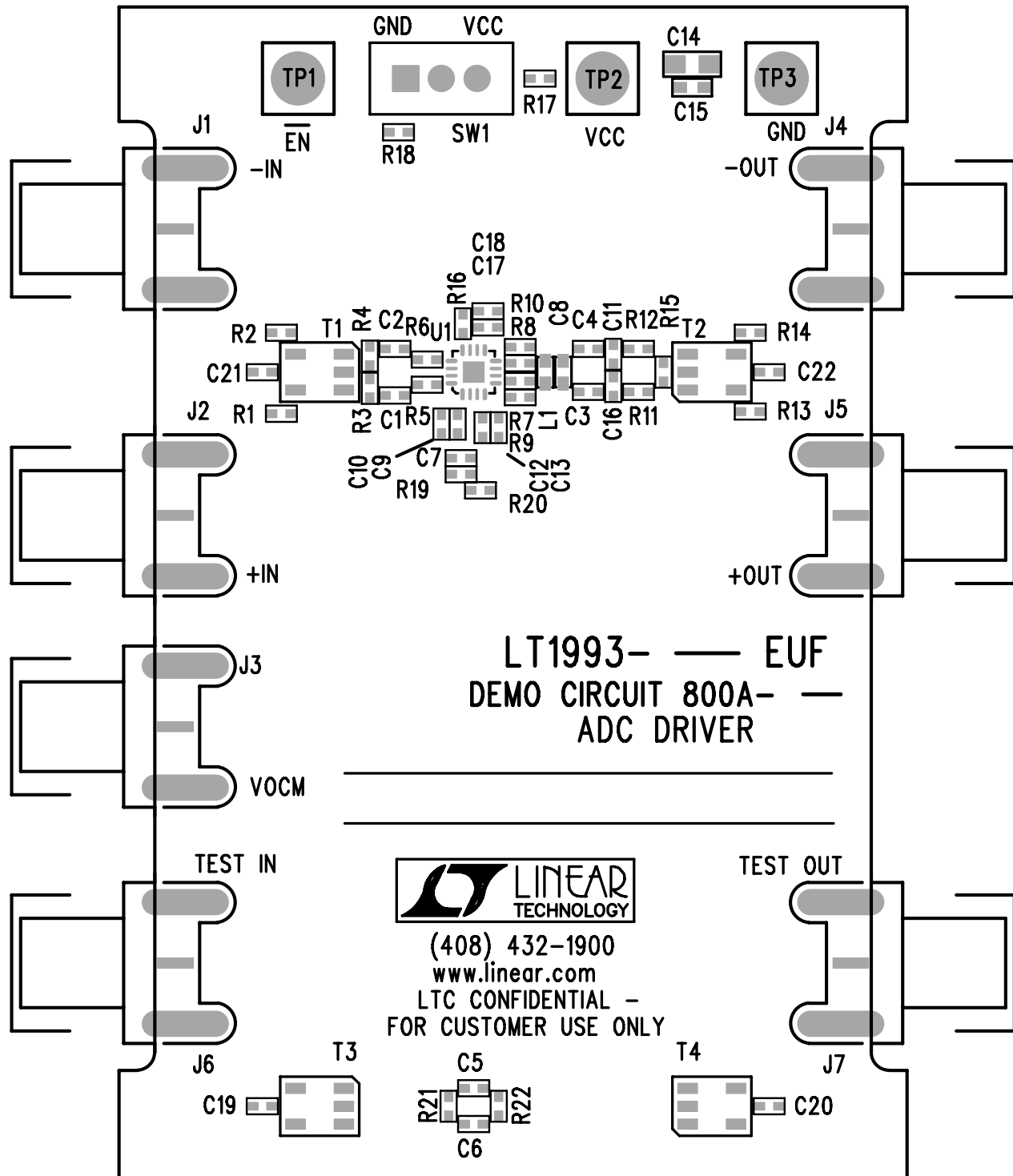
|              |            |            |
|--------------|------------|------------|
| Gain         | 2          | 2          |
| $V_{OCM}$    | 1.3        | 2.5        |
| $-INA/-INB$  | 1.3        | 3          |
| $+INA/+INB$  | 1.8        | 2          |
| $V_{INDIFF}$ | 0.5        | -1         |
| $R_R$        | 1          | 1          |
| Amp CM A     | 1.55       | 2.25       |
| Amp CM B     | <b>1.3</b> | 2.75       |
| $+V_{OUT}$   | 1.8        | 1.5        |
| $-V_{OUT}$   | <b>0.8</b> | <b>3.5</b> |

### Application (Demo) Boards

The DC800A Demo Board has been created for stand-alone evaluation of the LT1993-2 with either single-ended or differential input and output signals. As shown, it accepts a single-ended input and produces a single-ended output so that the LT1993-2 can be evaluated using standard laboratory test equipment. For more information on this Demo Board, please refer to the Demo Board section of this data sheet.

There are also additional demo boards available that combine the LT1993-2 with a variety of different Linear Technology ADCs. Please contact the factory for more information on these demo boards.

# TYPICAL APPLICATION



LINEAR TECHNOLOGY CORPORATION

800A REV 2  
11/08/04

TOP SILKSCREEN

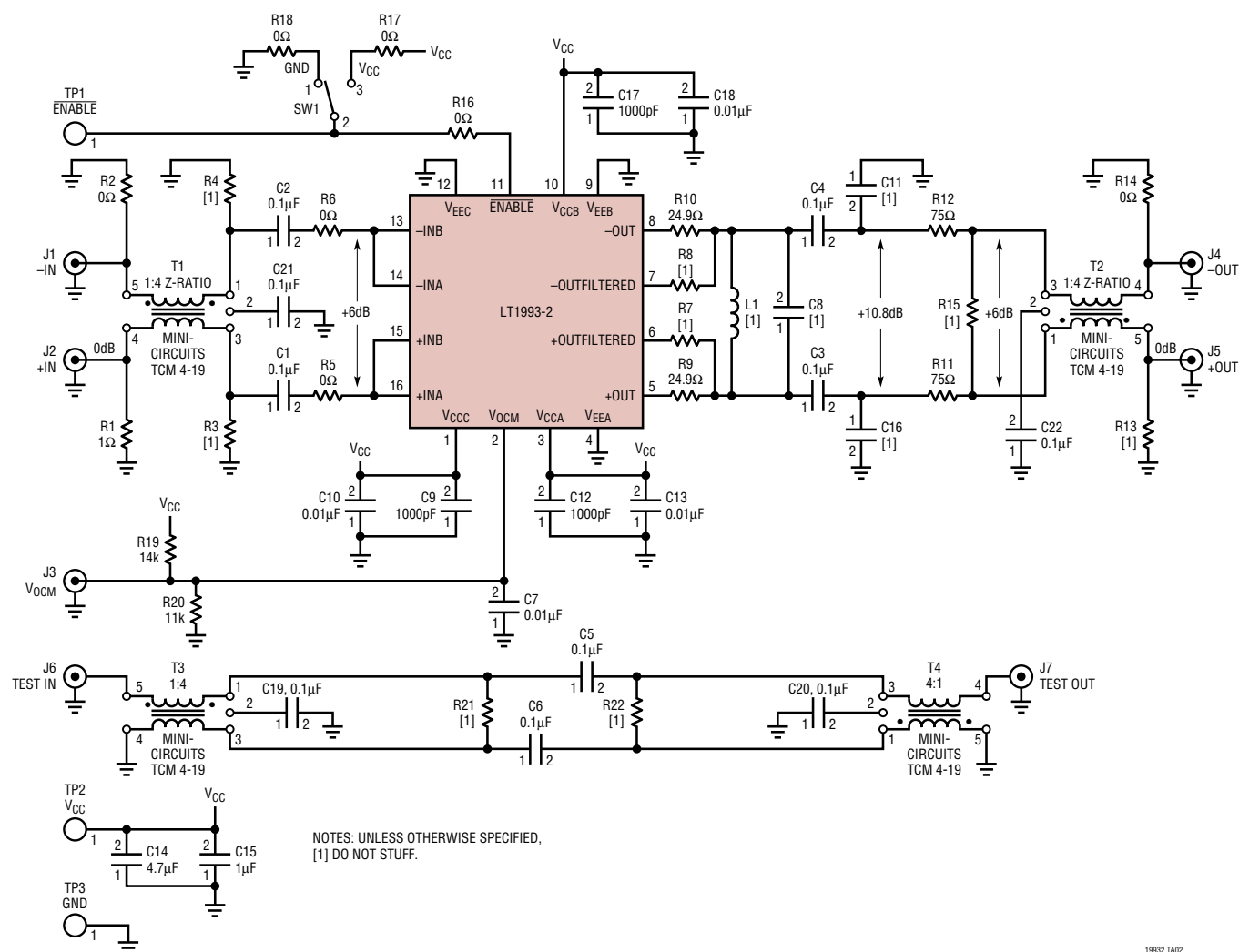


**REVISION HISTORY** (Revision history begins at Rev B)

| REV | DATE  | DESCRIPTION  | PAGE NUMBER |
|-----|-------|--|-------------|
| B   | 09/18 | Adding operating description for $V_{OCM}$ and output. | 17, 18      |

TYPICAL APPLICATION

Demo Circuit DC800A Schematic  
(AC Test Circuit)



NOTES: UNLESS OTHERWISE SPECIFIED,  
[1] DO NOT STUFF.

19932 TA02

RELATED PARTS

| PART NUMBER                | DESCRIPTION   | COMMENTS  |
|----------------------------|---|---|
| <a href="#">LT1993-4</a>   | 900MHz Differential Amplifier/ADC Driver                        | $A_V = 4V/V$ , $NF = 14.5dB$ , $OIP3 = 40dBm$ at 70MHz  |
| <a href="#">LT1993-10</a>  | 700MHz Differential Amplifier/ADC Driver                        | $A_V = 10V/V$ , $NF = 12.7dB$ , $OIP3 = 40dBm$ at 70MHz |
| <a href="#">LT5514</a>     | Ultralow Distortion IF Amplifier/ADC Driver                     | Digitally Controlled Gain Output $IP3$ 47dBm at 100MHz  |
| <a href="#">LT6600-2.5</a> | Very Low Noise Differential Amplifier and 2.5MHz Lowpass Filter | 86dB S/N with 3V Supply, SO-8 Package                   |
| <a href="#">LT6600-5</a>   | Very Low Noise Differential Amplifier and 5MHz Lowpass Filter   | 82dB S/N with 3V Supply, SO-8 Package                   |
| <a href="#">LT6600-10</a>  | Very Low Noise Differential Amplifier and 10MHz Lowpass Filter  | 82dB S/N with 3V Supply, SO-8 Package                   |
| <a href="#">LT6600-20</a>  | Very Low Noise Differential Amplifier and 20MHz Lowpass Filter  | 76dB S/N with 3V Supply, SO-8 Package                   |

Rev B

# Mouser Electronics

Authorized Distributor

Click to View Pricing, Inventory, Delivery & Lifecycle Information:

[Analog Devices Inc.:](#)

[LT1993IUD-2#PBF](#) [LT1993CUD-2#TRPBF](#) [LT1993CUD-2#PBF](#) [LT1993IUD-2#TRPBF](#) [DC800A-A](#)