

Evaluating the [ADN4651/ADN4652](#) 5 kV RMS, 600 Mbps LVDS Isolator (SOIC_W)

FEATURES

Isolated ground planes (logic side and bus side)
Convenient connections through SMA terminals
3.3 V or 2.5 V power on Side 1 (V_{IN1}/V_{DD1}) and Side 2 (V_{IN2}/V_{DD2})
Ground on Side 1 (GND_1) and Side 2 (GND_2)
LVDS input signals: D_{IN1+} , D_{IN1-} , D_{IN2+} , D_{IN2-}
LVDS output signals: D_{OUT1+} , D_{OUT1-} , D_{OUT2+} , D_{OUT2-}
Jumper-selectable supply power of 3.3 V or 2.5 V
Termination resistors on all LVDS drivers/receivers

EVALUATION KIT CONTENTS

[EVAL-ADN4651EB1Z](#) or [EVAL-ADN4652EB1Z](#) evaluation board

DOCUMENTS NEEDED

[ADN4650/ADN4651/ADN4652](#) data sheet

EQUIPMENT NEEDED

Signal generator
Oscilloscope

GENERAL DESCRIPTION

The [EVAL-ADN4651EB1Z](#) and [EVAL-ADN4652EB1Z](#) allow quick and easy evaluation of the [ADN4651/ADN4652](#) low-voltage differential signalling (LVDS) isolator without the need for external components. The [ADN4651/ADN4652](#) employ Analog Devices, Inc., iCoupler® technology to combine a 2-channel isolator with an LVDS receiver and driver into a single, 20-lead wide body SOIC package. They are capable of running at data rates of up to 600 Mbps with very low jitter.

The evaluation board has separate ground and power planes for each side of the isolator. This separation enables the evaluation of the [ADN4651/ADN4652](#) with galvanic isolation between both sides of the device. Jumper-selectable power supplies at 3.3 V or 2.5 V are required on each side of the [ADN4651/ADN4652](#). Using an on-chip LDO, 2.5 V can be provided from an external 3.3 V power supply.

Complete information about the [ADN4651/ADN4652](#) is available in the [ADN4650/ADN4651/ADN4652](#) data sheet, which should be consulted in conjunction with this user guide when using the evaluation boards.

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REVISION HISTORY

5/16—Rev. 0 to Rev. A

Added the EVAL-ADN4652EB1Z and ADN4652.....	Universal
Changes to Documents Needed Section	1
Added Figure 2; Renumbered Sequentially	2
Changes to Setting Up the Evaluation Board Section	3
Changes to Figure 5 Caption, Table 2, and Table 3	4
Changes to Figure 6 Caption and Radiated Emissions	
Test Results (EN 55022) Section.....	6
Added Figure 11 and Figure 12.....	8
Added Table 6; Renumbered Sequentially	12
Changes to Related Link Section.....	12

12/15—Revision 0: Initial Version

EVALUATION BOARD PHOTOGRAPHS

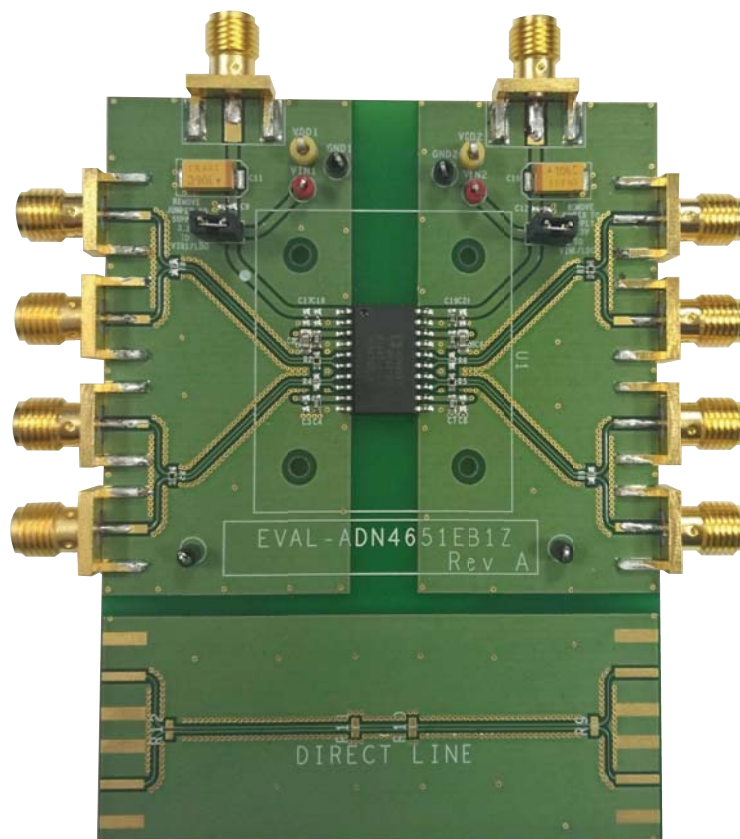


Figure 1. EVAL-ADN4651EB1Z Evaluation Board

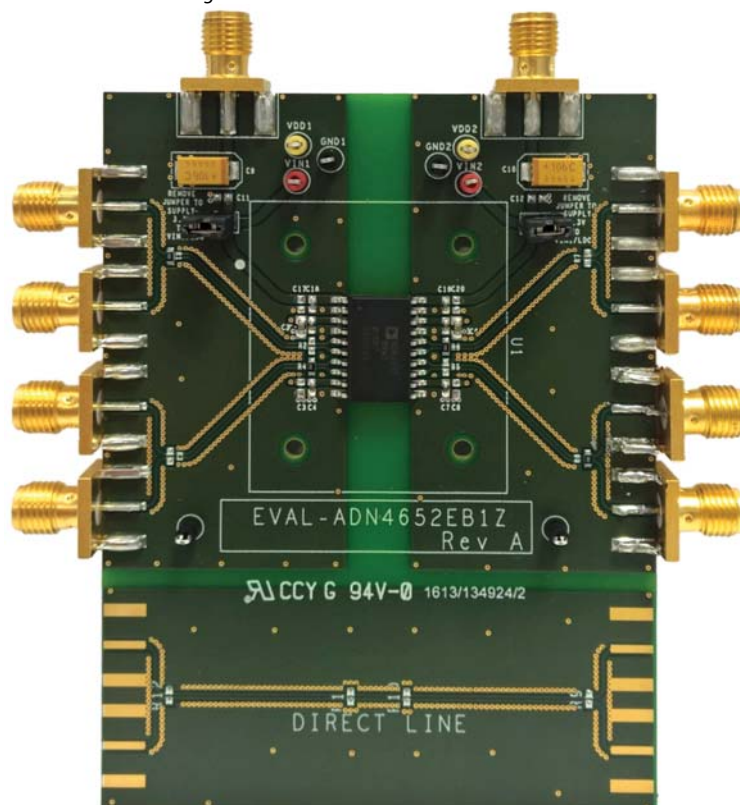


Figure 2. EVAL-ADN4652EB1Z Evaluation Board

EVALUATION BOARD CONFIGURATION

SETTING UP THE EVALUATION BOARD

On the [EVAL-ADN4651EB1Z/EVAL-ADN4652EB1Z](#), power supplies are configured using Jumpers P4 and P7 (see Table 1) and connected to the J9 and J10 SMA connectors (see Table 2 and Table 3). A 3.3 V power supply can be applied to Side 1 and/or Side 2 of the [ADN4651/ADN4652](#) by removing Jumpers P4 (Side 1) and P7 (Side 2). If a 2.5 V supply is connected to the board, the relevant jumper must be inserted (P4 for Side 1 and P7 for Side 2). At 300 MHz with a load resistance of 100 Ω , the maximum operating current from each power supply is 90 mA.

When using a 3.3 V power supply, V_{IN1} and V_{DD1} (Pin 1 and Pin 3 on the [ADN4651/ADN4652](#)) are bypassed to GND_1 using 1 μ F capacitors. V_{IN2} and V_{DD2} (Pin 20 and Pin 18 on the [ADN4651/ADN4652](#)) are bypassed to GND_2 using 1 μ F capacitors. When using a 2.5 V power supply, V_{IN1} or V_{IN2} is connected directly to V_{DD1} or V_{DD2} by shorting Jumpers P4 or P7, respectively. Both V_{DD1} pins are also bypassed to GND_1 with 0.1 μ F capacitors. Both V_{DD2} pins are also bypassed to GND_2 with 0.1 μ F capacitors.

An example operation of the [EVAL-ADN4651EB1Z](#) is shown in Figure 5 (signal generator and oscilloscope connections are reversed for [EVAL-ADN4652EB1Z](#), per Table 2 and Table 3). SMA connectors expose all LVDS inputs and outputs for the [EVAL-ADN4651EB1Z](#), but are reversed for the [EVAL-ADN4652EB1Z](#) (see Table 2 and Table 3). Connect a signal generator to the board using the J1 and J2 connectors and set up a 300 MHz square wave clock with an amplitude of 350 mV and an offset of 1.2 V. Connect the oscilloscope directly to the J5 and J6 connectors to perform timing measurements including propagation delay and skew. Precision measurements, for example, jitter, using a differential probe requires attaching the probe at the R7 or R3 resistors and potentially cutting the traces to the connectors to minimize reflections.

A plot of the oscilloscope connected via the J5 and J6 connectors is shown in Figure 3. Channel 3 (green) and Channel 4 (purple) show the J5 and J6 connectors separately (single-ended) with the differential signal (orange).

Operation of the second isolated LVDS channel is shown in Figure 4. In contrast to Figure 5, the oscilloscope now connects via the J3 and J4 connectors and the signal generator connects to the J7 and J8 connectors. Channel 3 (green) and Channel 4 (purple) show the J3 and J4 connectors separately (single-ended) with the differential signal (orange).



Figure 3. D_{OUT1-} and D_{OUT1+} with a 300 MHz Clock, Single-Ended and Differential



Figure 4. D_{OUT2-} and D_{OUT2+} with a 300 MHz Clock, Single-Ended and Differential

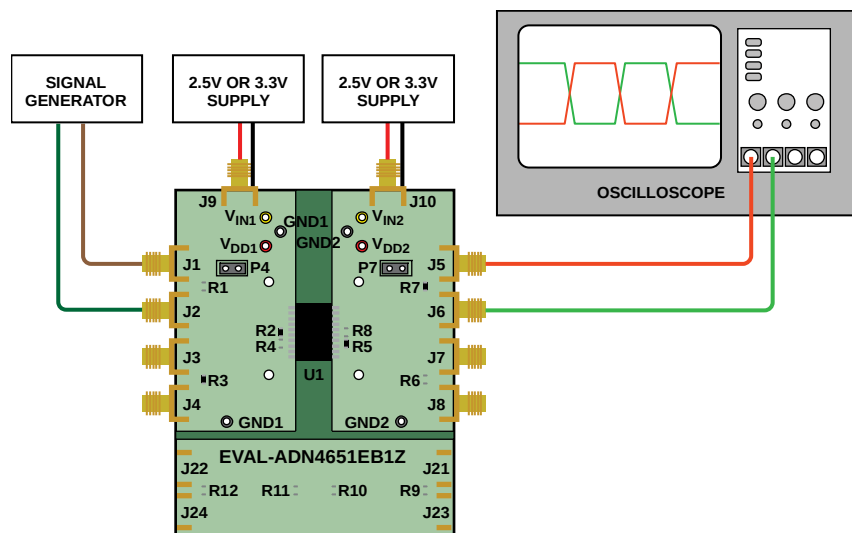


Figure 5. Basic LVDS Isolator Evaluation Board Operation for the [EVAL-ADN4651EB1Z](#); Scope and Signal Generator Reversed for the [EVAL-ADN4652EB1Z](#)

Table 1. Jumper Configuration

Jumper	Position	Description
P4	Open	3.3 V power supply connected to Connector J9 for V_{IN1}
	Closed	2.5 V power supply connected to Connector J9, V_{IN1} shorted to V_{DD1}
P7	Open	3.3 V power supply connected to Connector J9 for V_{IN2}
	Closed	2.5 V power supply connected to Connector J9, V_{IN2} shorted to V_{DD2}

Table 2. Side 1 Connector Descriptions

EVAL-ADN4651EB1Z Connector	EVAL-ADN4652EB1Z Connector	Description
J9	J9	Power supply, 3.3 V (Jumper P4 open) or 2.5 V (Jumper P4 closed)
J1	J3	D_{IN1+} , noninverted LVDS input for Channel 1
J2	J4	D_{IN1-} , inverted LVDS input for Channel 1
J3	J1	D_{OUT2+} , noninverted LVDS output for Channel 2
J4	J2	D_{OUT2-} , inverted LVDS output for Channel 2
J22	J22	Connects to Connector J21 (test trace for calibration)
J24	J24	Connects to Connector J23 (test trace for calibration)

Table 3. Side 2 Connector Descriptions

EVAL-ADN4651EB1Z Connector	EVAL-ADN4652EB1Z Connector	Description
J10	J10	Power supply, 3.3 V (Jumper P7 open) or 2.5 V (Jumper P7 closed)
J5	J7	D_{OUT1+} , noninverted LVDS output for Channel 1
J6	J8	D_{OUT1-} , inverted LVDS output for Channel 1
J7	J5	D_{IN2+} , noninverted LVDS input for Channel 2
J8	J6	D_{IN2-} , inverted LVDS input for Channel 2
J21	J21	Connects to Connector J22 (test trace for calibration)
J23	J23	Connects to Connector J24 (test trace for calibration)

RADIATED EMISSIONS TEST RESULTS (EN 55022)

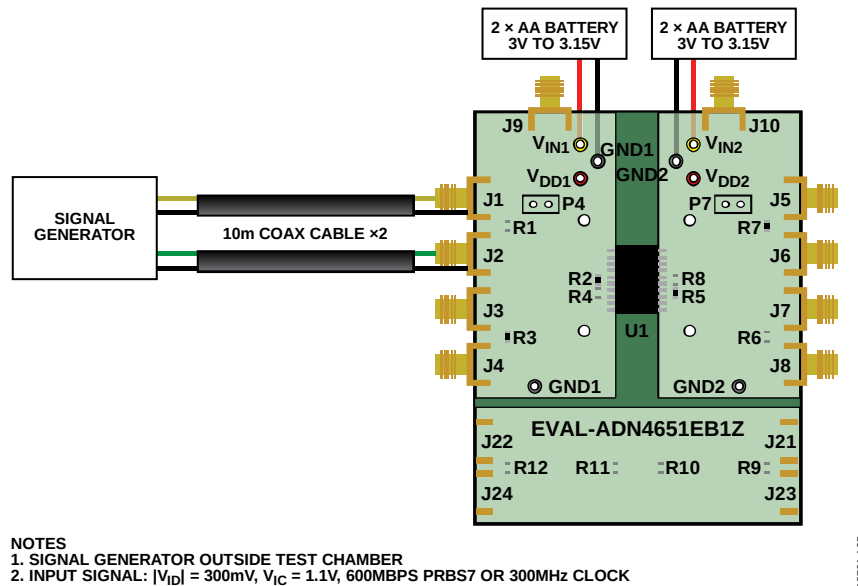


Figure 6. Test Setup for EN 55022 Radiated Emissions Testing for the EVAL-ADN4651EB1Z; Scope and Signal Generator Reversed for the EVAL-ADN4652EB1Z

Radiated emissions testing is performed with the EVAL-ADN4651EB1Z and EVAL-ADN4652EB1Z at an independent external test facility. Evaluating the EVAL-ADN4651EB1Z and EVAL-ADN4652EB1Z to the EN 55022 standard is undertaken in a 10 m radiated emissions test chamber, using the test setup shown in Figure 6. The setup comprises a battery-powered EVAL-ADN4651EB1Z/EVAL-ADN4652EB1Z connected to a signal generator located outside the chamber via coax cables. As specified by the EN 55022 standard, both horizontal and vertical peak scans are undertaken with any visible emissions peaks investigated using quasi-peak detector measurement. For each frequency measured using a quasi-peak detector, the unit under test rotates through 360 degrees to find the worst case angle. The receiving antenna then elevates from 1 m to 4 m in height to find the worst case elevation. The worst case quasi-peak measurements are compared to the EN 55022 Class B and Class A limits.

The test results for EVAL-ADN4651EB1Z and EVAL-ADN4652EB1Z are shown in Table 4 and a classification report for both evaluation boards is available on request (please contact Analog Devices or the distributor for support). Radiated emissions are measured across 30 MHz to 1 GHz and from 1 GHz to 3 GHz.

With a 600 Mbps PRBS input, the EVAL-ADN4651EB1Z/EVAL-ADN4652EB1Z passes the EN 55022 Class B limits. Plots for horizontal and vertical peak radiated emissions below 1 GHz are shown in Figure 7 and Figure 8, respectively, for the EVAL-ADN4651EB1Z; see the classification report for the EVAL-ADN4652EB1Z plots.

With a 300 MHz clock input, the EVAL-ADN4651EB1Z/EVAL-ADN4652EB1Z passes the EN 55022 Class A limits. To pass the Class B limits when isolating high frequency clocks, reduce the printed circuit board (PCB) clearance from the 8 mm implemented on the EVAL-ADN4651EB1Z/EVAL-ADN4652EB1Z to, for example, 2 mm.

Table 4. EN 55022 Radiated Emissions Classification

Test Condition	Result
600 Mbps PRBS	Passes EN 55022 Class B
300 MHz Clock	Passes EN 55022 Class A

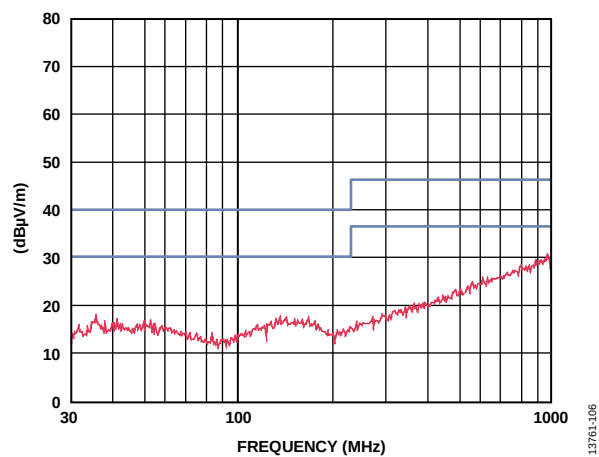


Figure 7. EVAL-ADN4651EB1Z Radiated Emissions (Horizontal, Peak, 30 MHz to 1 GHz) with 600 Mbps PRBS7 Input

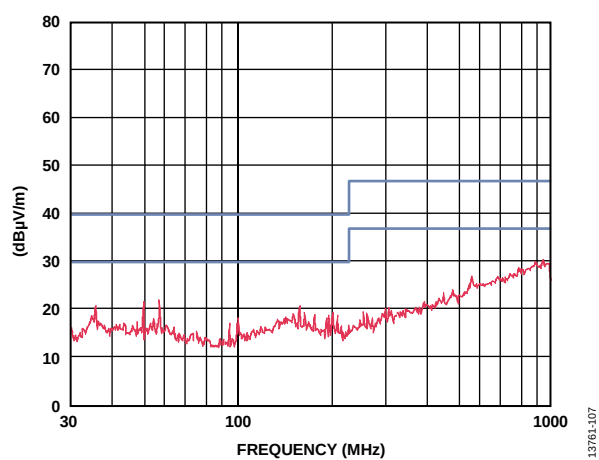


Figure 8. EVAL-ADN4651EB1Z Radiated Emissions (Vertical, Peak, 30 MHz to 1 GHz) with 600 Mbps PRBS7 Input

EVALUATION BOARD SCHEMATIC AND ARTWORK

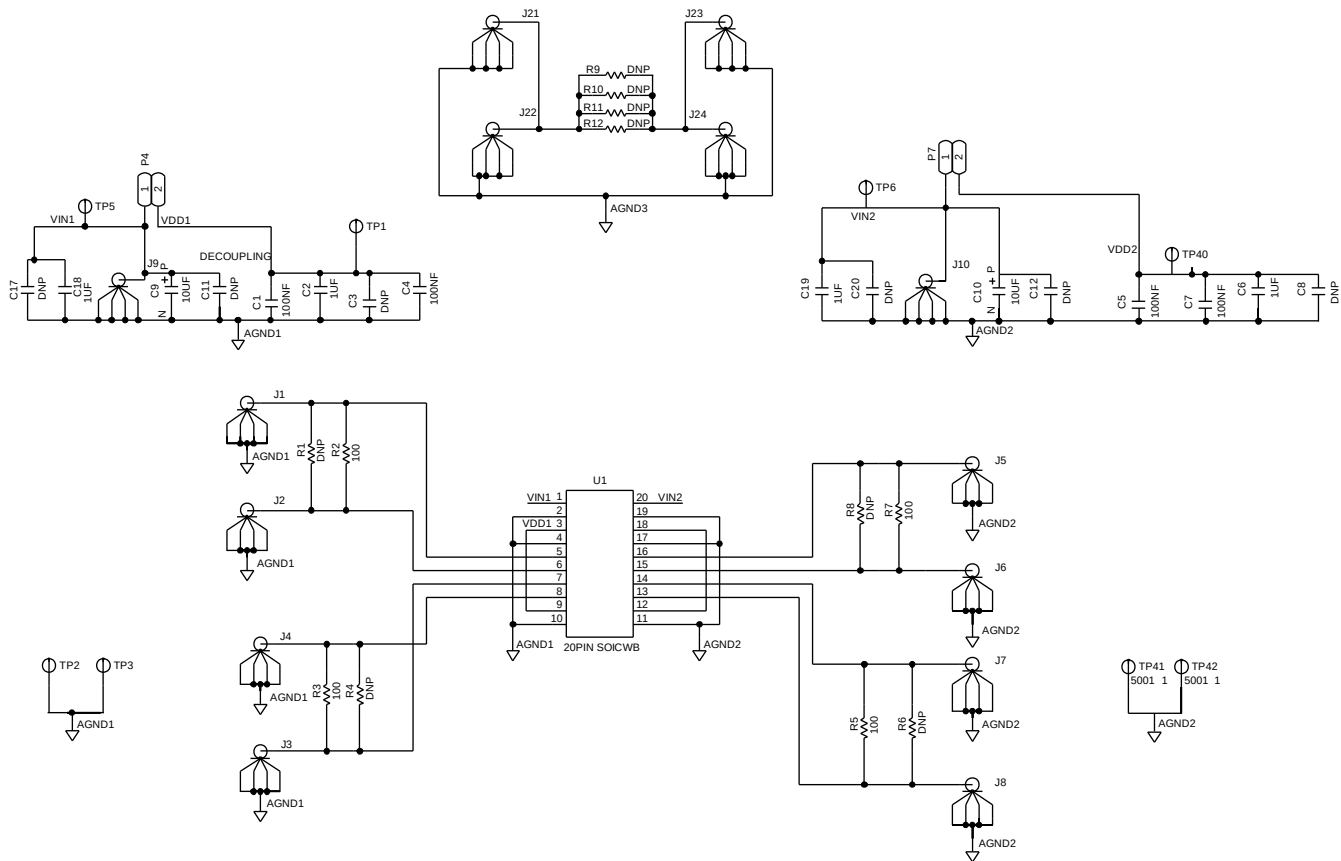


Figure 9. EVAL-ADN4651EB1Z Schematic

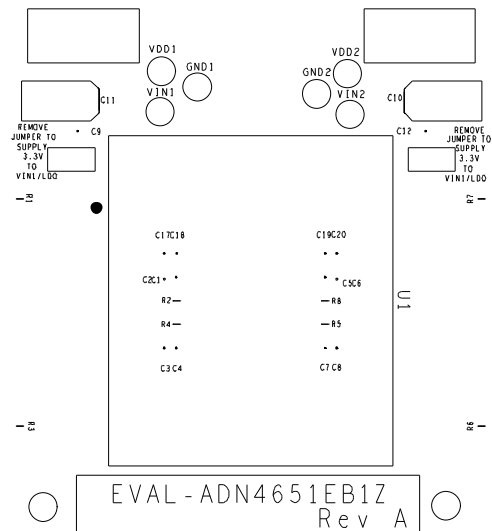


Figure 10. EVAL-ADN4651EB1Z Silkscreen

[illegible]

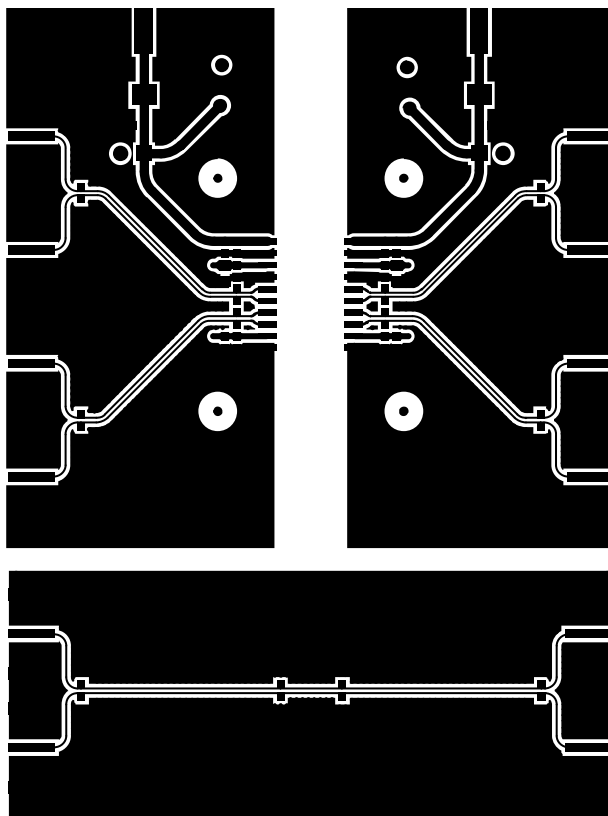


Figure 13. EVAL-ADN4651EB1Z/EVAL-ADN4652EB1Z Component Side

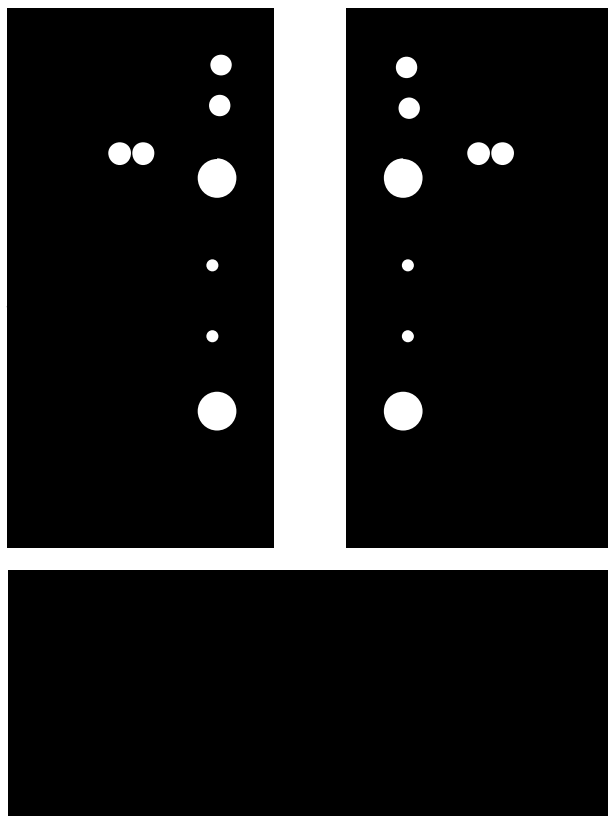


Figure 14. EVAL-ADN4651EB1Z/EVAL-ADN4652EB1Z Inner Layer 2, Ground

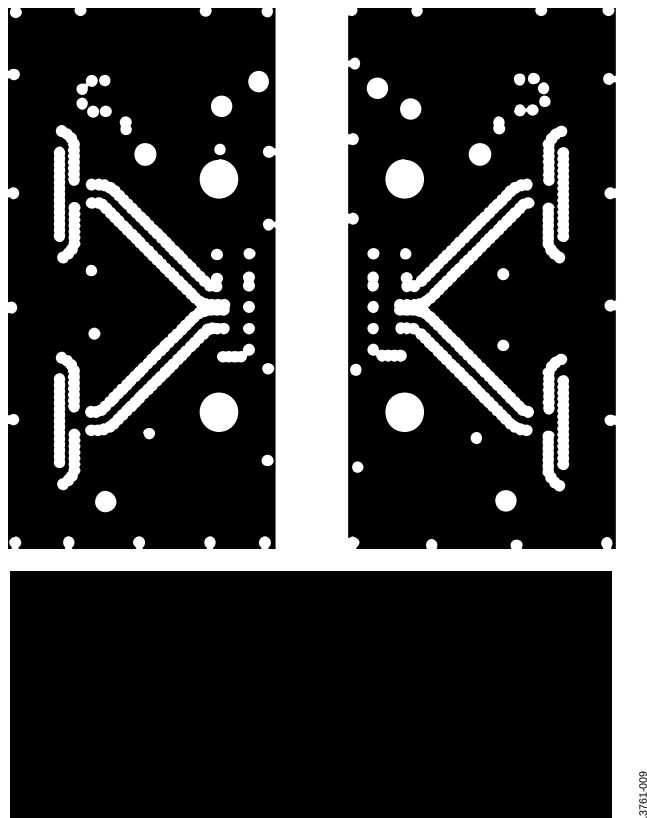


Figure 15. [EVAL-ADN4651EB1Z/EVAL-ADN4652EB1Z](#) Inner Layer 3, Power

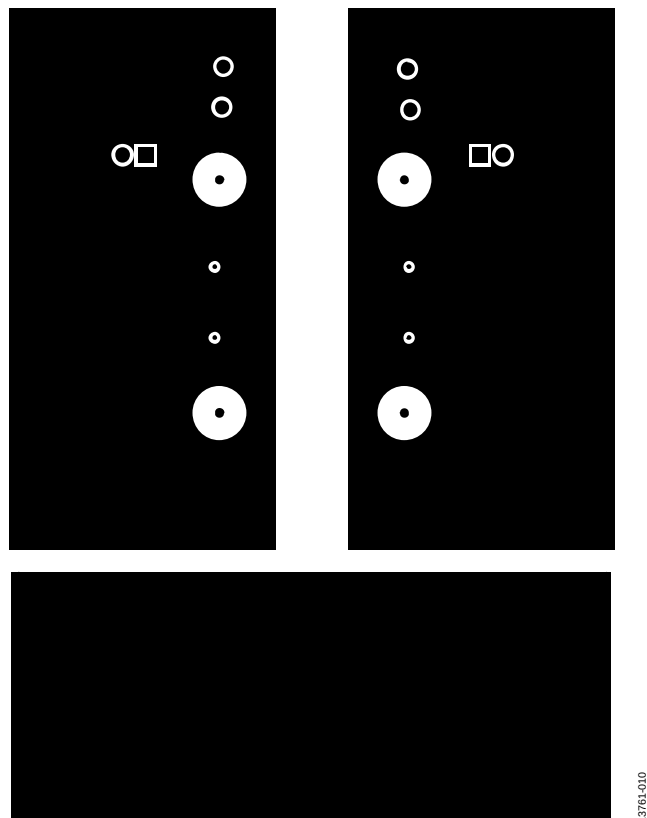


Figure 16. [EVAL-ADN4651EB1Z/EVAL-ADN4652EB1Z](#) Solder Side

ORDERING INFORMATION

BILL OF MATERIALS

Table 5. Bill of Materials for the [EVAL-ADN4651EB1Z](#)

Qty.	Reference Designator	Description	Manufacturer	Part Number
4	C1, C4, C5, C7	Capacitors, 100 nF, 0402	Multicomp	MC0402X104K100CT
2	C2, C6	Capacitors, 1 μ F, 0603	Multicomp	MC0603X105K100CT
4	C3, C8, C11, C12, C17, C20	Capacitors, 0402	Not fitted	Not applicable
2	C9, C10	Capacitors, tantalum, 10 μ F, Case C	AVX	TAJC106K016RNJ
2	C18, C19	Capacitors, 1 μ F, 0402	Multicomp	MC0402X105K6R3CT
10	J1 to J10	Connectors, SMA, edge	Johnson	142-0701-801
4	J21 to J24	Connectors, SMA, edge	Not fitted	Not applicable
2	P4, P7	2-pin, header and jumper	TE Connectivity	826926-2 and 3M/969102-0000-DA)
8	R1, R4, R6, R8 to R12	Resistors, 0402	Not fitted	Not applicable
4	R2, R3, R5, R7	Resistors, 100 Ω , 0402	Multicomp	MCMR04X1000FTL
2	TP1/VDD1, TP40/VDD2	Test points, yellow	Vero	20-313140
4	TP2, TP3, TP41, TP42	Test points, black	Vero	20-2137
2	TP5/VIN1, TP6/VIN2	Test points, red	Vero	20-313137
1	U1	ADN4651 5 kV rms, 600 Mbps, LVDS isolator	Analog Devices	ADN4651BRWZ

Table 6. Bill of Materials for the [EVAL-ADN4652EB1Z](#)

Qty.	Reference Designator	Description	Manufacturer	Part Number
4	C1, C4, C5, C7	Capacitors, 100 nF, 0402	Multicomp	MC0402X104K100CT
2	C2, C6	Capacitors, 1 μ F, 0603	Multicomp	MC0603X105K100CT
4	C3, C8, C11, C12, C17, C20	Capacitors, 0402	Not fitted	Not applicable
2	C9, C10	Capacitors, tantalum, 10 μ F, Case C	AVX	TAJC106K016RNJ
2	C18, C19	Capacitors, 1 μ F, 0402	Multicomp	MC0402X105K6R3CT
10	J1 to J10	Connectors, SMA, edge	Johnson	142-0701-801
4	J21 to J24	Connectors, SMA, edge	Not fitted	Not applicable
2	P4, P7	2-pin, header and jumper	TE Connectivity	826926-2 and 3M/969102-0000-DA)
8	R2, R3, R5, R7, R9 to R12	Resistors, 0402	Not fitted	Not applicable
4	R1, R4, R6, R8	Resistors, 100 Ω , 0402	Multicomp	MCMR04X1000FTL
2	TP1/VDD1, TP40/VDD2	Test points, yellow	Vero	20-313140
4	TP2, TP3, TP41, TP42	Test points, black	Vero	20-2137
2	TP5/VIN1, TP6/VIN2	Test points, red	Vero	20-313137
1	U1	ADN4652 5 kV rms, 600 Mbps, LVDS isolator	Analog Devices	ADN4652BRWZ

RELATED LINKS

Resource	Description
ADN4651	Product page, ADN4651 , 5 kV rms, 600 Mbps, dual-channel isolated LVDS
ADN4652	Product page, ADN4652 , 5 kV rms, 600 Mbps, dual-channel isolated LVDS

NOTES



ESD Caution

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

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