

Evaluation Board for the **AD5322** 12-Bit, Dual-Channel, Voltage Output DAC

FEATURES

Full featured evaluation board in conjunction with
nanoDAC® motherboard (**EVAL-MBnanoDAC-SDZ**)
 On-board references
 Various link options
 PC control in conjunction with Analog Devices, Inc., system
 demonstration platform (SDP)

PACKAGE CONTENTS

EVAL-AD5322DBZ evaluation board
EVAL-MBnanoDAC-SDZ motherboard

SOFTWARE NEEDED

EVAL-AD5322DBZ evaluation software

HARDWARE NEEDED

EVAL-SDP-CB1Z (SDP-B) board, must be purchased
 separately

DOCUMENTS NEEDED

Electronic version of the **AD5322** data sheet
 Electronic version of the **EVAL-AD5322DBZ** user guide

GENERAL DESCRIPTION

This user guide details the operation of the evaluation board for the **AD5322** dual-channel, voltage output, digital-to-analog converter (DAC).

The evaluation board is designed to help users quickly prototype new **AD5322** circuits and reduce design time. The **AD5322** operates from a single 2.5 V to 5.5 V supply.

For full data, see the **AD5322** data sheet, which must be consulted in conjunction with this user guide when using the evaluation board.

The evaluation board interfaces to the USB port of a PC via the **SDP-B** board. Software is available for download from the **EVAL-AD5322DBZ** evaluation board page to allow the user to program the **AD5322**.

EVAL-AD5322DBZ, EVAL-MBnanoDAC-SDZ, AND SDP-B BOARDS

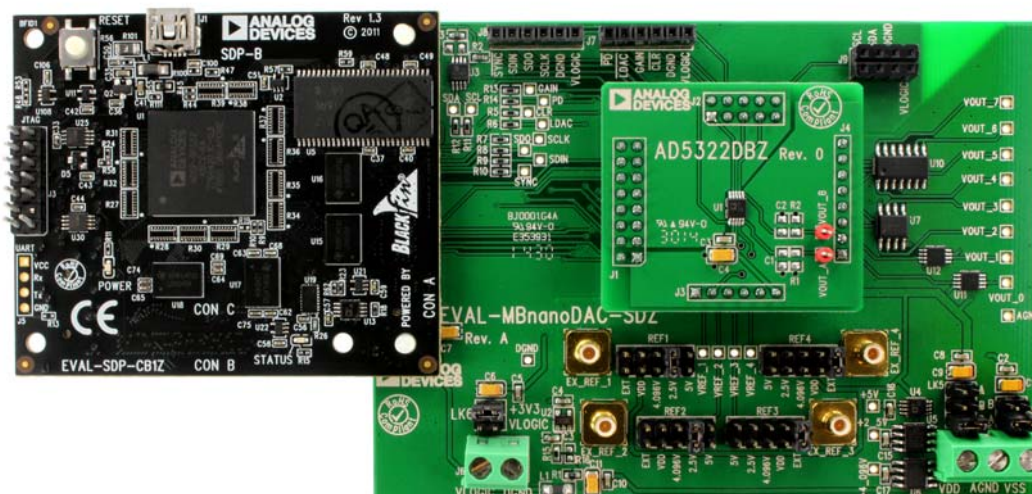


Figure 1.

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REVISION HISTORY

3/2017—Revision 0: Initial Version

EVALUATION BOARD HARDWARE

MOTHERBOARD POWER SUPPLIES

The [EVAL-MBnanoDAC-SDZ](#) motherboard supports single and dual power supplies.

The [EVAL-AD5322DBZ](#) evaluation board can be powered either from the SDP port or externally by the J5 and J6 connectors, as described in Table 1.

Both the AGND and DGND inputs are provided on the board. The AGND and DGND planes are connected at one location on the [EVAL-MBnanoDAC-SDZ](#). It is recommended that AGND and DGND not be connected elsewhere in the system to avoid ground loop problems.

All supplies are decoupled to ground with 10 μ F tantalum and 0.1 μ F ceramic capacitors.

Table 1. Power Supply Connectors

Connector No.	Label	Voltage
J5, Pin 1 (J5-1)	VDD	Analog positive power supply, V_{DD} . Single supply 5 V, dual supply 5 V.
J5, Pin 2 (J5-2)	AGND	Analog ground.
J5, Pin 3 (J5-3)	VSS	Analog negative power supply, V_{SS} . Dual supply -5 V.
J6, Pin 1 (J6-1)	VLOGIC	Digital supply from 1.8 V to V_{DD} of the daughter board DAC.
J6, Pin 2 (J6-2)	DGND	Digital ground.

Table 3. Link Functions

Link No.	Function
REF1 to REF4	These links select the reference source. Position EXT selects an off board voltage reference via the appropriate EXT_REF_x connector. Position VDD selects V_{DD} as the reference source. Position 4.096V selects the on-board 4.096 V reference as the reference source. Position 2.5V selects the on-board 2.5 V reference as the reference source. Position 5V selects the on-board 5 V reference as the reference source.
LK5	This link selects the positive DAC analog voltage source. Position A selects the internal voltage source from the SDP-B board. Position B selects the internal voltage source 3.3 V from the ADP121 on the motherboard. Position C selects an external supply voltage, V_{DD} .
LK6	This link selects the VLOGIC voltage source. Position 3.3V selects the digital voltage source from the SDP-B board, 3.3 V. Position VLOGIC selects an external digital supply voltage, V_{LOGIC} .
LK7	This link selects the negative DAC analog voltage source. Position A selects V_{SS} . Position B selects AGND.

LINK OPTIONS

A number of link options are incorporated in the [EVAL-MBnanoDAC-SDZ](#) and must be set for the required operating conditions before using the board. Table 2 describes the positions of the links to control the evaluation board via the [SDP-B](#) board using a PC and external power supplies. The functions of these link options are described in detail in Table 3. The positions listed in Table 2 and Table 3 match the evaluation board imprints (see Figure 12).

Table 2. Link Options Setup for [SDP-B](#) Control (Default)

Link No.	Position
REF1	2.5V
REF2	2.5V
REF3	EXT
REF4	EXT
LK5	C
LK6	3.3V
LK7	B

EVALUATION BOARD SOFTWARE QUICK START PROCEDURES

INSTALLING THE SOFTWARE

The [EVAL-AD5322DBZ](#) software is compatible with Windows® Vista (64-bit/32-bit), and Windows 7 (64-bit/32-bit).

The software must be installed before connecting the [SDP-B](#) board to the USB port of the PC to ensure that the [SDP-B](#) board is recognized when it connects to the PC.

To install the software, take the following steps:

1. Start the Windows operating system. Download the installation software from the [EVAL-AD5322DBZ](#) evaluation board page.
2. Run the setup.exe file from the installer folder if it does not open automatically.
3. After installation is completed, power up the evaluation board as described in the Motherboard Power Supplies section.
4. Connect the evaluation board to [SDP-B](#) board and the [SDP-B](#) board into the PC using the USB cable included in the evaluation kit.
5. When the software detects the evaluation board, click through any dialog boxes that appear to finalize the installation.

RUNNING THE SOFTWARE

To run the program, take the following steps:

1. Connect the evaluation board to the [SDP-B](#) board and connect the USB cable between the [SDP-B](#) board and the PC.
2. Power up the evaluation board as described in the Motherboard Power Supplies section.
3. From the **Start** menu, click **All Programs, Analog Devices, AD5322 Evaluation Software**.
4. If the [SDP-B](#) board is not connected to the USB port when the software is launched, a connectivity error displays (see Figure 2). Connect the evaluation board to the USB port of the PC and wait a few seconds. When the [SDP-B](#) board is detected, the display is updated (see Figure 3).

Alternatively, the software can be used without an evaluation board. The software runs in simulation mode displaying expected outputs based on the input data. The main window of the [AD5322](#) evaluation software then opens, as shown in Figure 4.

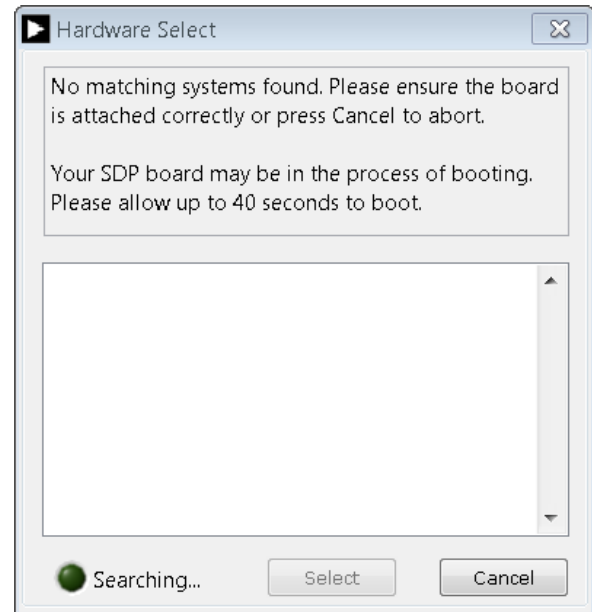


Figure 2. Connectivity Error

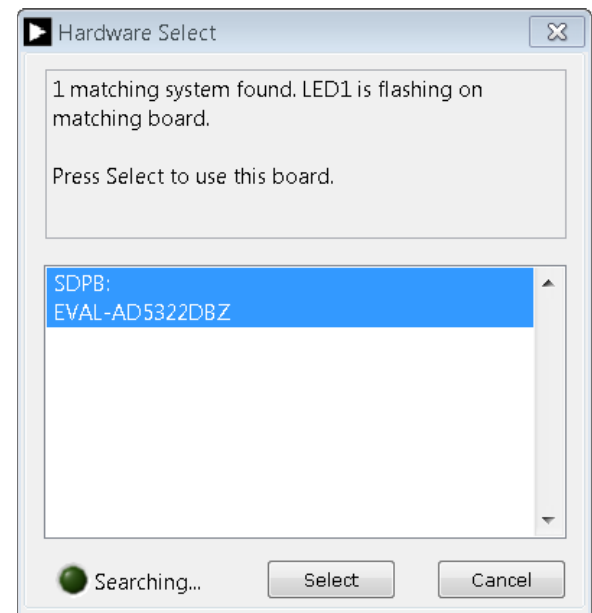


Figure 3. Hardware Select

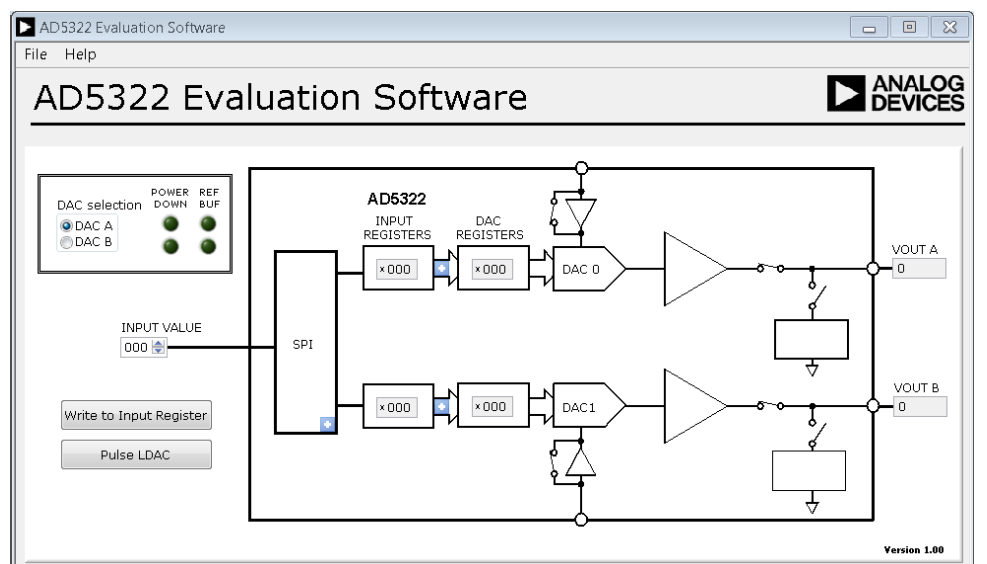


Figure 4. AD5322 Evaluation Software Main Window

SOFTWARE OPERATION

The software for the AD5322 allows the user to program values to the input and DAC registers of each DAC individually.

Write to Input Register

Click **Write to Input Register** to load the code of the input data control to the input register of the selected DAC in the **DAC selection** box.

LDAC Control

Click **Pulse LDAC** to bring the LDAC pin low and then back high. Doing this copies the data from the input registers to the DAC registers, and the outputs update accordingly.

Click the blue progressive disclosure option on the **SPI** block, and click the appropriate radio option to set the LDAC pin high or low. A dialog box appears that allows the user to select the LDAC setting, as shown in Figure 5.

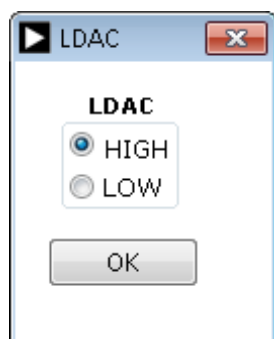


Figure 5. LDAC Selection Box in the LDAC Window

Power-Down Control

Each of the DACs can be powered down individually. Each DAC has an associated selection box allowing the DAC to operate in normal mode or three different power-down modes. Click the blue progressive disclosure option to access the selection box shown in

Figure 6. When the power-down setting for the selected DAC is set, click **OK** to write the appropriate values to the AD5322.

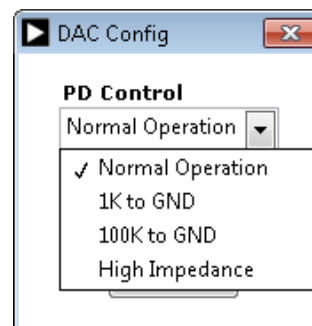


Figure 6. PD Control Dropdown Menu in the DAC Config Window

Buffer Control

The reference of each DAC can be buffered individually. Each DAC has an associated selection box allowing the reference to be buffered or unbuffered. Click the blue progressive disclosure option to access the selection box shown in Figure 7. When the buffer setting for the selected DAC is set, click **OK** to write the appropriate values to the AD5322.

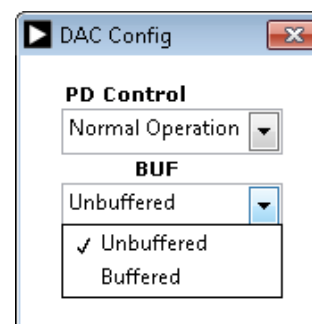


Figure 7. BUF Dropdown Menu in the DAC Config Window

EVALUATION BOARD SCHEMATICS AND ARTWORK

EVAL-MBnanoDAC-SDZ MOTHERBOARD

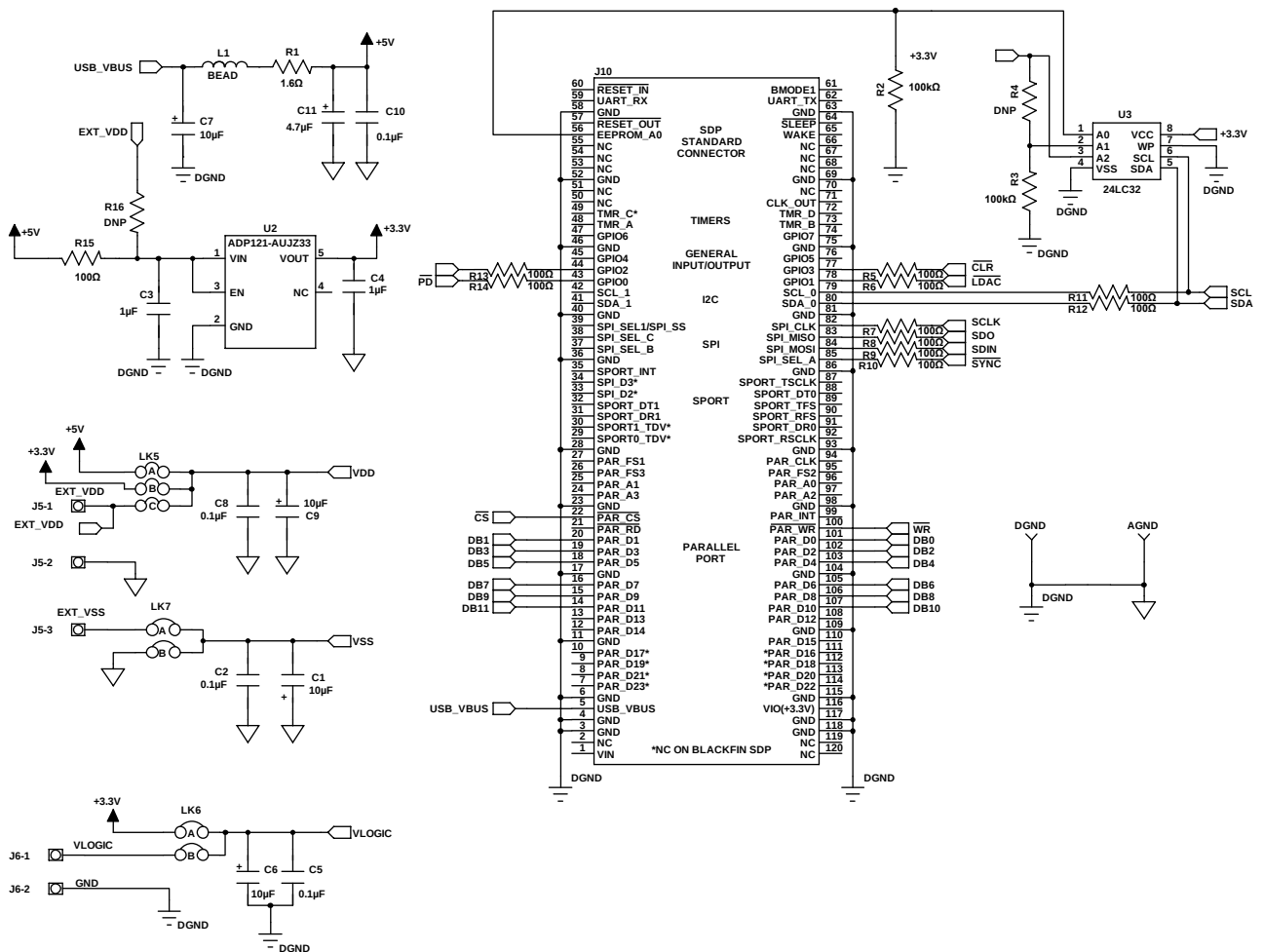


Figure 8. EVAL-MBnanoDAC-SDZ Motherboard SDB Connector and Power Supply

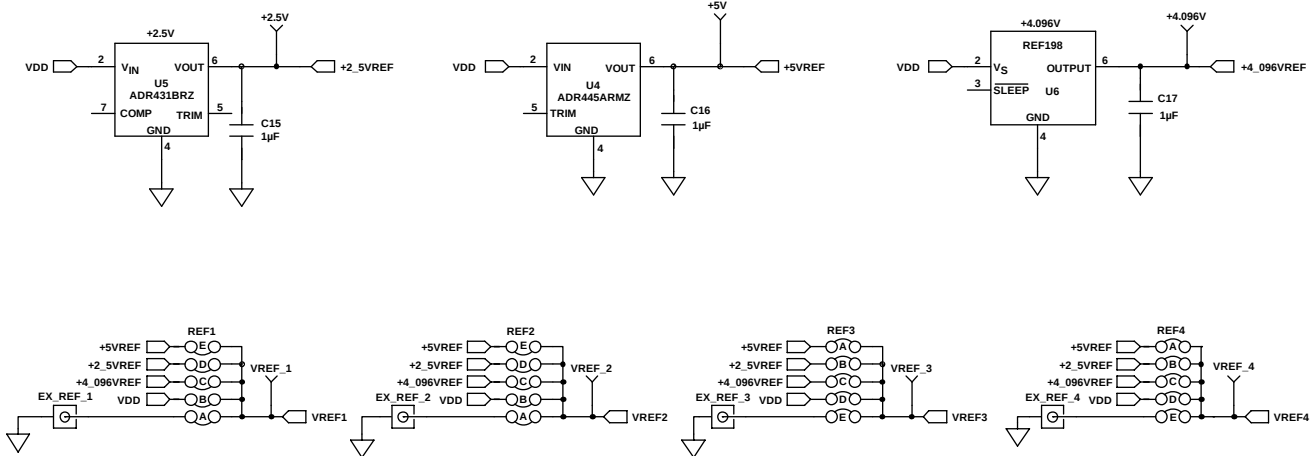


Figure 9. EVAL-MBnanoDAC-SDZ Motherboard Reference Voltage Selector Circuit

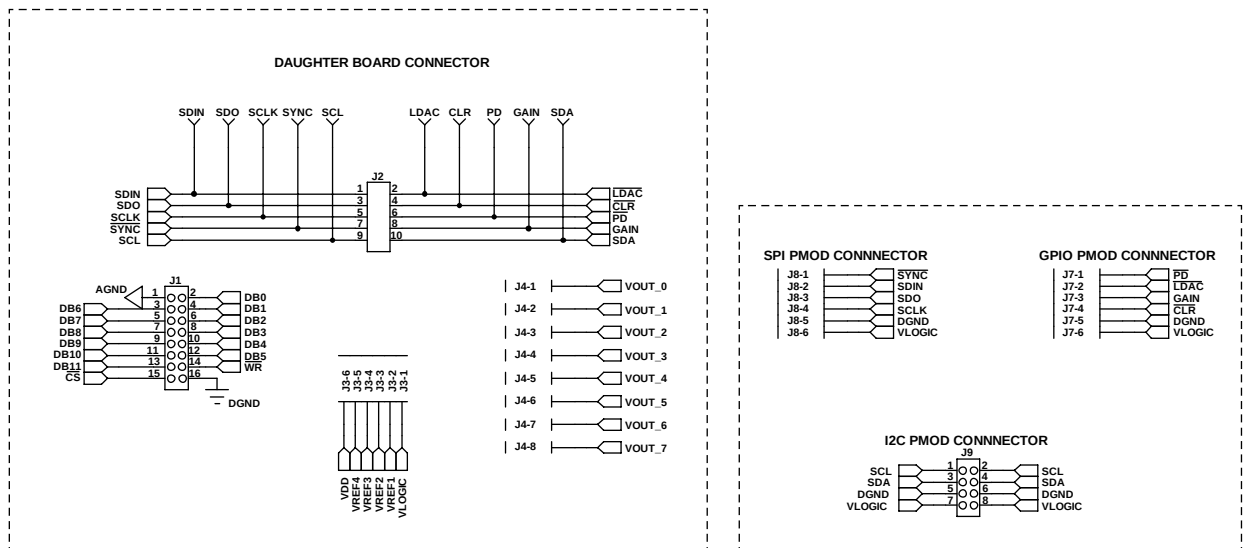


Figure 10. EVAL-MBnanoDAC-SDZ Motherboard Connectors to Daughter Board and Serial Interface

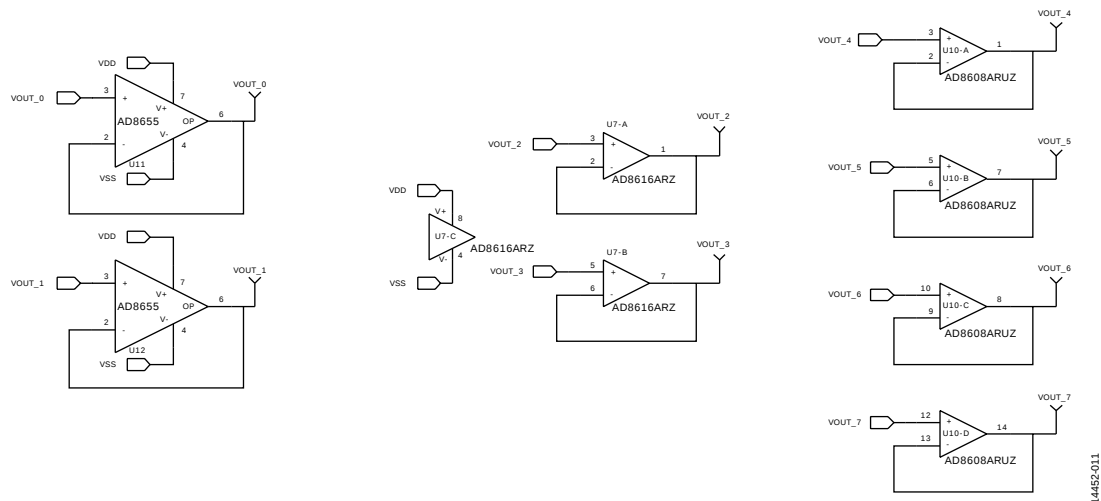


Figure 11. EVAL-MBnanoDAC-SDZ Motherboard Output Amplifier Circuit

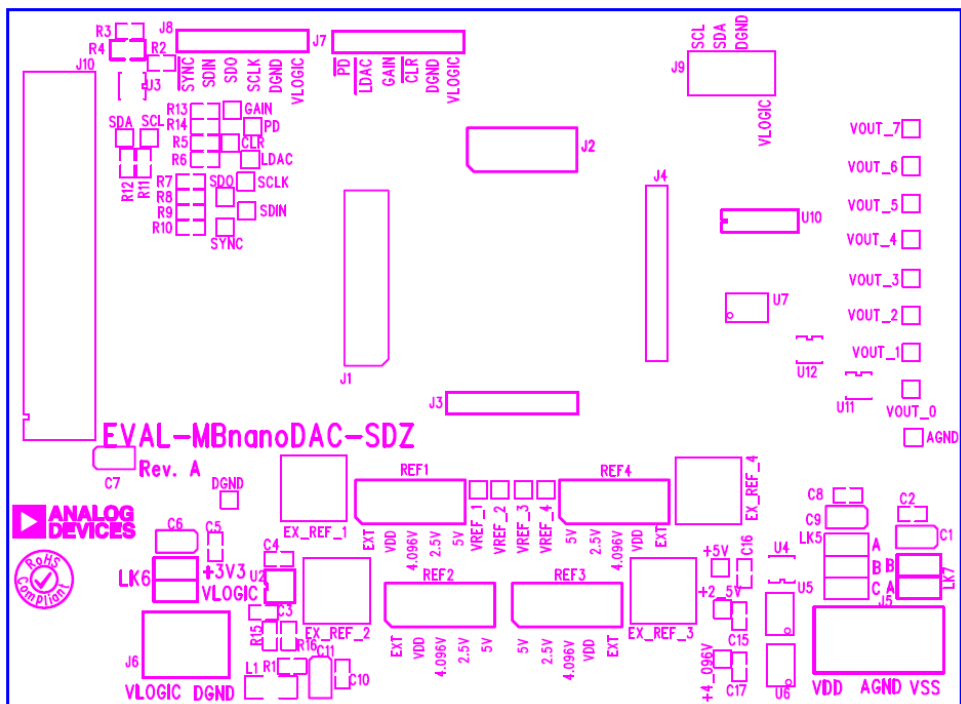


Figure 12. EVAL-MBnanoDAC-SDZ Motherboard Component Placement

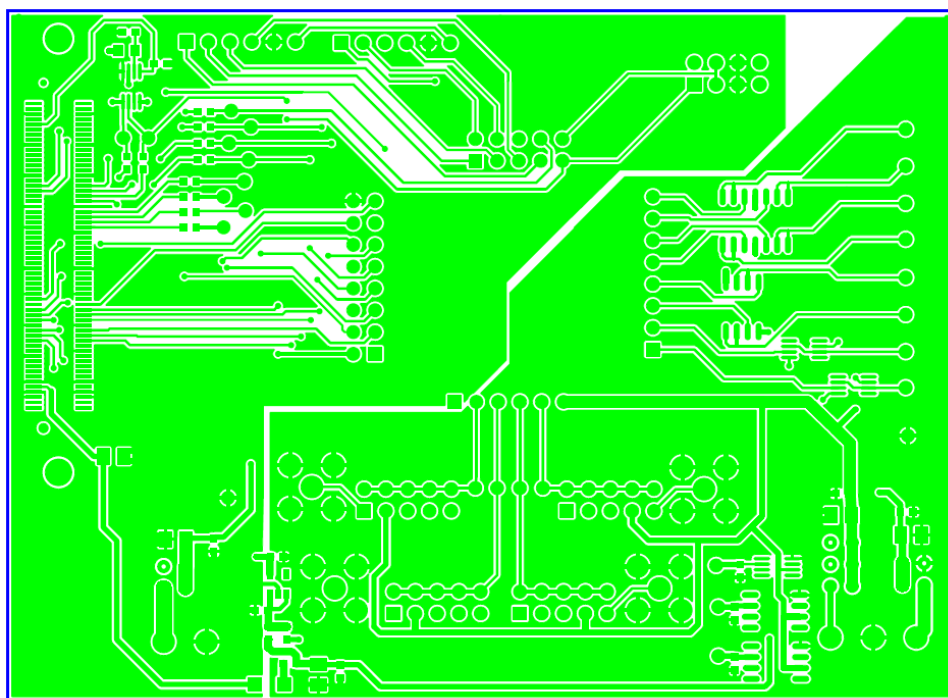
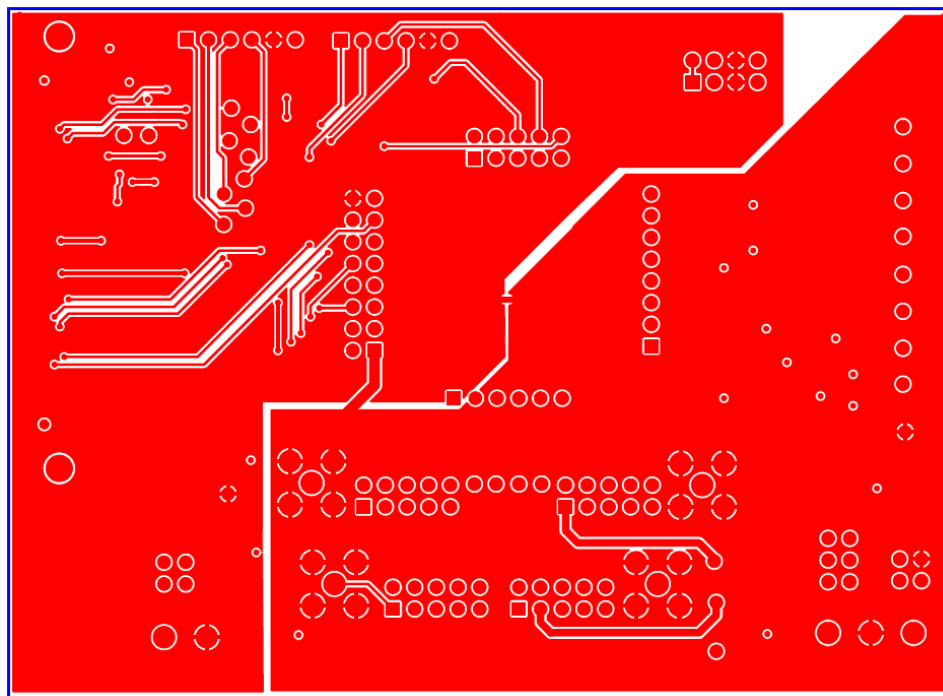
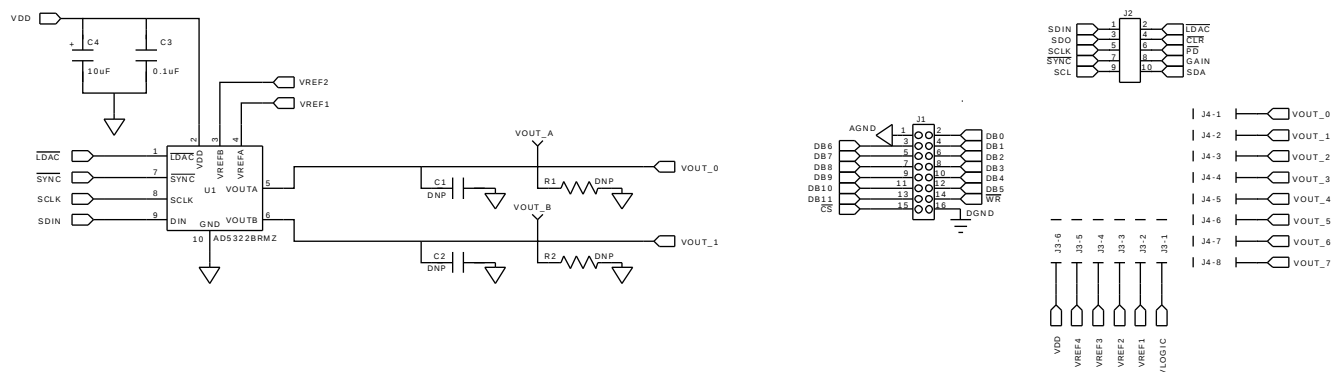


Figure 13. EVAL-MBnanoDAC-SDZ Motherboard Top Side Routing



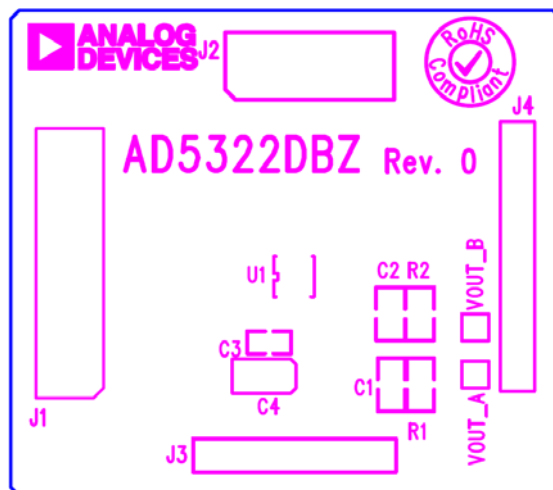
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Figure 14. EVAL-MBnanoDAC-SDZ Motherboard Bottom Side Routing

EVAL-AD5322DBZ DAUGHTER BOARD

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Figure 15. EVAL-AD5322DBZ Daughter Board Schematics



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Figure 16. EVAL-AD5322DBZ Daughter Board Component Placement

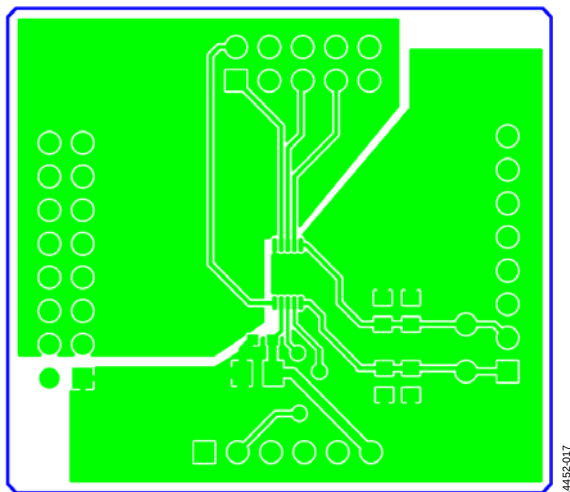


Figure 17. EVAL-AD5322DBZ Daughter Board Top Side Routing

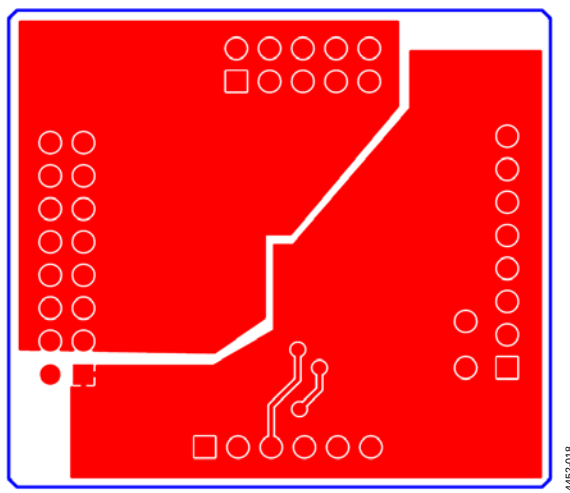


Figure 18. EVAL-AD5322DBZ Daughter Board Bottom Side Routing

ORDERING INFORMATION

BILL OF MATERIALS

Table 4. **EVAL-MBnanoDAC-SDZ** Motherboard

Qty	Reference Designator	Description	Supplier/Part Number ^{1, 2}
4	C1, C6, C7, C9	6.3 V, tantalum capacitor (Case A), 10 μ F, $\pm$ 20%	FEC/1190107
7	C2, C5, C8, C10, C15, C16, C17	50 V, X7R ceramic capacitor, 0.1 μ F, $\pm$ 10%	FEC/1759122
2	C3, C4	10 V, X5R, ceramic capacitor, 1 μ F, $\pm$ 10%	GRM188R61A105KA61D
1	C11	6.3 V, tantalum capacitor (Case A), 4.7 μ F, $\pm$ 20%	FEC/1432350
4	EXT_REF_1 to EXT_REF_4	Straight printed circuit board (PCB) mount SMB jack, 50 Ω	FEC/1206013
1	J1	Header, 2.54 mm, 2 $\times$ 8-way	FEC/2308428
1	J2	Header, 2.54 mm, 2 $\times$ 5-way	FEC/9689583
3	J3, J7, J8	Header, 2.54 mm, 1 $\times$ 6-way	FEC/9689508
1	J4	Header, 2.54 mm, 1 $\times$ 8-way	FEC/1766172
1	J5	3-pin terminal block	FEC/1667472
1	J6	2-pin terminal block	FEC/151789
1	J9	Header, 2.54 mm, 2 $\times$ 4-way	FEC/1667509
1	J10	120-way connector	FEC/1324660
1	L1	Inductor, SMD, 600 Ω	FEC/9526862
1	LK5	6-pin (3 $\times$ 2) 0.1", header and shorting block	FEC/148-535 and 150-411 (36-pin strip)
2	LK6, LK7	4-pin (2 $\times$ 2) 0.1", header and shorting block	FEC/148-535 and 150-411 (36-pin strip)
4	REF1 to REF4	10-pin (5 $\times$ 2) 0.1", header and shorting block	FEC/1022227 and 150-411
1	R1	Resistor, surge, 1.6 Ω , 1%, 0603	FEC/1627674
2	R2, R3	SMD resistor, 100 k Ω , 1%, 0603	FEC/9330402
11	R5 to R15	SMD resistor, 100 Ω , 1%, 0603	FEC/9330364
1	U2	3.3 V linear regulator	Analog Devices/ ADP121-AUJZ33R7
1	U3	32 kb I ² C serial EEPROM	FEC/1331330
1	U4	5 V reference, MSOP	Analog Devices/ ADR445ARMZ
1	U5	Ultralow noise XFET voltage reference	Analog Devices/ ADR431BRZ
1	U6	4.096 V reference	Analog Devices/ REF198ESZ
1	U7	Dual op amp	Analog Devices/ AD8616ARZ
1	U10	Quad op amp	Analog Devices/ AD8608ARMZ
2	U11, U12	Op amp	Analog Devices/ AD8655ARMZ

¹ FEC refers to Farnell Electronic Component Distributors.

² GRM refers to Murata Manufacturing Company.

Table 5. **EVAL-AD5322DBZ** Daughter Board

Qty	Reference Designator	Description	Supplier/Part Number ¹
2	C1, C2	Not applicable	Not inserted
1	C3	50 V, X7R, ceramic capacitor	FEC/1759122
1	C4	6.3 V, tantalum capacitor (Case A)	FEC/1190107
1	J1	16-pin (2 $\times$ 8) header	FEC/2308428 inserted from solder side
1	J2	10-pin (2 $\times$ 5) straight header, 2.54 mm pitch	FEC/9689583 inserted from solder side
1	J3	6-pin (1 $\times$ 6) straight header, 2.54 mm pitch	FEC/9689508 inserted from solder side
1	J4	Header, 2.54 mm, PCB, 1 $\times$ 8-way	FEC/1766172 inserted from solder side
1	R1, R2	Not applicable	Not inserted
1	U1	12-bit DAC	Analog Devices/ AD5322BRMZ
1	VOUT_A	Red test point	FEC/8731144 (pack)
1	VOUT_B	Red test point	FEC/8731144 (pack)

¹ FEC refers to Farnell Electronic Component Distributors.

NOTES

I²C refers to a communications protocol originally developed by Philips Semiconductors (now NXP Semiconductors).

**ESD Caution**

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

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