DS3922

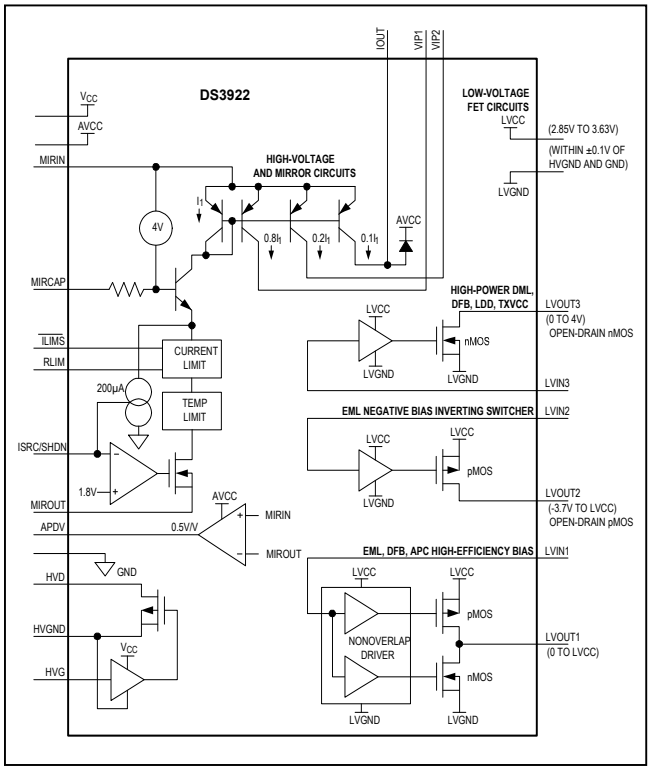
High-Speed Current Mirror and Integrated FETs for DC-DC Controller

General Description

The DS3922 high-speed current mirror integrates high-voltage devices necessary for monitoring the burst mode receive power signal in avalanche photodiode (APD) biasing and OLT applications. The device has two small and one large gain current mirror outputs to monitor the APD current. An adjustable current clamp limits current through the APD. The clamp also features an external shutdown. An integrated FET is also provided that can be used to quickly clamp the high-voltage bias to ground in the case of high optical input power. Integrated low-voltage FET circuits can be used to create buck, boost, and inverting DC-DC converters for efficient laser bias and EML bias applications.

The DS3922 is available in a 24-pin TQFN package and operates over an extended -40°C to +95°C temperature range.

Block Diagram



Benefits and Features

- Accurate Burst-Mode RSSI Measurement with Two Current Mirror Outputs Improves Dynamic Range
  - -32dBm to -5dBm Optical Input Range
  - ±0.5dB Accuracy
  - Sampling Period as Short as 300ns
  - Pin Discharge Option
- Low-Noise APD Bias with Shutdown Options Reduces Receiver Sensitivity
  - 15V to 76V APD Bias
  - External Capacitor Connection for Controlled RC Time Constant of APD Voltage Filter
  - Current Clamp with Adjustable Limit and External Shutdown with Limit Status
  - High-Voltage Switch FET for APD Fast Shutdown
- Supports Additional DC-DC Functions
  - Low-Voltage Synchronous Buck FETs for Efficient DFB Bias
  - Low-Voltage pMOSFET for Generating Negative Bias Voltage for EMLs
- Small Package Reduces Total Solution Size and Cost
  - 3.5mm x 3.5mm, 24-Pin TQFN Package with Exposed Pad

Applications

- Avalanche Photodiode (APD) Monitoring
- GPON OLT
- 10GPON OLT
- EML Bias
- 10G EPON

***Ordering Information* appears at end of data sheet.**

For related parts and recommended products to use with this part, refer to www.maximintegrated.com/DS3922.related.

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Absolute Maximum Ratings

Voltage on HVD, MIRIN, MIRCAP, and MIROUT Relative to HVGND .....-0.3V to +79V
Voltage on MIROUT Relative to HVGND ...-0.3V to (V_{MIRIN} + 0.3V)
Voltage on LVOUT1 Relative to LVGND .....-0.3V to (V_{LVCC} + 0.3V)
Voltage on LVOUT2 Relative to LVGND ..-4V to (V_{LVCC} + 0.3V)
Voltage on LVOUT3 Relative to LVGND .....-0.3V to +5V
Voltage on LVCC Relative to V_{CC}.....±0.1V
Voltage on All Other Pins Relative to GND .....-0.3V to (V_{CC} + 0.3V) not to exceed +4V
Continuous Power Dissipation (T_A = +70°C)
TQFN (derate 15.4mW/°C above +70°C).....1228.9mW
Storage Temperature Range..... -55°C to +135°C
Lead Temperature (soldering, 10s) .....+300°C
Soldering Temperature, Lead(Pb)-Free Reflow .....+260°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Package Thermal Characteristics (Note 1)

TQFN
Junction-to-Ambient Thermal Resistance (θ_{JA}) .....5.4°C/W
Junction-to-Case Thermal Resistance (θ_{JC}).....65.1°C/W

Note 1: Package thermal resistances were obtained using the method described in JEDEC specification JESD51-7, using a four-layer board. For detailed information on package thermal considerations, refer to **www.maximintegrated.com/thermal-tutorial.**

Electrical Characteristics

(V_{MIRIN} = 15V to 76V, V_{CC} = 2.85V to 3.63V, T_A = -40°C to +95°C, unless otherwise noted.) (Note 2)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Low-Voltage Supply	V_{CC}			2.85		3.63	V
Low-Voltage Current	I_{CC}	(Note 3)			1.5	3.0	mA
MIRIN Quiescent Current	I_{MIRIN}	V_{MIRIN} = 60V, ISRC/SHDN = 30kΩ to GND	I_{MIROUT} = 0µA		1	2	mA
			I_{MIROUT} = 1mA		3.2	4.5	
MIRIN Voltage	V_{MIRIN}			15		76	V
HV FET Turn-On Time	$t_{ON:HV}$	V_{DHV} falling from 90% to 10% of peak voltage			30		ns
HV FET On-Resistance	R_{DSONHV}	V_{GS} = 3.0V, I_D = 170mA			0.85	2	Ω
HVG Voltage	V_{GSHV}			0		V_{CC} + 0.3	V
HVD Voltage	V_{DHV}					76	V
HVD Leakage	I_{ILHV}			-1		+1	µA
Logic Input Thresholds: HVG, LVIN1, LVIN2, LVIN3	V_{IL}					0.25 x V_{CC}	V
	V_{IH}			0.65 x V_{CC}			
ISRC/SHDN Threshold	$V_{IL\ SHDN}$	Note: Compatible with 2.5V and 3.3V CMOS logic levels				1.4	V
	$V_{IH\ SHDN}$			V_{CC} - 0.2			
ISRC/SHDN Resistor	R_{ISRC}	(Note 4)		29.7	30	30.3	kΩ

Electrical Characteristics (continued)

(V_{MIRIN} = 15V to 76V, V_{CC} = 2.85V to 3.63V, T_A = -40°C to +95°C, unless otherwise noted.) (Note 2)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Maximum MIROUT Current	I_{CLAMP}	ISRC/SHDN = low	R_{LIM} = 40kΩ	1.37	2.1	3.21	mA
			R_{LIM} = 25kΩ	2.55	3.3	4.45	
		ISRC/SHDN = high				0.01	
MIROUT Capacitive Load	C_{MIROUT}	Total capacitance on MIROUT to achieve accuracy specification		330		500	pF
Logic Output Levels: $\overline{ILIMS}$	V_{OH}	$I_{\overline{ILIMS}}$ = +2mA		V_{CC} - 0.4			V
	V_{OL}	$I_{\overline{ILIMS}}$ = -2mA				0.4	
$\overline{ILIMS}$ Output Time	$t_{\overline{ILMS}}$	(Note 5)			1		µs
IOUT-to-MIROUT Ratio	K_{IOUT}	I_{MIROUT} = 1mA		0.090	0.100	0.110	A/A
VIP1-to-MIROUT Ratio	K_{VIP1}	I_{MIROUT} = 1mA		0.720	0.800	0.880	A/A
VIP2-to-MIROUT Ratio	K_{VIP2}	I_{MIROUT} = 1mA		0.180	0.200	0.220	A/A
K_{IOUT}, K_{VIP1}, and K_{VIP2} Voltage Variation	K_{VAR}	V_{MIRIN} = 40V ±10%			±0.3	±2.5	%
Mirror Voltage-Drop Monitor Load Capacitance	$V_{APDV:CAP}$	External capacitance required on APDV		50		250	pF
Mirror Voltage-Drop Monitor Output Voltage Variance	$V_{APDV:VAR}$	V_{MIRIN} = 40V ±10%		-1%		+1%	V
Mirror Voltage Drop	V_{MIRIN} - V_{MIROUT}	Current limit not exceeded, V_{SHDN} = 0V, I_{MIRIN} = 1mA			4		V
Mirror Voltage Drop vs. Current Change	(V_{MIROUT} 10µA - V_{MIROUT} 2.5mA)				40	110	mV
Shutdown Temperature	T_{SHDN}				150		°C
Hysteresis Temperature	T_{HYS}				20		°C
VIP1 Offset Current	$I_{VIP1OFF}$	R_{ISRC} = 30kΩ			20	40	µA
VIP2 Offset Current	$I_{VIP2OFF}$	R_{ISRC} = 30kΩ			19	30	µA
IOUT Offset Current	I_{OUTOFF}	R_{ISRC} = 30kΩ			18	25	µA

Low-Voltage FET Parameters

(V_{LVCC} = 2.85V to 3.63V, T_A = -40°C to +95°C, unless otherwise noted.) (Note 2)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
LVFET1P On-Resistance	$LV1P_{ON}$	V_{LVCC} = 3.3V		1		Ω
LVFET1N On-Resistance	$LV1N_{ON}$	V_{LVCC} = 3.3V		1		Ω
LVFET2P On-Resistance	$LV2P_{ON}$	V_{LVCC} = 3.3V		1.5		Ω
LVFET3N On-Resistance	$LV3N_{ON}$	V_{LVCC} = 3.3V		1		Ω
LVOUT1 Voltage	LVOUT1			LVGND to V_{LVCC}		V
LVOUT2 Voltage	LVOUT2			-3.7 to V_{LVCC}		V
LVOUT3 Voltage	LVOUT3			LVGND to +4		V

Note 2: Limits are 100% tested at T_A = +25°C. Limits over the operating temperature range and relevant supply voltage rating are guaranteed by design and characterization.

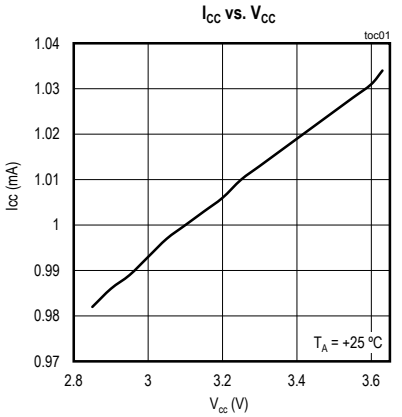
Note 3: ISRC/SHDN: Not connected. HV FET: 250kHz driven by 100Ω source with 2.97V square wave. HVD connected to GND.

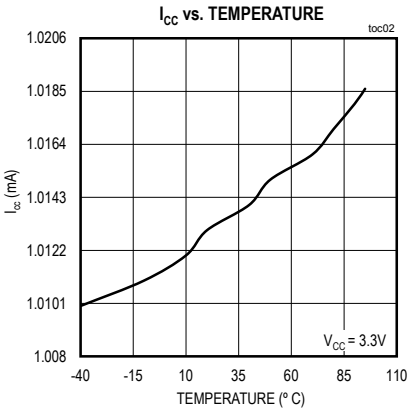
Note 4: External resistor connected to GND. This value guarantees accuracy of the DS3922.

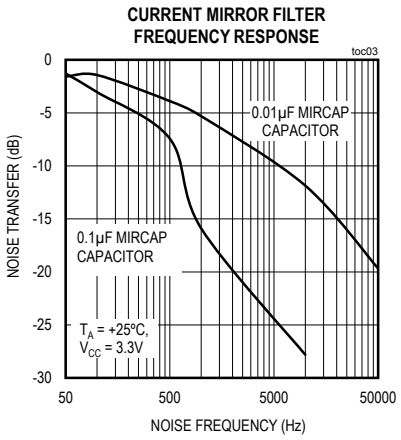
Note 5: Resistor connected to RLIM for 1mA clamp limit. I_{MIROUT} step from 10µA to 10mA. Time measured from I_{MIROUT} step to I_{MIROUT} < 1.1mA. See the *Typical Application Circuit*: C11 = 47pF, C1 = C2 = 0.1µF, V_{C1} = 30V; R1 = 100Ω.

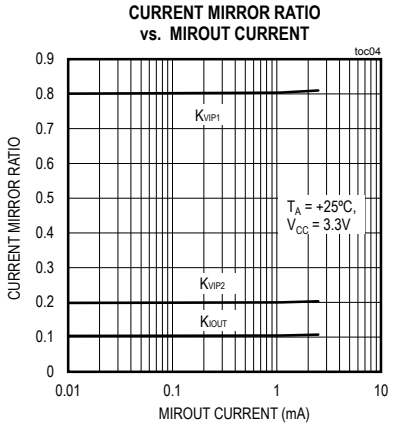
Typical Operating Characteristics

(T_A = +25°C, unless otherwise noted.)

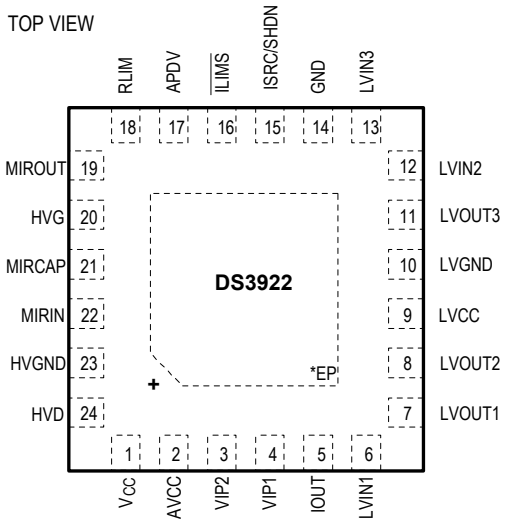








Pin Configuration



TQFN
(3.5mm x 3.5mm x 0.8mm)

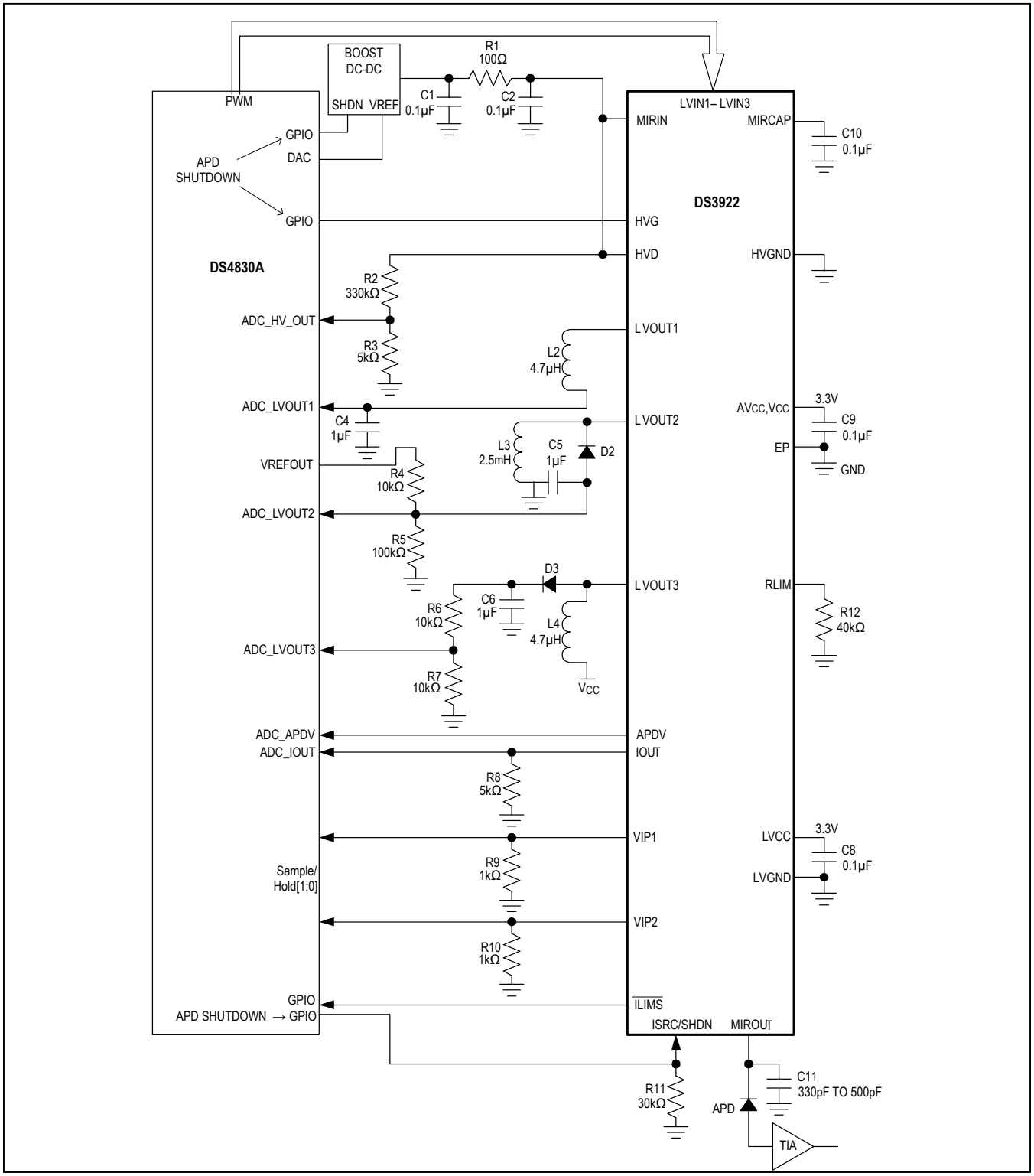
Pin Description

PIN	NAME	FUNCTION
1	V_{CC}	Digital 3.3V (Nominal) Supply
2	AVCC	Analog 3.3V (Nominal) Supply
3	VIP2	20% Current Mirror Output. Connect to resistor to ground.
4	VIP1	80% Current Mirror Output. Connect to resistor to ground.
5	IOUT	10% Current Mirror Output. If not used, do not connect.
6	LVIN1	Digital Input. Connect to an external PWM output to create buck DC-DC converter. Controls output LVOUT1.
7	LVOUT1	Push-Pull Output
8	LVOUT2	Open-Drain pMOS Output. This output does not have a diode connection to LVGND and can go a few volts below LVGND for inverter application.
9	LVCC	Low-Voltage Supply Voltage
10	LVGND	Low-Voltage Ground
11	LVOUT3	Open-Drain nMOS Output
12	LVIN2	Digital Input. Connect to an external PWM output to create buck or inverting DC-DC converter. Controls output LVOUT2.
13	LVIN3	Digital Input. Connect to an external PWM output to boost DC-DC converter. Controls output LVOUT3.
14	GND	Ground

Pin Description (continued)

PIN	NAME	FUNCTION
15	ISRC/SHDN	Dual-purpose pin: ISRC: A resistor connected to this pin controls the amount of current flowing through a current source connected to MIROUT. **Note:** During this mode of operation, the microcontroller pin (if connected) should be high impedance. SHDN: If pulled high, sets MIROUT to high impedance.
16	$\overline{\text{ILIMS}}$	Current-Limit Status. Active-low signal indicating that the current-limit threshold is exceeded.
17	APDV	APD Voltage Monitor. Provides output voltage used to calculate the voltage on the APD.
18	RLIM	Resistor Limit. Connect resistor between RLIM and GND to set the current clamp limit.
19	MIROUT	Current Mirror Output. Connect to the APD.
20	HVG	High-Voltage nMOS FET Gate. Connect to ground if not used.
21	MIRCAP	Mirror Filter. Connect external capacitor to filter voltage at MIROUT.
22	MIRIN	Current Mirror Input. Connect to high-voltage supply.
23	HVGND	High-Voltage nMOS FET Source
24	HVD	High-Voltage nMOS FET Drain. Connect to HVGND if not used.
—	EP	Exposed Pad. Connect to ground with a minimum of nine vias for thermal conductivity improvement. It is acceptable to use a solder mask between the IC and the ground pad. However, using a solder mask between the IC and the ground pad may cause thermal conductivity issue. It is not necessary to electrically connect the exposed pad to ground.

Typical Application Circuit



Detailed Description

The DS3922 contains high-voltage (HV) components required to monitor the APD bias current. The device's mirror outputs are a current that is a precise ratio of the output current across a large dynamic range. The mirror response time is fast enough to comply with GPON Rx burst-mode monitoring requirements. The device has a built-in current-limiting feature to protect APDs. This current limit is adjustable using an external resistor. The APD current can also be shut down by ISRC/SHDN or thermal shutdown. The internal HV FET may be used as a fast APD shutdown. Low-voltage FETs can be used to create various DC-DC converters.

Current Mirrors

The device includes three current mirrors, as shown in Figure 1. One is a 10:1 (10%) mirror connected at IOUT. The other two are a 1.25:1 (80%) and the 5:1 (20%) mirror connected to VIP1 and VIP2. On pins VIP1 and VIP2, resistors to ground should be selected such that the maximum voltage should be below the external ADC full scale. For example, if the maximum monitored current through the APD is 1mA, the mirror is 1.25:1 ratio, and then the correct resistor is approximately 780Ω for the external ADC having full scale of 0.625V.

Current Mirror Filter

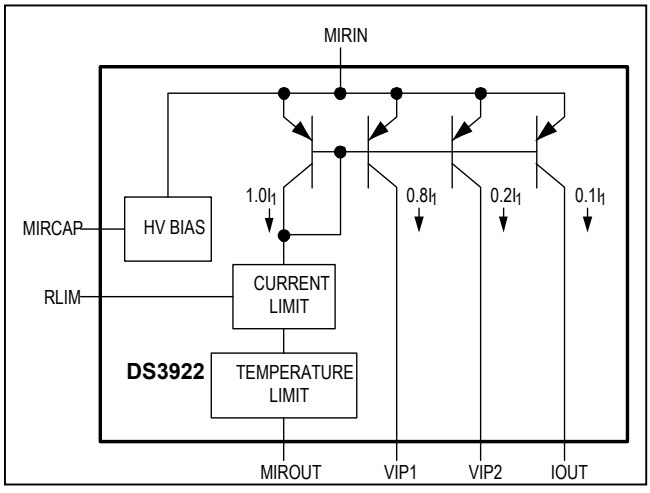


Figure 1. Current Mirrors

The device includes a filter to stabilize the MIROUT voltage. An external capacitor must be connected to the MIRCAP pin.

Current Source for Mirror Bias

The current mirror response time is improved by providing a continuous current source. This source is adjustable by changing the resistor connected to the ISRC/SHDN pin. However, only one value is allowed to guarantee performance (see the *Electrical Characteristics* section):

$$ISRC = (6/R_{ISRC}) \pm 6\%$$

Current Mirror Voltage-Drop Monitor

The device includes a voltage monitor that indicates the voltage drop across the current mirror. This signal is output on APDV. This signal should be used to accurately maintain the correct APD bias voltage in conjunction with the feedback resistors for the APD bias boost converter:

$$APDV = (V_{MIRIN} - V_{MIROUT})/2$$

Current Clamp

The device has a current-clamping circuit to protect the APD by limiting the amount of current from MIROUT. The current limit is defined by a resistor connected between RLIM and ground. A larger R_{LIM} results in a lower current clamp limit (see the *Electrical Characteristics* table).

Shutdown

The MIROUT output can be set to a high-impedance state using the ISRC/SHDN pin, effectively disabling the APD. The ISRC/SHDN pin is active high.

Low-Voltage FETs

These FETs can be used to create DC-DC converters for EML bias, high-efficiency DFB bias, and other possible applications.

High-Voltage Switching FET

An HV switching FET is included to optionally be used to quickly turn off the bias voltage to the APD. The strong HV FET can quickly discharge the capacitance on the MIRIN pin..

Applications Information

Layout Considerations

Proper PCB layout helps to reduce switching noise in the system. Keeping all PCB traces as short as possible reduces radiated noise, stray capacitance, and trace resistance.

Ordering Information

PART	TEMP RANGE	PIN-PACKAGE
DS3922T+	-40°C to +95°C	24 TQFN-EP**
DS3922T+T*	-40°C to +95°C	24 TQFN-EP**

+Denotes a lead(Pb)-free/RoHS-compliant package.
**Second T denotes tape and reel. First T denotes package type.*
***EP = Exposed pad.*

Package Information

For the latest package outline information and land patterns (footprints), go to **www.maximintegrated.com/packages**. Note that a "+", "#", or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

PACKAGE TYPE	PACKAGE CODE	OUTLINE NO.	LAND PATTERN NO.
24 TQFN-EP	T243A3+1	**21-0188**	**90-0122**

Revision History

REVISION NUMBER	REVISION DATE	DESCRIPTION	PAGES CHANGED
0	5/14	Initial release	—
1	3/15	Revised recommended usage of HV FET. Revised *General Description*, *Features*, *Applications*, *Pin Description*, *Detailed Description*, and *Typical Application Circuit*. Updated *Benefits and Features* section.	1, 7–10

For pricing, delivery, and ordering information, please contact Maxim Direct at 1-888-629-4642, or visit Maxim Integrated's website at www.maximintegrated.com.

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