Rev 2; 11/09

1Kb I²C/SMBus EEPROM with SHA-1 Engine

General Description

The DS28CN01 combines 1024 bits of EEPROM with challenge-and-response authentication security implemented with the Federal Information Publications (FIPS) 180-1/180-2 and ISO/IEC 10118-3 Secure Hash Algorithm (SHA-1). The memory is organized as four 32-byte pages. Data copy protection and EPROM emulation features are supported for each memory page. Each DS28CN01 has a guaranteed unique factory-programmed 64-bit registration number. Communication with the DS28CN01 is accomplished through an industry-standard I²C-compatible and SMBus™-compatible interface. The SMBus timeout feature resets the device's interface if a bus-timeout fault condition is detected.

Applications

PCB Unique Serialization

Accessory and Peripheral Identification

Equipment Registration and License Management

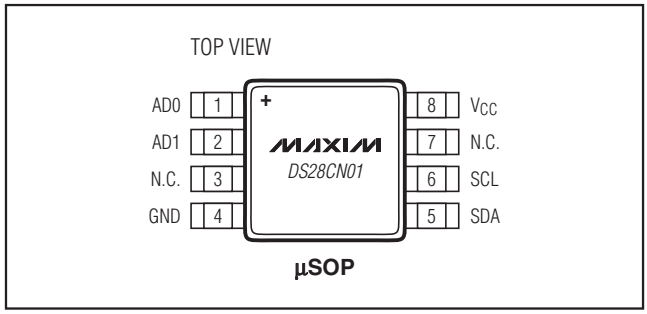
Network Node Identification

Printer Cartridge Configuration and Monitoring

Medical Sensor Authentication and Calibration

System Intellectual Property Protection

Pin Configuration



µSOP

Features

- **1024 Bits of EEPROM Memory Partitioned Into Four Pages of 256 Bits**
- **Dedicated Hardware-Accelerated SHA-1 Engine for Generating SHA-1 MACs**
- **EEPROM Memory Pages Can Be Individually Copy Protected or Put Into EPROM Mode (Program from 1 to 0 Only)**
- **Write Access Requires Knowledge of the Secret and the Capability of Computing and Transmitting a 160-Bit MAC as Authorization**
- **Unique, Factory-Programmed, and Tested 64-Bit Registration Number Assures Absolute Traceability Because No Two Parts are Alike**
- **Endurance 200,000 Cycles at +25°C**
- **Serial Interface User Programmable for I²C Bus and SMBus Compatibility**
- **Supports 100kHz and 400kHz I²C Communication Speeds**
- **+5.5V Tolerant Interface Pins**
- **Operating Ranges: +1.62V to +5.5V, -40°C to +85°C**
- **8-Pin µSOP Package**

Ordering Information

PART	TEMP RANGE	PIN-PACKAGE
DS28CN01U-A00+	-40°C to +85°C	8 µSOP
DS28CN01U-A00+T	-40°C to +85°C	8 µSOP

+Denotes a lead(Pb)-free/RoHS-compliant package.
T = Tape and reel.

Typical Operating Circuit appears at end of data sheet.

SMBus is a trademark of Intel Corp.

For pricing, delivery, and ordering information, please contact Maxim Direct at 1-888-629-4642, or visit Maxim's website at www.maxim-ic.com.

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ABSOLUTE MAXIMUM RATINGS

Voltage Range on Any Pin Relative to Ground.....-0.5V to +6V
Maximum Current on Any Pin.....±20mA
Operating Temperature Range .....-40°C to +85°C
Junction Temperature.....+150°C
Storage Temperature Range .....-55°C to +125°C
Soldering Temperature.....Refer to the IPC/JEDEC J-STD-020 Specification.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(T_A = -40°C to +85°C.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Supply Voltage	V_{CC}		1.62		5.50	V
Standby Current	I_{CCS}	Bus idle, V_{CC} = +5.5V			5.5	µA
Operating Current	I_{CCA}	Bus active at 400kHz, V_{CC} = +5.5V			500	µA
Power-Up Wait Time	t_{POIP}	(Note 2)			5	µs
EEPROM						
Programming Time	t_{PROG}	$V_{CC} \geq 2.0V$			10	ms
		$V_{CC} < 2.0V$			45	
Programming Current	I_{PROG}	V_{CC} = +5.5V			1.2	mA
Endurance (Notes 3, 4, 5)	N_{CY}	At +25°C	200,000			—
		At +85°C	50,000			
Data Retention (Notes 6, 7, 8)	t_{DR}	At +85°C	40			Years
SHA-1 ENGINE						
SHA-1 Computation Time	t_{CSHA}	See full version of the data sheet.				ms
SHA-1 Computation Current	I_{LCSHA}	See full version of the data sheet.				mA
SCL, SDA, AD1, AD0 PINS (Notes 9, 10)						
Low-Level Input Voltage	V_{IL}	$V_{CC} \geq 2.0V$	-0.3		0.3 × V_{CC}	V
		$V_{CC} < 2.0V$	-0.3		0.25 × V_{CC}	
High-Level Input Voltage	V_{IH}	$V_{CC} \geq 2.0V$	0.7 × V_{CC}		V_{CCMAX} + 0.3V	V
		$V_{CC} < 2.0V$	0.8 × V_{CC}		V_{CCMAX} + 0.3V	
Hysteresis of Schmitt Trigger Inputs (Note 2)	V_{HYS}	$V_{CC} \geq 2.0V$	0.05 × V_{CC}			V
		$V_{CC} < 2.0V$	0.1 × V_{CC}			
Low-Level Output Voltage at 4mA Sink Current, Open Drain	V_{OL}	$V_{CC} \geq 2.0V$			0.4	V
		$V_{CC} < 2.0V$			0.2 × V_{CC}	

ELECTRICAL CHARACTERISTICS (continued)

(T_A = -40°C to +85°C.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Output Fall Time from $V_{IH(MIN)}$ to $V_{IL(MAX)}$ with a Bus Capacitance from 10pF to 400pF (Notes 2, 11)	t_{OF}	$V_{CC} \geq 2.0V$	20 + 0.1C_B		250	ns
		$V_{CC} < 2.0V$	20 + 0.1C_B		300	
Pulse Width of Spikes that are Suppressed by the Input Filter	t_{SP}	(Note 2)			50	ns
Input Current with an Input Voltage Between 0.1V_{CC} and 0.9V_{CCMAX}	I_I	(Note 12)	-10		+10	µA
Input Capacitance	C_I	(Note 2)			10	pF
SCL Clock Frequency	f_{SCL}	(Note 13)			400	kHz
Bus Timeout	$t_{TIMEOUT}$	CM bit = 1 (Note 13)	25		75	ms
Hold-Time (Repeated) START Condition; After this Period, the First Clock Pulse is Generated	$t_{HD:STA}$	(Note 14)	0.6			µs
Low Period of the SCL Clock (Note 14)	t_{LOW}	$V_{CC} \geq 2.7V$	1.3			µs
		$V_{CC} \geq 2.0V$	1.5			
		$V_{CC} < 2.0V$	1.9			
High Period of the SCL Clock	t_{HIGH}	(Note 14)	0.6			µs
Setup Time for a Repeated START Condition	$t_{SU:STA}$	(Note 14)	0.6			µs
Data Hold Time (Notes 15, 16)	$t_{HD:DAT}$	$V_{CC} \geq 2.7V$	0.3		0.9	µs
		$V_{CC} \geq 2.0V$	0.3		1.1	
		$V_{CC} < 2.0V$	0.3		1.5	
Data Setup Time	$t_{SU:DAT}$	(Notes 2, 14, 17)	100			ns
Setup Time for STOP Condition	$t_{SU:STO}$	(Note 14)	0.6			µs
Bus Free Time Between a STOP and START Condition	t_{BUF}	(Note 14)	1.3			µs
Capacitive Load for Each Bus Line	C_B	(Notes 2, 14)			400	pF

Note 1: Specifications at -40°C are guaranteed by design and characterization only and not production tested.
Note 2: Guaranteed by design, characterization, and/or simulation only and not production tested.
Note 3: This specification is valid for each 8-byte memory row.
Note 4: Write-cycle endurance is degraded as T_A increases.
Note 5: Not 100% production tested; guaranteed by reliability monitor sampling.
Note 6: Data retention is degraded as T_A increases.
Note 7: Guaranteed by 100% production test at elevated temperature for a shorter time; equivalence of this production test to data sheet limit at operating temperature range is established by reliability testing.
Note 8: EEPROM writes can become nonfunctional after the data retention time is exceeded. Long-time storage at elevated temperatures is not recommended; the device can lose its write capability after 10 years at +125°C or 40 years at +85°C.
Note 9: All values are referred to $V_{IH(MIN)}$ and $V_{IL(MAX)}$ levels.
Note 10: See Figure 3.
Note 11: C_B = Total capacitance of one bus line in pF. If mixed with high-speed-mode devices, faster fall times according to I²C Bus Specification v2.1 are allowed.

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ELECTRICAL CHARACTERISTICS (continued)

(T_A = -40°C to +85°C.) (Note 1)

Note 12: The DS28CN01 does not obstruct the SDA and SCL lines if V_{CC} is switched off.

Note 13: The minimum SCL clock frequency is limited by the bus timeout feature. If the CM bit is 1 *and* SCL stays at the same logic level or SDA stays low for this interval, the DS28CN01 behaves as though it has sensed a STOP condition.

Note 14: System requirement.

Note 15: The DS28CN01 provides a hold time of at least 300ns for the SDA signal (referred to the $V_{IH(MIN)}$ of the SCL signal) to bridge the undefined region of the falling edge of SCL.

Note 16: The master can provide a hold time of 0ns minimum when writing to the device. This 0ns minimum is guaranteed by design, characterization, and/or simulation only, and not production tested.

Note 17: A fast-mode I²C bus device can be used in a standard-mode I²C bus system, but the requirement $t_{SU:DAT} \geq 250ns$ must then be met. This is automatically the case if the device does not stretch the low period of the SCL signal. If such a device does stretch the low period of the SCL signal, it must output the next data bit to the SDA line $t_{RMAX} + t_{SU:DAT} = 1000 + 250 = 1250ns$ (according to the standard-mode I²C bus specification) before the SCL line is released.

Pin Description

PIN	NAME	FUNCTION
1	AD0	Device Address Input Pin to Select the Slave Address. Sets slave address bits A[1:0] and must be connected to either GND, SDA, SCL, or V_{CC}.
2	AD1	Device Address Input Pin to Select the Slave Address. Sets slave address bits A[3:2] and must be connected to either GND, SDA, SCL, or V_{CC}.
3, 7	N.C.	No Connection
4	GND	Ground Supply
5	SDA	I²C/SMBus Bidirectional Serial Data Line. This pin must be connected to V_{CC} through a pullup resistor.
6	SCL	I²C/SMBus Serial Clock Input. This pin must be connected to V_{CC} through a pullup resistor.
8	V_{CC}	Power-Supply Input

Detailed Description

The DS28CN01 features a serial I²C/SMBus interface, 1Kb of SHA-1 secure EEPROM, a register page, and a unique registration number, as shown in the *Block Diagram*. The device communicates with a host processor through its I²C interface in standard mode or in fast mode. The user can switch the interface from I²C bus mode to SMBus mode. Two 4-level address pins allow 16 DS28CN01s to reside on the same bus segment.

Device Operation

Read and write access to the DS28CN01 is controlled through the I²C/SMBus serial interface. Since the DS28CN01 has memory areas and registers of different characteristics, there are several special cases to consider. See the *Read and Write* section in the full data sheet for details.

Serial Communication Interface

The serial interface uses a data line (SDA) plus a clock signal (SCL) for communication. Both SDA and SCL are bidirectional lines, connected to a positive supply voltage through a pullup resistor. When there is no communication, both lines are high. The output stages of devices connected to the bus must have an open-drain or open-collector output to perform the wired-AND function. Data can be transferred at rates of up to 100kbps in the standard mode, and up to 400kbps in the fast mode. The DS28CN01 works in both modes.

A device that sends data on the bus is defined as a transmitter and a device receiving data is a receiver. The device that controls the communication is called a master. The devices that are controlled by the master are slaves. The DS28CN01 is a slave device.

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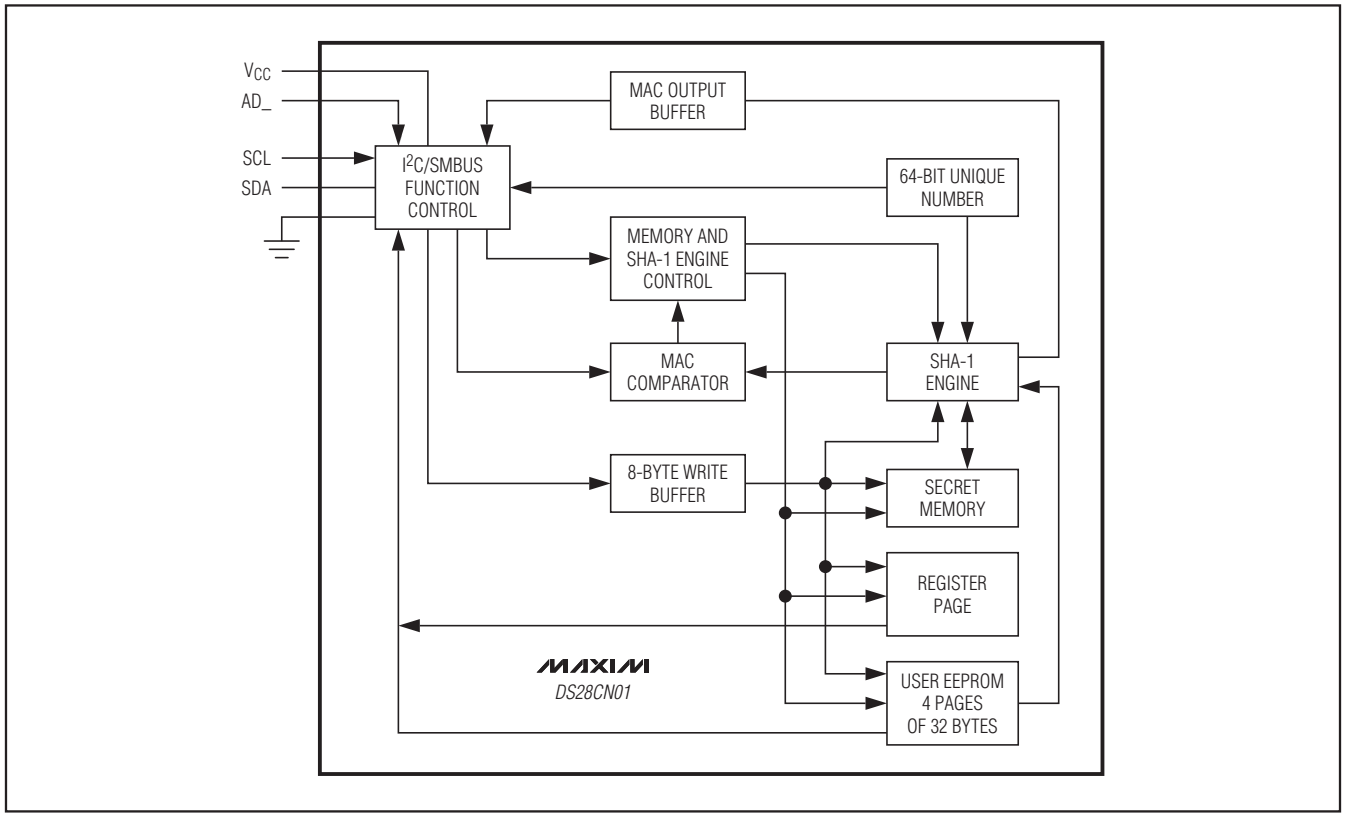
Block Diagram



Slave Address/Direction Byte

To be individually accessed, each device must have a slave address that does not conflict with other devices on the bus. The slave address to which the DS28CN01 responds is shown in Figure 1. The slave address is part of the slave-address/direction byte. The upper 3 bits of the DS28CN01 slave address are set to 101b. The AD0 pin controls address A0 and A1; AD1 controls A2 and A3. AD0 and AD1 can be connected to GND, V_{CC}, SCL, or SDA. Table 1 shows the translation of these four pin states to binary addresses. To be selected, the device must be addressed with A0 to A3 matching the binary address of the respective pins.

The last bit of the slave-address/direction byte (R/$\overline{W}$) defines the data direction. When set to a 0, subsequent data flows from master to slave (write-access mode); when set to a 1, data flows from slave to master (read-access mode).

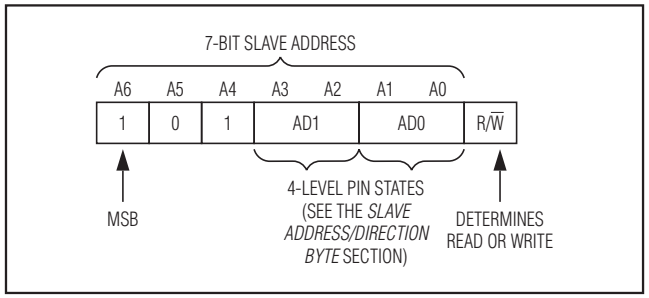


Figure 1. Slave Address

Table 1. Pin State to Binary Translation

AD1	A3	A2
GND	0	0
V_{CC}	0	1
SCL	1	0
SDA	1	1

AD0	A1	A0
GND	0	0
V_{CC}	0	1
SCL	1	0
SDA	1	1

1Kb I²C/SMBus EEPROM with SHA-1 Engine

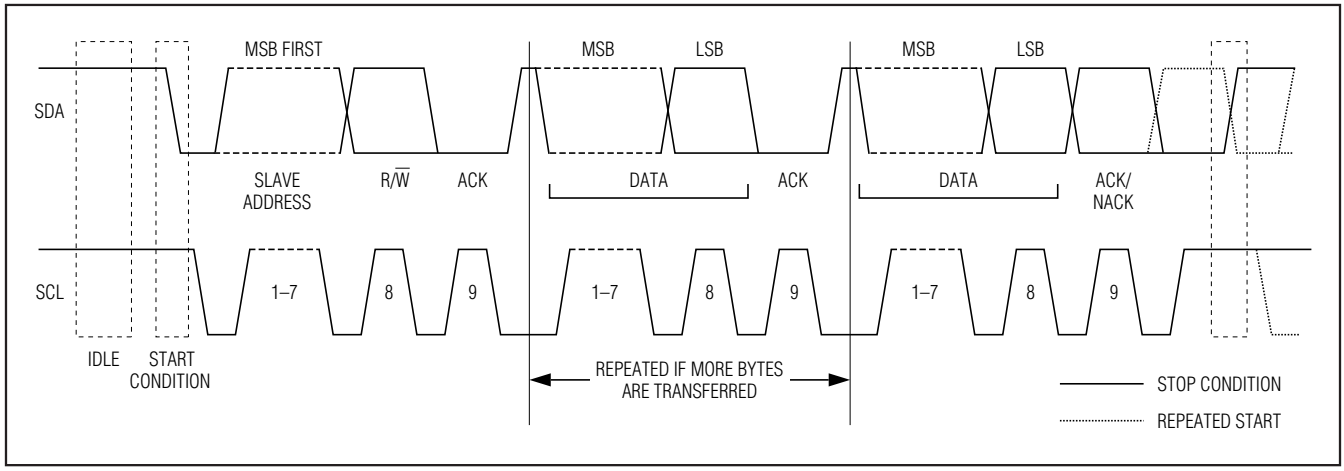


Figure 2. I²C/SMBus Protocol Overview

I²C/SMBus Protocol

Data transfers can be initiated only when the bus is not busy. The master generates the SCL, controls the bus access, generates the START and STOP conditions, and determines the number of bytes transferred on the SDA line between START and STOP. Data is transferred in bytes with the most significant bit being transmitted first. After each byte, an acknowledge bit follows to allow synchronization between master and slave. During any data transfer, SDA must remain stable whenever the clock line is high. Changes in the SDA line while SCL is high are interpreted as a START or a STOP. The protocol is illustrated in Figure 2. See Figure 3 for detailed timing references.

Bus Idle or Not Busy

Both SDA and SCL are inactive, i.e., in their logic-high states.

START Condition

To initiate communication with a slave, the master must generate a START condition. A START condition is defined as a change in state of SDA from high to low while SCL remains high.

STOP Condition

To end communication with a slave the master must generate a STOP condition. A STOP condition is defined as a change in state of SDA from low to high while SCL remains high.

Repeated START Condition

Repeated STARTs are commonly used for read accesses after having specified a memory address to read from in a preceding write access. The master can use a repeated START condition at the end of a data transfer to immediately initiate a new data transfer following the current one. A repeated START condition is generated the same way as a normal START condition, but without a preceding STOP condition.

Data Valid

With the exception of the START and STOP condition, transitions of SDA can occur only during the low state of SCL. The data on SDA must remain valid and unchanged during the entire high pulse of SCL plus the required setup and hold time ($t_{HD:DAT}$ after the falling edge of SCL and $t_{SU:DAT}$ before the rising edge of SCL; see Figure 3). There is one clock pulse per bit of data. Data is shifted into the receiving device during the rising edge of the SCL pulse.

When finished with writing, the master must release the SDA line for a sufficient amount of setup time (minimum $t_{SU:DAT} + t_R$ in Figure 3) before the next rising edge of SCL to start reading. The slave shifts out each data bit on SDA at the falling edge of the previous SCL pulse and the data bit is valid at the rising edge of the current SCL pulse. The master generates all SCL clock pulses, including those needed to read from a slave.

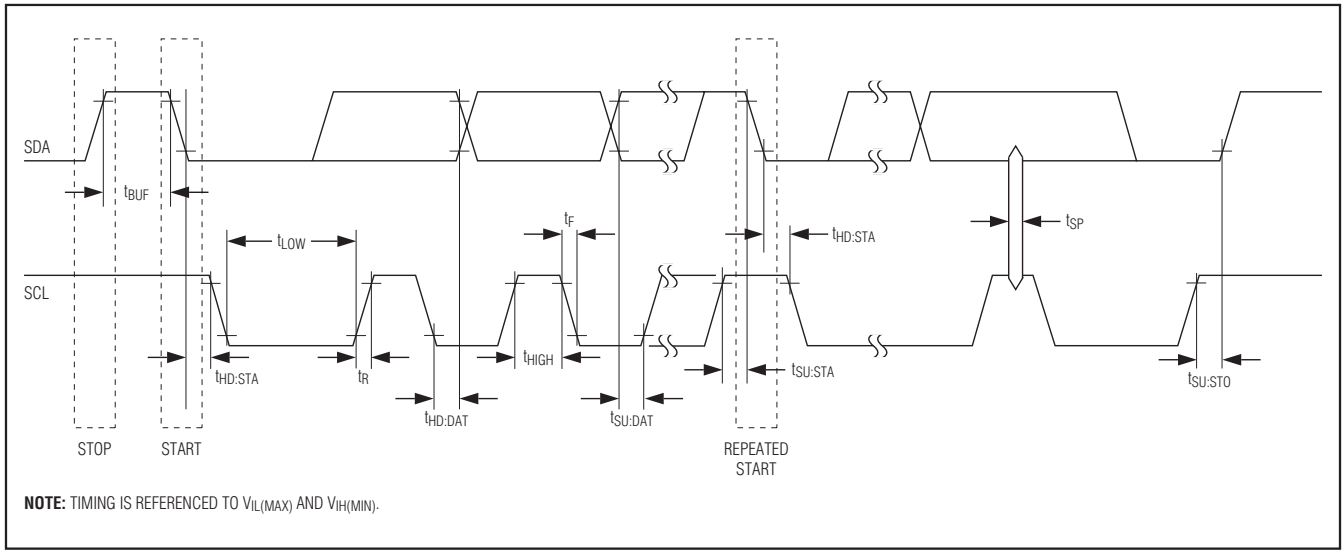


Figure 3. I²C/SMBus Timing Diagram

Acknowledged by Slave

A slave device, when addressed, is usually obliged to generate an acknowledge after the receipt of each byte. The master must generate the clock pulse for each acknowledge bit. A slave that acknowledges must pull down the SDA line during the acknowledge clock pulse so that it remains stable low during the high period of this clock pulse. Setup and hold times $t_{SU:DAT}$ and $t_{HD:DAT}$ must be taken into account.

Acknowledged by Master

To continue reading from a slave, the master is obliged to generate an acknowledge after the receipt of each byte. The master must generate the clock pulse for each acknowledge bit. A master that acknowledges must pull down the SDA line during the acknowledge clock pulse so that it remains stable low during the high period of this clock pulse. Setup and hold times $t_{SU:DAT}$ and $t_{HD:DAT}$ must be taken into account.

Not Acknowledged by Slave

A slave device may be unable to receive or transmit data either because of an invalid access mode, because the SHA-1 engine is running, or because a EEPROM write cycle is in progress. In this case, the DS28CN01 does not acknowledge any bytes that it refuses by leaving SDA high during the high period of the acknowledge-related clock pulse. See the *Read and Write* section in the full data sheet for a detailed list of situations where the DS28CN01 does not acknowledge.

Not Acknowledged by Master

At some time when receiving data, the master must terminate a read access. To achieve this, the master does not acknowledge the last byte that it has received from the slave by leaving SDA high during the high period of the acknowledge-related clock pulse. In response, the slave stops transmitting, allowing the master to generate a STOP condition.

Data Memory and Registers

For this section including Figures 4 and 5 and Table 2, refer to the full version of the data sheet.

Read and Write

This section discusses the read and write behavior of the EEPROM and the various registers. Refer to the full data sheet for details, including Tables 3 to 13.

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SHA-1 Computation Algorithm

This description of the SHA-1 computation is adapted from the Secure Hash Standard SHA-1 document that can be downloaded from the NIST website. Refer to the full version of the data sheet for more details.

Applications Information

SDA and SCL Pullup Resistors

SDA is an open-drain output on the DS28CN01 that requires a pullup resistor (see the *Typical Operating Circuit*) to realize high logic levels. Because the DS28CN01 uses SCL only as input (no clock stretching), the master can drive SCL either through an open-drain/collector output with a pullup resistor or a push-pull output.

Pullup Resistor RP Sizing

According to the I²C specification, a slave device must be able to sink at least 3mA at a V_{OL} of +0.4V. The SMBus specification requires a current sink capability of 4mA at +0.4V. The DS28CN01 can sink at least 4mA at +0.4V V_{OL} over its entire operating voltage range. This DC characteristic determines the minimum value of the pullup resistor: $R_{PMIN} = (V_{CC} - 0.4V)/4mA$. With a maximum operating voltage of +5.5V, the minimum value for the pullup resistor is 1.275kΩ. The "Minimum RP" line in Figure 6 shows how the minimum pullup resistor changes with the operating (pullup) voltage.

For I²C systems, the rise time and fall time are measured from 30% to 70% of the pullup voltage. The maximum bus capacitance C_B is 400pF. The maximum rise time must not exceed 300ns. Assuming maximum rise time, the maximum resistor value at any given capacitance C_B is calculated as: $R_{PMAX} = 300ns/(C_B \times \ln(7/3))$. For a bus capacitance of 400pF the maximum pullup resistor would be 885Ω.

Since an 885Ω pullup resistor, as would be required to meet the rise time specification and 400pF bus capacitance, is lower than R_{PMIN} at +5.5V, a different approach is necessary. The "Maximum Load" line in Figure 6 is generated by first calculating the minimum pullup resistor at any given operating voltage ("Minimum RP" line) and then calculating the respective bus capacitance that yields a rise time of 300ns.

Only for pullup voltages of +4V and lower can the maximum permissible bus capacitance of 400pF be maintained. A reduced bus capacitance of 300pF is acceptable for the entire operating voltage range. The corresponding pullup resistor value at the voltage is indicated by the "Minimum RP" line.

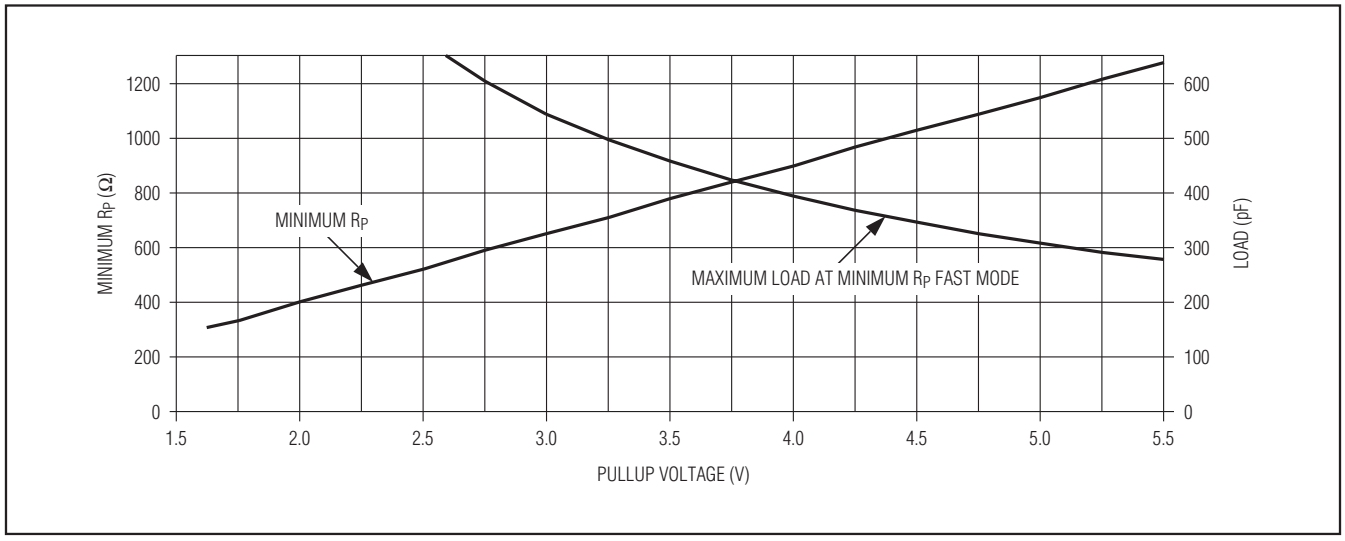
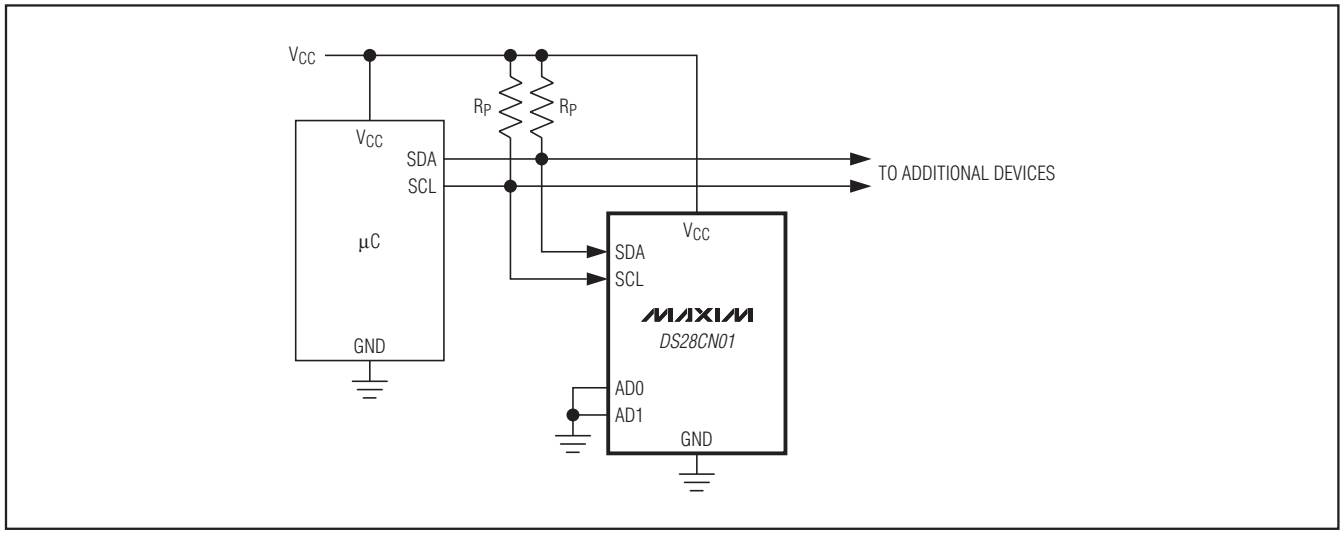


Figure 6. I²C Fast-Mode Pullup-Resistor Selection Chart

1Kb I²C/SMBus EEPROM with SHA-1 Engine

Typical Operating Circuit



Package Information

For the latest package outline information and land patterns, go to **www.maxim-ic.com/packages**. Note that a "+", "#", or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

PACKAGE TYPE	PACKAGE CODE	DOCUMENT NO.
8 µSOP	U8+3	**21-0036**

1Kb I²C/SMBus EEPROM with SHA-1 Engine

Revision History

REVISION NUMBER	REVISION DATE	DESCRIPTION	PAGES CHANGED
0	6/07	Initial release.	—
1	4/09	Created newer template-style data sheet.	All
2	11/09	Added condition “CM bit = 1” to the Bus Timeout specification in the *Electrical Characteristics*.	3

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