

Dual NV Audio Taper Digital Potentiometer

DS1881

General Description

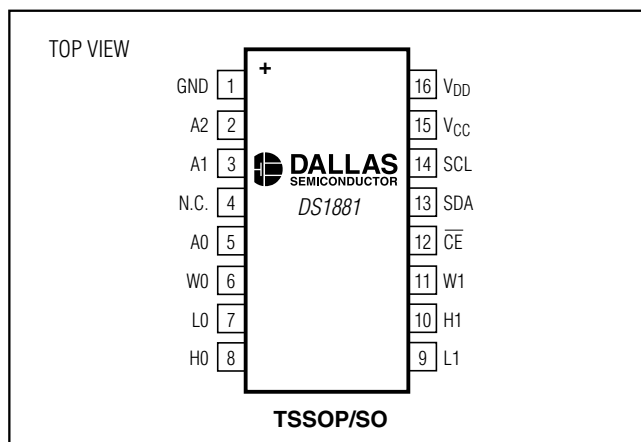
The DS1881 is a dual, nonvolatile (NV) digital potentiometer designed to operate in audio systems that require 5V signal levels. The potentiometer settings can be stored in EEPROM so that they are retained when the power is cycled. The DS1881 has separate supplies for the potentiometers (V_{CC}) and the communication circuitry (V_{DD}). For clickless/popless operation, a zero-crossing detector allows the wiper position to change when there is no voltage across the potentiometer. The device is also designed to minimize crosstalk, and the two digital potentiometers provide 0.5dB channel-to-channel matching to prevent volume differences between channels. Total harmonic distortion (THD) is also minimal as long as the wiper drives a high-impedance load.

Two attenuation configuration options provide optimum flexibility for the specific application. Configuration Option 1 provides 63 logarithmic tapered steps (0dB to -62dB, 1dB/step) plus a mute setting. Configuration Option 2 has 32 logarithmic steps plus mute and provides software compatibility with the DS1808. When Configuration Option 2 is used in combination with the 16-pin SO package, the DS1881 is both software and pin compatible with the DS1808 in 5V applications.

Applications

Notebook and PC Audio
Portable Audio Equipment
Car Stereo
Consumer Audio/Video

Pin Configuration



Features

- ◆ Dual, Audio Log Taper Potentiometers
- ◆ Low THD+N and Crosstalk
- ◆ 5V Analog Supply (Independent of Digital Supply)
- ◆ 3V to 5V Digital Supply Range
- ◆ Potentiometer Settings Configurable as NV or Volatile
- ◆ Zero-Crossing Detector Eliminates Switching Noise
- ◆ Two User-Configurable Attenuation Options
- ◆ Configuration Option 1: 63 Positions Provide 1dB Attenuation Steps from 0dB to -62dB Plus Mute
- ◆ Configuration Option 2: (Software-Compatible with the DS1808): 33 Positions Plus Mute as Follows
 - Positions 0–12: 1dB per Step for 12 Steps
 - Positions 13–24: 2dB per Step for 12 Steps
 - Positions 25–32: 3dB per Step for 8 Steps
- ◆ I²C-Compatible Serial Interface
- ◆ Three Address Pins Allow Up to 8 Devices on I²C Bus
- ◆ 45k Ω Potentiometer End-to-End Resistance
- ◆ Industrial Temperature Range (-40°C to +85°C)
- ◆ 16-Pin TSSOP or SO Package

Ordering Information

| PART | TEMP RANGE | VERSION (k Ω) | PIN-PACKAGE |
|-----------------|----------------|-----------------------|-----------------------------------|
| DS1881E-050+ | -40°C to +85°C | 45 | 16 TSSOP (173 mils) |
| DS1881E-050+T&R | -40°C to +85°C | 45 | 16 TSSOP (173 mils) Tape-and-Reel |
| DS1881Z-050+ | -40°C to +85°C | 45 | 16 SO (150 mils) |
| DS1881Z-050+T&R | -40°C to +85°C | 45 | 16 SO (150 mils) Tape-and-Reel |

+Denotes lead-free package.

Typical Operating Circuit appears at end of data sheet.

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ABSOLUTE MAXIMUM RATINGS

Voltage on V_{DD}, SDA, and SCL Relative to GND-0.5V to +6.0V
 Voltage on A2, A1, A0, and $\overline{\text{CE}}$ Relative to GND-0.5V to (V_{DD} + 0.5V), not to exceed +6.0V
 Voltage on V_{CC} Relative to GND-0.5V to +6.0V
 Voltage on H1, H0, W1, W0, L1, and L0 Relative to GND-0.5V to +6.0V

Maximum Resistor Current±3mA
 Operating Temperature Range-40°C to +85°C
 Programming Temperature Range0°C to +70°C
 Storage Temperature Range-55°C to +125°C
 Soldering Temperature.....See J-STD-020 Specification

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS

(T_A = -40°C to +85°C)

| PARAMETER | SYMBOL | CONDITIONS | MIN | TYP | MAX | UNITS |
|------------------------|-----------------|--------------|-----|-----|-----|-------|
| Digital Supply Voltage | V _{DD} | (Notes 1, 2) | 2.7 | | 5.5 | V |
| Analog Supply Range | V _{CC} | (Notes 1, 2) | 4.5 | | 5.5 | V |
| Potentiometer Voltages | | | 0 | | 5.5 | V |
| Wiper Current | | | | | ±1 | mA |

DC ELECTRICAL CHARACTERISTICS

(V_{DD} = +2.7V to +5.5V, V_{CC} = +4.5V to +5.5V, T_A = -40°C to +85°C.)

| PARAMETER | SYMBOL | CONDITIONS | MIN | TYP | MAX | UNITS |
|---|------------------|--|--------------------------|-----|--------------------------|-------|
| Digital Supply Current | I _{DD} | (Note 3) | | 200 | 250 | μA |
| Analog Supply Current | I _{CC} | (Note 4) | | 0.9 | 5 | μA |
| Input Logic 0 ($\overline{\text{CE}}$, SDA, SCL, A0, A1, A2) | V _{IL} | (Note 5) | -0.3 | | 0.3x V _{DD} | V |
| Input Logic 1 ($\overline{\text{CE}}$, SDA, SCL, A0, A1, A2) | V _{IH} | (Note 5) | 0.7 x V _{DD} | | V _{DD} + 0.3 | V |
| Output-Voltage Low (SDA) | V _{OL} | I _{OL} = 4mA | | | 0.4 | V |
| | | I _{OL} = 6mA | | | 0.6 | |
| Input Leakage Current | I _{LI} | | -1 | | +1 | μA |
| I/O Pin Input Current (SDA) | | 0.4V < V _{SDA} < (0.9 x V _{CC}) | -10 | | +10 | μA |
| I/O Capacitance | C _{I/O} | (Note 6) | | | 10 | pF |
| Power-Up Time | t _{PU} | | | | 1 | ms |

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ANALOG POTENTIOMETER CHARACTERISTICS

($V_{DD} = +2.7V$ to $+5.5V$, $V_{CC} = +4.5V$ to $+5.5V$, $T_A = -40^{\circ}C$ to $+85^{\circ}C$.)

| PARAMETER | SYMBOL | CONDITIONS | MIN | TYP | MAX | UNITS |
|---|-----------|---|-------|-------|-------|------------------|
| End-to-End Resistance | R_{EE} | $+25^{\circ}C$ | | 45 | | $k\Omega$ |
| End-to-End Resistance Tolerance | | $+25^{\circ}C$ | -20 | | +20 | % |
| Ratiometric Temperature Coefficient | | (Note 6) | | 30 | | ppm/ $^{\circ}C$ |
| End-to-End Resistance Temperature Coefficient | | (Note 6) | | 750 | | ppm/ $^{\circ}C$ |
| Wiper Resistance | R_W | | | 160 | 250 | Ω |
| Absolute Attenuation Tolerance | | (Note 7) | -0.5 | | +0.5 | dB |
| Mute Position Attenuation | | | | 80 | | dB |
| Step Size Deviation from Nominal | | (Note 7) | -0.25 | | +0.25 | dB |
| Interchannel Matching | | (Note 7) | -0.5 | | +0.5 | dB |
| -3dB Cutoff Frequency | | 10pF load | | 5 | | MHz |
| Output Noise | | (20Hz to 20kHz, grounded input, tap = -6dB) | | 2.2 | | μV_{RMS} |
| Crosstalk | | (1kHz, grounded input, tap = -6dB) | | -110 | | dB |
| THD+N | | 1kHz, tap = -6dB, $C_L = 10pF$ (Note 8) | | 0.005 | | % |
| Zero-Crossing Detection | t_{ZCD} | | | 38 | 50 | ms |

I²C CHARACTERISTICS (See Figure 4)

($V_{DD} = +2.7V$ to $+5.5V$, $V_{CC} = +4.5V$ to $+5.5V$, $T_A = -40^{\circ}C$ to $+85^{\circ}C$. Timing referenced to $V_{IL(MAX)}$ and $V_{IH(MIN)}$.)

| PARAMETER | SYMBOL | CONDITIONS | MIN | TYP | MAX | UNITS |
|---|--------------|------------|---------------|-----|-----|---------|
| SCL Clock Frequency | f_{SCL} | (Note 9) | 0 | | 400 | kHz |
| Bus Free Time Between STOP and START Conditions | t_{BUF} | | 1.3 | | | μs |
| Hold Time (Repeated) START Condition | $t_{HD:STA}$ | | 0.6 | | | μs |
| Low Period of SCL | t_{LOW} | | 1.3 | | | μs |
| High Period of SCL | t_{HIGH} | | 0.6 | | | μs |
| Data Hold Time | $t_{HD:DAT}$ | | 0 | | 0.9 | μs |
| Data Setup Time | $t_{SU:DAT}$ | | 100 | | | ns |
| START Setup Time | $t_{SU:STA}$ | | 0.6 | | | μs |
| SDA and SCL Rise Time | t_R | (Note 10) | 20 + $0.1C_B$ | | 300 | ns |
| SDA and SCL Fall Time | t_F | (Note 10) | 20 + $0.1C_B$ | | 300 | ns |
| STOP Setup Time | $t_{SU:STO}$ | | 0.6 | | | μs |
| SDA and SCL Capacitive Loading | C_B | (Note 10) | | | 400 | pF |
| EEPROM Write Time | t_W | (Note 11) | | 5 | 10 | ms |

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NV MEMORY CHARACTERISTICS

($V_{DD} = +2.7V$ to $+5.5V$, $V_{CC} = +4.5V$ to $+5.5V$, $T_A = 0^\circ C$ to $+70^\circ C$.)

| PARAMETER | SYMBOL | CONDITIONS | MIN | TYP | MAX | UNITS |
|-----------|--------|----------------|--------|-----|-----|-------|
| Writes | | +70°C (Note 6) | 50,000 | | | |

Note 1: All voltages are referenced to ground.

Note 2: The value of V_{DD} should never exceed V_{CC} , including during power-ups. V_{CC} must be applied before V_{DD} .

Note 3: I_{DD} is specified with $SDA = SCL = \overline{CE} = V_{DD}$, resistor pins floating, and digital inputs connected to V_{DD} or GND.

Note 4: I_{CC} is specified with $SDA = SCL = \overline{CE} = V_{DD}$, resistor pins floating, and digital inputs connected to V_{DD} or GND, after zero-crossing detection has timed out.

Note 5: The DS1881 will not obstruct the SDA and SCL lines if V_{DD} is switched off as long as the voltages applied to these inputs do not violate their minimum and maximum input voltage levels.

Note 6: Guaranteed by design.

Note 7: Above Position 50, these are typical maximum. Guaranteed by characterization.

Note 8: Load is representative of the input of a low-noise audio amp.

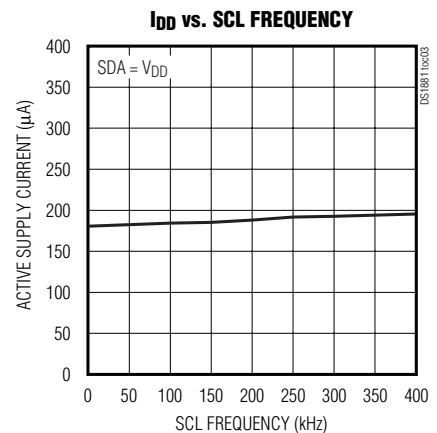
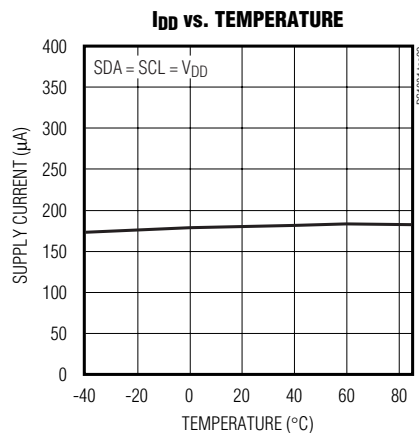
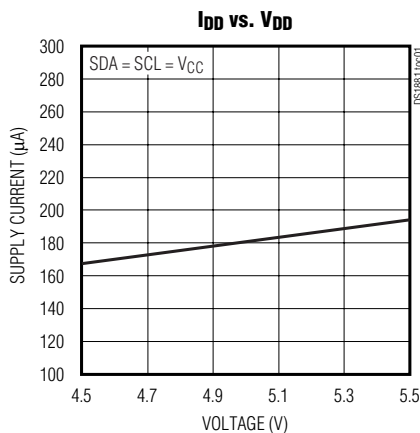
Note 9: Timing shown is for fast-mode (400kHz) operation. This device is also backward-compatible with I²C standard-mode timing.

Note 10: C_B —Total capacitance of one bus line in picofarads.

Note 11: If zero-crossing detection is enabled, the EEPROM write does not begin until the current zero-crossing detection is complete. Otherwise, EEPROM write begins after a STOP condition occurs.

Typical Operating Characteristics

($V_{DD} = V_{CC} = +5.0V$, $T_A = +25^\circ C$.)



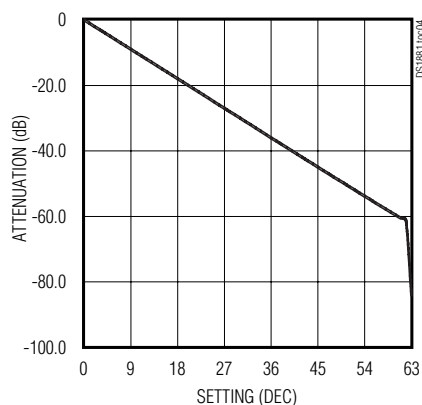
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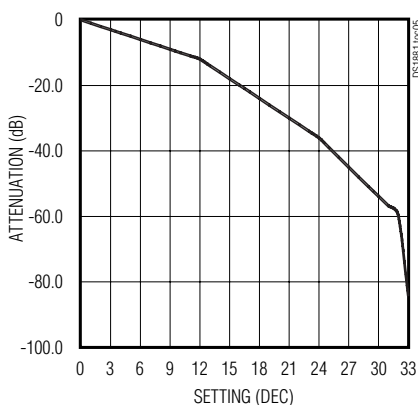
Typical Operating Characteristics (continued)

($V_{DD} = V_{CC} = +5.0V$, $T_A = +25^\circ C$.)

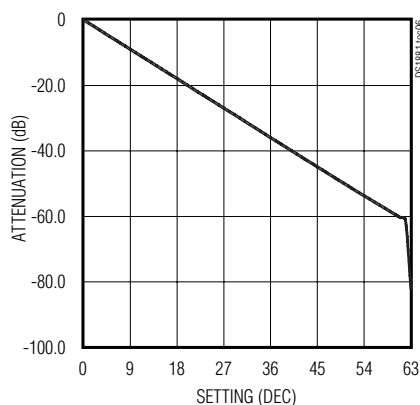
**POTENTIOMETER 0 (CONFIGURATION 1)
ATTENUATION vs. SETTING**



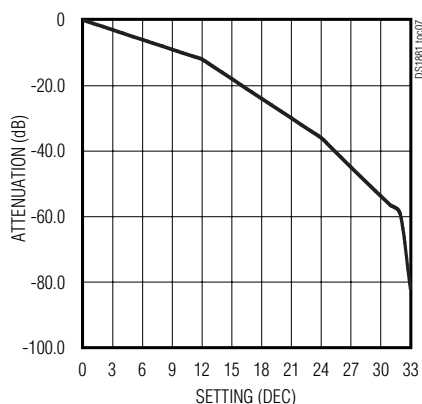
**POTENTIOMETER 0 (CONFIGURATION 2)
ATTENUATION vs. SETTING**



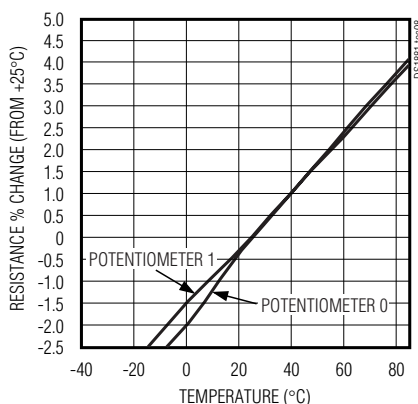
**POTENTIOMETER 1 (CONFIGURATION 1)
ATTENUATION vs. SETTING**



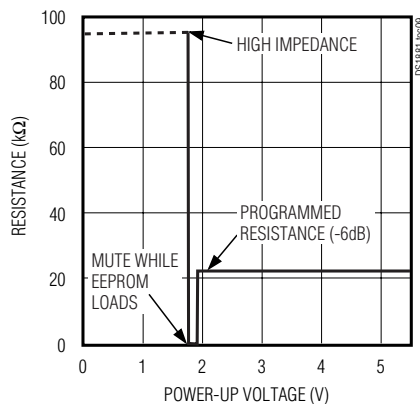
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ATTENUATION vs. SETTING**



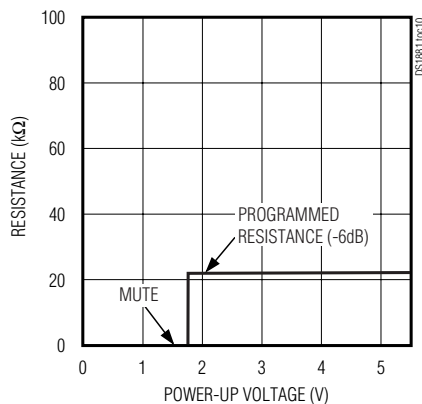
**END-TO-END RESISTANCE PERCENT
CHANGE FROM +25°C vs. TEMPERATURE**



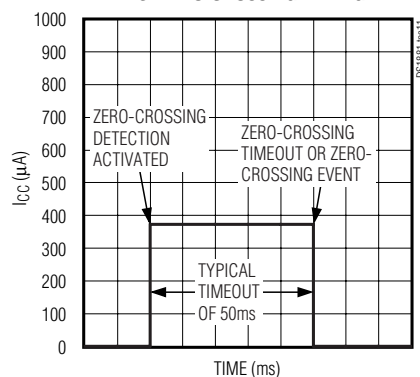
RESISTANCE vs. POWER-UP VOLTAGE



**RESISTANCE
vs. POWER-DOWN VOLTAGE**



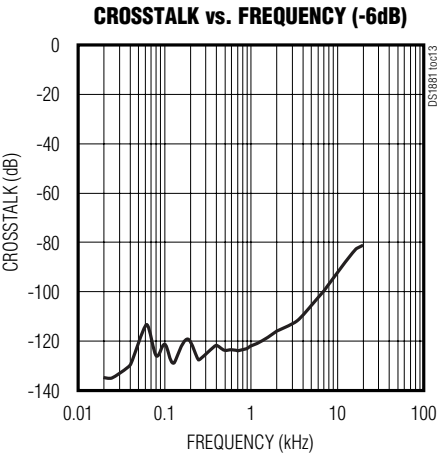
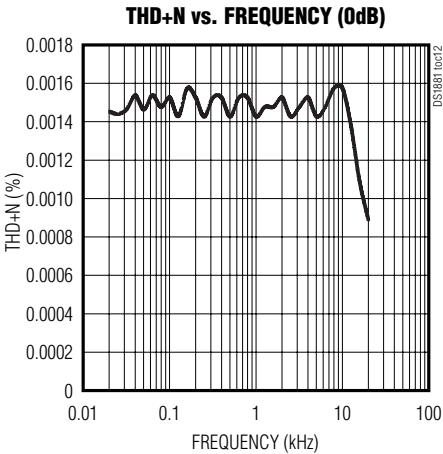
**SUPPLY CURRENT
vs. ZERO-CROSSING TIMING**



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Typical Operating Characteristics (continued)

(V_{DD} = V_{CC} = +5.0V, T_A = +25°C.)



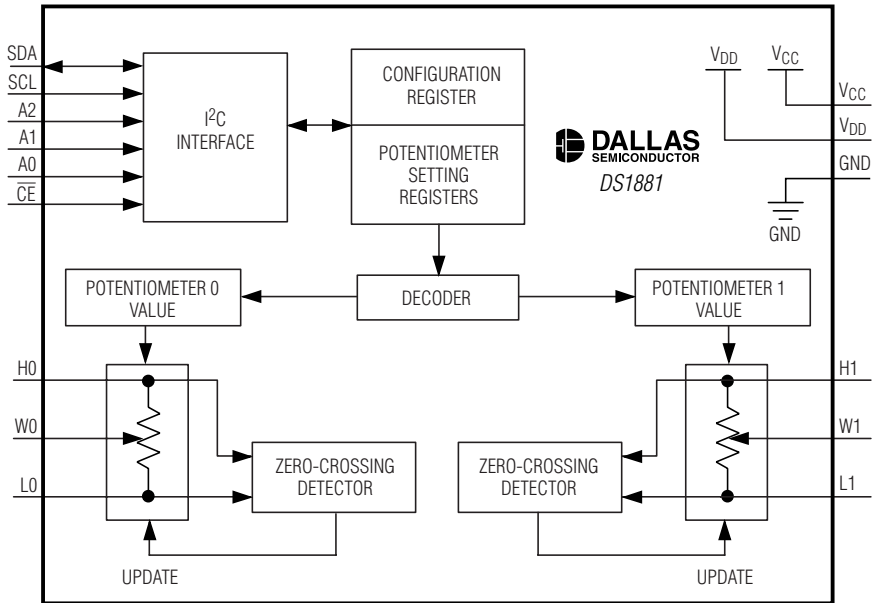
Pin Description

| PIN | NAME | FUNCTION |
|-----|------------------------|--|
| 1 | GND | Ground |
| 2 | A2 | I ² C Address Inputs. Inputs A0, A1, and A2 determine the I ² C slave address of the device. |
| 3 | A1 | |
| 4 | N.C. | No Connection |
| 5 | A0 | I ² C Address Input. Inputs A0, A1, and A2 determine the I ² C slave address of the device. |
| 6 | W0 | Wiper Terminal for Potentiometer 0 |
| 7 | L0 | Low Terminal for Potentiometer 0 |
| 8 | H0 | High Terminal for Potentiometer 0 |
| 9 | L1 | Low Terminal for Potentiometer 1 |
| 10 | H1 | High Terminal for Potentiometer 1 |
| 11 | W1 | Wiper Terminal for Potentiometer 1 |
| 12 | $\overline{\text{CE}}$ | Chip Enable. Enables SDA and SCL pins for I ² C communication. |
| 13 | SDA | I ² C Serial-Data Open-Drain I/O |
| 14 | SCL | I ² C Serial-Clock Input |
| 15 | V _{CC} | Analog Voltage Supply |
| 16 | V _{DD} | Digital Voltage Supply |

Dual NV Audio Taper Digital Potentiometer

Block Diagram

DS1881



Dual NV Audio Taper Digital Potentiometer

Detailed Description

The DS1881 is a dual-channel, digitally controlled, audio potentiometer. The *Block Diagram* illustrates the features of the DS1881. The following sections discuss these features in detail.

Potentiometer Configurations

The DS1881 potentiometers have two possible attenuation configuration options. The *Configuration Register* section discusses how to change between the two options. Note that both potentiometers are always set to the same option.

The factory default for both potentiometers is Option 1 (see Table 1). Option 1 provides 64 positions with 1dB attenuation per step for positions 0 through 62 and mute as position 63. Option 2 (see Table 2) is a 34-position configuration. From position 0, the first 12 steps have 1dB attenuation per step, the next 12 have 2dB attenuation per step, and the following 8 steps have 3dB attenuation per step. The last position, position 33, is the mute setting.

Zero-Crossing Detection

Zero-crossing detection is a user-selectable feature used to help eliminate clicking or popping noises during changes of potentiometer settings. See the *Configuration Register* section to learn how to enable the zero-crossing detection feature.

After the I²C master issues a command to change the wiper position and the DS1881 has responded with an acknowledge (ACK) to the command, the DS1881 has a 50ms window to change the wiper position. The DS1881 constantly monitors the voltage of the high and low terminals of both potentiometers. During the 50ms window, if the zero-crossing detection is enabled, then each potentiometer's wiper will change position if the high and low terminals of the same potentiometer become equal in potential (i.e., the magnitude of the input signal is zero). If a zero-crossing event does not occur within the 50ms window, then the wiper is allowed to change to the new position regardless of the state of the input signal. When the zero-crossing detection feature is not enabled, the DS1881 will allow wiper movement as soon as the DS1881 has issued the acknowledge to the master-controlling device.

Table 1. Configuration Option 1

| TAP POSITION | ATTENUATION (dB) |
|--------------|------------------|
| 0 | 0 |
| 1 | 1 |
| 2 | 2 |
| 3 | 3 |
| 4 | 4 |
| 5 | 5 |
| 6 | 6 |
| 7 | 7 |
| 8 | 8 |
| ... | ... |
| 40 | 40 |
| 41 | 41 |
| 42 | 42 |
| 43 | 43 |
| 44 | 44 |
| 45 | 45 |
| 46 | 46 |
| 47 | 47 |
| 48 | 48 |
| 49 | 49 |
| 50 | 50 |
| 51 | 51 |
| 52 | 52 |
| 53 | 53 |
| 54 | 54 |
| 55 | 55 |
| 56 | 56 |
| 57 | 57 |
| 58 | 58 |
| 59 | 59 |
| 60 | 60 |
| 61 | 61 |
| 62 | 62 |
| 63 | 80 |

Dual NV Audio Taper Digital Potentiometer

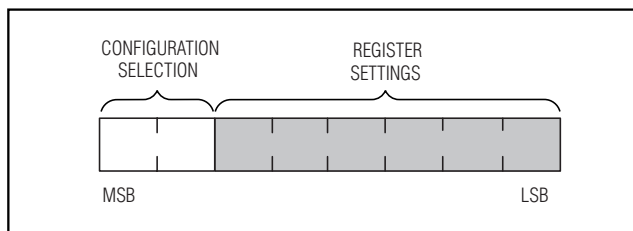
Table 2. Configuration Option 2

| TAP POSITION | ATTENUATION (dB) |
|--------------|------------------|
| 0 | 0 |
| 1 | 1 |
| 2 | 2 |
| 3 | 3 |
| 4 | 4 |
| 5 | 5 |
| 6 | 6 |
| 7 | 7 |
| 8 | 8 |
| 9 | 9 |
| 10 | 10 |
| 11 | 11 |
| 12 | 12 |
| 13 | 14 |
| 14 | 16 |
| 15 | 18 |
| 16 | 20 |
| 17 | 22 |
| 18 | 24 |
| 19 | 26 |
| 20 | 28 |
| 21 | 30 |
| 22 | 32 |
| 23 | 34 |
| 24 | 36 |
| 25 | 39 |
| 26 | 42 |
| 27 | 45 |
| 28 | 48 |
| 29 | 51 |
| 30 | 54 |
| 31 | 57 |
| 32 | 60 |
| 33 | 80 |

Command Byte

The Command Byte determines both the potentiometer wiper settings and the configuration of both potentiometers. This is done by setting the two MSBs of the Command Byte to one of three values. If 00 is set as the value for the two MSBs, then the wiper setting for Potentiometer 0 is to be programmed. If 01 is set as the value, then the wiper setting of Potentiometer 1 is to be programmed. See the *Potentiometer Wiper Setting* section for more details about writing the wiper setting. A value of 10 indicates that the Configuration Register is to be programmed. A value of 11 is reserved and is not to be used. See the *Configuration Register* section for more information. Any values other than the three discussed above will result in no action by the part. See below for the Command Byte structure.

Command Byte Structure



Dual NV Audio Taper Digital Potentiometer

Potentiometer Wiper Setting

If 00 or 01 are the values of the two MSBs of the Command Byte, then the wiper settings of the potentiometers are to be programmed. The lower 6 LSBs of

the Command Byte are then used to store the wiper settings for the selected potentiometer. See below for the potentiometer wiper setting details.

POTENTIOMETER WIPER REGISTER

| | |
|------------------|-------------|
| Factory Default: | XX111111b |
| Memory Type: | NV (EEPROM) |

| 0 | X | WIPER SETTING | | | | | |
|----|----|---------------|----|----|----|----|----|
| b7 | b6 | b5 | b4 | b3 | b2 | b1 | b0 |

| | |
|-----------|--|
| bits 7, 6 | Configuration Selection: Selects which potentiometer will be programmed. 00 = Potentiometer 0 will be programmed. 01 = Potentiometer 1 will be programmed. |
| bits 5–0 | These bits determine the wiper setting of the selected potentiometer. Available wiper settings are determined by the attenuation option as described in the <i>Configuration Register</i> section. |

Dual NV Audio Taper Digital Potentiometer

Configuration Register

If 10 is entered as the value of the two MSBs of the Command Byte, then the Configuration Register is to be modified. The three LSBs of the Configuration

Register control the NV/volatile wiper setting, the zero-crossing detection feature, and the potentiometer attenuation configuration.

CONFIGURATION REGISTER

| | |
|------------------|-------------|
| Factory Default: | 87h |
| Memory Type: | NV (EEPROM) |

| 1 | 0 | X | X | X | V/NV CONTROL | ZERO- CROSSING | POT CONFIG |
|----|----|----|----|----|-----------------|-------------------|---------------|
| b7 | b6 | b5 | b4 | b3 | b2 | b1 | b0 |

| | |
|--------------|---|
| bits 7, 6 | Configuration Selection: When bit 7 is set to a 1 and bit 6 is set to a 0, the following configuration bits can be set and stored in EEPROM. |
| bits 5, 4, 3 | These bits have no function. |
| bit 2 | Volatile/Nonvolatile Potentiometer Register Control Bit: A control bit that sets the potentiometer registers to be either volatile or nonvolatile memory. 0 = Potentiometer registers are set to nonvolatile memory storage. 1 = Potentiometer registers are set to volatile memory storage. On power-up, the potentiometer wipers are in the mute position (default). |
| bit 1 | Zero-Crossing Detection Enable Bit: A bit used to enable and disable the zero-crossing functionality. 0 = Zero-crossing detection is disabled. 1 = Zero-crossing detection is enabled (default). |
| bit 0 | Potentiometer Position Configuration: A control bit used to select the number of positions both potentiometers have. 0 = Potentiometers have 63 positions and mute. 1 = Potentiometers have 33 positions and mute (default). |

Dual NV Audio Taper Digital Potentiometer

I²C Interface for the DS1881

The \overline{CE} pin serves as a communication enable pin. When active ($\overline{CE} = 0$), the inputs SDA and SCL are recognized by the device. If inactive ($\overline{CE} = 1$), pins SDA and SCL are disabled, making I²C communication impossible.

Three pins, A0, A1, A2, serve as slave address inputs. For multidrop configurations, they allow eight such devices to be addressed by the same I²C bus. If the I²C address matches the hardware levels of these bits,

the DS1881 is allowed to receive communications from the I²C bus.

The I²C slave address byte is shown below. This is the first byte transmitted from the master to the DS1881. The upper nibble value is fixed to 0101. Bit values A2, A1, and A0 are determined by the states of the corresponding pins. The LSB, $\overline{R/\overline{W}}$, determines whether a read or write will be performed.

The next byte to be transmitted is the Command Byte (see the *Command Byte* section for details).

| SLAVE ADDRESS BYTE | | | | | | | |
|--------------------|---|---|---|-----|----|----|-----------------------------|
| 0 | 1 | 0 | 1 | A2 | A1 | A0 | $\overline{R/\overline{W}}$ |
| MSB | | | | LSB | | | |

Reading Pot Values

As shown in Figure 1, the DS1881 provides one read command operation. This operation allows the user to read both Potentiometer Wiper Setting Registers and the Configuration Register. To initiate a read operation, the $\overline{R/\overline{W}}$ bit of the slave address byte is set to 1. Communication to read the DS1881 begins with a START condition, which is issued by the master device. The slave address byte sent from the master device follows the START condition. Once a matching slave address byte has been received by the DS1881, the DS1881 responds with an acknowledge. The master can then begin to receive data. The value of the wiper

of Potentiometer 0 is the first returned from the DS1881. It is then followed by the value of Potentiometer 1 and then the value of the Configuration Register. Once the 8 bits of the Configuration Register have been sent, the master needs to issue an acknowledge, unless it is the last byte to be read, in which case the master issues a not acknowledge. If desired, the master may stop the communication transfer at this point by issuing the STOP condition after the not acknowledge. However, if the value of the three registers is needed again, the transfer can continue by clocking the 8 bits of the Potentiometer 0 value as described above.

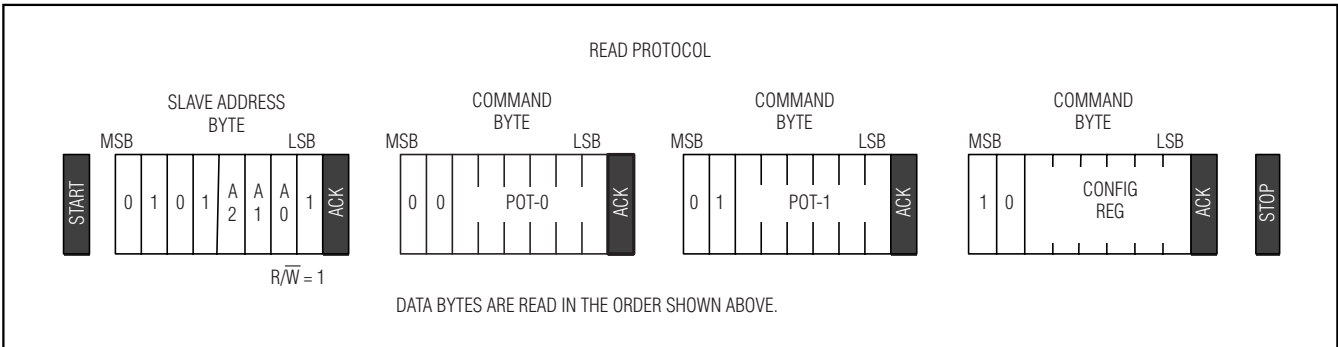


Figure 1. Read Protocol

Dual NV Audio Taper Digital Potentiometer

Writing Command Byte Values

An example of writing to the DS1881 is shown in Figure 2. The DS1881 has one write command that is used to change the Potentiometer Wiper Setting registers and the Configuration Register. All write operations begin with a START from the master, followed by a slave address byte. The R/W bit should be written to 0, which initiates a write command. Once the slave address byte has been issued and the master receives the acknowledge from the DS1881, potentiometer wiper data is transmitted to the DS1881 by the master device.

If the potentiometer has been configured to be written in nonvolatile memory (see the *Configuration Register* section), then the acknowledge needs to be followed with a STOP command. This command is required from the master at the end of data transmission to initiate the EEPROM write. The STOP command is also accepted if the user has configured the pot values to be written in volatile memory, but no EEPROM is written to.

I²C Serial Interface Descriptions

I²C interface supports a bidirectional data transmission protocol with device addressing. A device that sends data on the bus is defined as a transmitter, and a device receiving data as a receiver. The device that controls the message is called a master. The devices that are controlled by the master are slaves. The bus must be controlled by a master device that generates the serial clock (SCL), controls the bus access, and generates the START and STOP conditions. The DS1881 operates as a slave on the I²C bus. Connections to the bus are made by the open-drain I/O lines, SDA and SCL. The following I/O terminals control the I²C serial port: \overline{CE} , SDA, SCL, A0, A1, and A2. A data transfer protocol and a timing diagram are provided in Figures 3 and 4. The following terminology is commonly used to describe I²C data transfers.

I²C Definitions

Master Device: The master device controls the slave devices on the bus. The master device generates SCL clock pulses, START and STOP conditions.

Slave Devices: Slave devices send and receive data at the master's request.

Bus Idle or Not Busy: Time between STOP and START conditions when both SDA and SCL are inactive and in their logic-high states. When the bus is idle it often initiates a low-power mode for slave devices.

START Condition: A START condition is generated by the master to initiate a new data transfer with a slave. Transitioning SDA from high to low while SCL remains high generates a START condition. See the timing diagram for applicable timing.

STOP Condition: A STOP condition is generated by the master to end a data transfer with a slave. Transitioning SDA from low to high while SCL remains high generates a STOP condition. See the timing diagram for applicable timing.

Repeated START Condition: The master can use a repeated START condition at the end of one data transfer to indicate that it will immediately initiate a new data transfer following the current one. Repeated STARTS are commonly used during read operations to identify a specific memory address to begin a data transfer. A repeated START condition is issued identically to a normal START condition. See the timing diagram for applicable timing.

Bit Write: Transitions of SDA must occur during the low state of SCL. The data on SDA must remain valid and unchanged during the entire high pulse of SCL plus the setup and hold-time requirements (see Figure 4). Data is shifted into the device during the rising edge of the SCL.

Bit Read: At the end of a write operation, the master must release the SDA bus line for the proper amount of

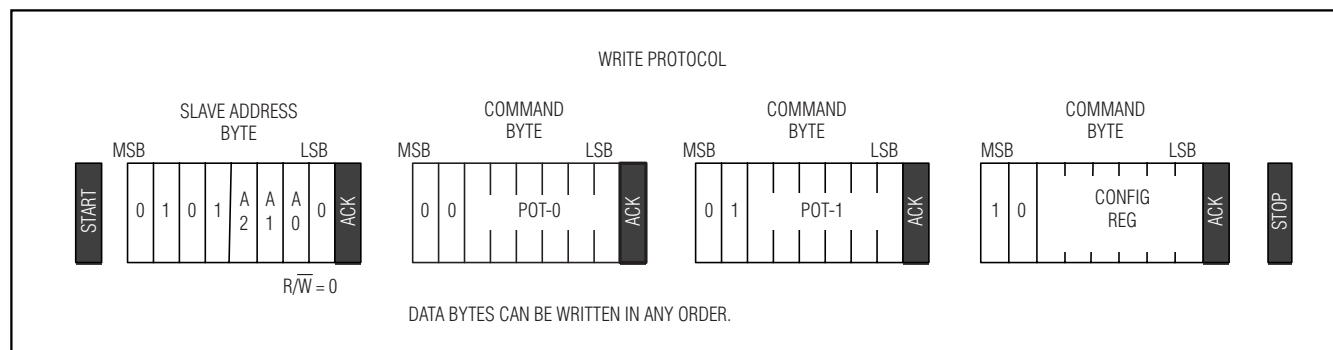


Figure 2. Write Protocol

Dual NV Audio Taper Digital Potentiometer

setup time (see Figure 4) before the next rising edge of SCL during a bit read. The device shifts out each bit of data on SDA at the falling edge of the previous SCL pulse and the data bit is valid at the rising edge of the current SCL pulse. Remember that the master generates all SCL clock pulses including when it is reading bits from the slave.

Acknowledgement (ACK and NACK): An Acknowledgement (ACK) or Not Acknowledge (NACK) is always the 9th bit transmitted during a byte transfer. The device

receiving data (the master during a read or the slave during a write operation) performs an ACK by transmitting a zero during the 9th bit. A device performs a NACK by transmitting a one during the 9th bit. Timing (Figure 4) for the ACK and NACK is identical to all other bit writes. An ACK is the acknowledgment that the device is properly receiving data. A NACK is used to terminate a read sequence or as an indication that the device is not receiving data.

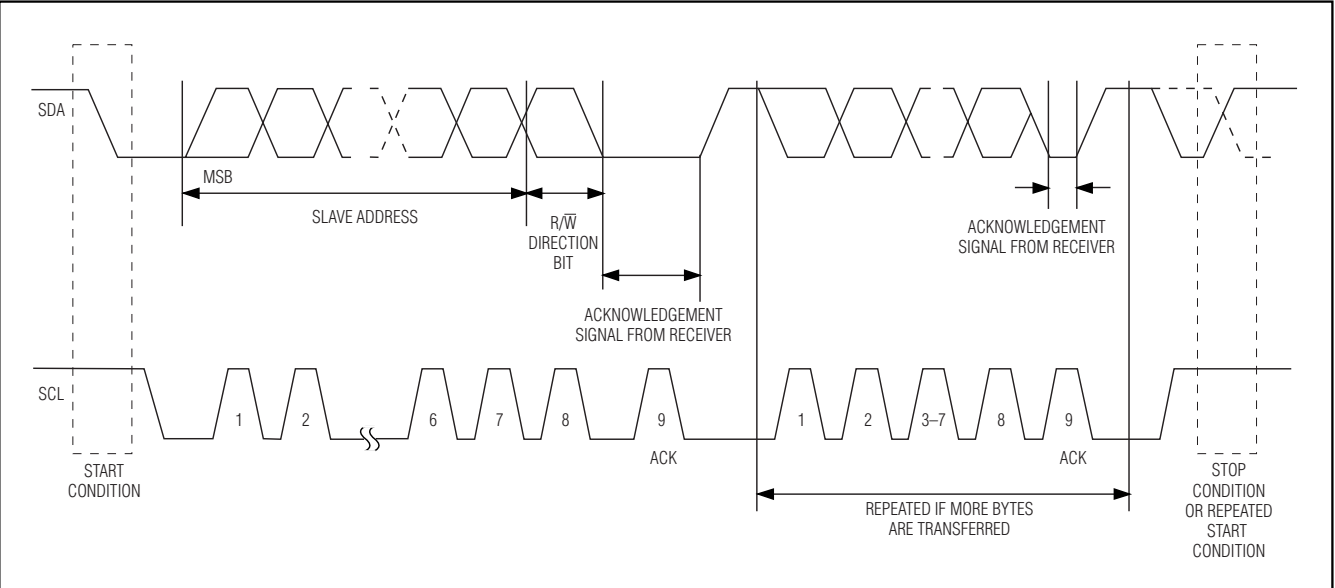


Figure 3. Data Transfer Protocol

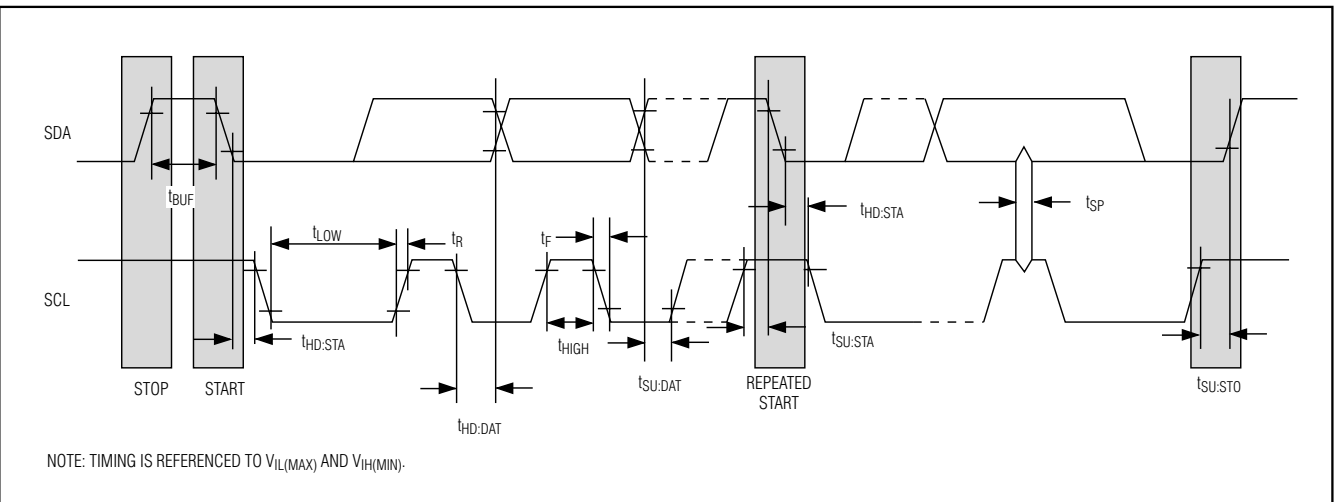


Figure 4. I²C Timing Diagram

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Byte Write: A byte write consists of 8 bits of information transferred from the master to the slave (most significant bit first) plus a 1-bit acknowledgement from the slave to the master. The 8 bits transmitted by the master are done according to the bit write definition and the acknowledgement is read using the bit read definition.

Byte Read: A byte read is an 8-bit information transfer from the slave to the master plus a 1-bit ACK or NACK from the master to the slave. The 8 bits of information that are transferred (most significant bit first) from the slave to the master are read by the master using the bit read definition, and the master transmits an ACK using the bit write definition to receive additional data bytes. The master must NACK the last byte read to terminate communication so the slave will return control of SDA to the master.

Slave Address Byte: Each slave on the I²C bus responds to a slave addressing byte sent immediately following a START condition. The slave address byte (Figure 5) contains the slave address in the most significant 7 bits and the R/W bit in the least significant bit.

The DS1881's slave address is 0101 A2 A1 A0 (binary), where A2, A1, and A0 are the values of the address pins. The address pins allow the device to respond to one of eight possible slave addresses. By writing the correct slave address with R/W = 0, the master indicates it will write data to the slave. If R/W = 1, the master will read data from the slave. If an incorrect slave address is written, the DS1881 will assume the master is communicating with another I²C device and ignore the communications until the next START condition is sent.

I²C Communication

Writing a Single Byte to a Slave: The master must generate a START condition, write the slave address byte (R/W = 0), write the byte of data, and generate a STOP condition. The master must read the slave's acknowledgement during all byte write operations.

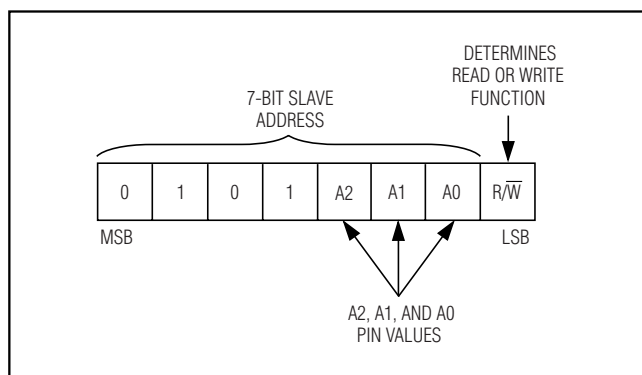


Figure 5. DS1881's Slave Address Byte

Writing Multiple Bytes to a Slave: To write multiple bytes to a slave, the master generates a START condition, writes the slave address byte (R/W = 0), writes the desired number of data bytes and generates a STOP condition. The DS1881 is capable of writing both potentiometer wiper settings and the Configuration Register with a single write transaction.

Acknowledge Polling: Any time an EEPROM location is written, the DS1881 requires the EEPROM write time (t_w) after the STOP condition to write the contents of the byte of data to EEPROM. During the EEPROM write time, the device will not acknowledge its slave address because it is busy. It is possible to take advantage of that phenomenon by repeatedly addressing the DS1881, which allows the next page to be written as soon as the DS1881 is ready to receive the data. The alternative to acknowledge polling is to wait for a maximum period of t_w to elapse before attempting to write again to the device.

EEPROM Write Cycles: When EEPROM writes occur to the memory, the DS1881 will write to all three EEPROM memory locations, even if only a single byte was modified. Because all three bytes are written, the bytes that were not modified during the write transaction are still subject to a write cycle. This can result in all three bytes being worn out over time by writing a single byte repeatedly. The DS1881's EEPROM write cycles are specified in the *NV Memory Characteristics* table. The specification shown is at the worst-case temperature. If zero-crossing detection is enabled, EEPROM write cycles cannot begin until after the zero-crossing detection is complete.

Reading a Single Byte from a Slave: To read a single byte from the slave, the master generates a START condition, writes the slave address byte with R/W = 1, reads the data byte with a NACK to indicate the end of the transfer, and generates a STOP condition. When a single byte is read, it will always be the Potentiometer 0 value.

Reading Multiple Bytes from a Slave: The read operation can be used to read multiple bytes with a single transfer. When reading bytes from the slave, the master simply ACKs the data byte if it desires to read another byte before terminating the transaction. After the master reads the last byte, it NACKs to indicate the end of the transfer and generates a STOP condition. The first byte read will be the Potentiometer 0 Wiper Setting. The next byte will be the Potentiometer 1 Wiper Setting. The third byte is the Configuration Register byte. If an ACK is issued by the master following the Configuration Register byte, then the DS1881 will send the Potentiometer 0 Wiper Setting again. This round robin reading will occur as long as each byte read is followed by an ACK from the master.

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Applications Information

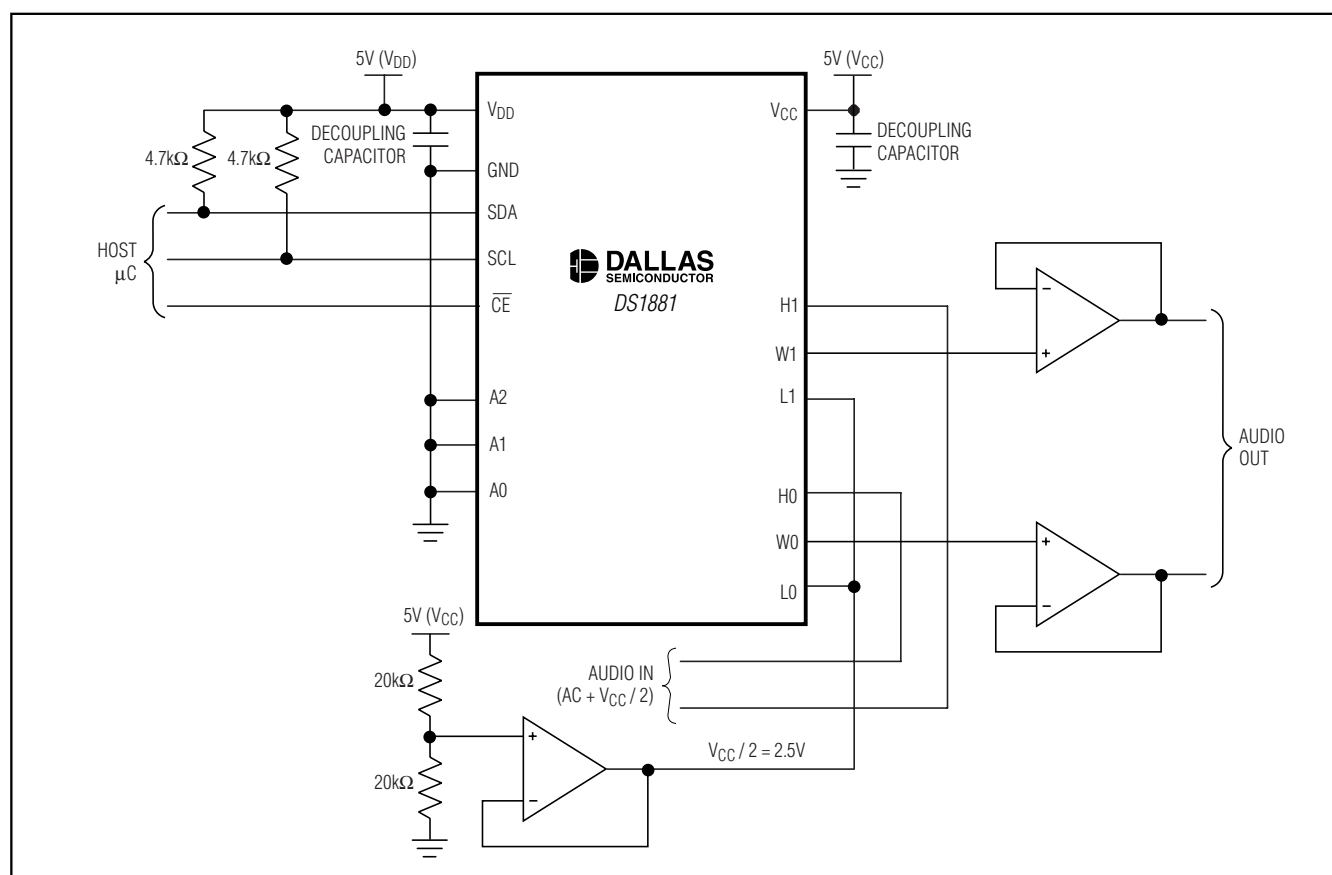
Power-Supply Decoupling

To achieve best results, it is recommended that the power supplies are decoupled with a $0.01\mu\text{F}$ or a $0.1\mu\text{F}$ capacitor. Use high-quality, ceramic, surface-mount capacitors, and mount the capacitors as close as possible to the voltage supplies and GND pins to minimize lead inductance.

SDA and SCL Pullup Resistors

SDA is an open-collector output on the DS1881 that requires a pullup resistor to realize high logic levels. A master using either an open-collector output with a pullup resistor or a push-pull output driver can be utilized for SCL. Pullup resistor values should be chosen to ensure that the rise and fall times listed in the AC Electrical Characteristics table are within specification.

Typical Operating Circuit



Chip Topology

TRANSISTOR COUNT: 52,353
SUBSTRATE CONNECTED TO GROUND

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