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### GENERAL DESCRIPTION

The DS1670 portable system controller is a circuit that incorporates many of the functions necessary for low-power portable products integrated into one chip. The device provides a real-time clock (RTC), NV RAM controller, microprocessor monitor, and a 3-channel, 8-bit analog-to-digital converter (ADC). Communication with the DS1670 is established through a simple 3-wire interface.

The RTC provides seconds, minutes, hours, day, date, month, and year information with leap year compensation. The RTC also provides an alarm interrupt. This interrupt works when the DS1670 is powered by the system power supply or when in battery-backup operation, so the alarm can be used to wake up a system that is powered down.

Automatic backup and write protection of an external SRAM is provided through the  $V_{CCO}$ ,  $\overline{CEOL}$ , and  $\overline{CEOH}$  pins. The backup energy source used to power the RTC is also used to retain RAM data in the absence of  $V_{CC}$  through the  $V_{CCO}$  pin. The chip-enable outputs to RAM ( $\overline{CEOL}$  and  $\overline{CEOH}$ ) are controlled during power transients to prevent data corruption.

### ORDERING INFORMATION

PART*	VOLTAGE (V)	PIN PACKAGE	TOP MARK†
DS1670E	3.3	20 TSSOP	DS1670E
DS1670E+	3.3	20 TSSOP	DS1670E
DS1670E/T&R	3.3	20 TSSOP	DS1670E
DS1670E+TRL	3.3	20 TSSOP	DS1670E
DS1670S	3.3	20 SO	DS1670S
DS1670S+	3.3	20 SO	DS1670S

\* All devices are specified over the 0°C to +70°C operating range.

† A “+” anywhere on the top mark denotes a lead-free device.

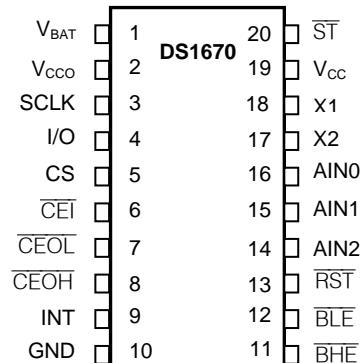
‡ Denotes a lead(Pb)-free/RoHS-compliant device.

### FEATURES

- **Provides Real-Time Clock**  
Counts Seconds, Minutes, Hours, Date of the Month, Month, Day of the Week, and Year with Leap Year Compensation Valid Up to 2100  
Power-Control Circuitry Supports System Power-On from Day/Time Alarm
- **Microprocessor Monitor**  
Halts Microprocessor During Power Fail  
Automatically Restarts Microprocessor after Power Failure  
Monitors Pushbutton for External Override  
Halts and Resets an Out-of-Control Microprocessor
- **NV RAM Control**  
Automatic Battery Backup and Write Protection to External SRAM
- **3-Channel, 8-Bit ADC**
- **Simple 3-Wire Interface**
- **3.3V Operation**
- **Underwriters Laboratory (UL) Recognized**

### PIN CONFIGURATION

TOP VIEW



**TSSOP (4.4mm)  
SO (300 mils)**

## DETAILED DESCRIPTION

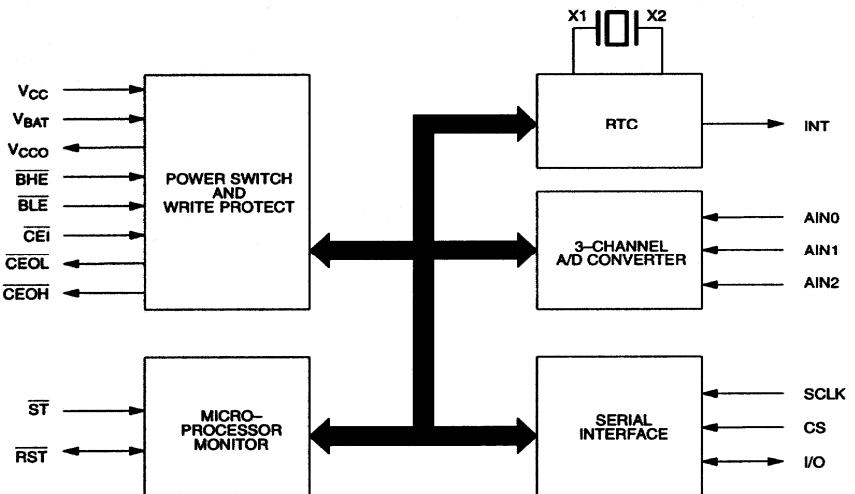
The microprocessor monitor circuitry of the DS1670 provides three basic functions. First, a precision temperature-compensated reference and comparator circuit monitors the status of  $V_{CC}$ . When an out-of-tolerance condition occurs, an internal power-fail signal is generated that forces the reset to the active state. When  $V_{CC}$  returns to an in-tolerance condition, the reset signals are kept in the active state for 250ms to allow the power supply and processor to stabilize. The second microprocessor monitor function is pushbutton reset control. The DS1670 debounces a pushbutton input and guarantees an active-reset pulse width of 250ms. The third function is a watchdog timer. The DS1670 has an internal timer that forces the reset signals to the active state if the strobe input is not driven low prior to watchdog timeout.

The DS1670 also provides a 3-channel, 8-bit successive approximation analog-to-digital converter. The converter has an internal 2.55V (typical) reference voltage generated by an on-board band-gap circuit. The ADC is monotonic (no missing codes) and has an internal analog filter to reduce high frequency noise.

## OPERATION

The block diagram in Figure 1 shows the main elements of the DS1670. The following paragraphs describe the function of each pin.

**DS1670 BLOCK DIAGRAM** Figure 1



## PIN DESCRIPTION

PIN	NAME	FUNCTION
1	V <sub>BAT</sub>	Battery Input for Standard 3V Lithium Cell or Other Energy Source. UL recognized to ensure against reverse charging when used with a lithium battery. Go to <a href="http://www.maxim-ic.com/qa/info/ul/">www.maxim-ic.com/qa/info/ul/</a> .
2	V <sub>CCO</sub>	External SRAM Power Supply Output. This pin is internally connected to V <sub>CC</sub> when V <sub>CC</sub> is within nominal limits. However, during power-fail V <sub>CCO</sub> is internally connected to the V <sub>BAT</sub> pin. Switchover occurs when V <sub>CC</sub> drops below the lower of V <sub>BAT</sub> or 2.7V.
3	SCLK	Serial Clock Input. Used to synchronize data movement on the serial interface.
4	I/O	Data Input/Output. This pin is the bidirectional data pin for the 3-wire interface.
5	CS	Chip Select. Must be asserted high during a read or a write for communication over the 3-wire serial interface. CS has an internal 40kΩ pulldown resistor.
6	CEI	RAM Chip-Enable In. Must be driven low to enable the external RAM.
7	CEOL	RAM Chip-Enable Out Low. Active-low chip-enable output for low-order SRAM byte.
8	CEOH	RAM Chip-Enable Out High. Active-low chip-enable output for high-order SRAM byte.
9	INT	Interrupt Output. This pin is an active-high output that can be used as an interrupt input to a microprocessor. The INT output remains high as long as the status bit causing the interrupt is present and the corresponding interrupt-enable bit is set. The INT pin operates when the DS1670 is powered by V <sub>CC</sub> or V <sub>BAT</sub> .
10	GND	Ground. DC power is provided to the device on this pin.
11	BHE	Byte High-Enable Input. This pin when driven low activates the CEOH output if CEI is also driven low.
12	BLE	Byte Low-Enable Input. This pin when driven low activates the CEOL output if CEI is also driven low.
13	RST	Active-Low Reset. The RST pin functions as a microprocessor reset signal. This pin is driven low 1) when V <sub>CC</sub> is outside of nominal limits; 2) when the watchdog timer has timed out; 3) during the power up reset period; and 4) in response to a pushbutton reset. The RST pin also functions as a pushbutton reset input. When the RST pin is driven low, the signal is debounced and timed such that a RST signal of at least 250ms is generated. This pin has an open-drain output with an internal 47kΩ pullup resistor.
14, 15, 16	AIN2, AIN1, AIN0	Analog Inputs. These pins are the three analog inputs for the 3-channel ADC.
17, 18	X2, X1	Connections for Standard 32.768kHz Quartz Crystal. For greatest accuracy, the DS1670 must be used with a crystal that has a specified load capacitance of 6pF. There is no need for external capacitors or resistors. Note: X1 and X2 are very high-impedance nodes. It is recommended that they and the crystal be guard-ringed with ground and that high frequency signals be kept away from the crystal area. For more information on crystal selection and crystal layout considerations, refer to <i>Application Note 58: Crystal Considerations with Dallas Real Time Clocks</i> . The DS1670 does not function without a crystal.
19	V <sub>CC</sub>	+3.3V Input DC Power. When 3.3V is applied within nominal limits, the device is fully accessible and data can be written and read. When V <sub>CC</sub> drops below 2.88V (typical) access to the device is prohibited. When V <sub>CC</sub> drops below the lower of V <sub>BAT</sub> and 2.7V (typical), the device is switched over to the backup power supply.
20	ST	Active-Low Strobe Input. The strobe input pin is used with the watchdog timer. If the ST pin is not driven low within the watchdog time period, the RST pin is driven low.

## POWER-UP/POWER-DOWN CONSIDERATIONS

The DS1670 was designed to operate with a power supply of 3.3V. When 3.3V are applied within nominal limits, the device becomes fully accessible after  $t_{RPU}$  (250ms typical). Before  $t_{RPU}$  elapses, all inputs are disabled. When  $V_{CC}$  drops below 2.88V (typical), the  $\overline{RST}$  pin is driven low. When  $V_{CC}$  drops below the lower of 2.7V (typical) or the battery voltage, the device is switched over to the backup power supply.

During power-up, when  $V_{CC}$  returns to an in-tolerance condition, the  $\overline{RST}$  pin is kept in the active state for 250ms (typical) to allow the power supply and microprocessor to stabilize.

## ADDRESS/COMMAND BYTE

The command byte for the DS1670 is shown in Figure 2. Each data transfer is initiated by a command byte. Bits 0 through 6 specify the addresses of the registers to be accessed. The MSB (bit 7) is the Read/Write bit. This bit specifies whether the accessed byte will be read or written. A read operation is selected if bit 7 is a 0 and a write operation is selected if bit 7 is a 1. The address map for the DS1670 is shown in Figure 3.

**ADDRESS/COMMAND BYTE** Figure 2

7	6	5	4	3	2	1	0
$\overline{RD}$ WR	A6	A5	A4	A3	A2	A1	A0

**DS1670 ADDRESS MAP** Figure 3

BIT 7						BIT 0						
00	0	10 SECONDS			SECONDS							
01	0	10 MINUTES			MINUTES							
02	0	12 24	10 HR A/P	10 HR	HOURS							
03	0	0	0	0	0	DAY						
04	0	0	10 DATE		DATE							
05	0	0	0	10	MONTH							
06	10 YEAR			YEAR								
07	M	10 SEC ALARM			SECONDS ALARM							
08	M	10 MIN ALARM			MINUTES ALARM							
09	M	12 24	10 HR A/P	10 HR	HOUR ALARM							
0A	M	0	0	0	DAY ALARM							
0B	CONTROL REGISTER											
0C	STATUS REGISTER											
0D	WATCHDOG REGISTER											
0E	ADC REGISTER											
0F	RESERVED											
7F												

## CLOCK, CALENDAR, AND ALARM

The time and calendar information is accessed by reading/writing the appropriate register bytes. Note that some bits are set to 0. These bits will always read 0 regardless of how they are written. Also note that registers 0 Fh to 7 Fh are reserved. These registers will always read 0 regardless of how they are written. The contents of the time, calendar, and alarm registers are in the Binary-Coded Decimal (BCD) format.

The DS1670 can run in either 12-hour or 24-hour mode. Bit 6 of the hours register is defined as the 12-hour or 24-hour mode select bit. When high, the 12-hour mode is selected. In the 12-hour mode, bit 5 is the AM/PM bit with logic 1 being PM. In the 24-hour mode, bit 5 is the second 10-hour bit (20-23 hours).

The DS1670 also contains a time of day alarm. The alarm registers are located in registers 07h to 0 Ah. Bit 7 of each of the alarm registers are mask bits (see Table 1). When all of the mask bits are logic 0, an alarm will occur once per week when the values stored in timekeeping registers 00h to 03h match the values stored in the time of day alarm registers. An alarm will be generated every day when mask bit of the day alarm register is set to 1. An alarm will be generated every hour when the day and hour alarm mask bits are set to 1. Similarly, an alarm will be generated every minute when the day, hour, and minute alarm mask bits are set to 1. When day, hour, minute, and seconds alarm mask bits are set to 1, an alarm will occur every second.

**TIME OF DAY ALARM BITS** Table 1

ALARM REGISTER MASK BITS (BIT 7)				DESCRIPTION
SECONDS	MINUTES	HOURS	DAYS	
1	1	1	1	Alarm once per second.
0	1	1	1	Alarm when seconds match.
0	0	1	1	Alarm when minutes and seconds match
0	0	0	1	Alarm when hours, minutes and seconds match.
0	0	0	0	Alarm when day, hours, minutes and seconds.

## SPECIAL PURPOSE REGISTERS

The DS1670 has two additional registers (control register and status register) that control the real-time clock and interrupts.

## CONTROL REGISTER

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
EOSC	WP	AIS1	AIS0	0	0	0	AIE

**EOSC (Enable Oscillator).** This bit when set to logic 0 will start the oscillator. When this bit is set to a logic 1, the oscillator is stopped and the DS1670 is placed into a low-power standby mode with a current drain of less than 200nA when in battery-backup mode. When the DS1670 is powered by V<sub>CC</sub>, the oscillator is always on regardless of the status of the EOSC bit; however, the real-time clock is incremented only when EOSC is a logic 0.

**WP (Write Protect).** Before any write operation to the real time clock or any other registers, this bit must be logic 0. When high, the write-protect bit prevents a write operation to any register.

**AIS0-AIS1 (Analog Input Select).** These 2 bits are used to determine the analog input for the analog-to-digital conversion. Table 2 lists the specific analog input that is selected by these two bits.

**AIE (Alarm Interrupt Enable).** When set to a logic 1, this bit permits the Interrupt Request Flag (IRQF) bit in the status register to assert INT. When the AIE bit is set to logic 0, the IRQF bit does not initiate the INT signal.

## ANALOG INPUT SELECTION Table 2

AIS1	AIS0	ANALOG INPUT
0	0	NONE
0	1	AIN0
1	0	AIN1
1	1	AIN2

## STATUS REGISTER

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
CU	LOBAT	0	0	0	0	0	IRQF

**CU (Conversion Update In Progress).** When this bit is a 1, an update to the ADC Register (register 0Eh) will occur within 488ms. When this bit is a 0, an update to the ADC Register will not occur for at least 244ms.

**LOBAT (Low Battery Flag).** This bit reflects the status of the backup power source connected to the V<sub>BAT</sub> pin. When V<sub>BAT</sub> is greater than 2.5V, LOBAT is set to a logic 0. When V<sub>BAT</sub> is less than 2.3 volts, LOBAT is set to a logic 1.

**IRQF (Interrupt Request Flag).** A logic 1 in the Interrupt Request Flag bit indicates that the current time has matched the time of day Alarm registers. If the AIE bit is also a logic 1, the INT pin will go high. IRQF is cleared by reading or writing to any of the alarm registers.

## POWER-UP DEFAULT STATES

These bits are set to a one upon initial power-up: EOSC, TD1 and TD0. These bits are cleared upon initial power-up: WP, AIS1, and AIS0.

## NONVOLATILE SRAM CONTROLLER

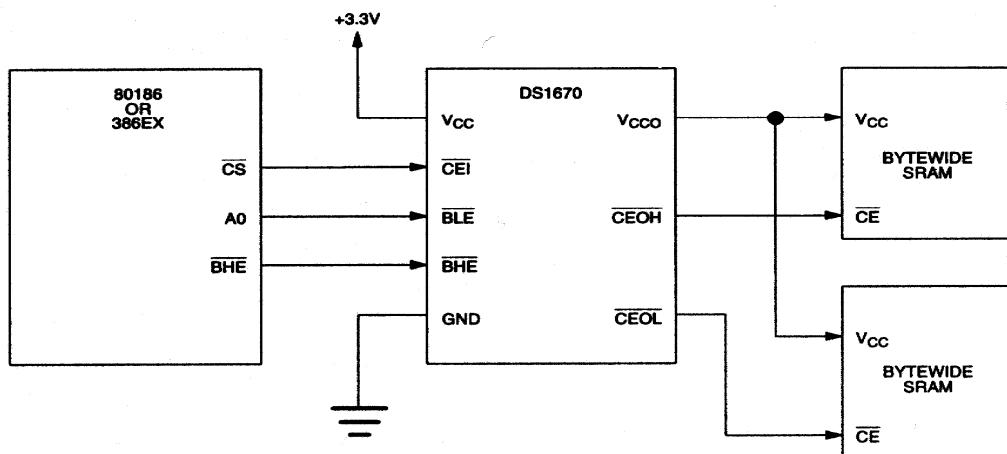
The DS1670 provides automatic backup and write protection for external SRAM. This function is provided by gating the chip enable signals and by providing a constant power supply through the V<sub>CC0</sub> pin. The DS1670 was specifically designed with the Intel 80186 and 386EX microprocessors in mind. As such, the DS1670 can provide access to the external SRAM in either byte-wide or word-wide format. This capability is provided by the chip enable scheme. Three input signals and two output signals are used for enabling the external SRAM(s) (see Figure 4). CEI (chip enable in), BHE (byte high enable), and BLE (byte low enable) are used for enabling either one or two external SRAMs through the CEOL (chip enable low) and the CEOH (chip enable high) outputs. Table 3 illustrates the function of these pins.

The DS1670 nonvolatilizes the external SRAM(s) by write protecting the SRAM(s) and by providing a back-up power supply in the absence of  $V_{CC}$ . When  $V_{CC}$  falls below 2.88V (typical), access to the external SRAM(s) are prohibited by forcing  $CEOL$  and  $CEOH$  high regardless of the level of  $CEI$ ,  $BLE$ , and  $BHE$ . Also at this point, the SRAM power supply ( $V_{CCO}$ ) is switched from  $V_{CC}$  to  $V_{BAT}$ . Upon power-up, access is prohibited until the end of  $t_{RPU}$ .

**EXTERNAL SRAM CHIP ENABLE** Table 3

$CEI$	$BHE$	$BLE$	$CEOL$	$CEOH$	FUNCTION
0	0	0	0	0	Word Transfer
0	0	1	1	0	Byte Transfer in upper half of data bus (D15-D8)
0	1	0	0	1	Byte Transfer in lower half of data bus (D7-D0)
0	1	1	1	1	External SRAMs disabled
1	X	X	1	1	External SRAMs disabled

**EXTERNAL SRAM INTERFACE (WORD-WIDE) TO THE DS1670** Figure 4



## MICROPROCESSOR MONITOR

The DS1670 monitors three vital conditions for a microprocessor: power supply, software execution, and external override.

First, a precision temperature-compensated reference and comparator circuit monitors the status of  $V_{CC}$ . When an out-of-tolerance condition occurs, an internal power-fail signal is generated which forces the  $RST$  pin to the active state, thus warning a processor-based system of impending power failure. The power-fail trip point is 2.88V (typical). When  $V_{CC}$  returns to an in-tolerance condition upon power-up, the reset signal is kept in the active state for 250ms (typical) to allow the power supply and microprocessor to stabilize. Note, however, that if the  $EOSC$  bit is set to a logic 1 (to disable the oscillator during battery-backup mode), the reset signal will be kept in an active state for 250ms plus the startup time of the oscillator.

The second monitoring function is pushbutton reset control. The DS1670 provides for a pushbutton switch to be connected to the  $RST$  output pin. When the DS1670 is not in a reset cycle, it continuously monitors the  $RST$  signal for a low-going edge. If an edge is detected, the DS1670 will debounce the

switch by pulling the RST line low. After the internal 250ms timer has expired, the DS1670 will continue to monitor the RST line. If the line is still low, the DS1670 will continue to monitor the line looking for a rising edge. Upon detecting release, the DS1670 will force the RST line low and hold it low for 250ms.

The third microprocessor monitoring function provided by the DS1670 is a watchdog timer. The watchdog timer function forces RST to the active state when the ST input is not stimulated within the predetermined time period. The time period is set by the Time Delay (TD) bits in the Watchdog Register. The time delay can be set to 250ms, 500ms, or 1000ms (see Figure 5). If TD0 and TD1 are both set to 0, the watchdog timer is disabled. When enabled, the watchdog timer starts timing out from the set time period as soon as RST is inactive. The default setting is for the watchdog timer to be enabled with 1000ms time delay. If a high-to-low transition occurs on the ST input pin prior to timeout, the watchdog timer is reset and begins to time-out again. If the watchdog timer is allowed to timeout, then the RST signal is driven to the active state for 250ms (typical). The ST input can be derived from microprocessor address signals, data signals, and/or control signals. To guarantee that the watchdog timer does not timeout, a high-to-low transition must occur at or less than the minimum period.

## WATCHDOG TIMEOUT CONTROL Figure 5

WATCHDOG REGISTER							
BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
0	0	0	0	0	0	TD1	TD0
WATCHDOG TIMEOUT							
TD1	TD0	WATCHDOG TIMEOUT					
0	0	Watchdog disabled					
0	1	250ms					
1	0	500ms					
1	1	1000ms					

## ANALOG-TO-DIGITAL CONVERTER

The DS1670 provides a 3-channel, 8-bit analog-to-digital converter. The ADC reference voltage (2.55V typical) is derived from an on-chip band-gap circuit. Three multiplexed analog inputs are provided through the AIN0, AIN1, and AIN2 pins. The ADC is monotonic (no missing codes) and uses a successive approximation technique to convert the analog signal into a digital code. An A/D conversion is the process of assigning a digital code to an analog input voltage. This code represents the input value as a fraction of the full-scale voltage (FSV) range. Thus, the FSV range is then divided by the ADC into 256 codes (8 bits). The FSV range is bounded by an upper limit equal to the reference voltage and the lower limit, which is ground. The DS1670 has a FSV of 2.55V (typical) that provides a resolution of 10mV. An input voltage equal to the reference voltage converts to FFh while an input voltage equal to ground converts to 00h. The relative linearity of the ADC is  $\pm 0.5$  LSB.

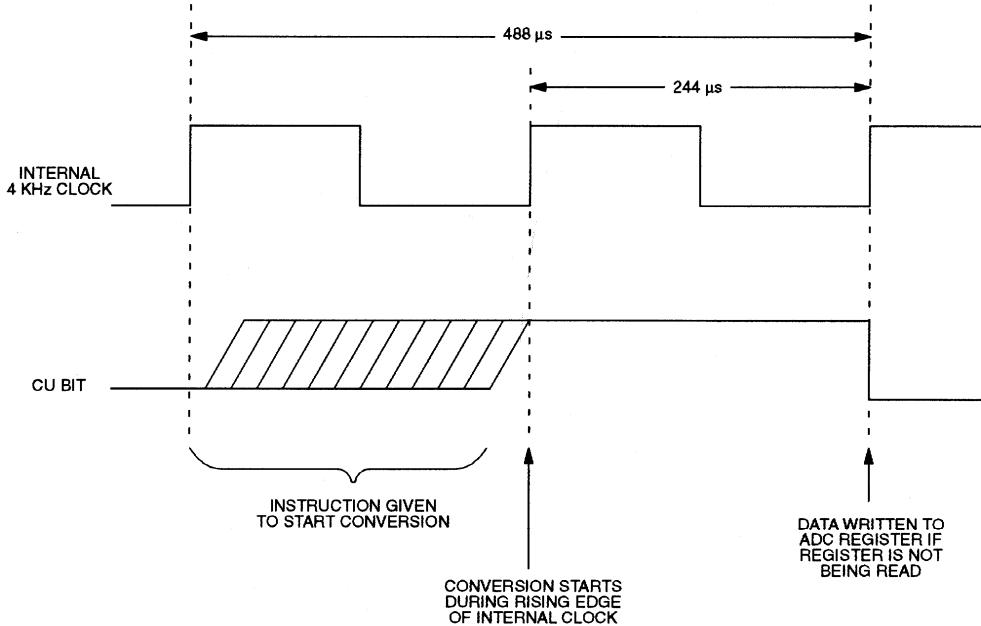
The ADC selects from one of three different analog inputs (AIN0–AIN2). The input that is selected is determined by the Analog Input Select (AIS) bits in the Control Register. Table 2 lists the specific analog

input that is selected by these 2 bits. Note also that the converter can be turned off by these bits to reduce power. When the ADC is turned on by setting AIS0 and AIS1 to any value other than 0,0 the analog input voltage is converted and written to the ADC Register within 488ms. An internal analog filter at the input reduces high frequency noise. Subsequent updates occur approximately every 10ms. If AIS0 and/or AIS1 are changed, updates will occur at the next 10ms conversion time.

The Conversion Update In Progress (CU) bit in the Status Register indicates when the ADC Register can be read. When this bit is a 1, an update to the ADC Register will occur within 488ms maximum. However, when this bit is 0 an update will not occur for at least 244ms. The CU bit should be polled before reading the ADC Register to ensure that the contents are stable during a read cycle. Once a read cycle to the ADC Register has been started, the DS1670 will not update that register until the read cycle has been completed. It should also be mentioned that taking CS low will abort the read cycle and will allow the ADC Register to be updated.

Figure 6 illustrates the timing of the CU bit relative to an instruction to begin conversion and the completion of that conversion.

### CU BIT TIMING Figure 6



### 3-WIRE SERIAL INTERFACE

Communication with the DS1670 is accomplished through a simple 3-wire interface consisting of the Chip Select (CS), Serial Clock (SCLK) and Input/Output (I/O) pins.

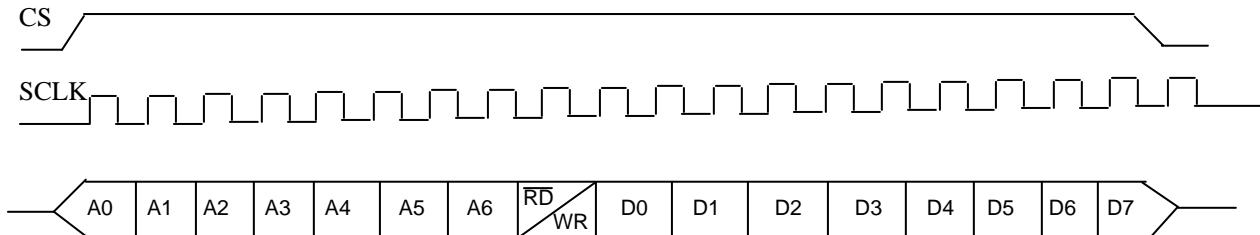
All data transfers are initiated by driving the CS input high. The CS input serves two functions. First, CS turns on the control logic, which allows access to the shift register for the address/command sequence. Second, the CS signal provides a method of terminating either single byte or multiple byte (burst) data transfer. A clock cycle is a sequence of a rising edge followed by a falling edge. For data input, data must be valid during the rising edge of the clock and data bits are output on the falling edge of the clock. If the CS input goes low, all data transfer terminates and the I/O pin goes to a high-impedance state.

Address and data bytes are always shifted LSB first into the I/O pin. Any transaction requires the address/command byte to specify a read or write to a specific register followed by one or more bytes of data. The address byte is always the first byte entered after CS is driven high. The most significant bit ( $\overline{RD/WR}$ ) of this byte determines if a read or write will take place. If this bit is 0, one or more read cycles will occur. If this bit is 1, one or more write cycles will occur.

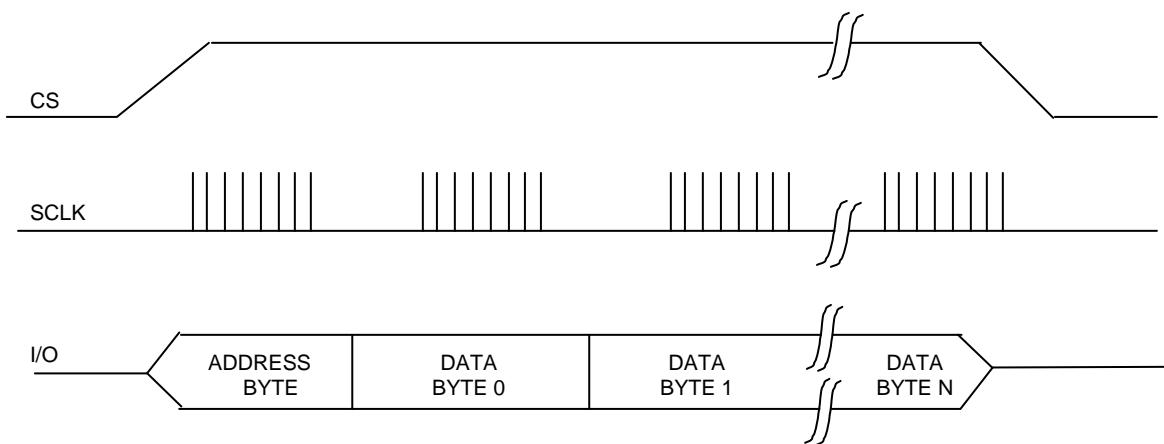
Data transfers can occur 1 byte at a time or in multiple-byte burst mode. After CS is driven high an address is written to the DS1670. After the address, one or more data bytes can be read or written. For a single-byte transfer 1 byte is read or written and then CS is driven low. For a multiple-byte transfer, multiple bytes can be read or written to the DS1670 after the address has been written. Each read or write cycle causes the register address to automatically increment. Incrementing continues until the device is disabled. After accessing register 0Eh, the address wraps to 00h.

Data transfer for single-byte transfer and multiple-byte burst transfer is illustrated in Figures 7 and 8.

### SINGLE-BYTE DATA TRANSFER Figure 7



### MULTIPLE-BYTE BURST TRANSFER Figure 8



## ABSOLUTE MAXIMUM RATINGS

Voltage on Any Pin Relative to Ground.....	-0.3V to +6V
Operating Temperature.....	0°C to +70°C
Storage Temperature.....	-55°C to +125°C
Soldering Temperature.....	See IPC/JEDEC J-STD-020 Specification

*This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect device reliability.*

## RECOMMENDED DC OPERATING CONDITIONS

( $T_A = 0^\circ\text{C}$  to  $+70^\circ\text{C}$ )

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Power-Supply Voltage	$V_{CC}$	2.97	3.3	3.63	V	1
Input Logic 1	$V_{IH}$	2.0		$V_{CC} + 0.3$	V	1
Input Logic 0	$V_{IL}$	-0.3		+0.8	V	1
Battery Voltage	$V_{BAT}$	2.5		3.7	V	1

**DC ELECTRICAL CHARACTERISTICS**  $(T_A = 0^\circ\text{C} \text{ to } +70^\circ\text{C})$ 

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Input Leakage	$I_{LI}$	-1		+1	$\mu\text{A}$	
CS Leakage	$I_{LO}$			150	$\mu\text{A}$	7
Logic 1 Output ( $I_{out} = -0.4 \text{ mA}$ )	$V_{OH}$	2.4			V	2
Logic 0 Output ( $I_{out} = 1.5 \text{ mA}$ )	$V_{OL}$			0.4	V	3
Active Supply Current (CS = $V_{CC} - 0.2$ )	$I_{CCA}$		0.75	1.0	mA	4
A/D Converter Current	$I_{ADC}$			200	$\mu\text{A}$	5
Standby Current (CS = $V_{IL}$ )	$I_{CCS}$			100	$\mu\text{A}$	6
Battery Current (Oscillator On)	$I_{BAT1}$		300	500	nA	
Battery Current (Oscillator Off)	$I_{BAT2}$			200	nA	
Internal RST Pull-up Resistor	$R_P$	35	47	60	$\text{k}\Omega$	
$V_{CC}$ Trip Point	$V_{CCTP}$	2.80	2.88	2.97	V	
$V_{CC}$ Switchover	$V_{CCSW}$	2.62	2.70	2.78	V	12
A/D Reference Voltage	$V_{ADC}$	2.47	2.55	2.63	V	
Pushbutton Detect	$PB_{DV}$	0.8		2.0	V	
Pushbutton Release	$PB_{RD}$		0.3	0.8	V	
Output Voltage	$V_{CCO}$	$V_{CC} - 0.3$			V	11
$V_{CCO}$ Output Current (Source = $V_{CC}$ )	$I_{CCO1}$			100	mA	13
$V_{CCO}$ Output Current (Source = $V_{BAT}$ )	$I_{CCO2}$			150	$\mu\text{A}$	14

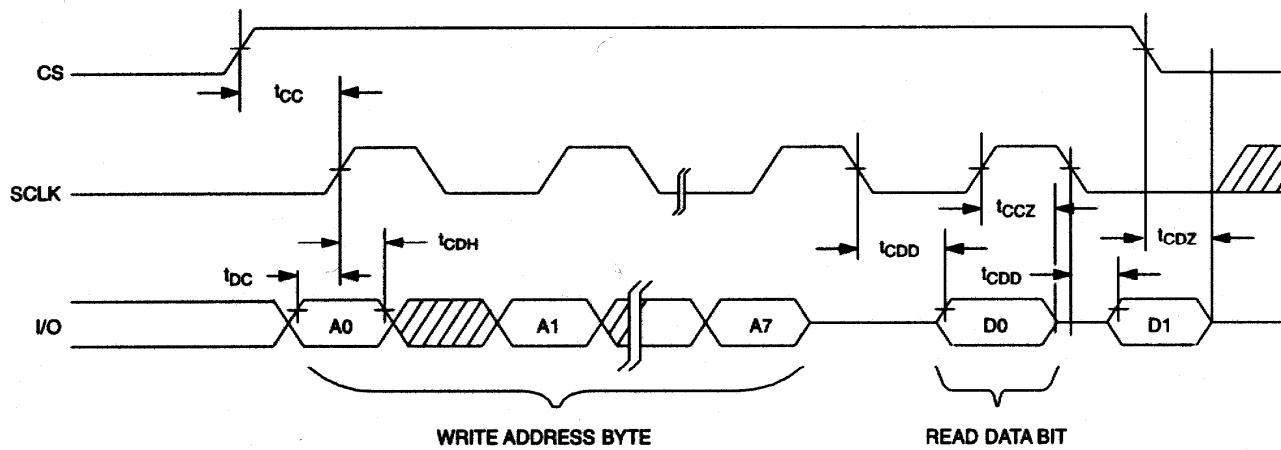
**CAPACITANCE**  $(T_A = +25^\circ\text{C})$ 

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Input Capacitance	$C_I$		10		pF	
I/O Capacitance	$C_{I/O}$		15		pF	
Crystal Capacitance	$C_X$		6		pF	

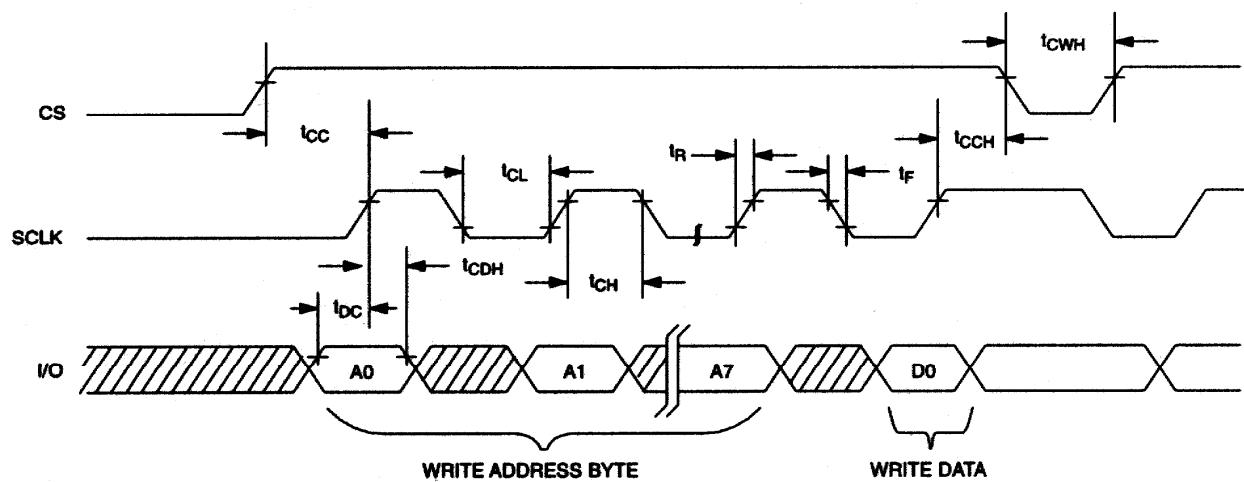
**AC ELECTRICAL CHARACTERISTICS** ( $V_{CC} = 3.3V \pm 10\%$ ,  $T_A = 0^\circ C$  to  $+70^\circ C$ .)

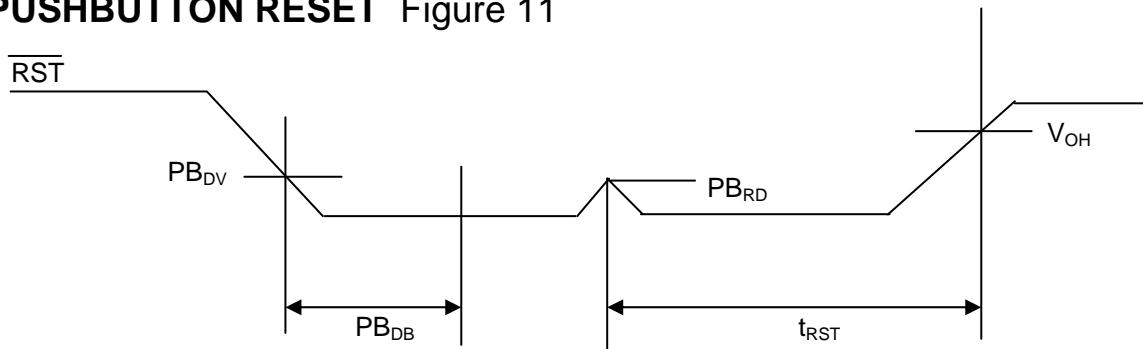
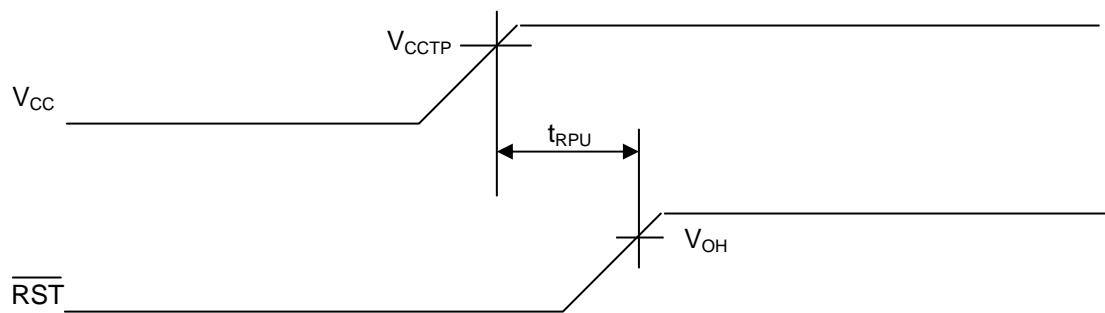
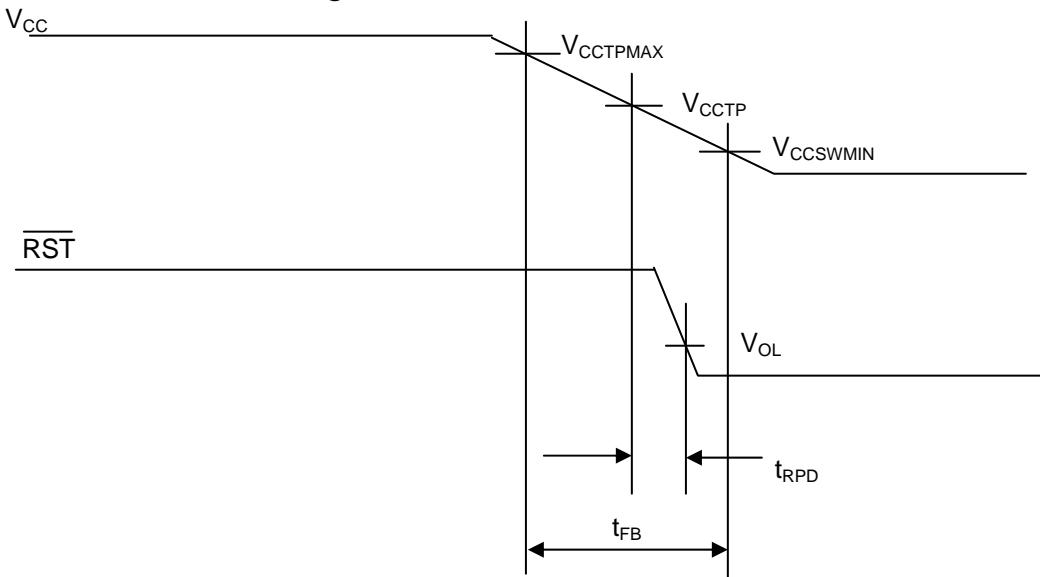
PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Data to Clock Setup	$t_{DC}$	100			ns	8
CLK to Data Hold	$t_{CDH}$	140			ns	8
CLK to Data Delay	$t_{CDD}$			400	ns	8, 9, 10
CLK to Low Time	$t_{CL}$	500			ns	8
CLK to High Time	$t_{CH}$	500			ns	8
CLK Frequency	$t_{CLK}$			1.0	MHz	8
CLK Rise and Fall	$t_R, t_F$			1000	ns	
CS to CLK Setup	$t_{CC}$	2			$\mu s$	8
CLK to CS Hold	$t_{CCH}$	120			ns	8
CS Inactive Time	$t_{CWH}$	2			$\mu s$	8
CS to I/O High-Z	$t_{CDZ}$			140	ns	8
SCLK to I/O High-Z	$t_{CCZ}$			140	ns	8
$V_{CC}$ Slew Rate (2.85V to 2.3V)	$t_F$	300			$\mu s$	
$V_{CC}$ Slew Rate (2.3V to 2.85V)	$t_R$	0			ns	
$V_{CC}$ Detect to $\overline{RST}$ ( $V_{CC}$ Falling)	$t_{RPD}$			100	ns	
Reset Active Time	$t_{RST}$		250		ms	15
Pushbutton Debounce	$PB_{DB}$		250		ms	15
$V_{CC}$ Detect to $\overline{RST}$ ( $V_{CC}$ Rising)	$t_{RPU}$		250		ms	15, 16
$\overline{ST}$ Pulse Width	$t_{ST}$	20			ns	
Chip Enable Propagation Delay to External SRAM	$t_{CED}$		8	15	ns	
Nominal Voltage to $V_{CC}$ Switchover Fall Time	$t_{FB}$	200			$\mu s$	

## TIMING DIAGRAM: READ DATA Figure 9



## TIMING DIAGERAM: WRITE DATA Figure 10



**PUSHBUTTON RESET** Figure 11**POWER-UP** Figure 12**POWER-DOWN** Figure 13

**NOTES:**

1. All voltages are referenced to ground.
2. Logic 1 voltages are specified at  $V_{CC} = 3.3V$ ,  $V_{OH} = V_{CC}$  for capacitive loads. Excludes  $\overline{RST}$  pin.
3. Logic 0 voltages are specified at  $V_{CC} = 3.3V$ ,  $V_{OL} = GND$  for capacitive loads.
4.  $I_{CCA}$  is specified with outputs open, CS set to a logic 1, SCLK = 500kHz, oscillator enabled, and DAC enabled.
5.  $I_{ADC}$  is specified with CS,  $V_{CCO}$  open and I/O, SCLK at logic 0. ADC is enabled.
6.  $I_{CCS}$  is specified with CS,  $V_{CCO}$  open and I/O, SCLK at logic 0. ADC is disabled.
7. CS has a  $40k\Omega$  pulldown resistor to ground.
8. Measured at  $V_{IH} = 2.0V$  or  $V_{IL} = 0.8V$  and 10ns maximum rise and fall time.
9. Measured at  $V_{OH} = 2.4V$  or  $V_{OL} = 0.4V$ .
10. Load capacitance = 50 pF.
11.  $I_{CCO} = 100$  mA,  $V_{CC} > V_{CCTP}$ .
12.  $V_{CCO}$  switchover from  $V_{CC}$  to  $V_{BAT}$  occurs when  $V_{CC}$  drops below the lower of  $V_{CCSW}$  and  $V_{BAT}$ .
13. Current from  $V_{CC}$  input pin to  $V_{CCO}$  output pin.
14. Current from  $V_{BAT}$  input pin to  $V_{CCO}$  output pin.
15. Time base is generated by very accurate crystal oscillator. Accuracy of this time period is based on the crystal that is used. A typical crystal with a specified load capacitance of 6pF will provide an accuracy within  $\pm 100$ ppm over the  $0^{\circ}\text{C}$  to  $+70^{\circ}\text{C}$  temperature range.
16. If the  $\overline{EOSC}$  bit in the Control Register is set to a logic 1,  $t_{RPU}$  is equal to 250ms plus the startup time of the crystal oscillator.

**PACKAGE INFORMATION**

For the latest package outline information and land patterns, go to [www.maxim-ic.com/packages](http://www.maxim-ic.com/packages).

PACKAGE TYPE	PACKAGE CODE	DOCUMENT NO.
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20 SO	W20+1	<a href="#">21-0042</a>

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