LTC6430-15
50MHz to 1200MHz Parallel Connected, Boosted OIP3, ADC/IF Amplifier

DESCRIPTION

Demonstration circuit 2090A features two LTC®6430-15s differential ADC/IF Amplifier connected in parallel at the inputs and outputs, boosting the output third order intercept point (OIP3) and the output power each by about 3dB higher. The parallel connection reduces the differential input and output impedance by one-half so the composite amplifier has 50Ω differential input and output impedances, this demo circuit uses 1:1 balun transformers to convert the differential I/O impedances to 50Ω single-ended so that the DC2090A can be easily evaluated with most RF test equipment.

Design files for this circuit board are available at http://www.linear.com/demo/DC2090A

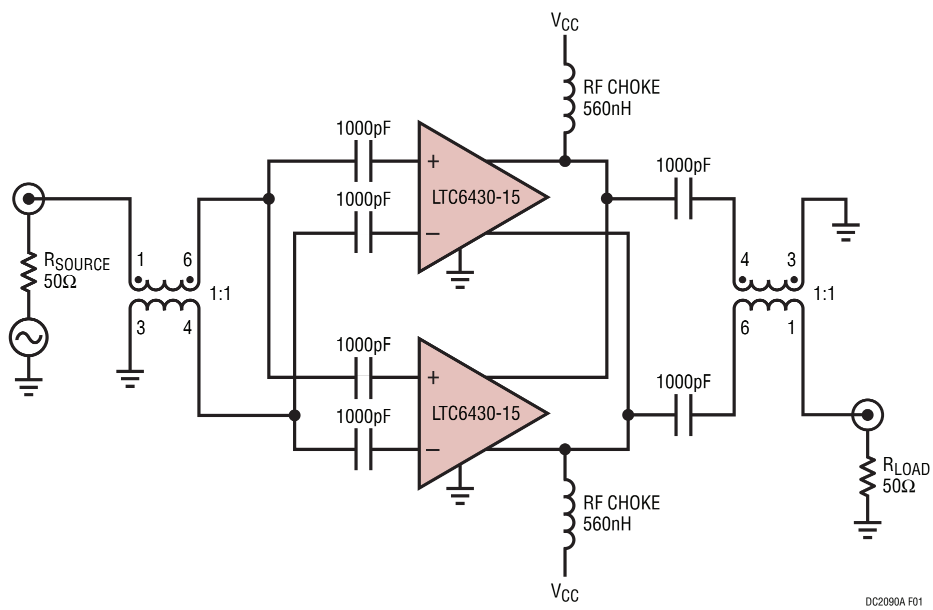


Figure 1. DC2090A Two LTC6430-15s in Parallel Simplified Schematic

PERFORMANCE SUMMARY Specifications are at T_A = 25°C

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Power Supply						
V_{CC}	Operating Supply Range	All V_{CC} Pins Plus ±OUT	4.75		5.25	V
I_{CC}	Current Consumption	Total Current		330		mA

FREQUENCY (MHZ)	POWER GAIN |S21| (dB)	OUTPUT THIRD ORDER INTERCEPT POINT * OIP3 (dBm)	OUTPUT THIRD ORDER INTERMODULATION* OIM3 (dBc)	SECOND HARMONIC DISTORTION** HD2 (dBc)	THIRD HARMONIC DISTORTION ** HD3 (dBc)	OUTPUT 1DB COMPRESSION POINT P1DB (dBm)	NOISE FIGURE‡ NF (dB)
50	13.4	49.7	–95.5	–84.6	–95.4	25.4	6.33
100	14.6	49.9	–95.7	–84.2	–96.4	25.5	4.14
200	14.8	51.0	-98.1	–84.3	–95.1	25.2	3.46
300	14.5	51.3	–98.6	–79.4	–88.0	25.7	4.10
400	14.1	50.8	–97.6	–82.7	–81.8	25.0	4.55
500	13.9	48.8	–93.6	–79.8	–78.6†	24.6	4.55
600	13.9	45.2	–96.4	–71.7	–80.8†	24.1	4.68
700	13.7	44.6	–85.2	–73.2†	–78.0†	24.0	5.05
800	13.8	43.2	–82.3	–70.8†	–76.7†	23.3	5.33
900	12.8	42.4	–80.8	–74.4†	–76.4†	23.3	5.52
1000	12.5	42.1	–80.3	–70.2†	–71.9†	23.3	5.61
1100	12.4	41.9	–79.9	–67.7†	–68.7†	23.5	5.77
1200	12.5	43.8	–83.6	–65.6†	–72.6†	23.5	6.08

Note: All figures are referenced to J1 (input port) and J4 (output port)

* Two-tone test conditions: Output power level = 5dBm/tone, tone spacing = 1MHz

** Single-tone test conditions: Output power level = 6dBm

† Outside of input and output transformers' working frequency range

‡ Small signal noise figure

OPERATION

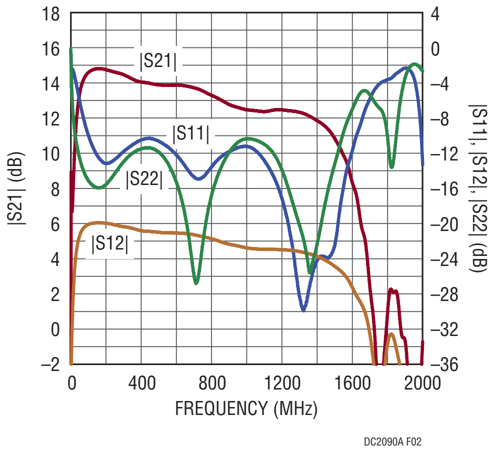


Figure 2. Demo Board S-Parameters

DC2090A is a high linearity, fixed gain amplifier. It is designed for ease of use. The demo circuit contains two LTC6430-15s that are connecting in parallel at each pair of inputs and outputs. Each of the individual LTC6430-15s is internally matched to 100Ω differential source and load impedance from 20MHz to 1400MHz. When connected in parallel, the impedance becomes 50Ω differential. Most test equipment have 50Ω single-ended input. To make measurement compatible, the 1:1 balun transformers have been added to convert the amplifier differential impedances to single-ended 50Ω. The other advantage of the parallel connection is that it gives higher output power and OIP3 by about 3dB each. Note that these devices are cross connected to improve the matching of the two 180º paths. It is very important that the two paths match to achieve the best 2nd and 3rd order harmonic suppression. The frequency range of the circuit is limited by the balun transformers. Hence, this demo board optimizes the amplifiers performance over the frequency range from 50MHz to 1200MHz. Figure 2 shows the DC2090A's two port S-Parameters.

The demo board requires a minimum of passive support components. At the board's input and output are the balun transformers. Each of these transformers (T1, T2) has a 1:1 impedance transformation ratio. The shunt capacitors (C18 and C19) help to match the input/output signals.

A pair of stability networks has been added to ensure low frequency stability. They consist of a 120pF capacitor (C5 and C8) and 174Ω resistor (R4 and R7) in parallel at the LTC6430-15's input network. Note that the input stability network does degrade performance below 150MHz. Low frequency performance can be improved by increasing the value of the capacitors (C5 and C8).

The input and output DC-blocking capacitors (C4, C10, C14, C15, C16 and C17) are required because this device is internally DC-biased for optimal operation. The frequency appropriate RF chokes (L1 and L2) and the de-coupling capacitors (C2, C3, C11 and C12) provide the proper DC bias to the RF ± OUT ports. A single 5V supply is required for the V_{CC} pins on the device.

L3, L4, C6 and C20 are optional components. They are for additional matching when further optimization to a lower or wider frequency range applications is required.

The T_DIODE1 and T_DIODE2 turrets (E1 and E3) can be forward biased to ground with 1mA of current. The measured voltage will be an indicator of the chip junction temperature (T_J).

Please note that a number of DNC pins are connected on the demo board. These connections are not necessary for normal operation, however, failure to float these pins may impair the operation of the device.

Table 2. DC2090A Board I/O Descriptions

CONNECTOR	FUNCTION
J1 (IN)	Single-ended input. Impedance matched to 50Ω. Drive from a 50Ω Network Analyzer or signal source.
J4 (OUT)	Single-ended output. Impedance matched to 50Ω. Drives a 50Ω network analyzer or spectrum analyzer
E1, (T_DIODE1)	The measured voltage will be an indicator of the chip junction temperature, U1
E3, (T_DIODE2)	The measured voltage will be an indicator of the chip junction temperature, U2
E2 , J5 (V_{CC})	Positive supply voltage source
E4, J6 (GND)	Supply ground

ADDITIONAL INFORMATION

As with any RF device, minimizing ground inductance is critical. Care should be taken during the board layout when using these exposed pad packages. A maximum of small-diameter vias should be placed underneath the exposed ground pad. This will ensure a good RF ground and low thermal impedance. Maximizing the copper ground plane will also improve heat spreading and lower the inductance to ground. It is a good idea to cover the via holes with solder mask on the back side of the PCB to prevent solder from wicking away from the critical PCB to the exposed pad interface.

The DC2090A is a wide bandwidth demo board, but it is not intended for operation down to DC. The lower frequency cutoff is limited by on-chip matching elements.

Table 3 shows the LTC643X-YY amplifier series and its associated demo boards. Each demo board lists the typical working frequency range and the input and output impedance of the amplifiers.

SETUP SIGNAL SOURCES AND SPECTRUM ANALYZER

The LTC6430-15 is an amplifier with high linearity performance. Therefore, the output intermodulation products are very low. Even using high dynamic range test equipment, third-order intercept (IP3) measurements can drive test setups to their limits. Consequently, accurate measurement of IP3 for a low distortion IC such as the LTC6430-15 requires certain precautions to be observed in the test setup as well as the testing procedure.

Table 3. The LTC643X-YY Amplifier Family and Corresponding Application Demo Boards

DEMO BOARD NUMBER	FREQUENCY RANGE (MHZ)	NOTES/APPLICATIONS	BOARD'S IN/OUT IMPEDANCE	AMPLIFIER	AMPLIFIER'S IMPEDANCE
DC1774A-A	50 to 350	Low Frequency	50Ω	LTC6430-15	Differential 100Ω
DC1774A-B	400 to 1000	Mid Frequency	50Ω	LTC6430-15	Differential 100Ω
DC1774A-C	100 to 1200	Wide Frequency	50Ω	LTC6431-15	Single-Ended 50Ω
DC2032A	50 to 1000	Cable Infrastructure	75Ω	LTC6430-15	Differential 100Ω
DC2077A	100 to 1200	Wide Frequency	50Ω	LTC6431-20	Single-Ended 50Ω
DC2153A	700 to 1700	High Frequency	50Ω	LTC6430-15	Differential 100Ω
DC2090A	50 to 1200	Power Doubler	50Ω	Dual LTC6430-15	Differential 50Ω

ADDITIONAL INFORMATION

SETUP SIGNAL SOURCES

Figure 3 shows a proposed IP3 test setup. This setup has low phase noise, good reverse isolation, high dynamic range, sufficient harmonic filtering and wideband impedance matching. The setup is outlined below:

a. High performance signal generators 1 and 2 (HP8644A) are used. These suggested generators have low harmonic distortion and very low phase noise.

b. High linearity amplifiers are used to improve the reverse isolation. This prevents cross talk between the two signal generators and provides higher output power.

c. A low pass filter is used to suppress the harmonic content from interfering with the test signal. Note that second order inputs can "mix" with the fundamental frequency to form intermodulation (IM) products of their own. We suggest filtering the harmonics to –50dBc or better.

d. The signal combiner from mini-circuits (ADP-2-9) combines the two isolated input signals. This combiner has a typical isolation of 27dB. For improved VSWR and isolation, the H-9 signal combiner from MA/COM is an alternative which features >40dB isolation and a wider frequency range. Passive devices (e.g. combiners) with magnetic elements can contribute nonlinearity to the signal chain and should be used cautiously.

e. The attenuator pads on all three ports of the signal combiner will further support isolation of the two input signal sources. They also reduce reflections and promote maximum power transfer with wideband impedance matching.

SETUP THE SPECTRUM ANALYZER

a. Adjust the spectrum analyzer for maximum possible resolution of the intermodulation products' amplitude in dBc. A narrower resolution bandwidth will take a longer time to sweep.

b. Optimize the dynamic range of the spectrum analyzer by adjusting the input attenuation. First, increase the spectrum analyzer's input attenuation (normally in steps of 5dB or 10dB). If the IM product levels decrease when the input attenuation is increased, then the input power level is too high for the spectrum analyzer to make a valid measurement. Most likely, the spectrum analyzer's 1st mixer was overloaded and producing its own IM products. If the IM reading holds constant with increased input attenuation, then a sufficient amount of attenuation was present. Adding too much attenuation will bury the intended IM signal in the noise floor. Therefore, select just enough attenuation to achieve a stable and valid measurement.

c. In order to achieve this valid measurement result, the test system must have lower total distortion than the DUT's intermodulation. For example, to measure 51dBm OIP3, the measured intermodulation products will be –92dBc below a –15dBm/tone input level and the test system must have intermodulation products approximately –98dBc or better. For best results, the IM products and noise floor should measure at least –102dBc before connecting the DUT.

QUICK START PROCEDURE

DC2090A can be set up to evaluate the performance of the LTC6430-15. Refer to Figure 3 for proper equipment connections and follow the procedure below:

TWO-TONE MEASUREMENT

Connect all test equipment as suggested in Figure 3.

1. The power labels of V_{CC} 4.75V to 5.25V and GND directly correspond to the power supply. Typical current consumption for two LTC6430-15s is about 330mA.
2. Apply two independent signals f1 and f2 from signal generator 1 and signal generator 2 at 300MHz and 301MHz, while setting the amplitude to –9dBm/tone at the demo board input (J1).
3. Monitor the output tone level on the spectrum analyzer. Adjust the signal generator levels such that the output power measures 5dBm/tone at the amplifier output J2, after correcting for external cable losses and attenuations.
4. Change the spectrum analyzer's center frequency and observe the two IM3 tones at 1MHz below and above the input frequencies. The frequencies of IM3_LOW and IM3_HIGH are 299MHz and 302MHz, respectively. The measurement levels should be approximately –92dBc; +51dBm is typical OIP3 performance for the demo board DC2090A at 300MHz.

   The OIP3 calculation is:

   $$OIP3 = P_{OUT} + \Delta IMD3/2$$

   where P_{OUT} is the lower output signal power of the fundamental products.

   $\Delta IMD3 = P_{OUT} - P_{IM3}$; P_{IM3} is the higher third-order intermodulation product.

SINGLE-TONE MEASUREMENT

5. Continue with step 4 above, turn off one signal source to measure gain and harmonic distortions.

QUICK START PROCEDURE

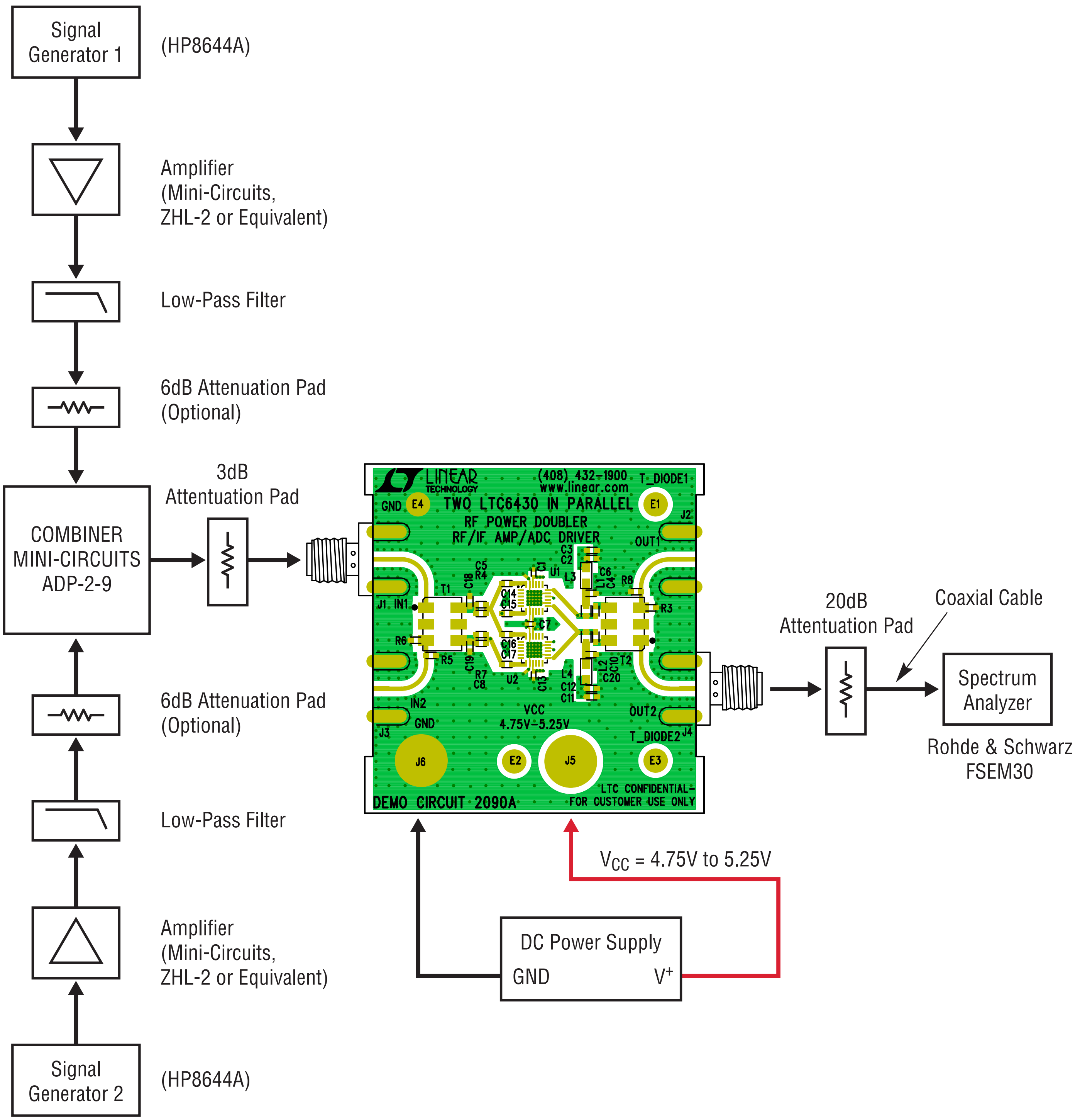
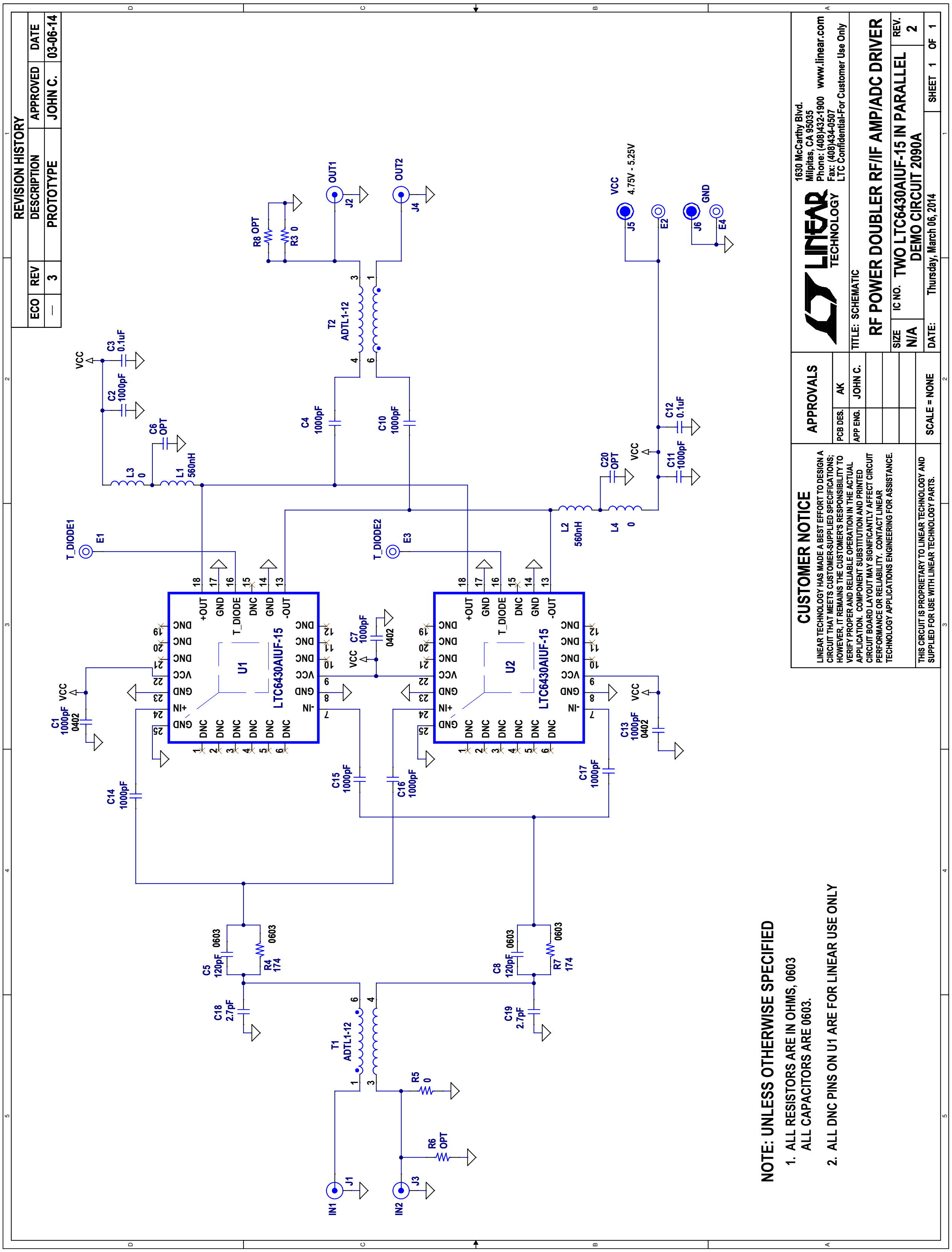


Figure 3. Proper Equipment Setup for IP3 Measurement

PARTS LIST

ITEM	QTY	REFERENCE	PART DESCRIPTION	MANUFACTURER/PART NUMBER
1	3	C1, C7, C13	CAP., X7R, 1000pF, 50V 5%, 0402	AVX, 04025C102JAT2A
2	8	C2, C4, C10, C11, C14–C17	CAP., X7R, 1000pF, 50V 5%, 0603	AVX, 06035C102JAT2A
3	2	C3, C12	CAP., X5R, 0.1µF, 10V, 10%, 0603	AVX, 0603ZD104KAT2A
4	2	C5, C8	CAP., NPO, 120pF, 50V, 5%, 0603	AVX, 06035A121JAT
5	2	C18, C19	CAP., NPO, 2.7pF, 50V, ±0.25pF, 0603	AVX, 06035A2R7CAT1A
6	0	C6, C20	CAP., 0603, OPT	
7	4	E1-E4	TESTPOINT, TURRET, .093"	MILL-MAX, 2501-2-00-80-00-00-07-0
8	2	J1, J4	CONN., SMA 50Ω EDGE-LAUNCH	E.F.JOHNSON, 142-0701-851
9	0	J2, J3	CON., OPT	
10	2	J5, J6	JACK, BANANA	KEYSTONE, 575-4
11	2	L1, L2	INDUCTOR, CHIP, 560nH, 5%, 0603LS-1608	COILCRAFT, 0603LS-561XJLB
12	2	L3, L4	INDUCTOR, CHIP, 0Ω, 0805	
13	2	R3, R6	RES., CHIP, 0Ω, 0603	VISHAY, CRCW06030000Z0ED
14	0	R5, R8	RES., OPT	
15	2	R4, R7	RES., CHIP, 174Ω, 1%, 0603	VISHAY, CRCW0603174RFKED
16	2	T1, T2	RF TRANSFORMER, CASE STYLE CD542	MINI-CIRCUITS, ADTL1-12+
17	2	U1, U2	BALANCED AMPLIFIER LTC6430AIUF-15, QFN24UF-4X4	LINEAR TECH., LTC6430AIUF-15

SCHEMATIC DIAGRAM



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