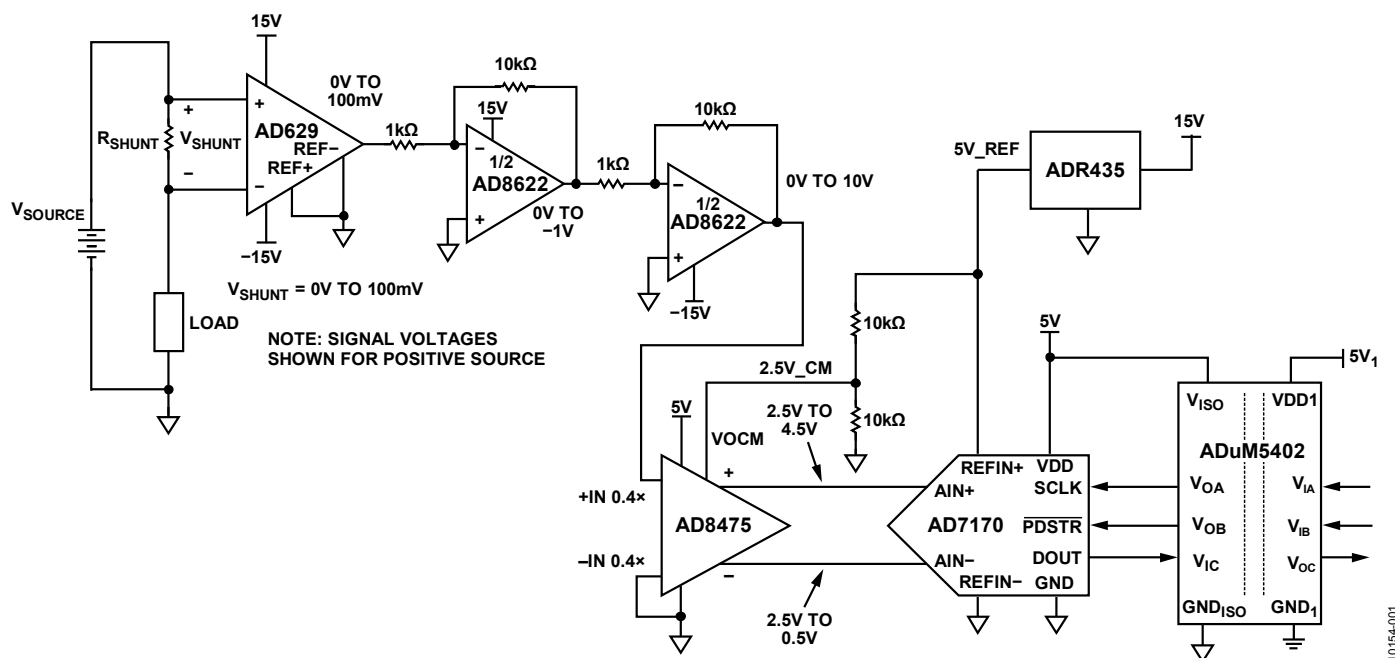


Devices Connected/Referenced	
AD629	High Common-Mode Voltage Difference Amplifier
AD8622	Precision, Low Noise, CMOS, Dual, Rail-to-Rail Output Op Amp
AD8475	Precision, Selectable Gain, Fully Differential Funnel Amplifier
ADuM5402	Quad-Channel Isolator with Integrated DC-to-DC Converter
ADR435	5 V, Low Noise, High Accuracy, XFET Voltage Reference
AD7170	12-Bit, Low Power Σ - Δ ADC



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The [AD629](#) amplifier accurately measures and buffers ($G = 1$) a small differential input voltage and rejects large positive common-mode voltages up to 270 V.

The dual [AD8622](#) is used to amplify the output of the [AD629](#) by a factor of 100. The [AD8475](#) funnel amplifier attenuates the signal ($G = 0.4$), converts it from single-ended to differential, and level shifts the signal to satisfy the analog input voltage range of the [AD7170](#) sigma-delta ADC.

Galvanic isolation is provided by the [ADuM5402](#) quad channel isolator. This is not only for protection but also to isolate the downstream circuitry from the high common-mode voltage. In addition to isolating the output data, the [ADuM5402](#) digital isolator can supply isolated +5.0 V for the circuit.

The measurement result from the [AD7170](#) is provided as a digital code utilizing a simple 2-wire, SPI-compatible serial interface.

This combination of parts provides an accurate high voltage positive and negative rail current sense solution with a small component count, low cost, and low power.

CIRCUIT DESCRIPTION

The circuit is designed for a full-scale shunt voltage of 100 mV at maximum load current I_{MAX} . Therefore, the value of the shunt resistor is $R_{SHUNT} = (500 \text{ mV})/(I_{MAX})$.

The [AD629](#), shown in Figure 2, is a difference amplifier designed with internal thin film resistors allowing continuous common-mode signals up to ± 270 V with transient protection to ± 500 V. For $REF(+)$ and $REF(-)$ grounded, the signal on the $+IN$ terminal is attenuated by a factor of 20. The signal is then amplified by a noise gain of 20, restoring the original amplitude at the output.

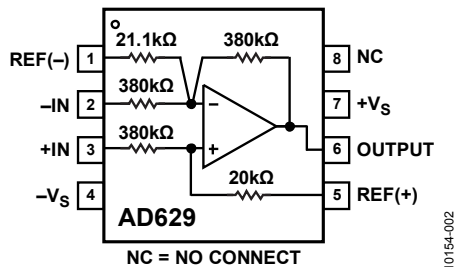


Figure 2. AD629 High Common-Mode Voltage Difference Amplifier

The CMRR is 77 dB minimum @ 500 Hz for the [AD629A](#), and 86 dB minimum @ 500 Hz for the [AD629B](#).

In order to maintain the desired common-mode rejection, there are several important conditions to meet. First, the ability of

the part to reject these common-mode signals is determined by the power supply voltage as shown in Figure 3. Failure to implement dual supplies of a sufficient voltage will reduce the common-mode rejection.

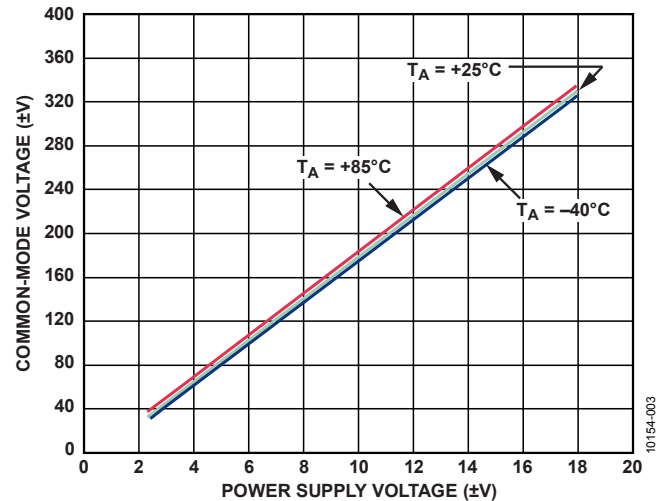


Figure 3. AD629 Common-Mode Voltage Range vs. Power Supply Voltage

Secondly, the [AD629](#) should only be operated in the unity gain mode using the internal matched thin film resistors. Changing the gain with external resistors will degrade the common-mode rejection due to mismatch errors.

The [AD8622](#) is a CMOS low power, precision, dual, rail-to-rail output op amp used primarily for amplifying the signal of interest.

By cascading two inverting gain stages with a gain of -10 , the 100 mV full-scale output of the [AD629](#) is amplified by a factor of 100 yielding a 10 V full-scale signal. These values can be either positive or negative, depending on the direction of the current.

The dual supplies of the [AD8622](#) allow both the input and output signals to swing above and below ground as required to measure bidirectional input currents.

In the final stage of the signal chain before conversion into a digital word, the [AD8622](#) output voltage is conditioned to fit the analog input voltage range of the ADC.

The [AD8475](#) "funnel amplifier," shown in Figure 4, provides two optional attenuation factors (0.4 and 0.8). In addition, the signal is converted into a differential one, and the common-mode voltage at the output is determined by the voltage on the VOCM pin. With a single 5 V supply, the analog input voltage range is ± 12.5 V (for a single-ended input).

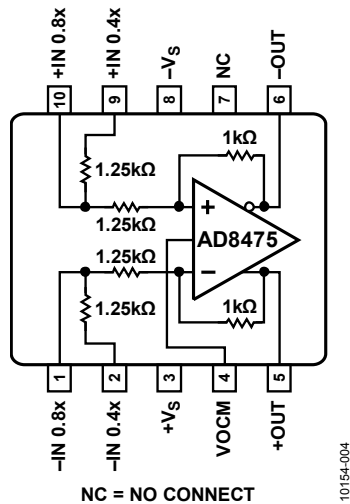


Figure 4. AD8475 Funnel Amplifier

As shown in Figure 1, the output common-mode voltage is set at 2.5 V by a resistor divider driven by the [ADR435](#) reference output of 5 V.

The primary source of noise in the system is the output noise of the AD629 of 15 μV p-p in the 0.1 Hz to 10 Hz bandwidth. For a 100 mV full-scale signal, this corresponds to a noise-free code resolution of

$$\text{Noise Free Code Resolution} = \log_2 \left(\frac{100\text{mV}}{15\mu\text{V}} \right) = \log_2(6666) = 12.7 \text{ bits}$$

The input noise of the AD8622 is only 0.2 μV p-p, which is negligible compared to the AD629. The output noise of the AD8475 is 2.5 μV p-p, which is also negligible at that point where the full-scale signal level is 4 V p-p.

Notice that the power supply voltage for the [AD7170](#) is supplied by the isolated power output (+5.0 V_{ISO}) of the ADuM5402 quad isolator.

The reference voltage for the [AD7170](#) is supplied by the [ADR435](#) precision XFET® reference. The [ADR435](#) has an initial accuracy of $\pm 0.12\%$ (A grade), and a typical temperature coefficient of 2 ppm/°C. The [ADR435](#) has a wide operating range (7.0 V to 18.0 V) and utilizes the +15.0 V rail for a power source.

Although it is possible to operate both the AD7170 VDD and REFIN(+) from the 5.0 V power supply, using a separate reference provides better accuracy.

The input voltage to the [AD7170](#) ADC is converted into an offset binary code at the output of the ADC. The [ADuM5402](#) provides the isolation for the DOUT data output, the SCLK input, and the $\overline{\text{PDRST}}$ input. Although the isolator is optional, it is recommended to protect the downstream digital circuitry

from the high common-mode voltage in the case of a fault condition.

The code is processed in the PC by using the SDP hardware board and LabVIEW software.

Figure 5 shows a comparison between the code seen at the output of the ADC recorded by LabVIEW and an ideal code calculated based on a perfect system. The plots show how the circuit achieves an end-point linearity error of less than 0.5% over the entire input voltage range (-100 mV to $+100\text{ mV}$). The offset error and gain error can be removed using software calibration if desired.

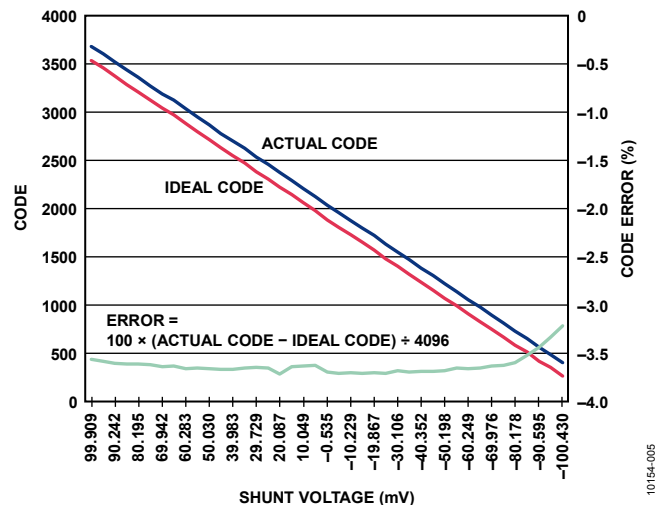


Figure 5. Plot of Actual Code, Ideal Code, and %Error vs. Shunt Voltage

PCB Layout Considerations

In any circuit where accuracy is crucial, it is important to consider the power supply and ground return layout on the board. The PCB should isolate the digital and analog sections as much as possible. This PCB was constructed in a 4-layer stack up with large area ground plane layers and power plane polygons. See the [MT-031 Tutorial](#) for more discussion on layout and grounding and the [MT-101 Tutorial](#) for information on decoupling techniques.

The power supply to the [AD7170](#) and [ADuM5402](#) should be decoupled with 10 μ F and 0.1 μ F capacitors to properly suppress noise and reduce ripple. The capacitors should be placed as close to the device as possible with the 0.1 μ F capacitor having a low ESR value. Ceramic capacitors are advised for all high frequency decoupling.

Care should be taken in considering the isolation gap between the primary and secondary sides of the [ADuM5402](#). The [EVAL-CN0240-SDPZ](#) board maximizes this distance by pulling back any polygons or components on the top layer and aligning them with the pins on the [ADuM5402](#).

Power supply lines should have as large a trace width as possible to provide low impedance paths and reduce glitch effects on the

supply line. Clocks and other fast switching digital signals should be shielded from other parts of the board by digital ground.

A complete design support package for this circuit note, including complete schematics and board layouts, can be found at www.analog.com/CN0240-DesignSupport.

COMMON VARIATIONS

There are a number of solutions available for high-side sensing of positive and negative sources. IC solutions using current sense amplifiers, difference amplifiers, or a combination of these are available. See the circuits described in the following circuit notes: [CN0100](#), [CN0188](#), [CN0218](#).

“High-Side Current Sensing: Difference Amplifier vs. Current Sense Amplifier,” *Analog Dialogue*, January 2008, describes the use of current sense and difference amplifiers. The article is available at www.analog.com/HighSide_CurrentSensing.

The following URLs link to Analog Devices products useful in solving the current sense problem:

Current sense amplifiers: www.analog.com/CurrentSenseAmps

Difference amplifiers: www.analog.com/DifferenceAmps

Instrumentation amplifiers: www.analog.com/InstrumentationAmps

CIRCUIT EVALUATION AND TEST

WARNING! HIGH VOLTAGE. THIS CIRCUIT MAY CONTAIN LETHAL VOLTAGES. DO NOT OPERATE, EVALUATE, OR TEST THIS CIRCUIT, OR BOARD ASSEMBLY, UNLESS YOU ARE A TRAINED PROFESSIONAL, WHO IS QUALIFIED TO HANDLE HIGH VOLTAGE CIRCUITRY. BEFORE APPLYING POWER, YOU MUST BE FAMILIAR WITH THE CIRCUITRY AND ALL REQUIRED PRECAUTIONS FOR WORKING WITH HIGH VOLTAGE CIRCUITS.

This circuit uses the [EVAL-CN0240-SDPZ](#) circuit board and the [EVAL-SDP-CB1Z](#) System Demonstration Platform (SDP) evaluation board. The two boards have 120-pin mating connectors, allowing for the quick setup and evaluation of the circuit's performance. The [EVAL-CN0240-SDPZ](#) board contains the circuit to be evaluated, as described in this note, and the SDP evaluation board is used with the CN0240 evaluation software to capture the data from the [EVAL-CN0240-SDPZ](#) circuit board.

Equipment Needed

- PC with a USB port and Windows® XP or Windows Vista® (32-bit), or Windows® 7 (32-bit)
- [EVAL-CN0240-SDPZ](#) circuit evaluation board
- [EVAL-SDP-CB1Z](#) SDP evaluation board
- CN0240 evaluation software
- Power supply: +6 V @ 1 A, or +6 V “wall wart”

- Dual power supply: ± 15 V @ 10 mA
- Shunt resistor with maximum voltage of 100 mV at the maximum load current.
- Source voltage and electronic load

Getting Started

Load the evaluation software by placing the CN0218 evaluation software disc in the CD drive of the PC. Using “My Computer,” locate the drive that contains the evaluation software disc and open the Readme file. Follow the instructions contained in the Readme file for installing and using the evaluation software.

Functional Block Diagram

See Figure 1 of this circuit note for the circuit block diagram and the EVAL-CN0240-SDPZ-SCH pdf file for the circuit schematics. This file is contained in the [CN0240 Design Support Package](#).

Setup

Connect the 120-pin connector on the [EVAL-CN0240-SDPZ](#) circuit board to the connector marked “CON A” on the [EVAL-SDP-CB1Z](#) evaluation (SDP) board. Nylon hardware should be used to firmly secure the two boards, using the holes provided at the ends of the 120-pin connectors.

Connect a shunt resistor (R_{SHUNT}) across the J4 input terminals with a load to ground as indicated in Figure 1. With power to the supply off, connect a +6 V power supply to the pins marked “+6 V” and “GND” on the board. If available, a +6 V “wall wart” can be connected to the barrel connector on the board and used in place of the +6 V power supply. Connect the USB cable supplied with the SDP board to the USB port on the PC. Note: Do not connect the USB cable to the mini USB connector on the SDP board at this time.

It is important to connect the system ground and the PCB isolated ground to guarantee correct voltage levels and operation. Test point 31 and test point 32 give access to the GND_ISO required to properly make this connection.

Lastly, before applying any high voltage to connector J4, be certain the ± 15 V supply (J5) is properly connected and has been turned on. If this supply is not active, any high voltage could potentially damage U2, the [AD629](#), as well as several other components on the PCB.

Test

Apply power to the +6 V supply (or “wall wart”) connected to the [EVAL-CN0240-SDPZ](#) circuit board. Connect the ± 15 V supplies to the [EVAL-CN0240-SDPZ](#) board U12 three-terminal screw connector. Launch the evaluation software and connect the USB cable from the PC to the USB mini-connector on the SDP board.

Once USB communications are established, the SDP board can be used to send, receive, and capture serial data from the EVAL-CN0240-SDPZ board. Data can be recorded for various values of load current as the electronic load is stepped.

Information and details regarding how to use the evaluation software for data capture can be found in the CN0240 evaluation software Readme file.

Information regarding the SDP board can be found in the [SDP User Guide](#).

LEARN MORE

CN0240 Design Support Package:

www.analog.com/CN0240-DesignSupport

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Data Sheets and Evaluation Boards

CN-0240 Circuit Evaluation Board (EVAL-CN0240-SDPZ)

System Demonstration Platform (EVAL-SDP-CB1Z)

AD629 Data Sheet

AD8622 Data Sheet

AD8475 Data Sheet

AD7170 Data Sheet

AD7170 Evaluation Board

ADR435 Data Sheet

ADuM5402 Data Sheet

ADuM5402 Evaluation Board

REVISION HISTORY

2/12—Revision 0: Initial Version

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