# 5 kV RMS Quad-Channel Digital Isolators

Data Sheet

# ADuM4400/ADuM4401/ADuM4402

## FEATURES

- Enhanced system-level ESD performance per IEC 61000-4-x
- Safety and regulatory approvals (RI-16 package)
  - UL recognition: 5000 V rms for 1 minute per UL 1577
  - CSA Component Acceptance Notice #5A
    - IEC 60601-1: 250 V rms (reinforced)
    - IEC 60950-1: 400 V rms (reinforced)
  - VDE Certificate of Conformity
  - DIN V VDE V 0884-10 (VDE V 0884-10):2006-12
    - $V_{IORM}$ = 846 V peak
- Low power operation
  - 5 V operation
    - 1.4 mA per channel maximum @ 0 Mbps to 2 Mbps
    - 4.3 mA per channel maximum @ 10 Mbps
    - 34 mA per channel maximum @ 90 Mbps
  - 3.3 V operation
    - 0.9 mA per channel maximum @ 0 Mbps to 2 Mbps
    - 2.4 mA per channel maximum @ 10 Mbps
    - 20 mA per channel maximum @ 90 Mbps
- Bidirectional communication
- 3.3 V/5 V level translation
- High temperature operation: 105°C
- High data rate: dc to 90 Mbps (NRZ)
- Precise timing characteristics
  - 2 ns maximum pulse width distortion
  - 2 ns maximum channel-to-channel matching
- High common-mode transient immunity: >25 kV/µs
- Output enable function
- 16-lead SOIC wide body package version (RW-16)
- 16-lead SOIC wide body enhanced creepage version (RI-16)

## APPLICATIONS

- General-purpose, high voltage, multichannel isolation
- Medical equipment
- Motor drives
- Power supplies

## GENERAL DESCRIPTION

The ADuM440x[1] are 4-channel digital isolators based on the Analog Devices, Inc., *i*Coupler® technology. Combining high speed CMOS and monolithic air core transformer technology, these isolation components provide outstanding performance characteristics that are superior to the alternatives, such as optocoupler devices and other integrated couplers.

The ADuM440x isolators provide four independent isolation channels in a variety of channel configurations and data rates (see the Ordering Guide). All models operate with the supply voltage on either side ranging from 3.0 V to 5.5 V, providing compatibility with lower voltage systems as well as enabling a voltage translation functionality across the isolation barrier. The ADuM440x isolators have a patented refresh feature that ensures dc correctness in the absence of input logic transitions and during power-up/power-down conditions.

This family of isolators, like many Analog Devices isolators, offers very low power consumption, consuming one-tenth to one-sixth the power of comparable isolators at comparable data rates up to 10 Mbps. All models of the ADuM440x provide low pulse width distortion (<2 ns for C grade). In addition, every model has an input glitch filter to protect against extraneous noise disturbances.

The ADuM440x contain circuit and layout enhancements to help achieve system-level IEC 61000-4-x compliance (ESD/burst/surge). The precise capability in these tests for the ADuM440x are strongly determined by the design and layout of the user's board or module. For more information, see the AN-793 Application Note, *ESD/Latch-Up Considerations with iCoupler Isolation Products*.

[1] Protected by U.S. Patents 5,952,849; 6,873,065; and 7,075,329.

## FUNCTIONAL BLOCK DIAGRAMS

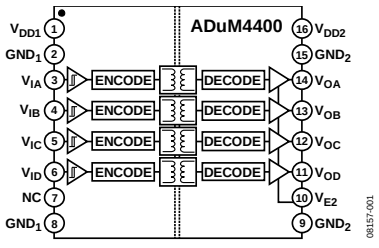


Figure 1. ADuM4400

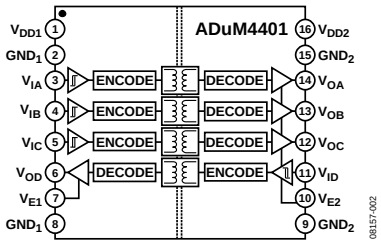


Figure 2. ADuM4401

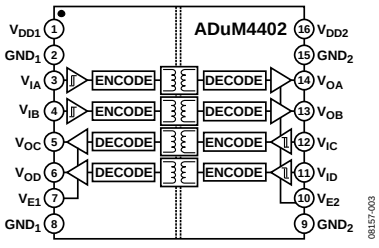


Figure 3. ADuM4402

Rev. F

Document Feedback



One Technology Way, P.O. Box 9106, Norwood, MA 02062-9106, U.S.A.
Tel: 781.329.4700 
Technical Support www.analog.com

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Change to Logic High Output Voltage Parameter and Logic low Output Voltage Parameter; Table 9 ... 5
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Changes to Table 14 ... 7

**9/2016—Rev. C to Rev. D**

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Changes to Figure 8 to Figure 13 ... 13
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**2/2012—Rev. B to Rev. C**

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**10/2011—Rev. A to Rev. B**

Added Logic Low Output Voltage, Table 3 ... 3
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**4/2009—Revision 0: Initial Version**

# SPECIFICATIONS

## ELECTRICAL CHARACTERISTICS—5 V OPERATION

All typical specifications are at $T_A$ = 25°C, $V_{DD1}$ = $V_{DD2}$ = 5 V. Minimum/maximum specifications apply over the entire recommended operation range of 4.5 V ≤ $V_{DD1}$ ≤ 5.5 V, 4.5 V ≤ $V_{DD2}$ ≤ 5.5 V, and −40°C ≤ $T_A$ ≤ 105°C, unless otherwise noted. Switching specifications are tested with $C_L$ = 15 pF and CMOS signal levels, unless otherwise noted.

**Table 1.**

| | | A Grade | | | B Grade | | | C Grade | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| **Parameter** | **Symbol** | **Min** | **Typ** | **Max** | **Min** | **Typ** | **Max** | **Min** | **Typ** | **Max** | **Unit** | **Test Conditions** |
| SWITCHING SPECIFICATIONS | | | | | | | | | | | | |
| Data Rate | | | | 1 | | | 10 | | | 90 | Mbps | Within PWD limit |
| Propagation Delay | $t_{PHL}$, $t_{PLH}$ | 50 | 65 | 100 | 20 | 32 | 50 | 18 | 27 | 32 | ns | 50% input to 50% output |
| Pulse Width Distortion | PWD | | | 40 | | | 3 | | 0.5 | 2 | ns | $\lvert t_{PLH} - t_{PHL} \rvert$ |
| Change vs. Temperature | | | 11 | | | 5 | | | 3 | | ps/°C | |
| Pulse Width | PW | 1000 | | | 100 | | | 11.1 | | | ns | Within PWD limit |
| Propagation Delay Skew | $t_{PSK}$ | | | 50 | | | 15 | | | 10 | ns | Between any two units |
| Channel Matching | | | | | | | | | | | | |
| Codirectional | $t_{PSKCD}$ | | | 50 | | | 3 | | | 2 | ns | |
| Opposing-Direction | $t_{PSKOD}$ | | | 50 | | | 6 | | | 5 | ns | |

**Table 2.**

| | | 1 Mbps—A, B, C Grades | | | 10 Mbps—B, C Grades | | | 90 Mbps—C Grade | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| **Parameter** | **Symbol** | **Min** | **Typ** | **Max** | **Min** | **Typ** | **Max** | **Min** | **Typ** | **Max** | **Unit** | **Test Conditions** |
| SUPPLY CURRENT | | | | | | | | | | | | |
| ADuM4400 | $I_{DD1}$ | | 2.9 | 3.5 | | 9.0 | 11.6 | | 72 | 100 | mA | |
| | $I_{DD2}$ | | 1.2 | 1.9 | | 3.0 | 5.5 | | 19 | 36 | mA | |
| ADuM4401 | $I_{DD1}$ | | 2.5 | 3.2 | | 7.4 | 10.6 | | 59 | 82 | mA | |
| | $I_{DD2}$ | | 1.6 | 2.4 | | 4.4 | 6.5 | | 32 | 46 | mA | |
| ADuM4402 | $I_{DD1}$ | | 2.0 | 2.8 | | 6.0 | 7.5 | | 51 | 62 | mA | |
| | $I_{DD2}$ | | 2.0 | 2.8 | | 6.0 | 7.5 | | 51 | 62 | mA | |

**Table 3. For All Models**

| **Parameter** | **Symbol** | **Min** | **Typ** | **Max** | **Unit** | **Test Conditions** |
|---|---|---|---|---|---|---|
| DC SPECIFICATIONS | | | | | | |
| Logic High Input Threshold | $V_{IH}$ | 2.0 | | | V | |
| Logic Low Input Threshold | $V_{IL}$ | | | 0.8 | V | |
| Logic High Output Voltage | $V_{OH}$ | $V_{DDx}$ − 0.1 | 5.0 | | V | $I_{Ox}$ = −20 μA, $V_{Ix}$ = $V_{IxH}$ |
| | | $V_{DDx}$ − 0.4 | 4.8 | | V | $I_{Ox}$ = −3.2 mA, $V_{Ix}$ = $V_{IxH}$ |
| Logic Low Output Voltage | $V_{OL}$ | | 0.0 | 0.1 | V | $I_{Ox}$ = 20 μA, $V_{Ix}$ = $V_{IxL}$ |
| | | | 0.04 | 0.1 | V | $I_{Ox}$ = 400 μA, $V_{Ix}$ = $V_{IxL}$ |
| | | | 0.2 | 0.4 | V | $I_{Ox}$ = 3.2 mA, $V_{Ix}$ = $V_{IxL}$ |
| Input Current per Channel | $I_I$ | −10 | +0.01 | +10 | μA | 0 V ≤ $V_{Ix}$ ≤ $V_{DDx}$ |
| Supply Current per Channel | | | | | | |
| Quiescent Input Supply Current | $I_{DDI(Q)}$ | | 0.57 | 0.83 | mA | |
| Quiescent Output Supply Current | $I_{DDO(Q)}$ | | 0.23 | 0.35 | mA | |
| Dynamic Input Supply Current | $I_{DDI(D)}$ | | 0.20 | | mA/Mbps | |
| Dynamic Output Supply Current | $I_{DDO(D)}$ | | 0.05 | | mA/Mbps | |
| AC SPECIFICATIONS | | | | | | |
| Output Rise/Fall Time | $t_R$/$t_F$ | | 2.5 | | ns | 10% to 90% |
| Common-Mode Transient Immunity[1] | \|CM\| | 25 | 35 | | kV/μs | $V_{Ix}$ = $V_{DDx}$, $V_{CM}$ = 1000 V, transient magnitude = 800 V |
| Output Disable Propagation Delay | $t_{PHZ}$, $t_{PLH}$ | | 6 | 8 | ns | High/low-to-high impedance |
| Output Enable Propagation Delay | $t_{PZH}$, $t_{PZL}$ | | 6 | 8 | ns | High impedance-to-high/low |
| Refresh Rate | $f_r$ | | 1.2 | | Mbps | |

[1] |CM| is the maximum common-mode voltage slew rate that can be sustained while maintaining $V_O$ > 0.8 $V_{DD}$. The common-mode voltage slew rates apply to both rising and falling common-mode voltage edges.

## ELECTRICAL CHARACTERISTICS—3.3 V OPERATION

All typical specifications are at $T_A$ = 25°C, $V_{DD1}$ = $V_{DD2}$ = 3.3 V. Minimum/maximum specifications apply over the entire recommended operation range: 3.0 V ≤ $V_{DD1}$ ≤ 3.6 V, 3.0 V ≤ $V_{DD2}$ ≤ 3.6 V, and −40°C ≤ $T_A$ ≤ 105°C, unless otherwise noted. Switching specifications are tested with $C_L$ = 15 pF and CMOS signal levels, unless otherwise noted.

**Table 4.**

| | | A Grade | | | B Grade | | | C Grade | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| **Parameter** | **Symbol** | **Min** | **Typ** | **Max** | **Min** | **Typ** | **Max** | **Min** | **Typ** | **Max** | **Unit** | **Test Conditions** |
| SWITCHING SPECIFICATIONS | | | | | | | | | | | | |
| Data Rate | | | | 1 | | | 10 | | | 90 | Mbps | Within PWD limit |
| Propagation Delay | $t_{PHL}$, $t_{PLH}$ | 50 | 75 | 100 | 20 | 38 | 50 | 20 | 34 | 45 | ns | 50% input to 50% output |
| Pulse Width Distortion | PWD | | | 40 | | | 3 | | 0.5 | 2 | ns | $\lvert t_{PLH} - t_{PHL} \rvert$ |
| Change vs. Temperature | | | 11 | | | 5 | | | 3 | | ps/°C | |
| Pulse Width | PW | 1000 | | | 100 | | | 11.1 | | | ns | Within PWD limit |
| Propagation Delay Skew | $t_{PSK}$ | | | 50 | | | 22 | | | 16 | ns | Between any two units |
| Channel Matching | | | | | | | | | | | | |
| Codirectional | $t_{PSKCD}$ | | | 50 | | | 3 | | | 2 | ns | |
| Opposing-Direction | $t_{PSKOD}$ | | | 50 | | | 6 | | | 5 | ns | |

**Table 5.**

| | | 1 Mbps—A, B, C Grades | | | 10 Mbps—B, C Grades | | | 90 Mbps—C Grade | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| **Parameter** | **Symbol** | **Min** | **Typ** | **Max** | **Min** | **Typ** | **Max** | **Min** | **Typ** | **Max** | **Unit** | **Test Conditions** |
| SUPPLY CURRENT | | | | | | | | | | | | |
| ADuM4400 | $I_{DD1}$ | | 1.6 | 2.1 | | 4.8 | 7.1 | | 37 | 54 | mA | |
| | $I_{DD2}$ | | 0.7 | 1.2 | | 1.8 | 2.3 | | 11 | 15 | mA | |
| ADuM4401 | $I_{DD1}$ | | 1.4 | 1.9 | | 0.1 | 5.6 | | 31 | 44 | mA | |
| | $I_{DD2}$ | | 0.9 | 1.5 | | 2.5 | 3.3 | | 17 | 24 | mA | |
| ADuM4402 | $I_{DD1}$ | | 1.2 | 1.7 | | 3.3 | 4.4 | | 24 | 39 | mA | |
| | $I_{DD2}$ | | 1.2 | 1.7 | | 3.3 | 4.4 | | 24 | 39 | mA | |

**Table 6. For All Models**

| **Parameter** | **Symbol** | **Min** | **Typ** | **Max** | **Unit** | **Test Conditions** |
|---|---|---|---|---|---|---|
| DC SPECIFICATIONS | | | | | | |
| Logic High Input Threshold | $V_{IH}$ | 1.6 | | | V | |
| Logic Low Input Threshold | $V_{IL}$ | | | 0.4 | V | |
| Logic High Output Voltage | $V_{OH}$ | $V_{DDx}$ − 0.1 | 3.0 | | V | $I_{Ox}$ = −20 μA, $V_{Ix}$ = $V_{IxH}$ |
| | | $V_{DDx}$ − 0.4 | 2.8 | | V | $I_{Ox}$ = −3.2 mA, $V_{Ix}$ = $V_{IxH}$ |
| Logic Low Output Voltage | $V_{OL}$ | | 0.0 | 0.1 | V | $I_{Ox}$ = 20 μA, $V_{Ix}$ = $V_{IxL}$ |
| | | | 0.04 | 0.1 | V | $I_{Ox}$ = 400 μA, $V_{Ix}$ = $V_{IxL}$ |
| | | | 0.2 | 0.4 | V | $I_{Ox}$ = 3.2 mA, $V_{Ix}$ = $V_{IxL}$ |
| Input Current per Channel | $I_I$ | −10 | +0.01 | +10 | μA | 0 V ≤ $V_{Ix}$ ≤ $V_{DDx}$ |
| Supply Current per Channel | | | | | | |
| Quiescent Input Supply Current | $I_{DDI(Q)}$ | | 0.31 | 0.49 | mA | |
| Quiescent Output Supply Current | $I_{DDO(Q)}$ | | 0.19 | 0.27 | mA | |
| Dynamic Input Supply Current | $I_{DDI(D)}$ | | 0.10 | | mA/Mbps | |
| Dynamic Output Supply Current | $I_{DDO(D)}$ | | 0.03 | | mA/Mbps | |
| AC SPECIFICATIONS | | | | | | |
| Output Rise/Fall Time | $t_R$/$t_F$ | | 3 | | ns | 10% to 90% |
| Common-Mode Transient Immunity[1] | \|CM\| | 25 | 35 | | kV/μs | $V_{Ix}$ = $V_{DDx}$, $V_{CM}$ = 1000 V, transient magnitude = 800 V |
| Output Disable Propagation Delay | $t_{PHZ}$, $t_{PLH}$ | | 6 | 8 | ns | High/low-to-high impedance |
| Output Enable Propagation Delay | $t_{PZH}$, $t_{PZL}$ | | 6 | 8 | ns | High impedance-to-high/low |
| Refresh Rate | $f_r$ | | 1.2 | | Mbps | |

[1] |CM| is the maximum common-mode voltage slew rate that can be sustained while maintaining $V_O$ > 0.8 $V_{DD}$. The common-mode voltage slew rates apply to both rising and falling common-mode voltage edges.

## ELECTRICAL CHARACTERISTICS—MIXED 5 V/3.3 V OPERATION

All typical specifications are at $T_A$ = 25°C, $V_{DD1}$ = 5 V, $V_{DD2}$ = 3.3 V. Minimum/maximum specifications apply over the entire recommended operation range: 4.5 V ≤ $V_{DD1}$ ≤ 5.5 V, 3.0 V ≤ $V_{DD2}$ ≤ 3.6 V, and −40°C ≤ $T_A$ ≤ 105°C, unless otherwise noted. Switching specifications are tested with $C_L$ = 15 pF and CMOS signal levels, unless otherwise noted.

**Table 7.**

| Parameter | Symbol | A Grade | | | B Grade | | | C Grade | | | Unit | Test Conditions |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | Min | Typ | Max | Min | Typ | Max | Min | Typ | Max | | |
| SWITCHING SPECIFICATIONS | | | | | | | | | | | | |
| Data Rate | | | | 1 | | | 10 | | | 90 | Mbps | Within PWD limit |
| Propagation Delay | $t_{PHL}$, $t_{PLH}$ | 50 | 70 | 50 | 15 | 35 | 50 | 20 | 30 | 40 | ns | 50% input to 50% output |
| Pulse Width Distortion | PWD | | | 40 | | | 3 | | 0.5 | 2 | ns | $\lvert t_{PLH} - t_{PHL} \rvert$ |
| Change vs. Temperature | | | 11 | | | 5 | | | 3 | | ps/°C | |
| Pulse Width | PW | 1000 | | | 100 | | | 11.1 | | | ns | Within PWD limit |
| Propagation Delay Skew | $t_{PSK}$ | | | 50 | | | 22 | | | 14 | ns | Between any two units |
| Channel Matching | | | | | | | | | | | | |
| Codirectional | $t_{PSKCD}$ | | | 50 | | | 3 | | | 2 | ns | |
| Opposing-Direction | $t_{PSKOD}$ | | | 50 | | | 6 | | | 5 | ns | |

**Table 8.**

| Parameter | Symbol | 1 Mbps—A, B, C Grades | | | 10 Mbps—B, C Grades | | | 90 Mbps—C Grade | | | Unit | Test Conditions |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | Min | Typ | Max | Min | Typ | Max | Min | Typ | Max | | |
| SUPPLY CURRENT | | | | | | | | | | | | |
| ADuM4400 | $I_{DD1}$ | | 2.9 | 3.5 | | 9.0 | 11.6 | | 72 | 100 | mA | |
| | $I_{DD2}$ | | 0.7 | 1.2 | | 1.8 | 2.3 | | 11 | 15 | mA | |
| ADuM4401 | $I_{DD1}$ | | 2.5 | 3.2 | | 7.4 | 10.6 | | 59 | 82 | mA | |
| | $I_{DD2}$ | | 0.9 | 1.5 | | 2.5 | 3.3 | | 17 | 24 | mA | |
| ADuM4402 | $I_{DD1}$ | | 2.0 | 2.8 | | 6.0 | 7.5 | | 46 | 62 | mA | |
| | $I_{DD2}$ | | 1.2 | 1.7 | | 3.3 | 4.4 | | 24 | 39 | mA | |

**Table 9. For All Models**

| Parameter | Symbol | Min | Typ | Max | Unit | Test Conditions |
|---|---|---|---|---|---|---|
| DC SPECIFICATIONS | | | | | | |
| Logic High Input Threshold | $V_{IH}$ | 2.0 | | | V | |
| Logic Low Input Threshold | $V_{IL}$ | | | 0.8 | V | |
| Logic High Output Voltage | $V_{OH}$ | $V_{DDx}$ − 0.1 | 3.0 | | V | $I_{Ox}$ = −20 μA, $V_{Ix}$ = $V_{IxH}$ |
| | | $V_{DDx}$ − 0.4 | 2.8 | | V | $I_{Ox}$ = −3.2 mA, $V_{Ix}$ = $V_{IxH}$ |
| Logic Low Output Voltage | $V_{OL}$ | | 0.0 | 0.1 | V | $I_{Ox}$ = 20 μA, $V_{Ix}$ = $V_{IxL}$ |
| | | | 0.04 | 0.1 | V | $I_{Ox}$ = 400 μA, $V_{Ix}$ = $V_{IxL}$ |
| | | | 0.2 | 0.4 | V | $I_{Ox}$ = 3.2 mA, $V_{Ix}$ = $V_{IxL}$ |
| Input Current per Channel | $I_I$ | −10 | +0.01 | +10 | μA | 0 V ≤ $V_{Ix}$ ≤ $V_{DDx}$ |
| Supply Current per Channel | | | | | | |
| Quiescent Input Supply Current | $I_{DDI(Q)}$ | | 0.57 | 0.83 | mA | |
| Quiescent Output Supply Current | $I_{DDO(Q)}$ | | 0.29 | 0.27 | mA | |
| Dynamic Input Supply Current | $I_{DDI(D)}$ | | 0.20 | | mA/Mbps | |
| Dynamic Output Supply Current | $I_{DDO(D)}$ | | 0.03 | | mA/Mbps | |
| AC SPECIFICATIONS | | | | | | |
| Output Rise/Fall Time | $t_R$/$t_F$ | | 3 | | ns | 10% to 90% |
| Common-Mode Transient Immunity[1] | \|CM\| | 25 | 35 | | kV/μs | $V_{Ix}$ = $V_{DDx}$, $V_{CM}$ = 1000 V, transient magnitude = 800 V |
| Output Disable Propagation Delay | $t_{PHZ}$, $t_{PLH}$ | | 6 | 8 | ns | High/low-to-high impedance |
| Output Enable Propagation Delay | $t_{PZH}$, $t_{PZL}$ | | 6 | 8 | ns | High impedance-to-high/low |
| Refresh Rate | $f_r$ | | 1.2 | | Mbps | |

[1] |CM| is the maximum common-mode voltage slew rate that can be sustained while maintaining $V_O$ > 0.8 $V_{DD}$. The common-mode voltage slew rates apply to both rising and falling common-mode voltage edges.

## ELECTRICAL CHARACTERISTICS—MIXED 3.3 V/5 V OPERATION

All typical specifications are at $T_A$ = 25°C, $V_{DD1}$ = 3.3 V, $V_{DD2}$ = 5 V. Minimum/maximum specifications apply over the entire recommended operation range: 3.0 V ≤ $V_{DD1}$ ≤ 3.6 V, 4.5 V ≤ $V_{DD2}$ ≤ 5.5 V, and −40°C ≤ $T_A$ ≤ +105°C, unless otherwise noted. Switching specifications are tested with $C_L$ = 15 pF and CMOS signal levels, unless otherwise noted.

**Table 10.**

| | | A Grade | | | B Grade | | | C Grade | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| **Parameter** | **Symbol** | **Min** | **Typ** | **Max** | **Min** | **Typ** | **Max** | **Min** | **Typ** | **Max** | **Unit** | **Test Conditions** |
| SWITCHING SPECIFICATIONS | | | | | | | | | | | | |
| Data Rate | | | | 1 | | | 10 | | | 90 | Mbps | Within PWD limit |
| Propagation Delay | $t_{PHL}$, $t_{PLH}$ | 50 | 70 | 100 | 15 | 35 | 50 | 20 | 30 | 40 | ns | 50% input to 50% output |
| Pulse Width Distortion | PWD | | | 40 | | | 3 | | 0.5 | 2 | ns | $\lvert t_{PLH} - t_{PHL} \rvert$ |
| Change vs. Temperature | | | 11 | | | 5 | | | 3 | | ps/°C | |
| Pulse Width | PW | 1000 | | | 100 | | | 11.1 | | | ns | Within PWD limit |
| Propagation Delay Skew | $t_{PSK}$ | | | 50 | | | 22 | | | 14 | ns | Between any two units |
| Channel Matching | | | | | | | | | | | | |
| Codirectional | $t_{PSKCD}$ | | | 50 | | | 3 | | | 2 | ns | |
| Opposing-Direction | $t_{PSKOD}$ | | | 50 | | | 6 | | | 5 | ns | |

**Table 11.**

| | | 1 MBps—A, B, C Grades | | | 10 MBps—B, C Grades | | | 90 MBps—C Grade | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| **Parameter** | **Symbol** | **Min** | **Typ** | **Max** | **Min** | **Typ** | **Max** | **Min** | **Typ** | **Max** | **Unit** | **Test Conditions** |
| SUPPLY CURRENT | | | | | | | | | | | | |
| ADuM4400 | $I_{DD1}$ | | 1.6 | 2.1 | | 4.8 | 7.1 | | 37 | 54 | mA | |
| | $I_{DD2}$ | | 1.2 | 1.9 | | 3.0 | 5.5 | | 19 | 36 | mA | |
| ADuM4401 | $I_{DD1}$ | | 1.4 | 1.9 | | 4.1 | 5.6 | | 31 | 44 | mA | |
| | $I_{DD2}$ | | 1.6 | 2.4 | | 4.4 | 6.5 | | 32 | 46 | mA | |
| ADuM4402 | $I_{DD1}$ | | 1.2 | 1.7 | | 3.3 | 4.4 | | 24 | 39 | mA | |
| | $I_{DD2}$ | | 2.0 | 2.8 | | 6.0 | 7.5 | | 46 | 62 | mA | |

**Table 12. For All Models**

| **Parameter** | **Symbol** | **Min** | **Typ** | **Max** | **Unit** | **Test Conditions** |
|---|---|---|---|---|---|---|
| DC SPECIFICATIONS | | | | | | |
| Logic High Input Threshold | $V_{IH}$ | 1.6 | | | V | |
| Logic Low Input Threshold | $V_{IL}$ | | | 0.4 | V | |
| Logic High Output Voltage | $V_{OH}$ | $V_{DDx}$ − 0.1 | 5.0 | | V | $I_{Ox}$ = −20 µA, $V_{Ix}$ = $V_{IxH}$ |
| | | $V_{DDx}$ − 0.4 | 4.8 | | V | $I_{Ox}$ = −3.2 mA, $V_{Ix}$ = $V_{IxH}$ |
| Logic Low Output Voltage | $V_{OL}$ | | 0.0 | 0.1 | V | $I_{Ox}$ = 20 µA, $V_{Ix}$ = $V_{IxL}$ |
| | | | 0.04 | 0.1 | V | $I_{Ox}$ = 400 µA, $V_{Ix}$ = $V_{IxL}$ |
| | | | 0.2 | 0.4 | V | $I_{Ox}$ = 3.2 mA, $V_{Ix}$ = $V_{IxL}$ |
| Input Current per Channel | $I_I$ | −10 | +0.01 | +10 | µA | 0 V ≤ $V_{Ix}$ ≤ $V_{DDx}$ |
| Supply Current per Channel | | | | | | |
| Quiescent Input Supply Current | $I_{DDI(Q)}$ | | 0.31 | 0.49 | mA | |
| Quiescent Output Supply Current | $I_{DDO(Q)}$ | | 0.19 | 0.35 | mA | |
| Dynamic Input Supply Current | $I_{DDI(D)}$ | | 0.10 | | mA/Mbps | |
| Dynamic Output Supply Current | $I_{DDO(D)}$ | | 0.05 | | mA/Mbps | |
| AC SPECIFICATIONS | | | | | | |
| Output Rise/Fall Time | $t_R$/$t_F$ | | 2.5 | | ns | 10% to 90% |
| Common-Mode Transient Immunity[1] | \|CM\| | 25 | 35 | | kV/µs | $V_{Ix}$ = $V_{DDx}$, $V_{CM}$ = 1000 V, transient magnitude = 800 V |
| Output Disable Propagation Delay | $t_{PHZ}$, $t_{PLH}$ | | 6 | 8 | ns | High/low-to-high impedance |
| Output Enable Propagation Delay | $t_{PZH}$, $t_{PZL}$ | | 6 | 8 | ns | High impedance-to-high/low |
| Refresh Rate | $f_r$ | | 1.1 | | Mbps | |

[1] |CM| is the maximum common-mode voltage slew rate that can be sustained while maintaining $V_O$ > 0.8 $V_{DD}$. The common-mode voltage slew rates apply to both rising and falling common-mode voltage edges.

## PACKAGE CHARACTERISTICS

**Table 13.**

| Parameter | Symbol | Min | Typ | Max | Unit | Test Conditions |
|---|---|---|---|---|---|---|
| Resistance (Input to Output)[1] | $R_{I-O}$ | | $10^{12}$ | | Ω | |
| Capacitance (Input to Output)[1] | $C_{I-O}$ | | 2.2 | | pF | f = 1 MHz |
| Input Capacitance[2] | $C_I$ | | 4.0 | | pF | |
| IC Junction-to-Case Thermal Resistance, Side 1 | $\theta_{JCI}$ | | 33 | | °C/W | Thermocouple located at center of package underside |
| IC Junction-to-Case Thermal Resistance, Side 2 | $\theta_{JCO}$ | | 28 | | °C/W | |

[1] Device considered a 2-terminal device: Pin 1, Pin 2, Pin 3, Pin 4, Pin 5, Pin 6, Pin 7, and Pin 8 shorted together and Pin 9, Pin 10, Pin 11, Pin 12, Pin 13, Pin 14, Pin 15, and Pin 16 shorted together.
[2] Input capacitance is from any input data pin to ground.

## REGULATORY INFORMATION

The ADuM440x are approved by the organizations listed in Table 14. Refer to Table 19 and the Insulation Lifetime section for details regarding recommended maximum working voltages for specific cross-isolation waveforms and insulation levels.

**Table 14.**

| UL | CSA | VDE | CQC |
|---|---|---|---|
| Recognized under 1577 Component Recognition Program[1] | Approved under CSA Component Acceptance Notice #5A | Certified according to DIN V VDE V 0884-10 (VDE V 0884-10): 2006-12[2] | Approved under CQC11-471543-2015 |
| Single Protection 5000 V rms Isolation Voltage | Basic insulation per CSA 60950-1-07 and IEC 60950-1, 600 V rms (848 V peak) maximum working voltage | Reinforced insulation, 846 V peak | |
| | RW-16 package | | RW-16 package |
| | Reinforced insulation per CSA 60950-1-07 and IEC 60950-1, 380 V rms (537 V peak) maximum working voltage; reinforced insulation per IEC 60601-1 125 V rms (176 V peak) maximum working voltage | | Basic insulation per GB4943.1-2011, 760 V rms (1075 V peak) maximum working voltage, tropical climate, altitude ≤ 5000 m<br><br>Reinforced insulation per GB4943.1-2011, 380 V rms (537 V peak) maximum working voltage, tropical climate, altitude ≤ 5000 m |
| | RI-16 package | | RI-16 Package |
| | Reinforced insulation per CSA 60950-1-07 and IEC 60950-1, 400 V rms (565 V peak) maximum working voltage; reinforced insulation per IEC 60601-1 250 V rms (353 V peak) maximum working voltage | | Basic insulation per GB4943.1-2011, 820 V rms (1159 V peak) maximum working voltage, tropical climate, altitude ≤ 5000 m<br><br>Reinforced insulation per GB4943.1-2011, 401 V rms (578 V peak) maximum working voltage, tropical climate, altitude ≤ 5000 m |
| File E214100 | File 205078 | File 2471900-4880-0001 | File CQC16001150402 |

[1] In accordance with UL1577, each ADuM440x is proof tested by applying an insulation test voltage ≥ 6000 V rms for 1 second (current leakage detection limit = 10 μA).
[2] In accordance with DIN V VDE V 0884-10, each ADuM440x is proof tested by applying an insulation test voltage ≥1590 V peak for 1 sec (partial discharge detection limit = 5 pC). The * marking branded on the component designates DIN V VDE V 0884-10 approval.

## INSULATION AND SAFETY-RELATED SPECIFICATIONS

**Table 15.**

| Parameter | Symbol | Value | Unit | Conditions |
|---|---|---|---|---|
| Rated Dielectric Insulation Voltage | | 5000 | V rms | 1-minute duration |
| Minimum External Air Gap | L(I01) | 8.0 min | mm | Distance measured from input terminals to output terminals, shortest distance through air along the PCB mounting plane, as an aid to PC board layout |
| Minimum External Tracking (Creepage) RW-16 Package | L(I02) | 7.7 min | mm | Measured from input terminals to output terminals, shortest distance path along body |
| Minimum External Tracking (Creepage) RI-16 Package | L(I02) | 8.3 min | mm | Measured from input terminals to output terminals, shortest distance path along body |
| Minimum Internal Gap (Internal Clearance) | | 0.017 min | mm | Insulation distance through insulation |
| Tracking Resistance (Comparative Tracking Index) | CTI | >175 | V | DIN IEC 112/VDE 0303 Part 1 |

## DIN V VDE V 0884-10 (VDE V 0884-10) INSULATION CHARACTERISTICS

These isolators are suitable for reinforced electrical isolation only within the safety limit data. Maintenance of the safety data is ensured by means of protective circuits.

Note that the * marking on packages denotes DIN V VDE V 0884-10 approval for 846 V peak working voltage.

**Table 16.**

| Description | Conditions | Symbol | Characteristic | Unit |
|---|---|---|---|---|
| Installation Classification per DIN VDE 0110 | | | | |
| For Rated Mains Voltage ≤ 300 V rms | | | I to IV | |
| For Rated Mains Voltage ≤ 450 V rms | | | I to II | |
| For Rated Mains Voltage ≤ 600 V rms | | | I to II | |
| Climatic Classification | | | 40/105/21 | |
| Pollution Degree (DIN VDE 0110, Table 1) | | | 2 | |
| Maximum Working Insulation Voltage | | $V_{IORM}$ | 846 | V peak |
| Input-to-Output Test Voltage, Method b1 | $V_{IORM} \times 1.875 = V_{PR}$, 100% production test, $t_m$ = 1 sec, partial discharge < 5 pC | $V_{PR}$ | 1590 | V peak |
| Input-to-Output Test Voltage, Method a | | $V_{PR}$ | | |
| After Environmental Tests Subgroup 1 | $V_{IORM} \times 1.6 = V_{PR}$, $t_m$ = 60 sec, partial discharge < 5 pC | | 1375 | V peak |
| After Input and/or Safety Test Subgroup 2 and Subgroup 3 | $V_{IORM} \times 1.2 = V_{PR}$, $t_m$ = 60 sec, partial discharge < 5 pC | | 1018 | V peak |
| Highest Allowable Overvoltage | Transient overvoltage, $t_{TR}$ = 10 seconds | $V_{TR}$ | 6000 | V peak |
| Safety-Limiting Values | Maximum value allowed in the event of a failure; see Figure 4 | | | |
| Case Temperature | | $T_S$ | 150 | °C |
| Side 1 Current | | $I_{S1}$ | 265 | mA |
| Side 2 Current | | $I_{S2}$ | 335 | mA |
| Insulation Resistance at $T_S$ | $V_{IO}$ = 500 V | $R_S$ | $>10^9$ | Ω |

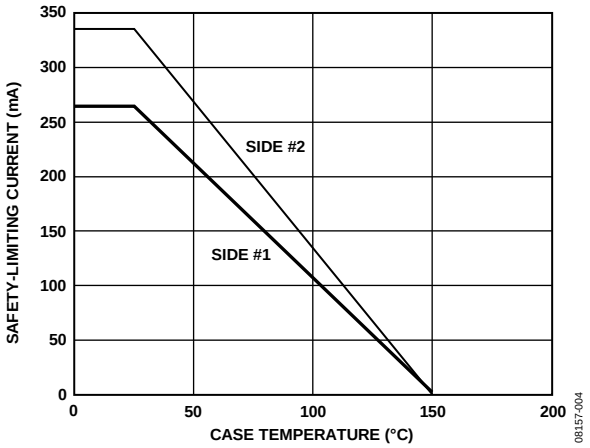



*Figure 4. Thermal Derating Curve, Dependence of Safety Limiting Values with Case Temperature per DIN V VDE V 0884-10*

## RECOMMENDED OPERATING CONDITIONS

**Table 17.**

| Parameter | Symbol | Min | Max | Unit |
|---|---|---|---|---|
| Operating Temperature | $T_A$ | −40 | +105 | °C |
| Supply Voltages[1] | $V_{DD1}$, $V_{DD2}$ | 3.0 | 5.5 | V |
| Input Signal Rise and Fall Times | | | 1.0 | ms |

[1] All voltages are relative to their respective ground.

# ABSOLUTE MAXIMUM RATINGS

**Table 18.**

| Parameter | Rating |
|---|---|
| Storage Temperature ($T_{ST}$) | −65°C to +150°C |
| Ambient Operating Temperature ($T_A$) | −40°C to +105°C |
| Supply Voltages ($V_{DD1}$, $V_{DD2}$)[1] | −0.5 V to +7.0 V |
| Input Voltage ($V_{IA}$, $V_{IB}$, $V_{IC}$, $V_{ID}$, $V_{E1}$, $V_{E2}$)[1, 2] | −0.5 V to $V_{DDI}$ + 0.5 V |
| Output Voltage ($V_{OA}$, $V_{OB}$, $V_{OC}$, $V_{OD}$)[1, 2] | −0.5 V to $V_{DDO}$ + 0.5 V |
| Average Output Current Per Pin[3] | |
| Side 1 ($I_{O1}$) | −18 mA to +18 mA |
| Side 2 ($I_{O2}$) | −22 mA to +22 mA |
| Common-Mode Transients[4] | −100 kV/µs to +100 kV/µs |

[1] All voltages are relative to their respective ground.
[2] $V_{DDI}$ and $V_{DDO}$ refer to the supply voltages on the input and output sides of a given channel, respectively. See the PC Board Layout section.
[3] See Figure 4 for maximum rated current values for various temperatures.
[4] Refers to common-mode transients across the insulation barrier. Common-mode transients exceeding the Absolute Maximum Rating can cause latch-up or permanent damage.

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

## ESD CAUTION

**ESD (electrostatic discharge) sensitive device.** Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

**Table 19. Maximum Continuous Working Voltage[1]**

| Parameter | Max | Unit | Constraint |
|---|---|---|---|
| AC Voltage, Bipolar Waveform | 565 | V peak | 50 year minimum lifetime |
| AC Voltage, Unipolar Waveform | | | |
| Reinforced Insulation | 846 | V peak | Maximum approved working voltage per IEC 60950-1 and VDE V 0884-10 |
| DC Voltage | | | |
| Reinforced Insulation | 846 | V peak | Maximum approved working voltage per IEC 60950-1 and VDE V 0884-10 |

[1] Refers to continuous voltage magnitude imposed across the isolation barrier. See the Insulation Lifetime section for more details.

**Table 20. Truth Table (Positive Logic)**

| $V_{Ix}$ Input[1] | $V_{Ex}$ Input | $V_{DDI}$ State[1] | $V_{DDO}$ State[1] | $V_{Ox}$ Output[1] | Notes |
|---|---|---|---|---|---|
| H | H or NC | Powered | Powered | H | |
| L | H or NC | Powered | Powered | L | |
| X | L | Powered | Powered | Z | |
| X | H or NC | Unpowered | Powered | H | Outputs return to input state within 1 µs of $V_{DDI}$ power restoration. |
| X | L | Unpowered | Powered | Z | |
| X | X | Powered | Unpowered | Indeterminate | Outputs return to input state within 1 µs of $V_{DDO}$ power restoration if $V_{Ex}$ state is H or NC. Outputs return to high impedance state within 8 ns of $V_{DDO}$ power restoration if $V_{Ex}$ state is L. |

[1] $V_{Ix}$ and $V_{Ox}$ refer to the input and output signals of a given channel (A, B, C, or D). $V_{Ex}$ refers to the output enable signal on the same side as the $V_{Ox}$ outputs. $V_{DDI}$ and $V_{DDO}$ refer to the supply voltages on the input and output sides of the given channel, respectively.

# PIN CONFIGURATIONS AND FUNCTION DESCRIPTIONS

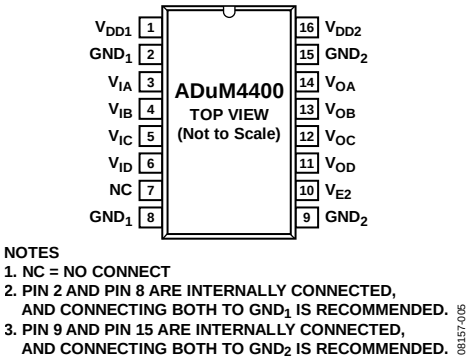



*Figure 5. ADuM4400 Pin Configuration*

**Table 21. ADuM4400 Pin Function Descriptions**

| Pin No. | Mnemonic | Description |
|---|---|---|
| 1 | $V_{DD1}$ | Supply Voltage for Isolator Side 1, 3.0 V to 5.5 V. |
| 2 | $GND_1$ | Ground 1. Ground reference for isolator Side 1. |
| 3 | $V_{IA}$ | Logic Input A. |
| 4 | $V_{IB}$ | Logic Input B. |
| 5 | $V_{IC}$ | Logic Input C. |
| 6 | $V_{ID}$ | Logic Input D. |
| 7 | NC | No Connect. |
| 8 | $GND_1$ | Ground 1. Ground reference for isolator Side 1. |
| 9 | $GND_2$ | Ground 2. Ground reference for isolator Side 2. |
| 10 | $V_{E2}$ | Output Enable 2. Active high logic input. $V_{Ox}$ outputs on Side 2 are enabled when $V_{E2}$ is high or disconnected. $V_{Ox}$ Side 2 outputs are disabled when $V_{E2}$ is low. In noisy environments, connecting $V_{E2}$ to an external logic high or low is recommended. |
| 11 | $V_{OD}$ | Logic Output D. |
| 12 | $V_{OC}$ | Logic Output C. |
| 13 | $V_{OB}$ | Logic Output B. |
| 14 | $V_{OA}$ | Logic Output A. |
| 15 | $GND_2$ | Ground 2. Ground reference for isolator Side 2. |
| 16 | $V_{DD2}$ | Supply Voltage for Isolator Side 2, 3.0 V to 5.5 V. |

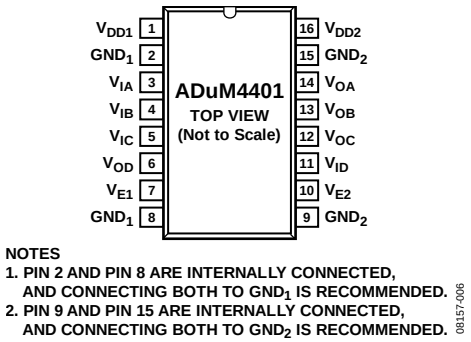



*Figure 6. ADuM4401 Pin Configuration*

**Table 22. ADuM4401 Pin Function Descriptions**

| Pin No. | Mnemonic | Description |
|---|---|---|
| 1 | $V_{DD1}$ | Supply Voltage for Isolator Side 1, 3.0 V to 5.5 V. |
| 2 | $GND_1$ | Ground 1. Ground reference for isolator Side 1. |
| 3 | $V_{IA}$ | Logic Input A. |
| 4 | $V_{IB}$ | Logic Input B. |
| 5 | $V_{IC}$ | Logic Input C. |
| 6 | $V_{OD}$ | Logic Output D. |
| 7 | $V_{E1}$ | Output Enable. Active high logic input. $V_{Ox}$ Side 1 outputs are enabled when $V_{E1}$ is high or disconnected. $V_{OX}$ Side 1 outputs are disabled when $V_{E1}$ is low. In noisy environments, connecting $V_{E1}$ to an external logic high or low is recommended. |
| 8 | $GND_1$ | Ground 1. Ground reference for isolator Side 1. |
| 9 | $GND_2$ | Ground 2. Ground reference for isolator Side 2. |
| 10 | $V_{E2}$ | Output Enable 2. Active high logic input. $V_{Ox}$ outputs on Side 2 are enabled when $V_{E2}$ is high or disconnected. $V_{Ox}$ Side 2 outputs are disabled when $V_{E2}$ is low. In noisy environments, connecting $V_{E2}$ to an external logic high or low is recommended. |
| 11 | $V_{ID}$ | Logic Input D. |
| 12 | $V_{OC}$ | Logic Output C. |
| 13 | $V_{OB}$ | Logic Output B. |
| 14 | $V_{OA}$ | Logic Output A. |
| 15 | $GND_2$ | Ground 2. Ground reference for isolator Side 2. |
| 16 | $V_{DD2}$ | Supply Voltage for Isolator Side 2, 3.0 V to 5.5 V. |

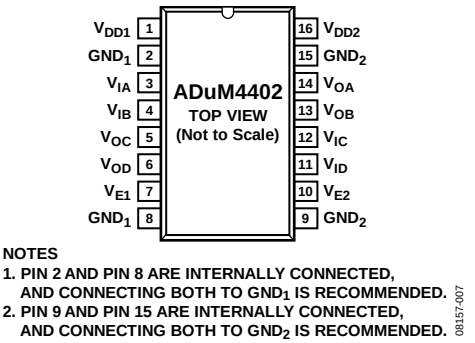



*Figure 7. ADuM4402 Pin Configuration*

**Table 23. ADuM4402 Pin Function Descriptions**

| Pin No. | Mnemonic | Description |
|---|---|---|
| 1 | $V_{DD1}$ | Supply Voltage for Isolator Side 1, 3.0 V to 5.5 V. |
| 2 | $GND_1$ | Ground 1. Ground reference for isolator Side 1. |
| 3 | $V_{IA}$ | Logic Input A. |
| 4 | $V_{IB}$ | Logic Input B. |
| 5 | $V_{OC}$ | Logic Output C. |
| 6 | $V_{OD}$ | Logic Output D. |
| 7 | $V_{E1}$ | Output Enable 1. Active high logic input. $V_{Ox}$ Side 1 outputs are enabled when $V_{E1}$ is high or disconnected. $V_{OX}$ Side 1 outputs are disabled when $V_{E1}$ is low. In noisy environments, connecting $V_{E1}$ to an external logic high or low is recommended. |
| 8 | $GND_1$ | Ground 1. Ground reference for isolator Side 1. |
| 9 | $GND_2$ | Ground 2. Ground reference for isolator Side 2. |
| 10 | $V_{E2}$ | Output Enable 2. Active high logic input. $V_{Ox}$ outputs on Side 2 are enabled when $V_{E2}$ is high or disconnected. $V_{Ox}$ Side 2 outputs are disabled when $V_{E2}$ is low. In noisy environments, connecting $V_{E2}$ to an external logic high or low is recommended. |
| 11 | $V_{ID}$ | Logic Input D. |
| 12 | $V_{IC}$ | Logic Input C. |
| 13 | $V_{OB}$ | Logic Output B. |
| 14 | $V_{OA}$ | Logic Output A. |
| 15 | $GND_2$ | Ground 2. Ground reference for isolator Side 2. |
| 16 | $V_{DD2}$ | Supply Voltage for Isolator Side 2, 3.0 V to 5.5 V. |

# TYPICAL PERFORMANCE CHARACTERISTICS

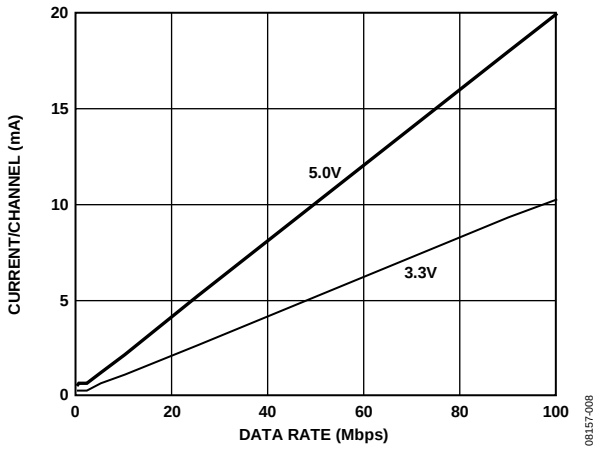



*Figure 8. Typical Input Supply Current per Channel vs. Data Rate (No Load)*

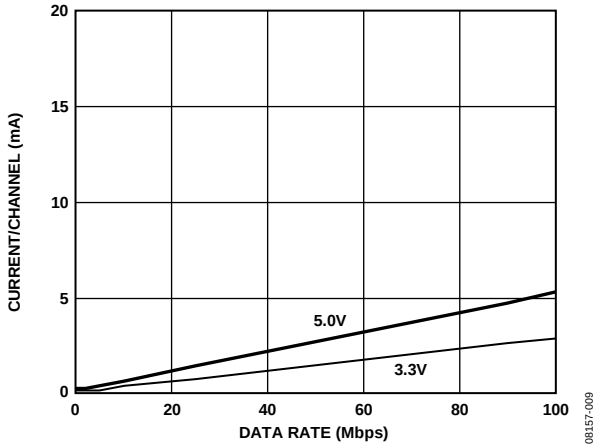



*Figure 9. Typical Output Supply Current per Channel vs. Data Rate (No Load)*

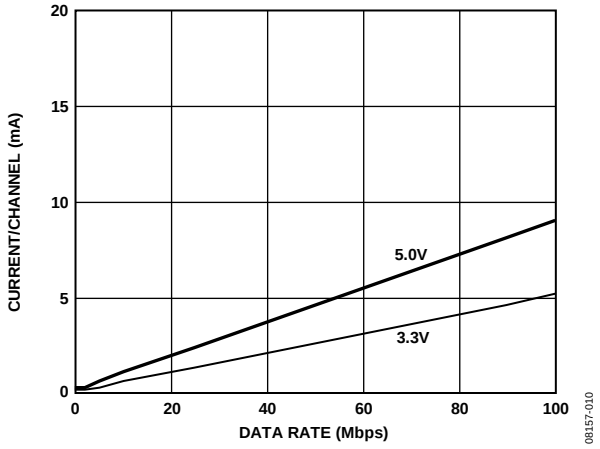



*Figure 10. Typical Output Supply Current per Channel vs. Data Rate (15 pF Output Load)*

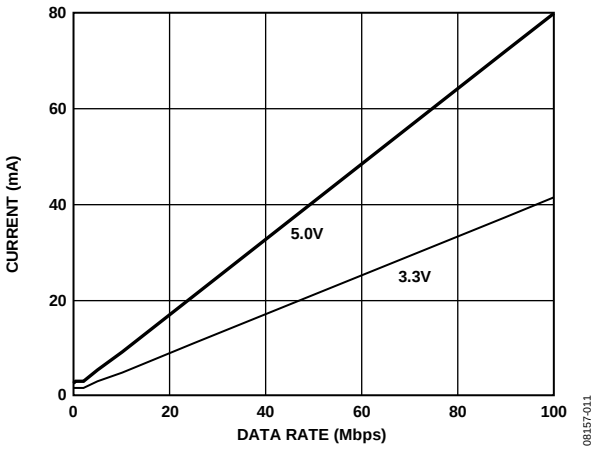



*Figure 11. Typical ADuM4400 $V_{DD1}$ Supply Current vs. Data Rate for 5 V and 3.3 V Operation*

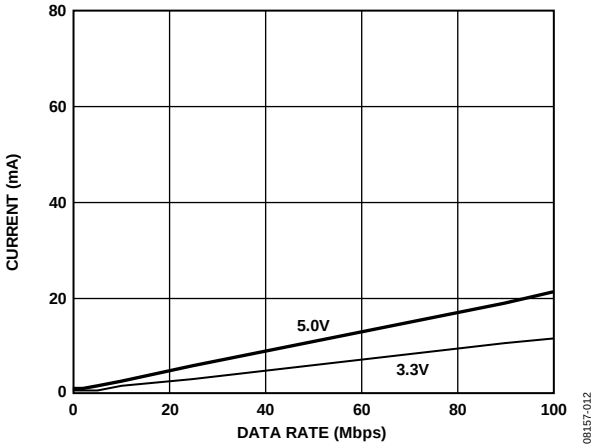



*Figure 12. Typical ADuM4400 $V_{DD2}$ Supply Current vs. Data Rate for 5 V and 3 V Operation*

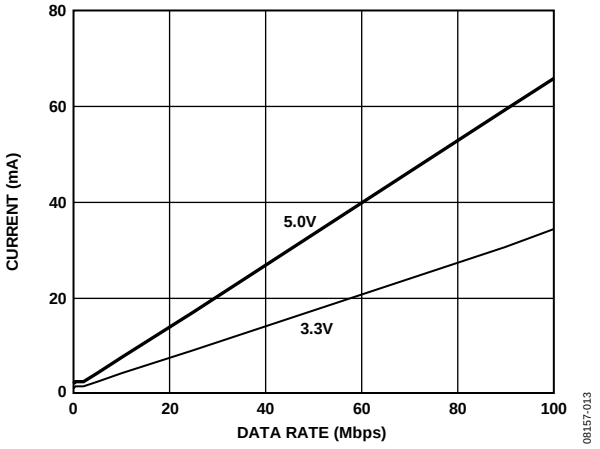



*Figure 13. Typical ADuM4401 $V_{DD1}$ Supply Current vs. Data Rate for 5 V and 3.3 V Operation*

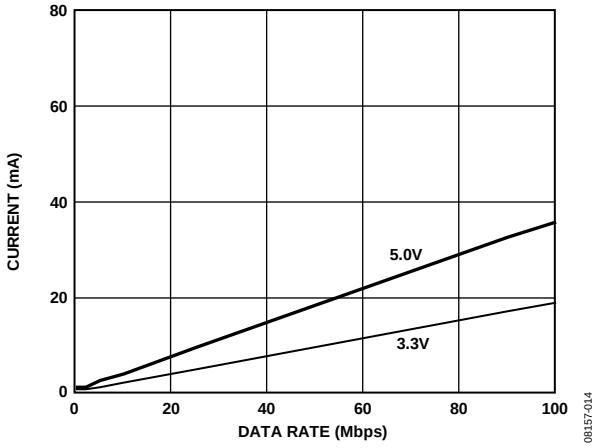



*Figure 14. Typical ADuM4401 $V_{DD2}$ Supply Current vs. Data Rate for 5 V and 3.3 V Operation*

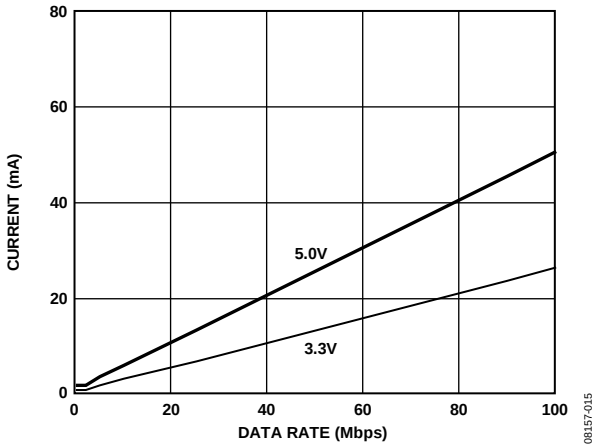



*Figure 15. Typical ADuM4402 $V_{DD1}$ or $V_{DD2}$ Supply Current vs. Data Rate for 5 V and 3.3 V Operation*

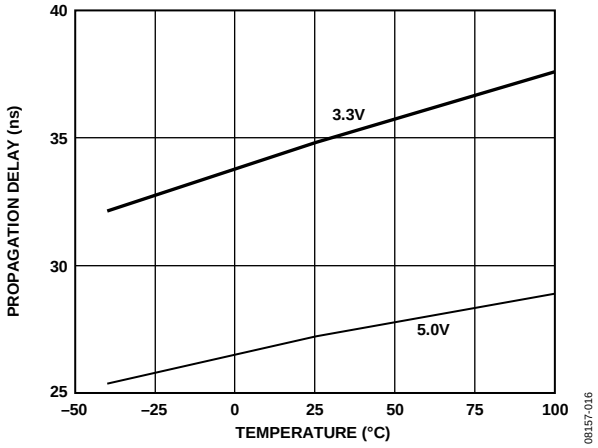



*Figure 16. Propagation Delay vs. Temperature, C Grade*

# APPLICATIONS INFORMATION

## PC BOARD LAYOUT

The ADuM440x digital isolators require no external interface circuitry for the logic interfaces. Power supply bypassing is strongly recommended at the input and output supply pins (see Figure 17). Bypass capacitors are most conveniently connected between Pin 1 and Pin 2 for $V_{DD1}$ and between Pin 15 and Pin 16 for $V_{DD2}$. The capacitor value should be between 0.01 µF and 0.1 µF. The total lead length between both ends of the capacitor and the input power supply pin should not exceed 20 mm. Bypassing between Pin 1 and Pin 8 and between Pin 9 and Pin 16 should also be considered unless the ground pair on each package side are connected close to the package.

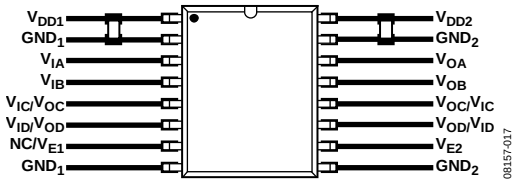



*Figure 17. Recommended Printed Circuit Board Layout*

In applications involving high common-mode transients, ensure that board coupling across the isolation barrier is minimized. Furthermore, the board layout should be designed such that any coupling that does occur equally affects all pins on a given component side. Failure to ensure this could cause voltage differentials between pins exceeding the Absolute Maximum Ratings of the device, thereby leading to latch-up or permanent damage.

See the AN-1109 Application Note for board layout guidelines.

## SYSTEM-LEVEL ESD CONSIDERATIONS AND ENHANCEMENTS

System-level ESD reliability (for example, per IEC 61000-4-x) is highly dependent on system design, which varies widely by application. The ADuM440x incorporate many enhancements to make ESD reliability less dependent on system design. The enhancements include

- ESD protection cells added to all input/output interfaces.
- Key metal trace resistances reduced using wider geometry and paralleling of lines with vias.
- The SCR effect, inherent in CMOS devices, minimized by using guarding and isolation techniques between PMOS and NMOS devices.
- Areas of high electric field concentration eliminated using 45° corners on metal traces.
- Supply pin overvoltage prevented with larger ESD clamps between each supply pin and its respective ground.

While the ADuM440x improve system-level ESD reliability, they are no substitute for a robust system-level design. See the AN-793 Application Note, *ESD/Latch-Up Considerations with iCoupler Isolation Products*, for detailed recommendations on board layout and system-level design.

## PROPAGATION DELAY-RELATED PARAMETERS

Propagation delay is a parameter that describes the length of time for a logic signal to propagate through a component. The propagation delay to a logic low output can differ from the propagation delay to logic high.

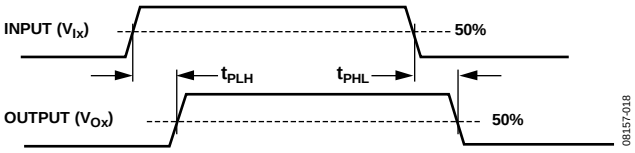



*Figure 18. Propagation Delay Parameters*

Pulse width distortion is the maximum difference between these two propagation delay values and is an indication of how accurately the input signal's timing is preserved.

Channel-to-channel matching refers to the maximum amount the propagation delay differs among channels within a single ADuM440x component.

Propagation delay skew refers to the maximum amount the propagation delay differs among multiple ADuM440x components operated under the same conditions.

## DC CORRECTNESS AND MAGNETIC FIELD IMMUNITY

Positive and negative logic transitions at the isolator input cause narrow (~1 ns) pulses to be sent via the transformer to the decoder. The decoder is bistable and is therefore either set or reset by the pulses, indicating input logic transitions. In the absence of logic transitions at the input for more than ~1 µs, a periodic set of refresh pulses indicative of the correct input state are sent to ensure dc correctness at the output. If the decoder receives no internal pulses for more than approximately 5 µs, the input side is assumed to be without power or nonfunctional; in which case, the isolator output is forced to a default state (see Table 20) by the watchdog timer circuit.

The limitation on the ADuM440x magnetic field immunity is set by the condition in which induced voltage in the transformer's receiving coil is large enough to either falsely set or reset the decoder. The following analysis defines the conditions under which this can occur. The 3 V operating condition of the ADuM440x is examined because it represents the most susceptible mode of operation.

The pulses at the transformer output have an amplitude greater than 1.0 V. The decoder has a sensing threshold at about 0.5 V, thereby establishing a 0.5 V margin in which induced voltages can be tolerated. The voltage induced across the receiving coil is given by

$$V = (-d\beta/dt)\Sigma\prod r_n^2; n = 1, 2,\ldots, N$$

where:
$\beta$ is the magnetic flux density (gauss).
$N$ is the number of turns in the receiving coil.
$r_n$ is the radius of the n$^{th}$ turn in the receiving coil (cm).

Given the geometry of the receiving coil in the ADuM440x and an imposed requirement that the induced voltage be at most 50% of the 0.5 V margin at the decoder, a maximum allowable magnetic field is calculated as shown in Figure 19.

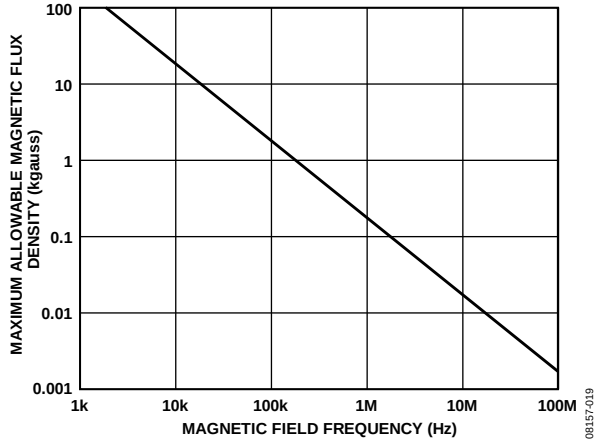



*Figure 19. Maximum Allowable External Magnetic Flux Density*

For example, at a magnetic field frequency of 1 MHz, the maximum allowable magnetic field of 0.2 kgauss induces a voltage of 0.25 V at the receiving coil. This is about 50% of the sensing threshold and does not cause a faulty output transition. Similarly, if such an event were to occur during a transmitted pulse (and was of the worst-case polarity), it would reduce the received pulse from >1.0 V to 0.75 V—still well above the 0.5 V sensing threshold of the decoder.

The preceding magnetic flux density values correspond to specific current magnitudes at given distances away from the ADuM440x transformers. Figure 20 expresses these allowable current magnitudes as a function of frequency for selected distances. As can be seen, the ADuM440x are immune and can be affected only by extremely large currents operated at high frequency and very close to the component. For the 1 MHz example noted, one would have to place a 0.5 kA current 5 mm away from the ADuM440x to affect the component's operation.

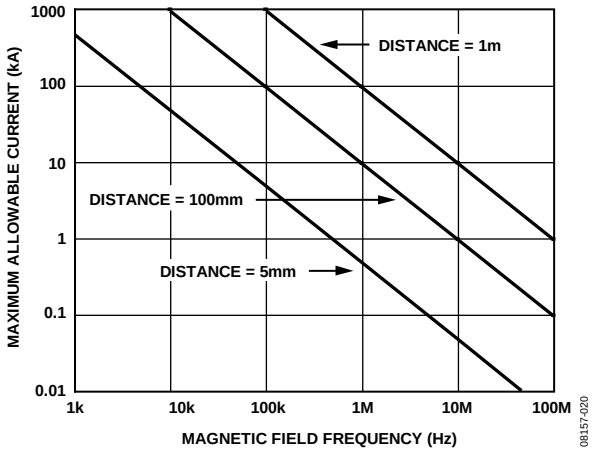



*Figure 20. Maximum Allowable Current for Various Current-to-ADuM440x Spacings*

Note that at combinations of strong magnetic field and high frequency, any loops formed by printed circuit board traces may induce sufficiently large error voltages to trigger the thresholds of succeeding circuitry. Care should be taken in the layout of such traces to avoid this possibility.

## POWER CONSUMPTION

The supply current at a given channel of the ADuM440x isolator is a function of the supply voltage, the channel's data rate, and the channel's output load.

For each input channel, the supply current is given by

$$I_{DDI} = I_{DDI\,(Q)} \qquad f \le 0.5f_r$$

$$I_{DDI} = I_{DDI\,(D)} \times (2f - f_r) + I_{DDI\,(Q)} \qquad f > 0.5f_r$$

For each output channel, the supply current is given by:

$$I_{DDO} = I_{DDO\,(Q)} \qquad f \le 0.5f_r$$

$$I_{DDO} = (I_{DDO\,(D)} + (0.5 \times 10^{-3}) \times C_L V_{DDO}) \times (2f - f_r) + I_{DDO\,(Q)} \qquad f > 0.5f_r$$

where:
$I_{DDI\,(D)}$, $I_{DDO\,(D)}$ are the input and output dynamic supply currents per channel (mA/Mbps).
$C_L$ is the output load capacitance (pF).
$V_{DDO}$ is the output supply voltage (V).
$f$ is the input logic signal frequency (MHz, half of the input data rate, NRZ signaling).
$f_r$ is the input stage refresh rate (Mbps).
$I_{DDI\,(Q)}$, $I_{DDO\,(Q)}$ are the specified input and output quiescent supply currents (mA).

To calculate the total $I_{DD1}$ and $I_{DD2}$, the supply currents for each input and output channel corresponding to $I_{DD1}$ and $I_{DD2}$ are calculated and totaled. Figure 8 and Figure 9 provide per channel supply currents as a function of data rate for an unloaded output condition. Figure 10 provides per channel supply current as a function of data rate for a 15 pF output condition. Figure 11 through Figure 15 provide total $I_{DD1}$ and $I_{DD2}$ as a function of data rate for ADuM4400/ADuM4401/ ADuM4402 channel configurations.

## INSULATION LIFETIME

All insulation structures eventually break down when subjected to voltage stress over a sufficiently long period. The rate of insulation degradation is dependent on the characteristics of the voltage waveform applied across the insulation. In addition to the testing performed by the regulatory agencies, Analog Devices carries out an extensive set of evaluations to determine the lifetime of the insulation structure within the ADuM440x.

Analog Devices performs accelerated life testing using voltage levels higher than the rated continuous working voltage. Acceleration factors for several operating conditions are determined. These factors allow calculation of the time to failure at the actual working voltage. The values shown in Table 19 summarize the peak voltage for 50 years of service life for a bipolar ac operating condition and the maximum CSA/VDE approved working voltages. In many cases, the approved working voltage is higher than the 50-year service life voltage. Operation at these high working voltages can lead to shortened insulation life in some cases.

The insulation lifetime of the ADuM440x depends on the voltage waveform type imposed across the isolation barrier. The *i*Coupler insulation structure degrades at different rates, depending on whether the waveform is bipolar ac, unipolar ac, or dc. Figure 21, Figure 22, and Figure 23 illustrate these different isolation voltage waveforms.

Bipolar ac voltage is the most stringent environment. The goal of a 50-year operating lifetime under the ac bipolar condition determines Analog Devices recommended maximum working voltage.

In the case of unipolar ac or dc voltage, the stress on the insulation is significantly lower. This allows operation at higher working voltages while still achieving a 50-year service life. The working voltages listed in Table 19 can be applied while maintaining the 50-year minimum lifetime, provided the voltage conforms to either the unipolar ac or dc voltage cases. Any cross-insulation voltage waveform that does not conform to Figure 22 or Figure 23 should be treated as a bipolar ac waveform, and its peak voltage should be limited to the 50-year lifetime voltage value listed in Table 19.

Note that the voltage presented in Figure 22 is shown as sinusoidal for illustration purposes only. It is meant to represent any voltage waveform varying between 0 V and some limiting value. The limiting value can be positive or negative, but the voltage cannot cross 0 V.

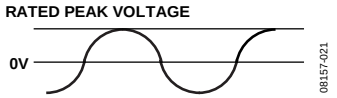



*Figure 21. Bipolar AC Waveform*

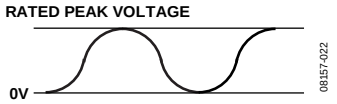



*Figure 22. Unipolar AC Waveform*

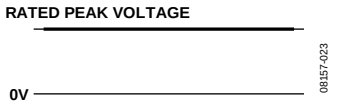
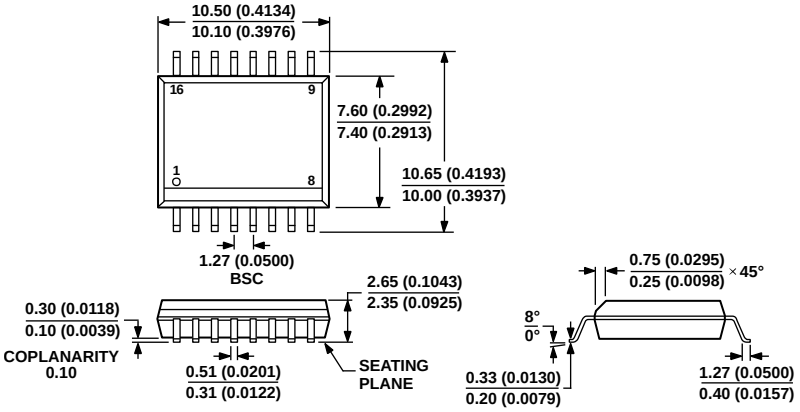



*Figure 23. DC Waveform*

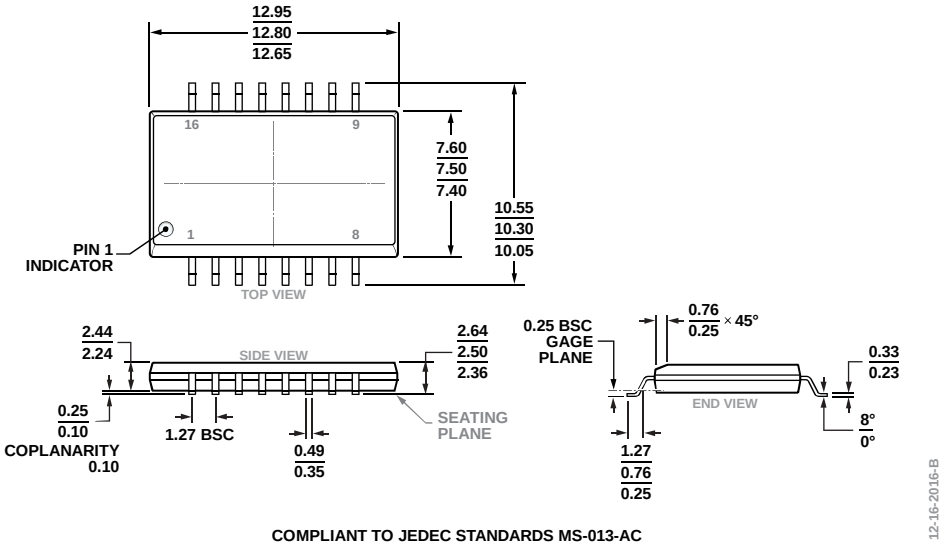
# OUTLINE DIMENSIONS




COMPLIANT TO JEDEC STANDARDS MS-013-AA
CONTROLLING DIMENSIONS ARE IN MILLIMETERS; INCH DIMENSIONS
(IN PARENTHESES) ARE ROUNDED-OFF MILLIMETER EQUIVALENTS FOR
REFERENCE ONLY AND ARE NOT APPROPRIATE FOR USE IN DESIGN.

03-27-2007-B

*Figure 24. 16-Lead Standard Small Outline Package [SOIC_W]*
*Wide Body (RW-16)*
*Dimensions shown in millimeters and (inches)*




COMPLIANT TO JEDEC STANDARDS MS-013-AC

12-16-2016-B

*Figure 25. 16-Lead Standard Small Outline Package, with Increased Creepage [SOIC_IC]*
*Wide Body*
*(RI-16-2)*
*Dimension shown in millimeters*

## ORDERING GUIDE

| Model[1, 2] | Number of Inputs, $V_{DD1}$ Side | Number of Inputs, $V_{DD2}$ Side | Maximum Data Rate (Mbps) | Maximum Propagation Delay, 5 V (ns) | Maximum Pulse Width Distortion (ns) | Temperature Range | Package Description | Package Option |
|---|---|---|---|---|---|---|---|---|
| ADuM4400ARWZ | 4 | 0 | 1 | 100 | 40 | −40°C to +105°C | 16-Lead SOIC_W | RW-16 |
| ADuM4400ARWZ-RL | 4 | 0 | 1 | 100 | 40 | −40°C to +105°C | 16-Lead SOIC_W | RW-16 |
| ADuM4400BRWZ | 4 | 0 | 10 | 50 | 3 | −40°C to +105°C | 16-Lead SOIC_W | RW-16 |
| ADuM4400BRWZ-RL | 4 | 0 | 10 | 50 | 3 | −40°C to +105°C | 16-Lead SOIC_W | RW-16 |
| ADuM4400CRWZ | 4 | 0 | 90 | 32 | 2 | −40°C to +105°C | 16-Lead SOIC_W | RW-16 |
| ADuM4400CRWZ-RL | 4 | 0 | 90 | 32 | 2 | −40°C to +105°C | 16-Lead SOIC_W | RW-16 |
| ADuM4400ARIZ | 4 | 0 | 1 | 100 | 40 | −40°C to +105°C | 16-Lead SOIC_IC | RI-16-2 |
| ADuM4400ARIZ-RL | 4 | 0 | 1 | 100 | 40 | −40°C to +105°C | 16-Lead SOIC_IC | RI-16-2 |
| ADuM4400BRIZ | 4 | 0 | 10 | 50 | 3 | −40°C to +105°C | 16-Lead SOIC_IC | RI-16-2 |
| ADuM4400BRIZ-RL | 4 | 0 | 10 | 50 | 3 | −40°C to +105°C | 16-Lead SOIC_IC | RI-16-2 |
| ADuM4400CRIZ | 4 | 0 | 90 | 32 | 2 | −40°C to +105°C | 16-Lead SOIC_IC | RI-16-2 |
| ADuM4400CRIZ-RL | 4 | 0 | 90 | 32 | 2 | −40°C to +105°C | 16-Lead SOIC_IC | RI-16-2 |
| ADuM4401ARWZ | 3 | 1 | 1 | 100 | 40 | −40°C to +105°C | 16-Lead SOIC_W | RW-16 |
| ADuM4401ARWZ-RL | 3 | 1 | 1 | 100 | 40 | −40°C to +105°C | 16-Lead SOIC_W | RW-16 |
| ADuM4401BRWZ | 3 | 1 | 10 | 50 | 3 | −40°C to +105°C | 16-Lead SOIC_W | RW-16 |
| ADuM4401BRWZ-RL | 3 | 1 | 10 | 50 | 3 | −40°C to +105°C | 16-Lead SOIC_W | RW-16 |
| ADuM4401CRWZ | 3 | 1 | 90 | 32 | 2 | −40°C to +105°C | 16-Lead SOIC_W | RW-16 |
| ADuM4401CRWZ-RL | 3 | 1 | 90 | 32 | 2 | −40°C to +105°C | 16-Lead SOIC_W | RW-16 |
| ADuM4401ARIZ | 3 | 1 | 1 | 100 | 40 | −40°C to +105°C | 16-Lead SOIC_IC | RI-16-2 |
| ADuM4401ARIZ-RL | 3 | 1 | 1 | 100 | 40 | −40°C to +105°C | 16-Lead SOIC_IC | RI-16-2 |
| ADuM4401BRIZ | 3 | 1 | 10 | 50 | 3 | −40°C to +105°C | 16-Lead SOIC_IC | RI-16-2 |
| ADuM4401BRIZ-RL | 3 | 1 | 10 | 50 | 3 | −40°C to +105°C | 16-Lead SOIC_IC | RI-16-2 |
| ADuM4401CRIZ | 3 | 1 | 90 | 32 | 2 | −40°C to +105°C | 16-Lead SOIC_IC | RI-16-2 |
| ADuM4401CRIZ-RL | 3 | 1 | 90 | 32 | 2 | −40°C to +105°C | 16-Lead SOIC_IC | RI-16-2 |
| ADuM4402ARWZ | 2 | 2 | 1 | 100 | 40 | −40°C to +105°C | 16-Lead SOIC_W | RW-16 |
| ADuM4402ARWZ-RL | 2 | 2 | 1 | 100 | 40 | −40°C to +105°C | 16-Lead SOIC_W | RW-16 |
| ADuM4402BRWZ | 2 | 2 | 10 | 50 | 3 | −40°C to +105°C | 16-Lead SOIC_W | RW-16 |
| ADuM4402BRWZ-RL | 2 | 2 | 10 | 50 | 3 | −40°C to +105°C | 16-Lead SOIC_W | RW-16 |
| ADuM4402CRWZ | 2 | 2 | 90 | 32 | 2 | −40°C to +105°C | 16-Lead SOIC_W | RW-16 |
| ADuM4402CRWZ-RL | 2 | 2 | 90 | 32 | 2 | −40°C to +105°C | 16-Lead SOIC_W | RW-16 |
| ADuM4402ARIZ | 2 | 2 | 1 | 100 | 40 | −40°C to +105°C | 16-Lead SOIC_IC | RI-16-2 |
| ADuM4402ARIZ-RL | 2 | 2 | 1 | 100 | 40 | −40°C to +105°C | 16-Lead SOIC_IC | RI-16-2 |
| ADuM4402BRIZ | 2 | 2 | 10 | 50 | 3 | −40°C to +105°C | 16-Lead SOIC_IC | RI-16-2 |
| ADuM4402BRIZ-RL | 2 | 2 | 10 | 50 | 3 | −40°C to +105°C | 16-Lead SOIC_IC | RI-16-2 |
| ADuM4402CRIZ | 2 | 2 | 90 | 32 | 2 | −40°C to +105°C | 16-Lead SOIC_IC | RI-16-2 |
| ADuM4402CRIZ-RL | 2 | 2 | 90 | 32 | 2 | −40°C to +105°C | 16-Lead SOIC_IC | RI-16-2 |

[1] Tape and reel is available. The addition of an -RL suffix designates a 13" (1,000 units) tape and reel option.
[2] Z = RoHS Compliant Part.

## NOTES


D08157-0-7/17(F)

# Mouser Electronics

Authorized Distributor

Click to View Pricing, Inventory, Delivery & Lifecycle Information:

Analog Devices Inc.:

ADUM4402CRIZ-RL ADUM4402CRIZ