



Integrated, Precision Battery Sensor for Automotive Systems

Data Sheet

ADuCM330WFS/ADuCM331WFS

FEATURES

High precision ADCs
Dual-channel, simultaneous sampling
IADC 20-bit $\Sigma\Delta$ (minimizes range switching)
VADC/TADC 20-bit $\Sigma\Delta$
Programmable ADC conversion rate from 4 Hz to 8 kHz
On-chip ± 5 ppm/ $^{\circ}\text{C}$ voltage reference
Current channel
Fully differential, buffered input
Programmable gain (from 4 to 512)
ADC absolute input range: -200 mV to $+300$ mV
Digital comparator with current accumulator feature
Voltage channel
Buffered, on-chip attenuator for 12 V battery input
Temperature channel
External and on-chip temperature sensor options
Microcontroller
ARM Cortex-M3 32-bit processor
16.384 MHz precision oscillator with 1% accuracy (high precision)
Serial wire debug (SWD) port supporting code download and debug
Automotive qualified integrated LIN transceiver
LIN 2.2A-compatible slave, 100 kbaud fast download option
SAE J2602-compatible slave
Low electromagnetic emissions
High electromagnetic immunity

Memory
96 kB programmable Flash/EE memory (ADuCM330WFS), ECC
128 kB programmable Flash/EE memory (ADuCM331WFS), ECC
10 kB SRAM, ECC
4 kB data Flash/EE memory, ECC
10,000 cycle Flash/EE endurance
20 year Flash/EE retention
In circuit download via SWD and LIN
On-chip peripherals
SPI
GPIO port
General-purpose timer
Wake-up timer
Watchdog timer
On-chip, power-on reset
Power
Operates directly from 12 V battery supply
Power consumption, 8 mA typical (16 MHz) at $T_A = -40^{\circ}\text{C}$ to $+115^{\circ}\text{C}$
Low power monitor mode
Package and temperature range
6 mm \times 6 mm, 32-lead LFCSP
Fully specified for -40°C to $+115^{\circ}\text{C}$ operation; additional specifications for 115°C to 125°C
AEC-Q100 qualified for automotive applications
Developed for use in ISO 26262 applications for ASIL Capability B

APPLICATIONS

Battery sensing and management for automotive and light mobility vehicles
Lead acid battery measurement for power supplies in industrial and medical domains

Rev. D

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TABLE OF CONTENTS

| | |
|---|----|
| Features | 1 |
| Applications | 1 |
| Revision History | 2 |
| Functional Block Diagram | 3 |
| General Description | 4 |
| Specifications | 5 |
| Absolute Maximum Ratings | 12 |
| Thermal Resistance | 12 |
| ESD Caution | 12 |
| Pin Configuration and Function Descriptions | 13 |

REVISION HISTORY

4/2020—Rev. C to Rev. D

| | |
|---------------------------|----|
| Changes to Table 1 | 6 |
| Changes to Figure 2 | 13 |
| Changes to Table 4 | 14 |

8/2019—Rev. B to Rev. C

| | |
|--|----|
| Change to Features Section | 1 |
| Changes to Figure 1 | 3 |
| Changes to General Description Section | 4 |
| Changes to Table 1 | 5 |
| Changes to Figure 2 and Table 4 | 13 |
| Changes to General Recommendations Section | 16 |

6/2019—Rev. A to Rev. B

| | |
|--|----|
| Change to Features Section | 1 |
| Changes to General Description Section | 4 |
| Changes to Table 1 | 10 |
| Changes to Ordering Guide | 17 |

| | |
|---|----|
| Terminology | 15 |
| Applications Information | 16 |
| Design Guidelines | 16 |
| Power and Ground Recommendations | 16 |
| Exposed Pad Thermal Recommendations | 16 |
| General Recommendations | 16 |
| Outline Dimensions | 17 |
| Ordering Guide | 17 |
| Automotive Products | 17 |

2/2019—Rev. 0 to Rev. A

| | |
|---|-----------|
| Added ADuCM330WFS | Universal |
| Changes to Features Section | 1 |
| Changes to Figure 1 | 3 |
| Changes to General Description Section | 4 |
| Changes to Flash/EE Memory Parameter, Table 1 | 8 |
| Added Note 14, Table 1; Renumbered Sequentially | 11 |
| Changes to Thermal Resistance Section and Table 3 | 12 |
| Changes to Ordering Guide | 17 |

12/2018—Revision 0: Initial Version

FUNCTIONAL BLOCK DIAGRAM

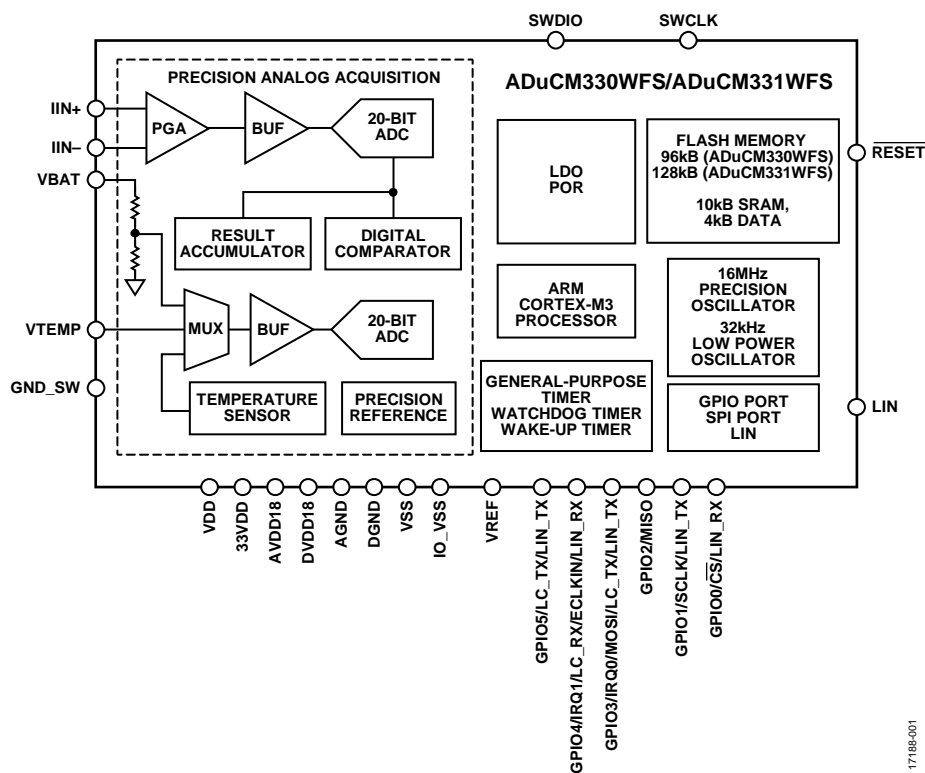


Figure 1.

1718B-001

GENERAL DESCRIPTION

The ADuCM330WFS/ADuCM331WFS are fully integrated, 8 kHz data acquisition systems that incorporate dual, high performance, multichannel, Σ - Δ analog-to-digital converters (ADCs), a 32-bit ARM® Cortex™-M3 processor, and flash. The ADuCM330WFS has 96 kB Flash/EE memory, and the ADuCM331WFS has 128 kB Flash/EE memory. Both devices have 4 kB data flash. Error correction code (ECC) is available on all flash and SRAM memories.

The ADuCM330WFS/ADuCM331WFS are complete system solutions for battery monitoring in 12 V automotive applications.

The ADuCM330WFS/ADuCM331WFS integrate all features required to precisely and intelligently monitor, process, and diagnose 12 V battery parameters including battery current, voltage, and temperature over a wide range of operating conditions.

Minimizing external system components, the devices are powered directly from a 12 V battery. On-chip, low dropout (LDO) regulators generate the supply voltage for two integrated Σ - Δ ADCs. The ADCs precisely measure battery current, voltage, and temperature to characterize the state of the health and the charge of the car battery.

The devices operate from an on-chip, 16.384 MHz high frequency oscillator that supplies the system clock that is routed through a programmable clock divider, from which the core clock operating frequency is generated. The devices also contain a 32.768 kHz oscillator for low power operation.

The analog subsystem consists of an ADC with a programmable gain amplifier (PGA) that allows the monitoring of various current and voltage ranges. The analog subsystem also includes an on-chip precision reference.

The ADuCM330WFS/ADuCM331WFS integrate a range of on-chip peripherals that can be configured under core software

control as required in the application. These peripherals include a serial port interface (SPI) serial input/output communication controller, six general-purpose input/output (GPIO) pins, one general-purpose timer, a wake-up timer, and a watchdog timer. See the [ADuCM330WFS/ADuCM331WFS Hardware Reference Manual](#) for more information.

The ADuCM330WFS/ADuCM331WFS are designed to operate in battery-powered applications where low power operation is critical. The microcontroller core can be configured in normal operating mode, resulting in an overall system current consumption of 18.5 mA when all peripherals are active. The devices can also be configured in a number of low power operating modes under direct program control, consuming <100 μ A.

The ADuCM330WFS/ADuCM331WFS include a local interconnect network (LIN) physical interface for single-wire, high voltage communications in automotive environments. The LIN transceiver is compliant to LIN 2.2A and Society of Automotive Engineers (SAE) J2602-2.

The devices operate from an external 3.6 V to 19 V (on VDD, Pin 26) voltage supply and are specified over the -40°C to $+115^{\circ}\text{C}$ temperature range, with additional typical specifications at $+115^{\circ}\text{C}$ to $+125^{\circ}\text{C}$.

The information in this data sheet is relevant for Silicon Revision P60.

The ADuCM330WFS/ADuCM331WFS are developed for use in ISO 26262 applications for Automotive Safety Integrity Level Capability B.

The ADuCM330WFS/ADuCM331WFS are low electromagnetic emissions and high electromagnetic immunity devices.

Multifunction pin names may be referenced by the relevant function only.

SPECIFICATIONS

VDD = 3.6 V to 19 V, ARM Cortex-M3 processor frequency (f_{CLK}) = 16.384 MHz, clock divider bits (CD) = 0, normal mode, and voltage reference (V_{REF}) = 1.2 V (internal), unless otherwise stated. Typical values noted reflect the approximate parameter mean at $T_A = 25^\circ\text{C}$ under nominal conditions, unless otherwise stated. Safe operation of the device is not guaranteed outside the temperature range of $T_A = -40^\circ\text{C}$ to $+115^\circ\text{C}$ or outside the specified VDD supply range. Parameters specified in the 115°C to 125°C temperature range of operation are functional within this range but with degraded performance.

Table 1.

| Parameter | Test Conditions/Comments | T _A = −40°C to +115°C | | | T _A = +115°C to +125°C ¹ | | | Unit |
|--|---|--|------|-------|--|-------|-----|------------|
| | | Min | Typ | Max | Min | Typ | Max | |
| ADC SPECIFICATIONS | | | | | | | | |
| Conversion Rate ¹ | ADC normal operating mode, chop off | 4 | | 8000 | | | | Hz |
| | ADC normal operating mode, chop on | 4 | | 2000 | | | | Hz |
| | ADC low power mode, chop on | 1 | | 656 | | | | Hz |
| Current Channel (IIN+/IIN− Only) | | | | | | | | |
| No Missing Codes ¹ | Valid for all ADC update rates and ADC modes | 20 | | | | | | Bits |
| Integral Nonlinearity (INL) ^{1, 2} | ADCFLT = 0x10001, 0x08101, 0x00007 | −200 | ±10 | +200 | | ±80 | | ppm of FSR |
| Offset Error ^{1, 3, 4} | Chop off, gain = 4, 8, or 16, external short, after user system calibration at 25°C, 1 LSB = (2.28/gain) μV | −100 | ±24 | +100 | | | | LSBs |
| | Chop off, gain = 32 or 64, external short, after user system calibration at 25°C, 1 LSB = (2.28/gain) μV | −160 | ±48 | +160 | | | | LSBs |
| | Chop off, gain = 512, external short, after user system calibration at 25°C, 1 LSB = (2.28/gain) μV | −1400 | ±60 | +1400 | | | | LSBs |
| | Chop on, external short, low power mode, gain = 64 or 512, processor powered down | −300 | ±50 | +250 | | ±250 | | nV |
| | Chop on, external short, after user system calibration at 25°C, VDD = 19 V | −0.65 | | +0.65 | | ±0.1 | | μV |
| | Offset Error Drift ^{1, 2, 5} | Chop off, gain of 4 to 64, normal mode | | ±0.48 | | | | LSB/°C |
| | | Chop on | | ±5 | | | ±5 | nV/°C |
| Total Gain Error ^{1, 3, 4, 6} | Factory calibrated at a gain of 8, PGASCALE = 0b01, normal mode | −0.5 | ±0.1 | +0.5 | | ±0.15 | | % |
| | Low power mode | −1 | ±0.2 | +1 | | ±0.2 | | % |
| Gain Drift ^{1, 7} | | | ±3 | | | ±3 | | ppm/°C |
| PGA Gain Mismatch Error | | | ±0.1 | | | ±0.1 | | % |
| Output Noise ^{1, 8} | Register PGASCALE, Bits[11:10] = 0x3 | | | | | | | |
| | Gain = 64, ADCFLT = 0x08101 | | 0.80 | 1.3 | | 1.2 | | μV rms |
| | Gain = 64, ADCFLT = 0x00007 | | 0.75 | 1.1 | | | | μV rms |
| | Gain = 32, ADCFLT = 0x08101 | | 1.00 | 1.5 | | 1.3 | | μV rms |
| | Gain = 32, ADCFLT = 0x00007 | | 0.80 | 1.2 | | | | μV rms |
| | Gain = 16, ADCFLT = 0x08101 | | 1.50 | 2.6 | | 2.0 | | μV rms |
| | Gain = 16, ADCFLT = 0x00007 | | 1.10 | 1.9 | | | | μV rms |
| | Gain = 8, ADCFLT = 0x08101 | | 2.10 | 4.1 | | 2.5 | | μV rms |
| | Gain = 8, ADCFLT = 0x00007 | | 1.60 | 2.4 | | | | μV rms |
| | Gain = 4, ADCFLT = 0x08101 | | 3.40 | 5.1 | | 4.0 | | μV rms |
| | Gain = 4, ADCFLT = 0x00007 | | 2.60 | 3.9 | | | | μV rms |

| Parameter | Test Conditions/Comments | T _A = –40°C to +115°C | | | T _A = +115°C to +125°C ¹ | | | Unit |
|--|---|----------------------------------|-----------|-------|--|-------|-----|------------|
| | | Min | Typ | Max | Min | Typ | Max | |
| Voltage Channel ^{1,9} | Gain = 64, ADCFLT = 0x10001 | | 1.55 | 2.0 | | 1.85 | | μV rms |
| | Gain = 32, ADCFLT = 0x10001 | | 1.6 | 2.3 | | 2.0 | | μV rms |
| | Gain = 16, ADCFLT = 0x10001 | | 1.8 | 2.5 | | 2.1 | | μV rms |
| | Gain = 8, ADCFLT = 0x10001 | | 2.5 | 3.5 | | 3.0 | | μV rms |
| | Gain = 4, ADCFLT = 0x10001 | | 4.3 | 6.5 | | 5.0 | | μV rms |
| | ADC low power mode, 221 Hz update rate, chop enabled, gain = 64 | | 0.6 | 0.9 | | 0.8 | | μV rms |
| | ADC low power mode, 221 Hz update rate, chop enabled, gain = 64 | | 0.6 | 0.9 | | 0.8 | | μV rms |
| No Missing Codes | Valid at all ADC update rates | 20 | | | | | | Bits |
| INL | From 6 V to 18 V, ADCFLT = 0x10001, 0x08101, 0x00007 | –350 | ±10 | +350 | | ±150 | | ppm of FSR |
| Offset Error ^{3,4} | Chop off, 1 LSB = 27.4 μV, after two-point calibration | –160 | ±16 | +160 | | | | LSB |
| | Chop on, after two-point calibration, offset measured using 0 V differential into voltage ADC (VADC) auxiliary pins | –16 | ±4.8 | +16 | | ±4.8 | | LSB |
| Offset Error Drift ⁵ | Chop off | | ±0.48 | | | ±1 | | LSB/°C |
| Total Gain Error ^{3,4,6} | After user system calibration at 25°C, includes resistor mismatch | –0.25 | ±0.06 | +0.25 | | ±0.1 | | % |
| | T _A = –25°C to +65°C | –0.15 | ±0.03 | +0.15 | | | | % |
| Gain Drift ⁷ | Includes resistor mismatch drift | | ±3 | | | ±3 | | ppm/°C |
| Output Noise ¹⁰ | 10 Hz update rate, chop on | | 50 | | | | | μV rms |
| | ADCFLT = 0x00007 | | 180 | 270 | | | | μV rms |
| | From 6 V to 18 V, ADCFLT = 0x08101 | | 280 | 350 | | 300 | | μV rms |
| | ADCFLT = 0x10001 | | 400 | 500 | | 470 | | μV rms |
| Temperature Channel ¹ | | | | | | | | |
| No Missing Codes | Valid at all ADC update rates | 20 | | | | | | Bits |
| INL | ADCFLT = 0x10001, 0x08101, 0x00007 | –60 | ±10 | +60 | | ±15 | | ppm of FSR |
| Offset Error ^{3,11} | Chop off, 1 LSB = 1.14 μV (unipolar mode), after two-point calibration | –160 | ±48 | +160 | | | | LSB |
| Offset Error ³ | Chop on | –80 | +16 | +80 | | ±16 | | LSB |
| Offset Error Drift | Chop off | | ±0.48 | | | ±0.48 | | LSB/°C |
| Total Gain Error ^{3,11} | | –0.25 | ±0.06 | +0.25 | | ±0.10 | | % |
| Gain Drift ⁷ | | | 3 | | | 3 | | ppm/°C |
| Output Noise | 1 kHz update rate, ADCFLT = 0x00007 | | 7.5 | 11.25 | | 10 | | μV rms |
| ADC SPECIFICATIONS, ANALOG INPUT | PGASCALE, Bits[11:10] = 0x3 | | | | | | | |
| Current Channel ¹ | | | | | | | | |
| Absolute Input Voltage Range | Applies to both IIN+ and IIN– | –200 | | +300 | | | | mV |
| Differential Input Voltage Range ¹² | Range = V _{REF} /gain, limited by absolute input voltage range | | ±1.2/gain | | | | | V |
| Input Leakage Current ¹³ | | –3 | | +3 | | ±0.2 | | nA |
| Input Offset Current ¹³ | | | 0.2 | 0.6 | | 0.4 | | nA |
| Voltage Channel | | | | | | | | |
| Absolute Input Voltage Range ¹ | Voltage ADC specifications are valid in this range | 6 | | 19 | | | | V |
| Input Voltage Range ¹ | | | 0 to 28.8 | | | | | V |

| Parameter | Test Conditions/Comments | T _A = -40°C to +115°C | | | T _A = +115°C to +125°C ¹ | | | Unit |
|--|--|----------------------------------|----------|-------|--|-----|-----|-------------|
| | | Min | Typ | Max | Min | Typ | Max | |
| VBAT Input Current | VBAT = 18 V | 5 | 9 | 13 | | 11 | | μA |
| Temperature Channel | V _{REF} ¹⁴ = AVDD18 and GND_SW | | | | | | | |
| Absolute Input Voltage Range ^{1, 15} | | 100 | | 1500 | | | | mV |
| Input Voltage Range ¹ | | | 0 to 1.4 | | | | | V |
| VTEMP Input Current ¹ | | | 2.5 | 10 | | 3.5 | | nA |
| VOLTAGE REFERENCE | | | | | | | | |
| Internal Reference | | | 1.2 | | | 1.2 | | V |
| Power-Up Time ¹ | | | 0.5 | | | 0.5 | | ms |
| Initial Accuracy ¹ | Measured at T _A = 25°C | -0.15 | | +0.15 | | | | % |
| Temperature Coefficient ^{1, 16} | | -20 | ±5 | +20 | | ±8 | | ppm/°C |
| Long-Term Stability ¹⁷ | | | 100 | | | | | ppm/1000 Hr |
| RESISTIVE ATTENUATOR | | | | | | | | |
| Divider Ratio | | | 24 | | | | | |
| Resistor Mismatch Drift | Implicit in the voltage channel gain error specification | | ±3 | | | | | ppm/°C |
| ADC GROUND SWITCH | | | | | | | | |
| Resistor to Ground | | 45 | 60 | 75 | | | | kΩ |
| TEMPERATURE SENSOR ^{1, 18} | Processor in hibernate mode, ADCFLT = chop on | | | | | | | |
| Accuracy | T _A = 115°C to 125°C | -3.5 | ±1 | +3.5 | | ±1 | | °C |
| | T _A = -40°C to +115°C | -3 | ±1 | +3 | | | | °C |
| | T _A = -25°C to +85°C | -2.5 | ±0.5 | +2.5 | | | | °C |
| | T _A = -10°C to +55°C | -2 | ±0.5 | +2 | | | | °C |
| ADC DIAGNOSTICS ¹ | | | | | | | | |
| AVDD18/136 Accuracy ^{2, 19} | SM101 | 12 | | 14 | | 13 | | mV |
| Current Channel | SM102 | | | | | | | |
| Diagnostic Current | | 35 | 50 | 65 | | | | μA |
| Diagnostic Current Matching | | -5 | ±0.5 | +5 | | | | μA |
| Internal Electrostatic Discharge (ESD) Resistor Matching | | -120 | | +120 | | | | Ω |
| Voltage Channel | | | | | | | | |
| Input Test Voltage (V _{BE}) | SM91-VBE | 525 | 700 | 875 | | | | mV |
| Voltage Attenuator Current Source Accuracy | SM92, differential voltage increase on the attenuator when current is on | 2.4 | | 3.2 | | 2.8 | | V |
| Diagnostic Attenuator Divider Ratio | | | 48 | | | | | |
| POWER-ON RESET (POR) ¹ | Refers to voltage at the VDD pin | | | | | | | |
| POR Trip Level | SM8 | 2.9 | 3.1 | 3.4 | | 3.3 | | V |
| POR Hysteresis | | | 0.1 | | | | | V |
| LOW VOLTAGE FLAG | | | | | | | | |
| Low Voltage Flag Level | Refers to voltage at the VDD pin | 2.6 | 2.75 | 3.00 | | | | V |

| Parameter | Test Conditions/Comments | T _A = –40°C to +115°C | | | T _A = +115°C to +125°C ¹ | | | Unit |
|--|--|----------------------------------|--------|-------|--|------|-----|--------|
| | | Min | Typ | Max | Min | Typ | Max | |
| WATCHDOG TIMER | | | | | | | | |
| Shortest Timeout Period | 32,768 Hz clock with a prescaler of 1 | | 122 | | | 122 | | μs |
| Longest Timeout Period | 32,768 Hz clock with a prescaler of 4096 | | 8192 | | | 8192 | | sec |
| SRAM SIZE | | | 10 | | | | | kB |
| FLASH/EE MEMORY | | | | | | | | |
| Program Flash Size | ADuCM330WFS | | 96 | | | | | kB |
| | ADuCM331WFS | | 128 | | | | | kB |
| Data Flash Size | | | 4 | | | | | kB |
| Endurance ²⁰ | | 10,000 | | | | | | Cycles |
| Data Retention ²¹ | | 20 | | | | | | Years |
| LOGIC INPUTS ¹ | | | | | | | | |
| Input Voltage | | | | | | | | |
| Low (V _{INL}) | | | | 0.4 | | | | V |
| High (V _{INH}) | | 2.0 | | | | | | V |
| LOGIC OUTPUTS ¹ | All logic outputs measured with ±1 mA load | | | | | | | |
| Output Voltage | | | | | | | | |
| High (V _{OH}) | | 33VDD – 0.4 | | | | | | V |
| Low (V _{OL}) | | | | 0.4 | | | | V |
| DIGITAL INPUTS ¹ | All digital inputs except RESET, SWDIO, and SWCLK | | | | | | | |
| Logic 1 Input Current (Leakage Current) | V _{INH} = 3.3 V | –10 | ±1 | +10 | | | | μA |
| Logic 0 Input Current (Leakage Current) | V _{INL} = 0 V | –10 | ±1 | +10 | | | | μA |
| Input Capacitance | | | 10 | | | | | pF |
| ON-CHIP OSCILLATORS | | | | | | | | |
| Low Frequency Oscillator | | | 32,768 | | | | | Hz |
| Accuracy | | –30 | ±5 | +30 | | | | % |
| | After a calibration from high frequency oscillator | –6 | | +6 | | | | % |
| High Frequency Oscillator | | | 16.384 | | | | | MHz |
| Accuracy (Calibration Function) ^{1, 22} | | –0.75 | ±0.5 | +0.75 | | | | % |
| High Precision Mode | | –1 | | +1 | | | | % |
| Low Precision Mode | | –3 | | +3 | | | | % |
| PROCESSOR START-UP TIME ¹ | | | | | | | | |
| At Power-On | Includes kernel power-on execution time, VDD drops to <0.8 V | | 18 | | | | | ms |
| Brownout | VDD drops below power-on reset voltage but not below 0.8 V | | 1.15 | | | | | ms |
| After Reset Event | Includes kernel power-on execution time | | 1.25 | | | | | ms |
| Wake-Up from LIN | | | 0.15 | | | | | ms |

| Parameter | Test Conditions/Comments | T _A = –40°C to +115°C | | | T _A = +115°C to +125°C ¹ | | | Unit |
|--|---|----------------------------------|-----------|-------------|--|-----|-----|----------|
| | | Min | Typ | Max | Min | Typ | Max | |
| LIN INPUT/OUTPUT GENERAL ¹ | | | | | | | | |
| Baud Rate | | 1000 | | 20,000 | | | | Bits/sec |
| VDD | Supply voltage range for which the LIN interface is functional | 6 | | 19 | | | | V |
| LIN Comparator Response Time | | | 38 | 90 | | | | μs |
| LIN DC PARAMETERS | | | | | | | | |
| Current Limit for Driver when LIN Bus is in Dominant State (I _{LIN_DOM_MAX}) | V _{BUS} = V _{BAT} (maximum) | 40 | | 200 | | | | mA |
| Driver Off (I _{LIN_PAS_REC}) ¹ | 6.0 V < voltage of LIN bus (V _{BUS}) < 19 V, VDD = input leakage voltage (V _{LIN}) – 0.7 V | | | 20 | | | | μA |
| Input Leakage Current at Receiver (I _{LIN_PAS_DOM}) ¹ | V _{LIN} = 0 V, V _{BAT} = 12 V, driver off | –1 | | | | | | mA |
| Control Unit Disconnected from Ground (I _{LIN_NO_GND}) ^{1, 23} | Ground = VDD, 0 V < V _{LIN} < 19 V, V _{BAT} = 12 V | –1 | | +1 | | | | mA |
| V _{BAT} Disconnected (I _{BUS_NO_BAT}) ¹ | VDD = ground, 0 V < V _{BUS} < 19 V | | | 30 | | | | μA |
| LIN Receiver Dominant State (V _{LIN_DOM}) ¹ | VDD > 6.0 V | | | 0.4 × VDD | | | | V |
| LIN Receiver Recessive State (V _{LIN_REC}) ¹ | VDD > 6.0 V | 0.6 × VDD | | | | | | V |
| LIN Receiver Threshold Center (V _{LIN_CNT}) ¹ | V _{LIN_CNT} = (receiver threshold of recessive to dominant bus edge (V _{TH_DOM}) + receiver threshold of dominant to recessive bus edge (V _{TH_REC}))/2, VDD > 6.0 V | 0.475 × VDD | 0.5 × VDD | 0.525 × VDD | | | | V |
| LIN Receiver Threshold Hysteresis (V _{HYS}) ¹ | V _{HYS} = V _{TH_REC} – V _{TH_DOM} | | | 0.175 × VDD | | | | V |
| LIN Dominant Output Voltage (V _{LIN_DOM_DRV_LOSUP}) ¹ | VDD = 6.0 V | | | | | | | |
| R _L = 500 Ω | | | | 1.2 | | | | V |
| R _L = 1000 Ω | | 0.6 | | | | | | V |
| LIN Dominant Output Voltage (V _{LIN_DOM_DRV_HISUP}) ¹ | VDD = 19 V | | | | | | | |
| R _L = 500 Ω | | | | 2 | | | | V |
| R _L = 1000 Ω | | 0.8 | | | | | | V |
| LIN Recessive Output Voltage (V _{LIN_RECESSIVE}) ¹ | | 0.8 × VDD | | | | | | V |
| V _{BAT} Shift ^{1, 23} | | 0 | | 0.115 × VDD | | | | V |
| Ground Shift ^{1, 23} | | 0 | | 0.115 × VDD | | | | V |
| Slave Termination Resistance (R _{SLAVE}) | | 20 | 30 | 47 | | 30 | | kΩ |
| Voltage Drop at the Serial Diode (V _{SERIAL_DIODE}) ¹ | | 0.4 | 0.7 | 1 | | | | V |

| Parameter | Test Conditions/Comments | T _A = −40°C to +115°C | | | T _A = +115°C to +125°C ¹ | | | Unit |
|---|--|----------------------------------|------|------|--|-----|-----|------|
| | | Min | Typ | Max | Min | Typ | Max | |
| LIN AC PARAMETERS ¹ | | | | | | | | |
| Duty Cycle 1 (D1) | Bus load conditions (C _{BUS} R _{BUS}): 1 nF 1 kΩ or 6.8 nF 660 Ω or 10 nF 500 Ω Threshold recessive maximum (TH _{REC(MAX)}) = 0.744 × V _{BAT} , threshold dominant maximum (TH _{DOM(MAX)}) = 0.581 × V _{BAT} , supply voltage at transceiver (V _{SUP}) = 6.0 V to 19 V, t _{BIT} = 50 μs, D1 = t _{BUS_REC(MIN)} /(2 × t _{BIT}) | 0.396 | | | | | | |
| Duty Cycle 2 (D2) | Threshold recessive minimum (TH _{REC(MIN)}) = 0.284 × V _{BAT} , threshold dominant minimum (TH _{DOM(MIN)}) = 0.422 × V _{BAT} , V _{SUP} = 6.0 V to 19 V, t _{BIT} = 50 μs, D2 = t _{BUS_REC(MAX)} /(2 × t _{BIT}) | | | | 0.581 | | | |
| Duty Cycle 3 (D3) ²³ | TH _{REC(MAX)} = 0.778 × V _{BAT} , TH _{DOM(MAX)} = 0.616 × V _{BAT} , V _{DD} = 6.0 V to 19 V, t _{BIT} = 96 μs, D3 = t _{BUS_REC(MIN)} /(2 × t _{BIT}) | 0.417 | | | | | | |
| Duty Cycle 4 (D4) ²³ | TH _{REC(MIN)} = 0.389 × V _{BAT} , TH _{DOM(MIN)} = 0.251 × V _{BAT} , V _{DD} = 6.0 V to 19 V, t _{BIT} = 96 μs, D4 = t _{BUS_REC(MAX)} /(2 × t _{BIT}) | | | | 0.590 | | | |
| Propagation Delay of Receiver (t _{RX_PD}) ²³ | | | | | 6 | | | μs |
| Symmetry of Receiver Propagation Delay Rising Edge (t _{RX_SYM}) ²³ | With respect to falling edge (t _{RX_SYM} = propagation delay rising edge (t _{RX_PDR}) – propagation delay falling edge (t _{RX_PDF})) | −2 | | | +2 | | | μs |
| POWER REQUIREMENTS | | | | | | | | |
| Power Supply Voltages | | | | | | | | |
| VDD (Pin 26) | | 3.6 | | 19 | | | | V |
| DVDD33 (Pin 21) | | 3.2 | 3.35 | 3.5 | 3.3 | | | V |
| AVDD18 (Pin 19) | | 1.83 | 1.88 | 1.93 | 1.88 | | | V |
| DVDD18 (Pin 22) | | 1.83 | 1.88 | 1.93 | 1.88 | | | V |
| POWER CONSUMPTION | | | | | | | | |
| Supply Current (I _{DD}) Processor, Normal Mode ²⁴ | Clock Divider Setting 0 (CD0) (peripheral clock (PCLK) = 16 MHz), 16 MHz 1% mode, ADCs off, reference buffer off, executing code from program flash | | 8 | 17 | 9 | | | mA |
| | Clock Divider Setting 1 (CD1) (PCLK = 8 MHz), 16 MHz 1% mode, ADCs off, reference buffer off, executing code from program flash | | 6 | | 7 | | | mA |
| | CD0 (PCLK = 16 MHz), 16 MHz 1% mode, ADCs on, reference buffer on, executing code from program flash | | 9.5 | 18.5 | 10 | | | mA |
| I _{DD} Processor, Powered Down | Precision oscillator off, ADC off, external LIN master pull-up resistor present, measured with wake-up and watchdog timers clocked from low power oscillator, maximum value is at 105°C, and VDD = 18 V | | 55 | 100 | | | | μA |
| I _{DD} LIN | | | 500 | | | | | μA |
| I _{DD} Current Channel ADC (IADC) | Gain = 4, 8, or 16 | | 700 | | | | | μA |
| | Gain = 32 or 64 | | 800 | | | | | μA |
| | Low power mode, gain = 64 | | 350 | | | | | μA |

| Parameter | Test Conditions/Comments | T _A = –40°C to +115°C | | | T _A = +115°C to +125°C ¹ | | | Unit |
|---|------------------------------|----------------------------------|-----|-----|--|-----|-----|------|
| | | Min | Typ | Max | Min | Typ | Max | |
| I _{DD} ADC Temperature and Voltage Channel 1 (ADC1) Voltage ADC (VADC) | | | 550 | | | | | μA |
| I _{DD} Internal Reference (1.2 V) | | | 150 | | | | | μA |
| I _{DD} High Frequency Oscillator | Reduction from 1% to 3% mode | | 50 | | | | | μA |

¹ Guaranteed by design, but not production tested.

² Valid for PGA current ADC gain settings of 4, 8, 16, 32, and 64.

³ These specifications include temperature drift.

⁴ A system calibration removes this error at a given temperature (and at a given gain for the current channel).

⁵ The offset error drift is included in the offset error. This typical specification is an indicator of the offset error due to temperature drift. This typical value is the mean of the temperature drift characterization data distribution.

⁶ Includes internal reference temperature drift.

⁷ The gain drift is included in the total gain error. This parameter is an indicator of the gain error due to the temperature drift in the ADC. The typical value of this parameter is the mean of the temperature drift characterization data distribution.

⁸ For data rates of 4 kHz and 8 kHz with a PGA gain = 32 or greater, allow 10 ms settling time after ADC Current Channel 0 (ADC0) wakes up from power-down mode.

⁹ Voltage channel specifications include resistive attenuator input stage, unless otherwise stated.

¹⁰ RMS noise is referred to voltage attenuator input. For example, at an ADC data output frequency (f_{ADC}) = 1 kHz, the typical rms noise at the ADC input is 7.5 μV. Scaling by the attenuator (1:24) yields these input referred noise figures.

¹¹ Valid after an initial self calibration.

¹² It is possible to extend the ADC input range by up to 10% by modifying the factory set value of the gain calibration register or using system calibration. This approach can also be used to reduce the ADC input range (LSB size).

¹³ Valid for a differential input less than 10 mV.

¹⁴ The reference voltage, V_{REF}, for the ADC is provided by the signal pair, AVDD18 and GND_SW.

¹⁵ The absolute value of the voltage of VTEMP and GND_SW must be 100 mV (minimum) for accurate operation of the temperature ADC (T_{ADC}).

¹⁶ Measured using the box method.

¹⁷ The long-term stability specification is accelerated and noncumulative. The drift in subsequent 1000 hour periods is significantly lower than in the first 1000 hour period.

¹⁸ Die temperature.

¹⁹ Valid after an initial self gain calibration.

²⁰ Endurance is qualified to 10,000 cycles, as per JEDEC Standard 22 Method A117 and measured at –40°C, +25°C, and +115°C. Typical endurance at 25°C is 100,000 cycles.

²¹ Data retention lifetime equivalent at junction temperature (T_J) = 85°C, as per JEDEC Standard 22 Method A117. Data retention lifetime derates with junction temperature.

²² Measured with LIN communication active.

²³ Not production tested but are supported by LIN compliance testing.

²⁴ Typical additional supply current consumed during Flash/EE memory programming is 3 mA, and typical additional supply current consumed during erase cycles is 1 mA.

ABSOLUTE MAXIMUM RATINGS

The ADuCM330WFS/ADuCM331WFS operate directly from the 12 V battery supply and is fully specified over the -40°C to $+115^{\circ}\text{C}$ temperature range, unless otherwise noted.

Table 2.

| Parameter | Rating |
|--|---|
| AGND to DGND to VSS to IO_VSS | $-0.3\text{ V to }+0.3\text{ V}$ |
| VBAT to AGND | $-22\text{ V to }+40\text{ V}$ |
| VDD to VSS | $-0.3\text{ V to }+40\text{ V}$ |
| LIN to IO_VSS | $-18\text{ V to }+40\text{ V}$ |
| Digital Input and Output Voltage to DGND | $-0.3\text{ V to DVDD33} + 0.3\text{ V}$ |
| ADC Inputs to AGND | $-0.3\text{ V to AVDD18} + 0.3\text{ V}$ |
| ESD Rating | |
| Human Body Model (HBM) Rating ¹ | HBM-ADI0082 |
| All Pins Except LIN and VBAT | $\pm 2.0\text{ kV}$ |
| LIN | $\pm 6\text{ kV}$ |
| VBAT | $\pm 4\text{ kV}$ |
| IEC 61000-4-2 | |
| LIN and VBAT | $\pm 8\text{ kV}$ |
| Storage Temperature Range | $-55^{\circ}\text{C to }+150^{\circ}\text{C}$ |
| Junction Temperature | |
| Transient | 150°C |
| Continuous | 130°C |
| Lead Temperature | |
| Soldering Reflow ² | 260°C |
| Lifetime ³ | |
| Normal Mode | |
| At -40°C | 480 Hours |
| At 23°C | 1600 Hours |
| At 60°C | 5200 Hours |
| At 85°C | 640 Hours |
| At 105°C | 80 Hours |
| Standby Mode | |
| At -40°C | 12,648 Hours |
| At 25°C | 60,000 Hours |
| At 50°C | 50,000 Hours |

¹ Based on ANSI/ESD STM5.1-2007.

² JEDEC Standard J-STD-020.

³ Using an activation energy of 0.7 eV, verified using high temperature operating life (HTOL) at 125°C for 1000 hours.

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

THERMAL RESISTANCE

Thermal performance is directly linked to printed circuit board (PCB) design and operating environment. Close attention to PCB thermal design is required.

θ_{JA} is the natural convection junction to ambient thermal resistance measured in a one cubic foot sealed enclosure. θ_{JC} is the junction to case thermal resistance.

Table 3. Thermal Resistance

| Package Type | θ_{JA} | θ_{JC} | Unit |
|-----------------------|---------------|---------------|----------------------|
| CP-32-15 ¹ | 40 | 15 | $^{\circ}\text{C/W}$ |

¹ Test Condition 1: thermal impedance simulated values are based on JEDEC 4-layer test board.

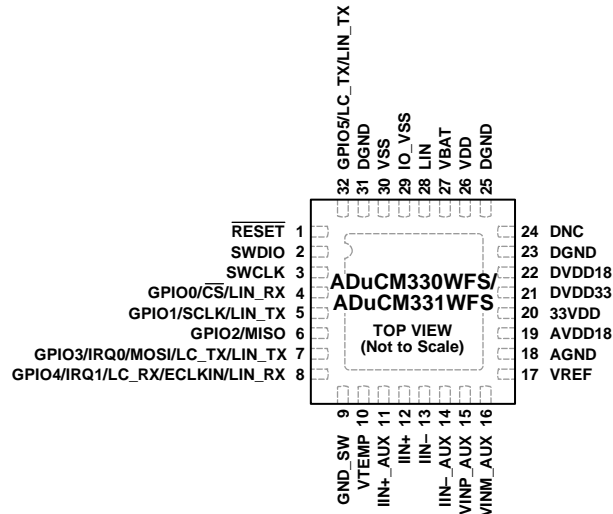
ESD CAUTION



ESD (electrostatic discharge) sensitive device.

Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS



NOTES

1. DNC = DO NOT CONNECT. THIS PIN IS INTERNALLY CONNECTED. THEREFORE, DO NOT EXTERNALLY CONNECT TO THIS PIN.
2. IT IS RECOMMENDED THAT THE EXPOSED PAD BE SOLDERED TO GROUND FOR THERMAL REASONS.

17188-002

Figure 2. Pin Configuration

Table 4. Pin Function Descriptions

| Pin No. | Mnemonic | Type ¹ | Description |
|---------|--------------------------------|-------------------|--|
| 1 | RESET | I | Reset Input. Active low. This pin has an internal pull-up resistor to 33VDD. |
| 2 | SWDIO | I/O | ARM Cortex-M3 Processor Debug Data Input and Output. At power-on, this output is disabled and pulled high via an internal pull-up resistor. This pin can be left unconnected when not in use. |
| 3 | SWCLK | I | ARM Cortex-M3 Processor Debug Clock Input. This is an input only pin and has an internal pull-up resistor. This pin can be left unconnected when not in use. |
| 4 | GPIO0/ \overline{CS} /LIN_RX | I/O | General-Purpose Input/Output 0 (GPIO0). By default, this pin is configured as an input. The pin has an internal 25 k Ω pull-up resistor to 33VDD and can be left unconnected when not in use. Chip Select (\overline{CS}). When configured, this pin also operates the SPI chip select input. Local Interconnect Network Receiver (LIN_RX). This pin can be configured as the receiver pin for LIN frames in external transceiver mode. |
| 5 | GPIO1/SCLK/LIN_TX | I/O | General-Purpose Input/Output 1 (GPIO1). By default, this pin is configured as an input. This pin is used by the kernel in external mode. See the ADuCM330WFS/ADuCM331WFS Hardware Reference Manual for more information. The pin has an internal 25 k Ω pull-up resistor to 33VDD and can be left unconnected when not in use. Serial Clock Input (SCLK). When configured, this pin operates the SPI serial clock input. Local Interconnect Network Transmitter (LIN_TX). This pin can be configured as the transmitter pin for LIN frames in external transceiver mode. |
| 6 | GPIO2/MISO | I/O | General-Purpose Input/Output 2 (GPIO2). By default, this pin is configured as an input. The pin has an internal 25 k Ω pull-up resistor to 33VDD and can be left unconnected when not in use. Master Input/Slave Output (MISO). When configured, this pin also operates the SPI master input/slave output. |
| 7 | GPIO3/IRQ0/MOSI/LC_TX/LIN_TX | I/O | General-Purpose Input/Output 3 (GPIO3). By default, this pin is configured as an input. This pin is used by the kernel in external mode. See the ADuCM330WFS/ADuCM331WFS Hardware Reference Manual for more information. The pin has an internal 25 k Ω pull-up resistor to 33VDD and can be left unconnected when not in use. Interrupt Request (IRQ0). This pin can also be configured as the External Interrupt Request 0. Master Output/Slave Input (MOSI). This pin can be configured as an SPI master output/slave input pin. LIN Conformance Transmitter (LC_TX). This pin can be connected to the LIN physical transmitter for LIN conformance testing. Local Interconnect Network Transmitter (LIN_TX). This pin can also be connected as the transmitter pin for LIN frames in external transceiver mode. |

| Pin No. | Mnemonic | Type ¹ | Description |
|------------|------------------------------------|-------------------|---|
| 8 | GPIO4/IRQ1/LC_RX/ ECLKIN/LIN_RX | I/O | General-Purpose Input/Output 4 (GPIO4). By default, this pin is configured as an input. This pin is used by the kernel in external mode. See the ADuCM330WFS/ADuCM331WFS Hardware Reference Manual for more information. The pin has an internal 25 k Ω pull-up resistor to 33VDD and can be left unconnected when not in use. Interrupt Request (IRQ1). This pin can be configured as the External Interrupt Request 1. LIN Conformance Receiver (LC_RX). This pin can be connected to the LIN physical receiver for LIN conformance testing. External Clock (ECLKIN). This pin can be configured as the external clock input. Local Interconnect Network Receiver (LIN_RX). This pin can be configured as the receiving pin for LIN frames in external transceiver mode. |
| 9 | GND_SW | I | Switch to Internal Analog Ground Reference. This pin is the negative input for the external temperature channel. |
| 10 | VTEMP | I | External Pin for Negative Temperature Coefficient (NTC)/Positive Temperature Coefficient (PTC) Temperature Measurement. |
| 11 | IIN+_AUX | S | Auxiliary Positive Differential Input Pin. If not used, connect this pin to AGND. |
| 12 | IIN+ | I | Positive Differential Input for Current Channel. |
| 13 | IIN- | I | Negative Differential Input for Current Channel. |
| 14 | IIN-_AUX | S | Auxiliary Negative Differential Input Pin. If not used, connect this pin to AGND. |
| 15 | VINP_AUX | S | Auxiliary Input Voltage Positive Channel. If not used, connect this pin to AGND. |
| 16 | VINM_AUX | S | Auxiliary Input Voltage Negative Channel. If not used, connect this pin to AGND. |
| 17 | VREF | S | Voltage Reference Pin. Connect this pin via a 470 nF capacitor to ground. This pin can also be used to input an external voltage reference. This pin cannot be used to supply an external circuit. |
| 18 | AGND | S | Ground Reference for On-Chip Precision Analog Circuits. |
| 19 | AVDD18 | S | Supply from Analog LDO. Do not connect this pin to a low impedance external circuit. ² |
| 20 | 33VDD | S | 3.3 V Supply. Connect to DVDD33. Do not connect this pin to a low impedance external circuit. ² |
| 21 | DVDD33 | S | 3.3 V Supply. Connect to 33VDD. Do not connect this pin to a low impedance external circuit. ² |
| 22 | DVDD18 | S | 1.8 V Supply. Do not connect this pin to a low impedance external circuit. ² |
| 23, 25, 31 | DGND | S | Ground Reference for On-Chip Digital Circuits. |
| 24 | DNC | | Do Not Connect. This pin is internally connected. Therefore, do not externally connect to this pin. |
| 26 | VDD | S | Battery Power Supply for On-Chip Regulator. |
| 27 | VBAT | S | Battery Voltage Input to Resistor Divider. |
| 28 | LIN | I/O | Local Interconnect Network Physical Interface Input/Output. |
| 29 | IO_VSS | S | Ground Reference for LIN. |
| 30 | VSS | S | Ground Reference. This pin is the ground reference for the internal voltage regulators. |
| 32 | GPIO5/LC_TX/LIN_TX | I/O | General-Purpose Input/Output 5 (GPIO5). By default, this pin is configured as an input. This pin is checked by the kernel on every reset. See the ADuCM330WFS/ADuCM331WFS Hardware Reference Manual for more information. The pin has an internal 25 k Ω pull-up resistor to 33VDD and can be left unconnected when not in use. LIN Conformance Transmitter (LC_TX). This pin can be connected to the LIN physical transmitter for LIN conformance testing. Local Interconnect Network Transmitter (LIN_TX). This pin can be configured as the transmitter pin for LIN frames in external transceiver mode. |
| | EPAD | | Exposed Pad. It is recommended that the exposed pad be soldered to ground for thermal reasons. |

¹ I is input, I/O is input/output, and S is supply.

² Using the 1.8 V or 3.3 V supply to power an external circuit can have POR, electromagnetic compliance (EMC), and self heating implications. Device evaluation and testing completed without an external load attached.

TERMINOLOGY

Conversion Rate

The conversion rate specifies the rate at which an output result is available from the ADC after the ADC has settled.

The Σ - Δ conversion techniques used on this device mean that, although the ADC front-end signal is oversampled at a relatively high sample rate, a subsequent digital filter is used to decimate the output. Use of a digital filter provides a valid 20-bit data conversion result at output rates from 4 Hz to 8 kHz.

When software switches from one input to another on the same ADC, the digital filter must first be cleared and then allowed to average a new result. Depending on the configuration of the ADC and the type of filter, this averaging can require multiple conversion cycles.

Integral Nonlinearity (INL)

INL is the maximum deviation of any code from a straight line passing through the endpoints of the transfer function. The endpoints of the transfer function are zero scale, which is a point $\frac{1}{2}$ LSB below the first code transition, and full scale, which is a point $\frac{1}{2}$ LSB above the last code transition (111...110 to 111...111). The error is expressed as a percentage of full scale.

Positive INL is the deviation from a straight line through $\frac{1}{2}$ LSB above midscale code transition to $\frac{1}{2}$ LSB above the last code transition.

Negative INL is the deviation from a straight line from a point $\frac{1}{2}$ LSB below the first code transition to a point $\frac{1}{2}$ LSB above the midscale code transition.

No Missing Codes

No missing codes is a measure of the differential nonlinearity of the ADC. The error is expressed in bits and specifies the number of codes (ADC results) as 2^N bits, where N equals no missing codes, guaranteed to occur through the full ADC input range.

Offset Error

Offset error is the deviation of the first code transition ADC input voltage from the ideal first code transition.

Offset Error Drift

Offset error drift is the variation in absolute offset error with respect to temperature. This error is expressed as LSB/ $^{\circ}$ C or nV/ $^{\circ}$ C.

Gain Error

Gain error is a measure of the span error of the ADC. It is a measure of the difference between the measured and the ideal span between any two points in the transfer function.

Output Noise

The output noise is specified as the standard deviation (or $1 \times \Sigma$) of ADC output code distribution collected when the ADC input voltage is at a dc voltage. It is expressed as μ V rms or nV rms. The output, or rms noise, is used to calculate the effective resolution of the ADC as defined by the following equation, measured in bits:

$$\text{Effective Resolution} = \log_2(\text{Full-Scale Range}/\text{rms Noise})$$

The peak-to-peak noise is defined as the deviation of codes that fall within $6.6 \times \Sigma$ of the distribution of ADC output codes collected when the ADC input voltage is at dc. The peak-to-peak noise is therefore calculated as $6.6 \times$ the rms noise.

The peak-to-peak noise can be used to calculate the ADC noise free code resolution for which there is no code flicker within a $6.6 \times \Sigma$ limit as defined by the following equation, measured in bits:

$$\text{Noise Free Code Resolution} = \log_2(\text{Full-Scale Range}/\text{Peak-to-Peak Noise})$$

APPLICATIONS INFORMATION

DESIGN GUIDELINES

Before starting design and layout of the ADuCM330WFS/ADuCM331WFS on a PCB, it is recommended that the designer become familiar with the following guidelines that describe any special circuit considerations and layout requirements needed.

POWER AND GROUND RECOMMENDATIONS

Place capacitors that are connecting to the ADuCM330WFS/ADuCM331WFS as close to the pins of the device as possible, with minimal trace length.

Capacitors connected to the 33VDD, AVDD18, and DVDD18 pins must have a low equivalent series resistance (ESR) rating.

All components must be rated accordingly to the temperature range expected by the application.

EXPOSED PAD THERMAL RECOMMENDATIONS

It is required that the exposed pad on the underside of the ADuCM330WFS/ADuCM331WFS be connected to ground to achieve the best electrical and thermal performance. It is recommended that the user connect an exposed continuous copper plane on the PCB to the ADuCM330WFS/ADuCM331WFS exposed pad, and that the copper plane have several vias to achieve the lowest possible resistive thermal path for heat dissipation to flow through the bottom of the PCB. It is recommended that these vias be solder filled or plugged.

GENERAL RECOMMENDATIONS

It is highly recommended to use the schematic given with the component values shown in Figure 3. The component values shown in Figure 3 were chosen from the characterization tests and evaluated for optimum performance of the ADuCM330WFS/ADuCM331WFS.

Configure the GPIOs as inputs with pull-up resistors enabled to obtain the lowest possible current consumption in shutdown mode.

Set the ARM Cortex-M3 processor clock speed to the minimum required to meet the application requirements.

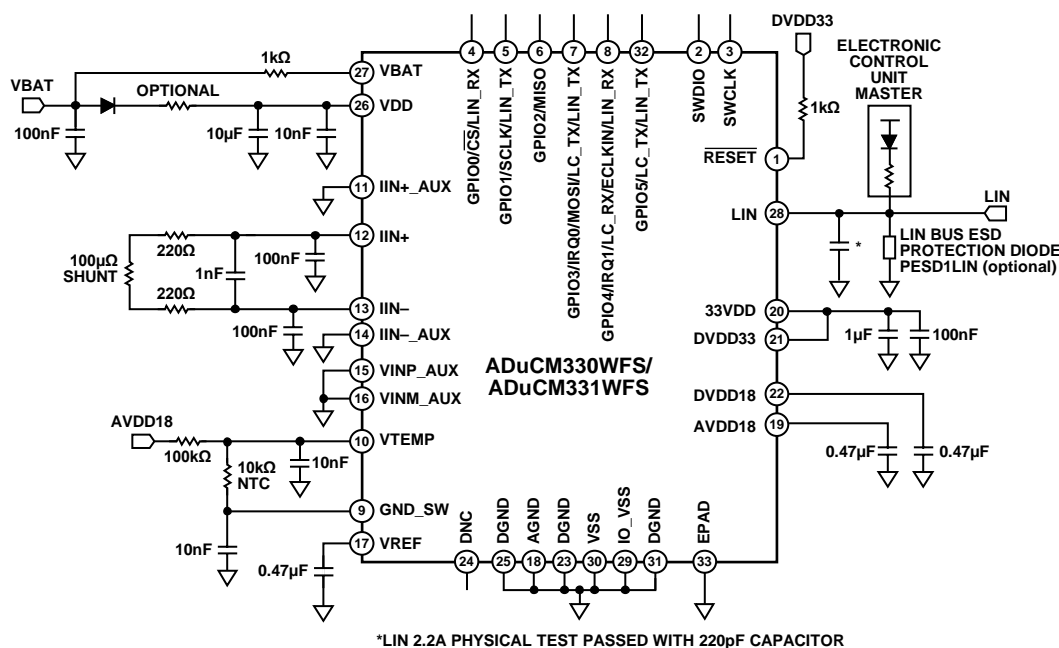
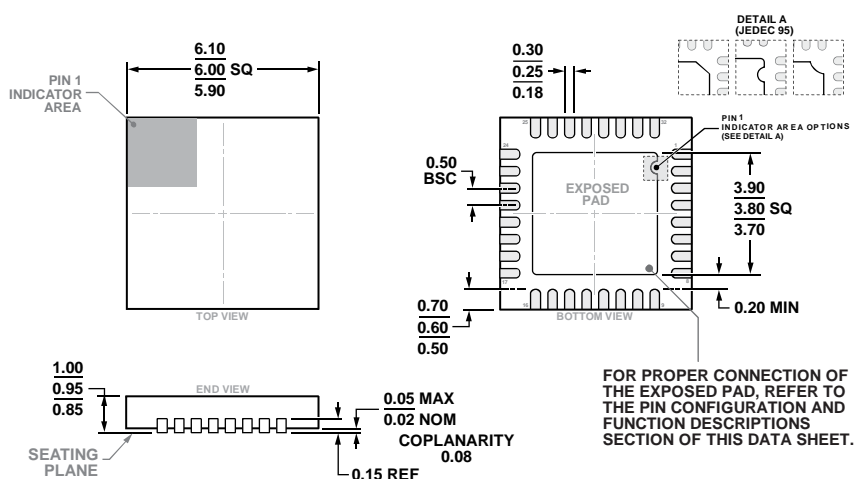


Figure 3. External Components Recommended for Proper Operation

17188-003

OUTLINE DIMENSIONS



COMPLIANT TO JEDEC STANDARDS MO-220-VJJD-7

Figure 4. 32-Lead Lead Frame Chip Scale Package [LFCSP]
6 mm × 6 mm Body and 0.95 mm Package Height
(CP-32-15)

Dimensions shown in millimeters

ORDERING GUIDE

| Model ^{1, 2} | Temperature Range ³ | Program Flash/ Data Flash/SRAM | Package Description | Package Option |
|-----------------------|--------------------------------|-----------------------------------|--|----------------|
| ADuCM330WFSBCPZ-RL | −40°C to +115°C | 96 kB/4 kB/10 kB | 32-Lead Lead Frame Chip Scale Package [LFCSP] | CP-32-15 |
| ADuCM331WFSBCPZ-RL | −40°C to +115°C | 128 kB/4 kB/10 kB | 32-Lead Lead Frame Chip Scale Package [LFCSP] | CP-32-15 |
| EVAL-ADUCM331QSPZ | | | Socketed Evaluation Board with Switches and LEDs | |

¹ Z = RoHS Compliant Part.² W = Qualified for Automotive Applications.³ The ADuCM330WFS/ADuCM331WFS are functional but have degraded performance at temperatures from 115°C to 125°C.

AUTOMOTIVE PRODUCTS

The ADuCM330WFS and ADuCM331WFS models are available with controlled manufacturing to support the quality and reliability requirements of automotive applications. Note that these automotive models may have specifications that differ from the commercial model; therefore, designers should review the Specifications section of this data sheet carefully. Only the automotive grade products shown are available for use in automotive applications. Contact your local Analog Devices, Inc., account representative for specific product ordering information and to obtain the specific Automotive Reliability reports for these models.

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