

### FEATURES

**Single-input HDMI receiver with dual channel LVDS transmitter outputs**  
**HDMI receiver support**  
 148.5 MHz maximum TMDS clock frequency  
 High-bandwidth Digital Content Protection (HDCP) 1.4 support with internal HDCP keys  
 Adaptive HDMI equalizer  
 5 V detect and hot plug assert for HDMI port  
 Extended colorimetry, including sYCC601, Adobe RGB, Adobe YCC 601, xvYCC extended gamut color  
**LVDS transmitters**  
 Dual channel 24-bit OpenLDI interface  
 Supports 6-bit and 8-bit nonbalanced OpenLDI or 8-bit video electronics standards association (VESA) formats  
**Audio support including high bit rate (HBR) and Direct Stream Digital (DSD)**  
**S/PDIF (IEC 60958-compatible) digital audio support**

**Dedicated, flexible audio output port**  
**Dolby® TrueHD DTS-HD Master Audio™**  
**General**

Internal EDID RAM  
 Integrated consumer electronics control (CEC) controller  
 Standard identification (STDI) circuit  
 Any to any, 3 × 3 color space conversion (CSC) matrix  
 100-ball, 9 mm × 9 mm CSP\_BGA package  
 Qualified for automotive applications

### APPLICATIONS

Projectors  
 Automotive infotainment headunits  
 Automotive infotainment displays  
 Digital signage

### FUNCTIONAL BLOCK DIAGRAM

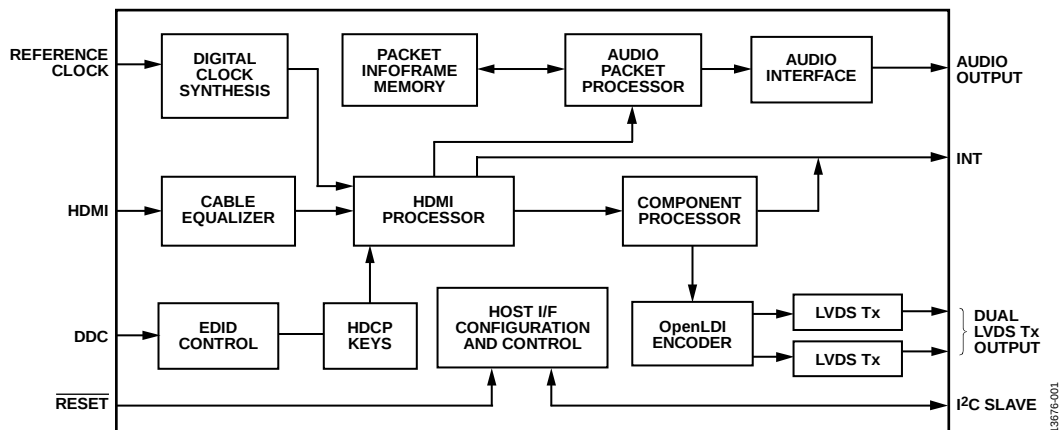


Figure 1.

136765-001

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## REVISION HISTORY

### 9/2018—Rev. B to Rev. C

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### 5/2017—Rev. A to Rev. B

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### 12/2015—Rev. 0 to Rev. A

|                                 |    |
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### 10/2015—Revision 0: Initial Version

## GENERAL DESCRIPTION

The **ADV7613** is a high quality, low power, single-input HDMI to LVDS display bridge. It incorporates an HDMI capable receiver that supports up to 1080p, 60 Hz.

The HDMI port has dedicated 5 V detect and hot plug assert pins. The HDMI receiver also includes an integrated equalizer that ensures the robust operation of the interface with long cables.

The **ADV7613** has an audio output port for the audio data extracted from the HDMI stream. HDMI audio formats include super audio CD (SACD) via Direct Stream Digital® (DSD) and HBR. The HDMI receiver has an advanced mute controller that prevents audible extraneous noise in the audio output.

The **ADV7613** contains a component processor (CP) that processes the video signals from the HDMI receiver. It provides features such as contrast, brightness and saturation adjustments,

STDI detection block, free run, and synchronization alignment controls.

The LVDS encoder can package data into 6-bit or 8-bit non-dc balanced OpenLDI mapping or 8-bit VESA mapping. The **ADV7613** can output 24-bit OpenLDI data via dual-channel LVDS transmitters, up to a maximum resolution of 1080p, 60 Hz received at the input. The maximum output clock supported by a single LVDS output port is 92 MHz.

The **ADV7613** is offered in an automotive grade and a consumer grade. The operating temperature range is  $-40^{\circ}\text{C}$  to  $+85^{\circ}\text{C}$ .

Fabricated in an advanced CMOS process, the **ADV7613** is provided in a  $9\text{ mm} \times 9\text{ mm}$ , 100-ball CSP\_BGA, RoHS-compliant package.

## DETAILED FUNCTIONAL BLOCK DIAGRAM

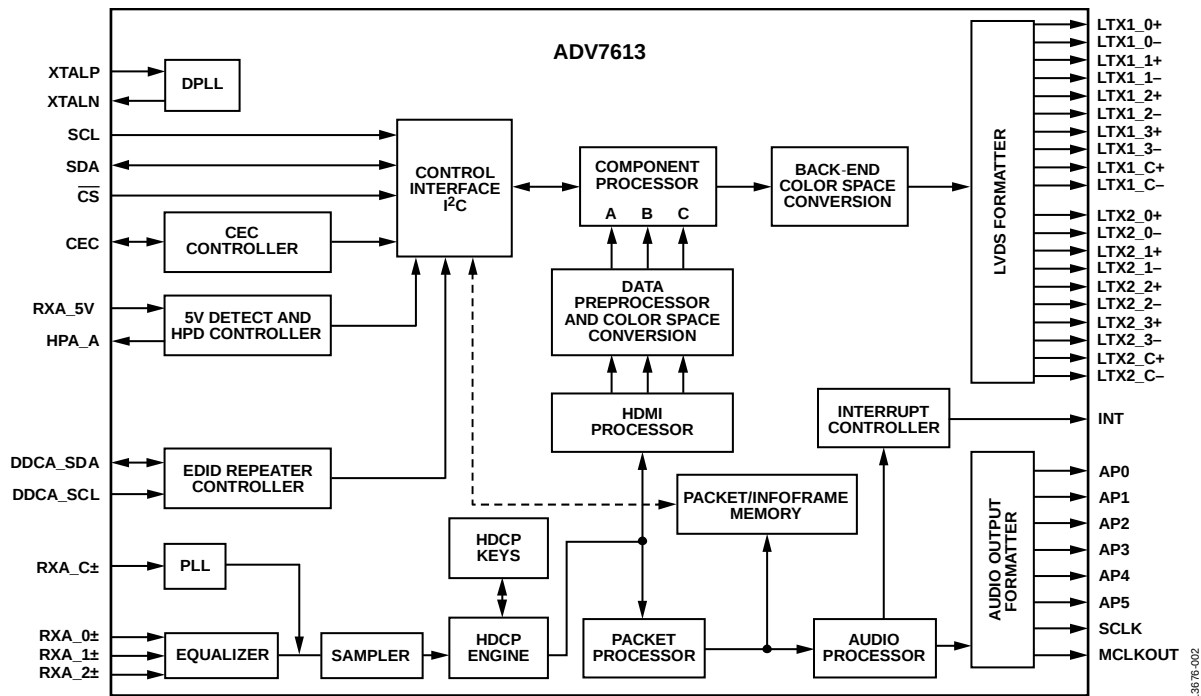


Figure 2. Detailed Functional Block Diagram

# SPECIFICATIONS

## ELECTRICAL CHARACTERISTICS

DVDD = 1.71 V to 1.89 V, DVDDIO = 3.135 V to 3.465 V, PVDD = 1.71 V to 1.89 V, TVDD = 3.135 V to 3.465 V, CVDD = 1.71 V to 1.89 V, LTX\_VDD = 1.71 V to 1.89 V. T<sub>MIN</sub> to T<sub>MAX</sub> = -40°C to +85°C, unless otherwise noted.

Table 1.

| Parameter                                  | Symbol               | Test Conditions/Comments                                                                                                                                                                                         | Min   | Typ | Max   | Unit |
|--------------------------------------------|----------------------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|-------|-----|-------|------|
| DIGITAL INPUTS                             |                      |                                                                                                                                                                                                                  |       |     |       |      |
| Input High Voltage                         | V <sub>IH</sub>      | XTALN and XTALP pins                                                                                                                                                                                             | 1.2   |     |       | V    |
|                                            |                      | Other digital inputs                                                                                                                                                                                             | 2     |     |       | V    |
| Input Low Voltage                          | V <sub>IL</sub>      | XTALN and XTALP pins                                                                                                                                                                                             |       |     | 0.4   | V    |
|                                            |                      | Other digital inputs                                                                                                                                                                                             |       |     | 0.8   | V    |
| Input Current                              | I <sub>IN</sub>      | $\overline{CS}$ pin                                                                                                                                                                                              | -60   |     | +60   | μA   |
|                                            |                      | XTALN and XTALP pins                                                                                                                                                                                             |       | ±15 |       | μA   |
|                                            |                      | Other digital inputs                                                                                                                                                                                             |       | ±10 |       | μA   |
| Input Capacitance <sup>1</sup>             | C <sub>IN</sub>      |                                                                                                                                                                                                                  |       |     | 10    | pF   |
| DIGITAL INPUTS (5 V TOLERANT) <sup>2</sup> |                      | DDCA_SCL, DDCA_SDA                                                                                                                                                                                               |       |     |       |      |
| Input High Voltage                         | V <sub>IH</sub>      |                                                                                                                                                                                                                  | 2.6   |     |       | V    |
| Input Low Voltage                          | V <sub>IL</sub>      |                                                                                                                                                                                                                  |       |     | 0.8   | V    |
| Input Current                              | I <sub>IN</sub>      |                                                                                                                                                                                                                  | -80   |     | +80   | μA   |
| Input Leakage Current                      | I <sub>IN</sub>      | RXA_5V                                                                                                                                                                                                           | -100  |     | +100  | μA   |
| DIGITAL OUTPUTS                            |                      |                                                                                                                                                                                                                  |       |     |       |      |
| Output High Voltage                        | V <sub>OH</sub>      |                                                                                                                                                                                                                  | 2.4   |     |       | V    |
| Output Low Voltage                         | V <sub>OL</sub>      |                                                                                                                                                                                                                  |       |     | 0.4   | V    |
| High Impedance Leakage Current             | I <sub>LEAK</sub>    | HPA_A <sup>3</sup>                                                                                                                                                                                               | -100  |     | +100  | μA   |
|                                            |                      | Other digital outputs                                                                                                                                                                                            | -10   |     | +10   | μA   |
| Output Capacitance <sup>4</sup>            | C <sub>OUT</sub>     |                                                                                                                                                                                                                  |       |     | 20    | pF   |
| POWER REQUIREMENTS                         |                      |                                                                                                                                                                                                                  |       |     |       |      |
| Termination Power Supply                   | TVDD                 |                                                                                                                                                                                                                  | 3.135 | 3.3 | 3.465 | V    |
| Digital Input/Output (I/O) Power Supply    | DVDDIO               |                                                                                                                                                                                                                  | 3.135 | 3.3 | 3.465 | V    |
| Digital Core Power Supply                  | DVDD                 |                                                                                                                                                                                                                  | 1.71  | 1.8 | 1.89  | V    |
| Phase-Locked Loop (PLL) Power Supply       | PVDD                 |                                                                                                                                                                                                                  | 1.71  | 1.8 | 1.89  | V    |
| Comparator Power Supply                    | CVDD                 |                                                                                                                                                                                                                  | 1.71  | 1.8 | 1.89  | V    |
| LVDS Power Supply                          | LTX_VDD              |                                                                                                                                                                                                                  | 1.71  | 1.8 | 1.89  | V    |
| CURRENT CONSUMPTION <sup>4</sup>           |                      |                                                                                                                                                                                                                  |       |     |       |      |
| Configuration 1                            |                      | Pseudorandom test pattern; 1360 × 768p at 60 Hz input resolution; 85 MHz pixel clock; 25°C operating temperature; DVDD, PVDD, CVDD, and LTX_DVDD = 1.8 V; DVDDIO and TVDD = 3.3 V; LVDS Port 2 used              |       |     |       |      |
| Termination Power Supply                   | I <sub>TVDD</sub>    |                                                                                                                                                                                                                  |       | 50  |       | mA   |
| Digital I/O Power Supply                   | I <sub>DVDDIO</sub>  |                                                                                                                                                                                                                  |       | 6   |       | mA   |
| Digital Core Power Supply                  | I <sub>DVDD</sub>    |                                                                                                                                                                                                                  |       | 68  |       | mA   |
| PLL Power Supply                           | I <sub>PVDD</sub>    |                                                                                                                                                                                                                  |       | 29  |       | mA   |
| Comparator Power Supply                    | I <sub>CVDD</sub>    |                                                                                                                                                                                                                  |       | 65  |       | mA   |
| LVDS Power Supply                          | I <sub>LTX_VDD</sub> |                                                                                                                                                                                                                  |       | 45  |       | mA   |
| Configuration 2                            |                      | Checker one-dot × one-dot test pattern; 1920 × 720p at 60 Hz input resolution; 92 MHz pixel clock; 25°C operating temperature; DVDD, PVDD, CVDD, and LTX_DVDD = 1.8 V; DVDDIO and TVDD = 3.3 V; LVDS Port 2 used |       |     |       |      |
| Termination Power Supply                   | I <sub>TVDD</sub>    |                                                                                                                                                                                                                  |       | 58  |       | mA   |
| Digital I/O Power Supply                   | I <sub>DVDDIO</sub>  |                                                                                                                                                                                                                  |       | 6   |       | mA   |
| Digital Core Power Supply                  | I <sub>DVDD</sub>    |                                                                                                                                                                                                                  |       | 102 |       | mA   |

| Parameter                       | Symbol                  | Test Conditions/Comments                                                                                                                                                                                                   | Min | Typ | Max | Unit |
|---------------------------------|-------------------------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|-----|-----|-----|------|
| PLL Power Supply                | I <sub>PVDD</sub>       | Pseudorandom test pattern; 1920 × 1080p at 60 Hz input resolution; 148.5 MHz pixel clock; 85°C operating temperature; DVDD, PVDD, CVDD, and LTX_DVDD = 1.89 V; DVDDIO and TVDD = 3.465 V; LVDS Port 1 and LVDS Port 2 used |     | 29  |     | mA   |
| Comparator Power Supply         | I <sub>CVDD</sub>       |                                                                                                                                                                                                                            |     | 66  |     | mA   |
| LVDS Power Supply               | I <sub>LTX_VDD</sub>    |                                                                                                                                                                                                                            |     | 43  |     | mA   |
| Configuration 3                 |                         |                                                                                                                                                                                                                            |     |     |     |      |
| Termination Power Supply        | I <sub>TVDD</sub>       |                                                                                                                                                                                                                            |     |     | 70  | mA   |
| Digital I/O Power Supply        | I <sub>DVDDIO</sub>     |                                                                                                                                                                                                                            |     |     | 15  | mA   |
| Digital Core Power Supply       | I <sub>DVDD</sub>       |                                                                                                                                                                                                                            |     |     | 147 | mA   |
| PLL Power Supply                | I <sub>PVDD</sub>       |                                                                                                                                                                                                                            |     |     | 44  | mA   |
| Comparator Power Supply         | I <sub>CVDD</sub>       |                                                                                                                                                                                                                            |     |     | 96  | mA   |
| LVDS Power Supply               | I <sub>LTX_VDD</sub>    |                                                                                                                                                                                                                            |     |     | 88  | mA   |
| POWER-DOWN CURRENT <sup>4</sup> |                         |                                                                                                                                                                                                                            |     |     |     |      |
| Terminator Power Supply         | I <sub>TVDD_PD</sub>    |                                                                                                                                                                                                                            |     | 327 |     | μA   |
| Digital I/O Power Supply        | I <sub>DVDDIO_PD</sub>  |                                                                                                                                                                                                                            |     | 387 |     | μA   |
| Digital Core Power Supply       | I <sub>DVDD_PD</sub>    |                                                                                                                                                                                                                            |     | 102 |     | μA   |
| PLL Power Supply                | I <sub>PVDD_PD</sub>    |                                                                                                                                                                                                                            |     | 223 |     | μA   |
| Comparator Power Supply         | I <sub>CVDD_PD</sub>    |                                                                                                                                                                                                                            |     | 74  |     | μA   |
| LVDS Power Supply               | I <sub>LTX_VDD_PD</sub> |                                                                                                                                                                                                                            |     | 323 |     | μA   |

<sup>1</sup> Data characterized by evaluation.

<sup>2</sup> The following pins are 5 V tolerant inputs: DDCA\_SCL, DDCA\_SDA, and RXA\_5V.

<sup>3</sup> The HPA\_A pin is a 5 V tolerant output.

<sup>4</sup> Data characterized by evaluation.

## LVDS TRANSMITTER (OpenLDI MAPPING)

Table 2.

| Parameter                              | Symbol          | Min   | Typ       | Max      | Unit |
|----------------------------------------|-----------------|-------|-----------|----------|------|
| <b>OpenLDI OUTPUTS<sup>1</sup></b>     |                 |       |           |          |      |
| Differential Output Voltage            | V <sub>OD</sub> | 247   | 350       | 454      | mV   |
| Offset Output Voltage                  | V <sub>OS</sub> | 1.125 | 1.2       | 1.375    | V    |
| Change in V <sub>OD</sub> Mismatch     |                 |       |           | 50       | mV   |
| Change in V <sub>OS</sub> Mismatch     |                 |       |           | 50       | mV   |
| <b>OpenLDI TRANSMITTER<sup>2</sup></b> |                 |       |           |          |      |
| OpenLDI Output Rise Time               | t <sub>R</sub>  |       | 0.21 × UI | 0.3 × UI | ps   |
| OpenLDI Output Fall Time               | t <sub>F</sub>  |       | 0.21 × UI | 0.3 × UI | ps   |

<sup>1</sup> Measurement performed using a 100 Ω termination resistor.

<sup>2</sup> Data characterized by evaluation, using a 100 Ω source termination resistor. UI is unit interval, that is, the bit width.

## DATA AND I<sup>2</sup>C TIMING CHARACTERISTICS

Table 3.

| Parameter                    | Symbol         | Min | Typ      | Max   | Unit |
|------------------------------|----------------|-----|----------|-------|------|
| <b>CLOCK AND CRYSTAL</b>     |                |     |          |       |      |
| Crystal (XTAL) Frequency     |                |     | 28.63636 |       | MHz  |
| XTAL Frequency Stability     |                |     |          | ±50   | ppm  |
| Input Clock Range (TMDS)     |                | 25  |          | 148.5 | MHz  |
| OpenLDI Output Clock Range   |                | 25  |          | 92    | MHz  |
| <b>I<sup>2</sup>C PORTS</b>  |                |     |          |       |      |
| SCL Frequency                |                |     |          | 400   | kHz  |
| SCL Minimum Pulse Width High | t <sub>1</sub> | 600 |          |       | ns   |
| SCL Minimum Pulse Width Low  | t <sub>2</sub> | 1.3 |          |       | μs   |
| Start Condition Hold Time    | t <sub>3</sub> | 600 |          |       | ns   |

| Parameter                                           | Symbol          | Min   | Typ | Max   | Unit         |
|-----------------------------------------------------|-----------------|-------|-----|-------|--------------|
| Start Condition Setup Time                          | $t_4$           | 600   |     |       | ns           |
| SDA Setup Time                                      | $t_5$           | 100   |     |       | ns           |
| SCL and SDA Rise Time                               | $t_6$           |       |     | 300   | ns           |
| SCL and SDA Fall Time                               | $t_7$           |       |     | 300   | ns           |
| Stop Condition Setup Time                           | $t_8$           | 0.6   |     |       | $\mu$ s      |
| RESET FEATURE                                       |                 |       |     |       |              |
| Reset Pulse Width                                   |                 | 5     |     |       | ms           |
| Reset Pulse to First I <sup>2</sup> C Transaction   |                 | 5     |     |       | ms           |
| I <sup>2</sup> S PORT, MASTER MODE                  |                 |       |     |       |              |
| SCLK Mark to Space Ratio                            | $t_{15}:t_{16}$ | 45:55 |     | 55:45 | % Duty Cycle |
| Left/Right Clock (LRCLK) Data Transition Time       | $t_{17}$        |       |     | 10    | ns           |
|                                                     | $t_{18}$        |       |     | 10    | ns           |
| I <sup>2</sup> Sx <sup>1</sup> Data Transition Time | $t_{19}$        |       |     | 5     | ns           |
|                                                     | $t_{20}$        |       |     | 5     | ns           |

<sup>1</sup> I<sup>2</sup>Sx signals (where x = 0, 1, 2, or 3) are available on the AP1 to AP4 pins (see Table 6).

### Timing Diagrams

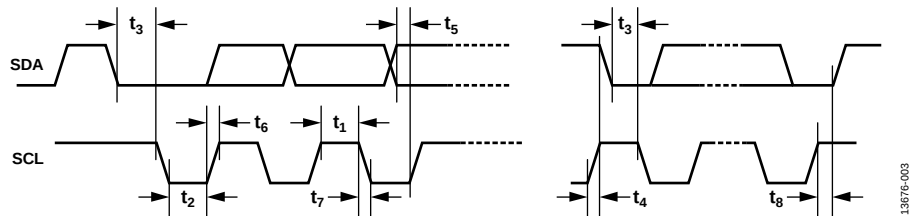
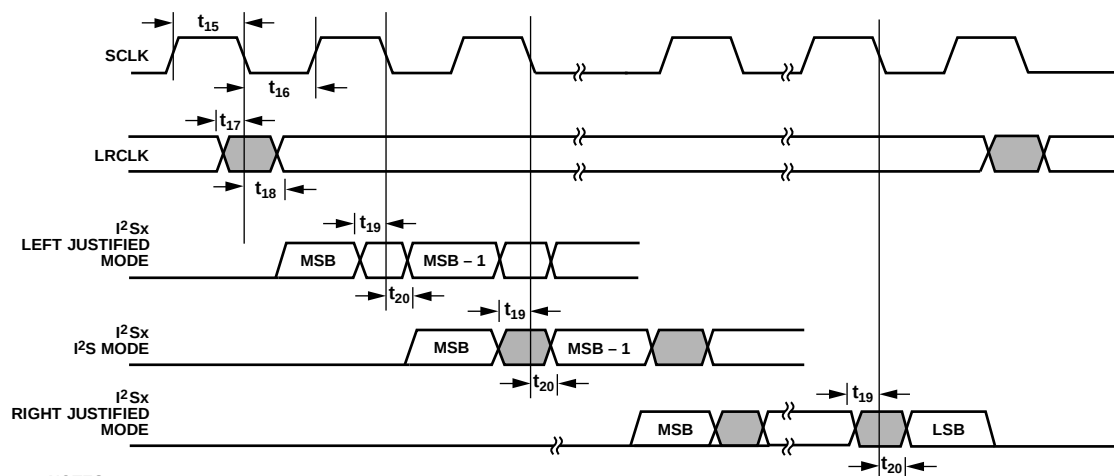


Figure 3. I<sup>2</sup>C Timing



#### NOTES

1. THE LRCLK SIGNAL IS AVAILABLE ON THE AP5 PIN.
2. I<sup>2</sup>Sx SIGNALS (WHERE x = 0, 1, 2, OR 3) ARE AVAILABLE ON THE FOLLOWING PINS: AP1, AP2, AP3, AND AP4.

Figure 4. I<sup>2</sup>S Timing

## ABSOLUTE MAXIMUM RATINGS

Table 4.

| Parameter                                       | Rating                           |
|-------------------------------------------------|----------------------------------|
| DVDD to GND                                     | 2.2 V                            |
| PVDD to GND                                     | 2.2 V                            |
| DVDDIO to GND                                   | 4.0 V                            |
| CVDD to GND                                     | 2.2 V                            |
| TVDD to GND                                     | 4.0 V                            |
| LTX_VDD to GND                                  | 2.2 V                            |
| Digital Inputs to GND                           | GND – 0.3 V to DVDDIO + 0.3 V    |
| 5 V Tolerant Digital Inputs to GND <sup>1</sup> | 5.3 V                            |
| Digital Outputs to GND                          | GND – 0.3 V to DVDDIO + 0.3 V    |
| XTALP, XTALN                                    | –0.3 V to PVDD + 0.3 V           |
| SCL, SDA Data Pins to DVDDIO                    | DVDDIO – 0.3 V to DVDDIO + 3.6 V |
| Maximum Junction Temperature ( $T_{JMAX}$ )     | 125°C                            |
| Storage Temperature Range                       | –60°C to +150°C                  |
| Infrared Reflow Soldering (20 sec)              | 260°C                            |
| Operating Temperature Range                     | –40°C to +85°C                   |

<sup>1</sup> The following inputs are 3.3 V inputs but are 5 V tolerant: DDCA\_SCL and DDCA\_SDA.

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

## THERMAL RESISTANCE

To reduce power consumption when using the ADV7613, turn off the unused sections of the device.

Due to printed circuit board (PCB) metal variation and, therefore, variation in PCB heat conductivity, the value of  $\theta_{JA}$  may differ for various PCBs.

It is possible to obtain the most efficient measurement solution by using the package surface temperature to estimate the die temperature because this solution eliminates the variance associated with the  $\theta_{JA}$  value.

When using the device, the maximum junction temperature ( $T_{JMAX}$ ) must not go above 125°C. The following equation calculates the junction temperature using the measured package surface temperature and applies only when no heat sink is used on the device under test (DUT):

$$T_J = T_S + (\Psi_{JT} \times W_{TOTAL}).$$

where:

$T_J$  is the junction temperature.

$T_S$  is the package surface temperature (°C).

$\Psi_{JT} = 0.81^\circ\text{C/W}$  for the 100-ball CSP\_BGA (based on a 2s2p test board defined in the JEDEC specification).

$$W_{TOTAL} = ((PVDD \times I_{PVDD}) + (0.2 \times TVDD \times I_{TVDD}) + (CVDD \times I_{CVDD}) + (DVDD \times I_{DVDD}) + (DVDDIO \times I_{DVDDIO}) + (LTX\_VDD \times I_{LTX\_VDD})).$$

where 0.2 is 20% of the TVDD power that is dissipated on the device itself.

## ESD CAUTION



### ESD (electrostatic discharge) sensitive device.

Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

## PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

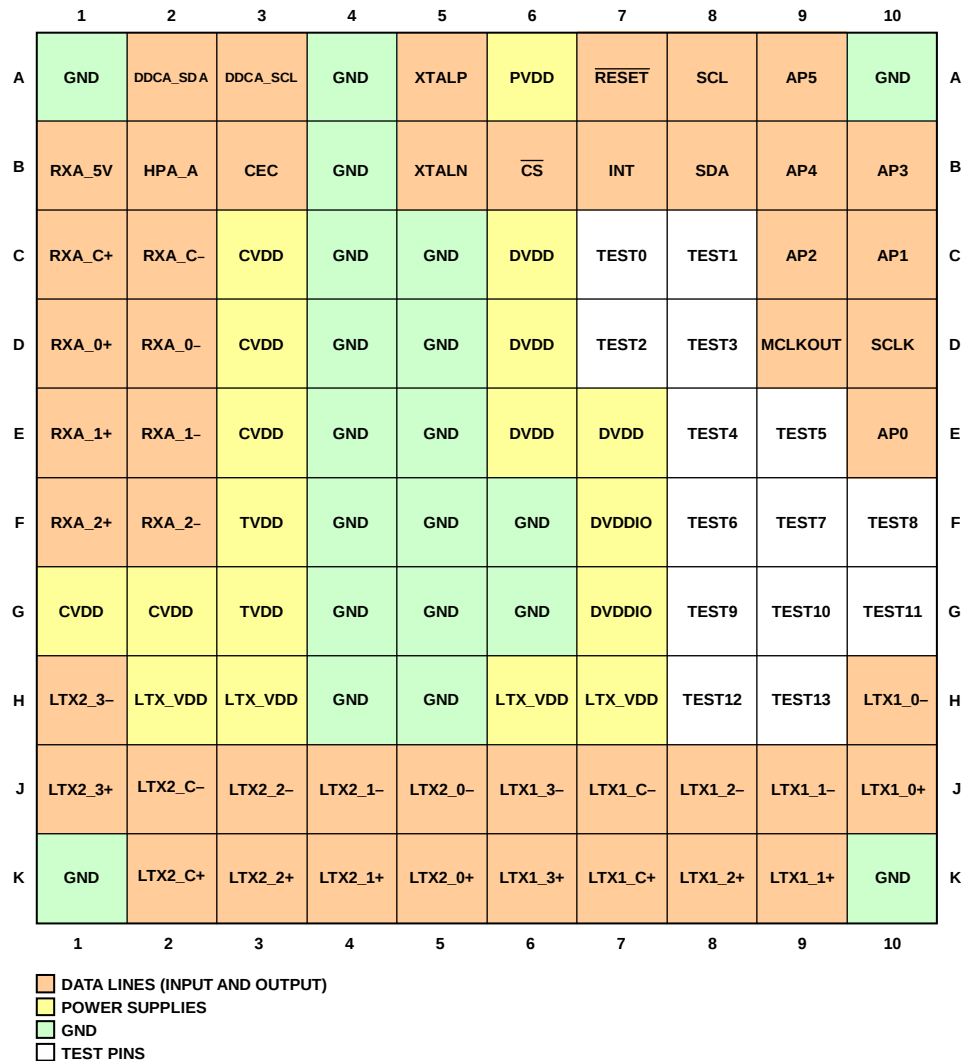


Figure 5. Pin Configuration

Table 5. Pin Function Descriptions

| Pin No                                                                       | Mnemonic | Type                  | Description                                                                                                                                                              |
|------------------------------------------------------------------------------|----------|-----------------------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| A1, A4, A10, B4, C4, C5, D4, D5, E4, E5, F4 to F6, G4 to G6, H4, H5, K1, K10 | GND      | Ground                | Ground.                                                                                                                                                                  |
| A2                                                                           | DDCA_SDA | HDMI Rx DDC           | HDCEP Slave Serial Data for HDMI Port A.                                                                                                                                 |
| A3                                                                           | DDCA_SCL | HDMI Rx DDC           | HDCEP Slave Serial Clock for HDMI Port A.                                                                                                                                |
| A5                                                                           | XTALP    | Miscellaneous analog  | Input for 28.63636 MHz Crystal or an External 1.8 V, 28.63636 MHz Clock Oscillator Source to Clock the <a href="#">ADV7613</a> .                                         |
| A6                                                                           | PVDD     | Power                 | Digital PLL Supply Voltage (1.8 V).                                                                                                                                      |
| A7                                                                           | RESET    | Miscellaneous digital | System Reset Input, Active Low. A minimum low reset pulse width of 5 ms is required to reset the <a href="#">ADV7613</a> circuitry.                                      |
| A8                                                                           | SCL      | Miscellaneous digital | I <sup>2</sup> C Port Serial Clock Input. SCL is the clock line for the control port.                                                                                    |
| A9                                                                           | AP5      | Audio output          | Audio Output Pin 5. This pin is configurable to output S/PDIF digital audio, HBR or DSD. The AP5 pin typically provides the LRCLK signal for the I <sup>2</sup> S modes. |
| B1                                                                           | RXA_5V   | HDMI input            | 5 V Detect Pin for HDMI Port A.                                                                                                                                          |

| Pin No                                               | Mnemonic               | Type                  | Description                                                                                                                                                                                                         |
|------------------------------------------------------|------------------------|-----------------------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| B2                                                   | HPA_A                  | Miscellaneous digital | Hot Plug Assert. This pin can be configured to output the hot plug assert signal for HDMI Port A.                                                                                                                   |
| B3                                                   | CEC                    | Digital input/output  | Consumer Electronics Control Channel.                                                                                                                                                                               |
| B5                                                   | XTALN                  | Miscellaneous analog  | Crystal Output.                                                                                                                                                                                                     |
| B6                                                   | $\overline{\text{CS}}$ | Miscellaneous digital | Chip Select. This pin must be set low for the <a href="#">ADV7613</a> to process I <sup>2</sup> C messages. Pulling this line up causes the I <sup>2</sup> C state machine to ignore I <sup>2</sup> C transmission. |
| B7                                                   | INT                    | Miscellaneous digital | Interrupt. This pin can be active low or active high, open drain or transistor to transistor logic (TTL). The events that trigger an interrupt are under user configuration.                                        |
| B8                                                   | SDA                    | Miscellaneous digital | I <sup>2</sup> C Port Serial Data Input/Output. SDA is the data line for the control port.                                                                                                                          |
| B9                                                   | AP4                    | Audio output          | Audio Output 4. This pin is configurable to output S/PDIF digital audio, HBR, or I <sup>2</sup> S.                                                                                                                  |
| B10                                                  | AP3                    | Audio output          | Audio Output 3. This pin is configurable to output S/PDIF digital audio, HBR, or I <sup>2</sup> S.                                                                                                                  |
| C1                                                   | RXA_C+                 | HDMI input            | Digital Input Clock True of HDMI Port A.                                                                                                                                                                            |
| C2                                                   | RXA_C–                 | HDMI input            | Digital Input Clock Complement of HDMI Port A.                                                                                                                                                                      |
| C3, D3, E3, G1, G2                                   | CVDD                   | Power                 | HDMI Analog Block Supply Voltage (1.8 V).                                                                                                                                                                           |
| C6, D6, E6, E7                                       | DVDD                   | Power                 | Digital Core Supply Voltage (1.8 V).                                                                                                                                                                                |
| C7, C8, D7, D8, E8, E9, F8 to F10, G8 to G10, H8, H9 | TEST0 to TEST13        | Miscellaneous         | Test Pins. Connect these pins to ground via 1 kΩ resistors.                                                                                                                                                         |
| C9                                                   | AP2                    | Audio output          | Audio Output 2. This pin is configurable to output S/PDIF digital audio, HBR, DSD, or I <sup>2</sup> S mode.                                                                                                        |
| C10                                                  | AP1                    | Audio output          | Audio Output 1. This pin is configurable to output S/PDIF digital audio, HBR, or DSD.                                                                                                                               |
| D1                                                   | RXA_0+                 | HDMI input            | Digital Input Channel 0 True of HDMI Port A.                                                                                                                                                                        |
| D2                                                   | RXA_0–                 | HDMI input            | Digital Input Channel 0 Complement of HDMI Port A.                                                                                                                                                                  |
| D9                                                   | MCLKOUT                | Audio output          | Master Clock. This pin is configurable to output the audio master clock signal.                                                                                                                                     |
| D10                                                  | SCLK                   | Audio output          | Serial Clock. This pin is configurable to output the audio serial clock.                                                                                                                                            |
| E1                                                   | RXA_1+                 | HDMI input            | Digital Input Channel 1 True of HDMI Port A.                                                                                                                                                                        |
| E2                                                   | RXA_1–                 | HDMI input            | Digital Input Channel 1 Complement HDMI Port A.                                                                                                                                                                     |
| E10                                                  | AP0                    | Audio Output          | Audio Output 0. This pin is configurable to output S/PDIF digital audio, HBR, DSD, or I <sup>2</sup> S.                                                                                                             |
| F1                                                   | RXA_2+                 | HDMI input            | Digital Input Channel 2 True of HDMI Port A.                                                                                                                                                                        |
| F2                                                   | RXA_2–                 | HDMI input            | Digital Input Channel 2 Complement of HDMI Port A.                                                                                                                                                                  |
| F3, G3                                               | TVDD                   | Power                 | Termination Supply Voltage (3.3 V).                                                                                                                                                                                 |
| F7, G7                                               | DVDDIO                 | Power                 | Digital I/O Supply Voltage (3.3 V).                                                                                                                                                                                 |
| H1                                                   | LTX2_3–                | LVDS output           | LVDS Output Channel 3 Complement of LVDS Output Port 2.                                                                                                                                                             |
| H2, H3, H6, H7                                       | LTX_VDD                | Power                 | LVDS Supply Voltage (1.8 V).                                                                                                                                                                                        |
| H10                                                  | LTX1_0–                | LVDS output           | LVDS Output Channel 0 Complement of LVDS Output Port 1.                                                                                                                                                             |
| J1                                                   | LTX2_3+                | LVDS output           | LVDS Output Channel 3 True of LVDS Output Port 2.                                                                                                                                                                   |
| J2                                                   | LTX2_C–                | LVDS output           | LVDS Clock Complement of LVDS Output Port 2.                                                                                                                                                                        |
| J3                                                   | LTX2_2–                | LVDS output           | LVDS Output Channel 2 Complement of LVDS Output Port 2.                                                                                                                                                             |
| J4                                                   | LTX2_1–                | LVDS output           | LVDS Output Channel 1 Complement of LVDS Output Port 2.                                                                                                                                                             |
| J5                                                   | LTX2_0–                | LVDS output           | LVDS Output Channel 0 Complement of LVDS Output Port 2.                                                                                                                                                             |
| J6                                                   | LTX1_3–                | LVDS output           | LVDS Output Channel 3 Complement of LVDS Output Port 1.                                                                                                                                                             |
| J7                                                   | LTX1_C–                | LVDS output           | LVDS Clock Complement of LVDS Output Port 1.                                                                                                                                                                        |
| J8                                                   | LTX1_2–                | LVDS output           | LVDS Output Channel 2 Complement of LVDS Output Port 1.                                                                                                                                                             |
| J9                                                   | LTX1_1–                | LVDS output           | LVDS Output Channel 1 Complement of LVDS Output Port 1.                                                                                                                                                             |
| J10                                                  | LTX1_0+                | LVDS output           | LVDS Output Channel 0 True of LVDS Output Port 1.                                                                                                                                                                   |
| K2                                                   | LTX2_C+                | LVDS output           | LVDS Clock True of LVDS Output Port 2.                                                                                                                                                                              |
| K3                                                   | LTX2_2+                | LVDS output           | LVDS Output Channel 2 True of LVDS Output Port 2.                                                                                                                                                                   |

| Pin No | Mnemonic | Type        | Description                                       |
|--------|----------|-------------|---------------------------------------------------|
| K4     | LTX2_1+  | LVDS output | LVDS Output Channel 1 True of LVDS Output Port 2. |
| K5     | LTX2_0+  | LVDS output | LVDS Output Channel 0 True of LVDS Output Port 2. |
| K6     | LTX1_3+  | LVDS output | LVDS Output Channel 3 True of LVDS Output Port 1. |
| K7     | LTX1_C+  | LVDS output | LVDS Clock True of LVDS Output Port 1.            |
| K8     | LTX1_2+  | LVDS output | LVDS Output Channel 2 True of LVDS Output Port 1. |
| K9     | LTX1_1+  | LVDS output | LVDS Output Channel 1 True of LVDS Output Port 1. |

## POWER SUPPLY RECOMMENDATIONS

### POWER-UP SEQUENCE

The recommended power-up sequence for the [ADV7613](#) is to power up the 3.3 V supplies first, followed by the 1.8 V supplies. Hold the **RESET** line low for at least 5 ms after the supplies have powered up. Allow a minimum additional 5 ms before carrying out the first I<sup>2</sup>C transaction.

Alternatively, power up the [ADV7613](#) by asserting all supplies simultaneously. In this case, take care while the supplies are being established to ensure that a lower voltage supply does not go above a higher voltage supply level. Hold the **RESET** line low for at least 5 ms after the supplies have powered up. Allow a minimum additional 5 ms before carrying out the first I<sup>2</sup>C transaction.

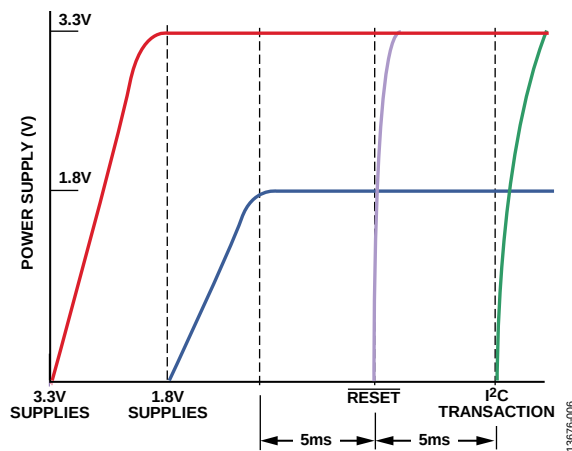


Figure 6. Recommended Power-Up Sequence

### POWER-DOWN SEQUENCE

The [ADV7613](#) power supplies can be deasserted simultaneously as long as a higher rated supply (for example, TVDD/DVDDIO) does not fall to a voltage level less than a lower rated supply (for example, DVDD), and the absolute maximum ratings specifications are followed.

## THEORY OF OPERATION

### HDMI RECEIVER

The HDMI receiver supports HDTV formats of up to 1080p. The HDMI-compatible receiver on the [ADV7613](#) allows active equalization of the HDMI data signals. This equalization compensates for the high frequency losses inherent in HDMI and DVI cabling, especially at longer cable lengths and higher frequencies. The HDMI-compatible receiver is capable of equalizing for cable lengths up to 20 meters to achieve robust receiver performance.

The HDMI receiver offers advanced audio functionality. The receiver contains an audio mute controller that can detect a variety of conditions that may result in audible extraneous noise in the audio output. Upon detection of these conditions, the audio signal can be ramped down or muted to prevent audio clicks or pops. The HDMI receiver supports the reception of all types of audio data described in the HDMI specifications, including the following:

- LPCM (uncompressed audio)
- IEC 61937 (compressed audio)
- DSD audio (1-bit audio)
- HBR audio (high bit rate compressed audio)
- Audio sample, HBR, DSD packet support
- Support for EDID RAM

There is no Deep Color support in the [ADV7613](#).

### HDCP REPEATER FUNCTIONALITY

With the inclusion of HDCP, displays can receive encrypted video content. The HDMI interface of the [ADV7613](#) allows authentication of a video receiver, decryption of encoded data at the receiver, and renewability of that authentication during transmission, as specified by the HDCP 1.4 specification.

### COMPONENT PROCESSOR (CP)

The [ADV7613](#) has two any to any,  $3 \times 3$  color space conversion (CSC) matrices. The first CSC block is located in front of the CP section. The second CSC block is located at the back of the CP section. Each CSC enables YCrCb to RGB and RGB to YCrCb conversions.

CP features include

- Support for 525p, 625p, 720p, 1080p, as well as some graphics standard (WVGA, WXGA)
- Manual adjustments including gain (contrast), offset (brightness), hue, and saturation
- Free run output mode that provides stable timing when no video input is present
- Standard identification enabled by the STDI block

### LVDS TRANSMITTER FEATURES

The LVDS or OpenLDI encoder can package data into 6-bit or 8-bit non-dc balanced OpenLDI mapping, or 8-bit VESA mapping. The [ADV7613](#) can output 24-bit OpenLDI data over

two LVDS transmitters up to a maximum input resolution of 1080p at 60 Hz.

The two LVDS output ports (Port 1 and Port 2) can drive two identical LVDS display panels with video streams from a single video data stream received by the HDMI receiver block.

In the dual LVDS transmitter mode of the [ADV7613](#), the OpenLDI encoder splits the single video stream received by the HDMI block into two video streams; the odd video stream and the even video stream. LVDS Output Port 1 outputs the even video stream and LVDS Output Port 2 outputs the odd video stream.

When connected to the dual LVDS receiver panel, LVDS Output Port 1 must be connected to the even LVDS receiver port of the LVDS panel. LVDS Output Port 2 must be connected to the odd receiver port of the LVDS panel.

In the single LVDS transmitter mode, the video is output on either LVDS Output Port 1 or LVDS Output Port 2.

The maximum video resolution supported by a single LVDS output port must have a clock frequency of 92 MHz or less.

### I<sup>2</sup>C INTERFACE

The [ADV7613](#) supports a 2-wire serial (I<sup>2</sup>C-compatible) interface.

### OTHER FEATURES

Other features of the [ADV7613](#) include the following:

- Programmable interrupt output pin, INT
- Chip select,  $\overline{\text{CS}}$

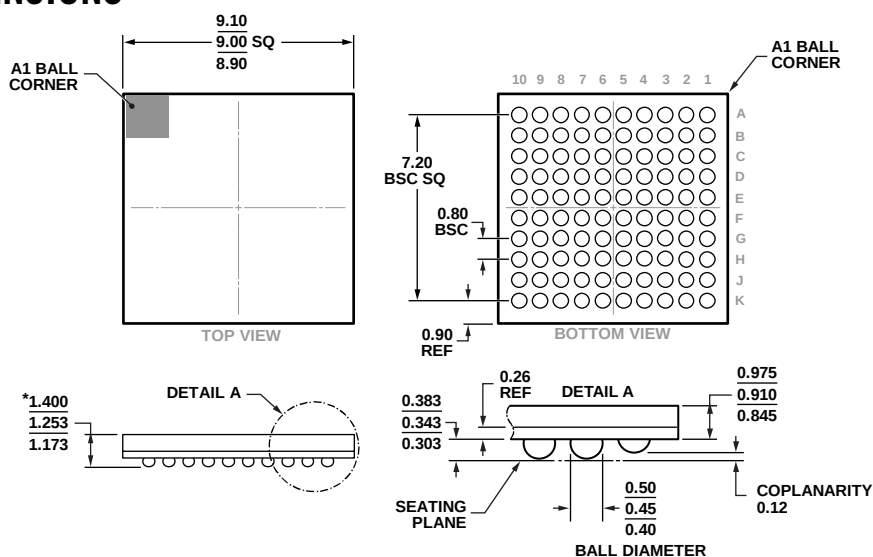
### AUDIO OUTPUT DATA

The audio output pins (AP0 to AP5) can output audio data in a number of formats as described in Table 6.

**Table 6. Description of Audio Formats Supported**

| Pin No. | Mnemonic | I <sup>2</sup> S/SPDIF Interface        | DSD Interface              |
|---------|----------|-----------------------------------------|----------------------------|
| E10     | AP0      | SPDIF0                                  | DSD0A (first DSD channel)  |
| C10     | AP1      | I <sup>2</sup> S0/SPDIF0                | DSD0B (second DSD channel) |
| C9      | AP2      | I <sup>2</sup> S1/SPDIF1                | DSD1A (third DSD channel)  |
| B10     | AP3      | I <sup>2</sup> S2/SPDIF2                | DSD1B (fourth DSD channel) |
| B9      | AP4      | I <sup>2</sup> S3/SPDIF3                | DSD2A (fourth DSD channel) |
| A9      | AP5      | LRCLK (left/right channel clock output) | DSD2B (fifth DSD channel)  |
| D9      | MCLKOUT  | Master clock output (MCLK)              | Not applicable             |
| D10     | SCLK     | Bit or serial clock output (SCLK)       | Not applicable             |

## OUTLINE DIMENSIONS



\*COMPLIANT TO JEDEC STANDARDS MO-275-DDAB-1  
WITH THE EXCEPTION OF THE PACKAGE HEIGHT

Figure 7. 100-Ball Chip Scale Package Ball Grid Array [CSP\_BGA]  
(BC-100-4)  
Dimensions shown in millimeters

## ORDERING GUIDE

| Model             | Temperature Range | Package Description                                   | Package Option |
|-------------------|-------------------|-------------------------------------------------------|----------------|
| ADV7613BBCZ       | -40°C to +85°C    | 100-Ball Chip Scale Package Ball Grid Array [CSP_BGA] | BC-100-4       |
| ADV7613BBCZ-RL    | -40°C to +85°C    | 100-Ball Chip Scale Package Ball Grid Array [CSP_BGA] | BC-100-4       |
| ADV7613WBBCZ      | -40°C to +85°C    | 100-Ball Chip Scale Package Ball Grid Array [CSP_BGA] | BC-100-4       |
| ADV7613WBBCZ-RL   | -40°C to +85°C    | 100-Ball Chip Scale Package Ball Grid Array [CSP_BGA] | BC-100-4       |
| ADV7613WBBCZ-P    | -40°C to +85°C    | 100-Ball Chip Scale Package Ball Grid Array [CSP_BGA] | BC-100-4       |
| ADV7613WBBCZ-P-RL | -40°C to +85°C    | 100-Ball Chip Scale Package Ball Grid Array [CSP_BGA] | BC-100-4       |
| EVAL-ADV7613FEBZ  |                   | Evaluation Board                                      |                |

## AUTOMOTIVE PRODUCTS

The [ADV7613W](#) models are available with controlled manufacturing to support the quality and reliability requirements of automotive applications. Note that these automotive models may have specifications that differ from the commercial models; therefore, designers should review the Specifications section of this data sheet carefully. Only the automotive grade products shown are available for use in automotive applications. Contact your local Analog Devices account representative for specific product ordering information and to obtain the specific Automotive Reliability reports for these models.

I<sup>2</sup>C refers to a communications protocol originally developed by Philips Semiconductors (now NXP Semiconductors).

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