60 MHz, G = +2, 16 × 16 Buffered Analog Crosspoint Switch

Data Sheet **ADV3205**

FEATURES

- 16 × 16 high speed nonblocking switch array
- Serial or parallel programming of switch array
- Serial data out allows daisy-chaining control of multiple 16 × 16 devices to create larger switch arrays
- Complete solution
  - Buffered inputs
  - 16 output amplifiers
  - Operates on ±5 V supplies
  - Low supply current of 50 mA
- Excellent video performance, V_S = ±5 V
  - −3 dB bandwidth: 60 MHz
  - 0.1 dB gain flatness: 10 MHz
  - 0.1% differential gain error (R_L = 1 kΩ)
  - 0.1° differential phase error (R_L = 1 kΩ)
- Low all hostile crosstalk: −67 dB at 5 MHz
- Output disable allows connection of multiple devices without loading the output bus
- $\overline{\text{RESET}}$ pin allows disabling of all outputs
  - Power-on reset capability with capacitor to ground
- 100-lead LQFP (14 mm × 14 mm)

APPLICATIONS

- CCTV surveillance
- Video routers (NTSC, PAL, S-Video, SECAM)
- Video conferencing

FUNCTIONAL BLOCK DIAGRAM

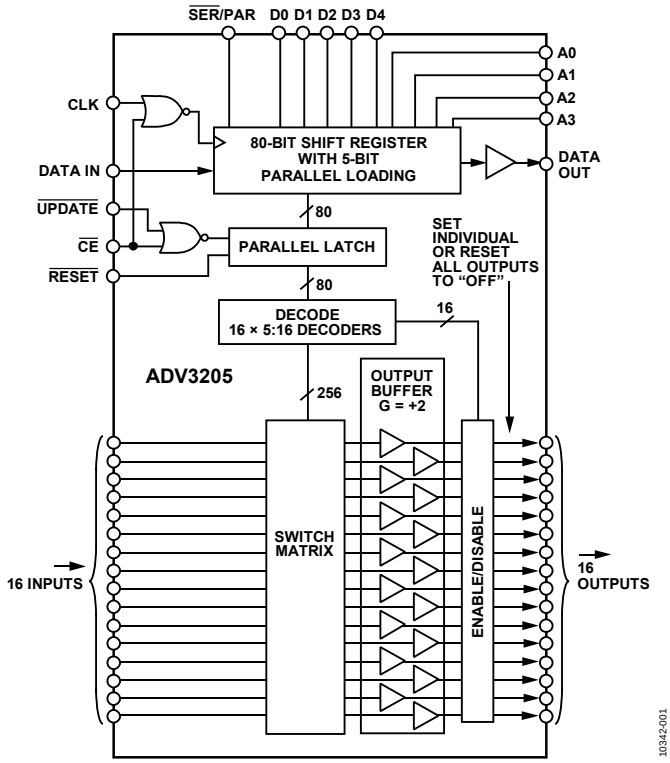


Figure 1.

GENERAL DESCRIPTION

The ADV3205 is a fully buffered crosspoint switch matrix that operates on ±5 V, making it ideal for video applications. It offers a −3 dB signal bandwidth of 60 MHz and channel switch times of less than 60 ns with 0.1% settling. The ADV3205 has excellent crosstalk performance, and ground/power pins surround all inputs and outputs to provide extra shielding required for the most demanding applications. The differential gain and differential phase of better than 0.1% and 0.1°, respectively, along with 0.1 dB flatness out to 10 MHz, make the ADV3205 an excellent choice for many video applications.

The ADV3205 includes 16 independent output buffers that can be placed into a disabled state for paralleling crosspoint outputs. The ADV3205 has a gain of +2 and operates on voltage supplies of ±5 V while consuming only 34 mA of current. Channel switching is performed via a serial digital control (which can accommodate daisy-chaining of several devices) or via a parallel control, allowing updating of an individual output without reprogramming the entire array.

The ADV3205 is packaged in a 100-lead LQFP and is available over the commercial temperature range of 0°C to 70°C.

Rev. 0

One Technology Way, P.O. Box 9106, Norwood, MA 02062-9106, U.S.A.
Tel: 781.329.4700 www.analog.com
Fax: 781.461.3113

TABLE OF CONTENTS

REVISION HISTORY

12/11—Revision 0: Initial Version

SPECIFICATIONS

T_A = 25°C, V_S = ±5 V, R_L = 150 Ω, unless otherwise noted.

Table 1.

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
DYNAMIC PERFORMANCE					
−3 dB Bandwidth	V_{OUT} = 200 mV p-p	41	60		MHz
	V_{OUT} = 2 V p-p		25		MHz
Gain Flatness	0.1 dB, V_{OUT} = 200 mV p-p		10		MHz
Propagation Delay	V_{OUT} = 2 V p-p		20		ns
Settling Time	0.1%, 2 V output step		23		ns
Slew Rate	2 V output step		100		V/µs
NOISE/DISTORTION PERFORMANCE					
Differential Gain Error	NTSC, R_L = 1 kΩ		0.1		%
Differential Phase Error	NTSC, R_L = 1 kΩ		0.1		Degrees
Crosstalk, All Hostile	f = 5 MHz		−67		dB
Off Isolation	f = 5 MHz, one channel		−100		dB
Input Voltage Noise	0.1 MHz to 10 MHz		12		nV/√Hz
DC PERFORMANCE					
Gain Error			0.5		%
Gain Matching	Channel-to-channel		0.7		%
Gain Temperature Coefficient			20		ppm/°C
OUTPUT CHARACTERISTICS					
Output Resistance	Enabled		0.3		Ω
	Disabled	3.4	4		kΩ
Output Capacitance	Disabled		5		pF
Output Voltage Swing	No Load	±3.2	±3.5		V
	I_{OUT} = 20 mA	±2.7	±3		V
Short-Circuit Current			55		mA
INPUT CHARACTERISTICS					
Input Offset Voltage	All configurations		±5	±10	mV
	Temperature coefficient		10		µV/°C
Input Voltage Range	No load		±1.5		V
Input Capacitance	Any switch configuration		4		pF
Input Resistance	Any number of connected outputs		50		MΩ
Input Bias Current	Any number of enabled inputs		±1		µA
SWITCHING CHARACTERISTICS					
Enable On Time			80		ns
Switching Time, 2 V Step	50% update to 1% settling		50		ns
Switching Transient (Glitch)			20		mV p-p
POWER SUPPLIES					
Supply Current	AV_{CC} outputs enabled, no load		45	50	mA
	AV_{CC} outputs disabled		31	35	mA
	AV_{EE} outputs enabled, no load		45	50	mA
	AV_{EE} outputs disabled		31	35	mA
	DV_{CC} outputs enabled, no load		8	13	mA
DYNAMIC PERFORMANCE					
Supply Voltage Range	AV_{CC}	4.5		5.5	V
	AV_{EE}	−5.5		−4.5	V
	DV_{CC}	4.5		5.5	V
PSRR	DC	75	80		dB
	f = 100 kHz		60		dB
	f = 1 MHz		40		dB

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
OPERATING TEMPERATURE RANGE					
Temperature Range	Operating (still air)	0		70	°C
θ_{JA}	Operating (still air)		40		°C/W

TIMING CHARACTERISTICS (SERIAL MODE)

Table 2.

Parameter	Symbol	Limit			Unit
		Min	Typ	Max	
Serial Data Setup Time	t_1	20			ns
CLK Pulse Width	t_2	100			ns
Serial Data Hold Time	t_3	20			ns
CLK Pulse Separation, Serial Mode	t_4	100			ns
CLK-to-$\overline{\text{UPDATE}}$ Delay	t_5	0			ns
$\overline{\text{UPDATE}}$ Pulse Width	t_6	50			ns
CLK-to-DATA OUT Valid, Serial Mode	t_7			200	ns
Propagation Delay, $\overline{\text{UPDATE}}$ to Switch On or Off				50	ns
Data Load Time, CLK = 5 MHz, Serial Mode			16		µs
CLK, $\overline{\text{UPDATE}}$ Rise and Fall Times				100	ns
$\overline{\text{RESET}}$ Time				200	ns

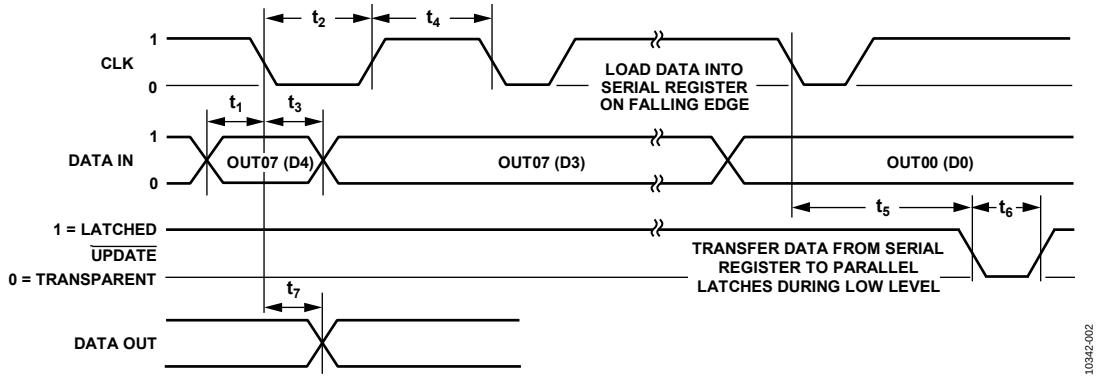


Figure 2. Timing Diagram, Serial Mode

Table 3. Logic Levels

V_{IH}	V_{IL}	V_{OH}	V_{OL}	I_{IH}	I_{IL}	I_{OH}	I_{OL}
$\overline{\text{RESET}}$, $\overline{\text{SER}}$/PAR CLK, DATA IN, $\overline{\text{CE}}$, $\overline{\text{UPDATE}}$	$\overline{\text{RESET}}$, $\overline{\text{SER}}$/PAR CLK, DATA IN, $\overline{\text{CE}}$, $\overline{\text{UPDATE}}$	DATA OUT	DATA OUT	$\overline{\text{RESET}}$, $\overline{\text{SER}}$/PAR CLK, DATA IN, $\overline{\text{CE}}$, $\overline{\text{UPDATE}}$	$\overline{\text{RESET}}$, $\overline{\text{SER}}$/PAR CLK, DATA IN, $\overline{\text{CE}}$, $\overline{\text{UPDATE}}$	DATA OUT	DATA OUT
2.0 V min	0.8 V max	2.7 V min	0.5 V max	20 µA max	−400 µA min	−400 µA max	3.0 mA min

TIMING CHARACTERISTICS (PARALLEL MODE)

Table 4.

Parameter	Symbol	Limit		Unit
		Min	Max	
Parallel Data Setup Time	t_{1d}	20		ns
Address Setup Time	t_{1a}	20		ns
CLK Enable Width	t_2	100		ns
Parallel Data Hold Time	t_{3d}	20		ns
Address Hold Time	t_{3a}	20		ns
CLK Pulse Separation	t_4	100		ns
CLK-to-$\overline{\text{UPDATE}}$ Delay	t_5	0		ns
$\overline{\text{UPDATE}}$ Pulse Width	t_6	50		ns
Propagation Delay, $\overline{\text{UPDATE}}$ to Switch On or Off			50	ns
CLK, $\overline{\text{UPDATE}}$ Rise and Fall Times			100	ns
$\overline{\text{RESET}}$ Time			200	ns

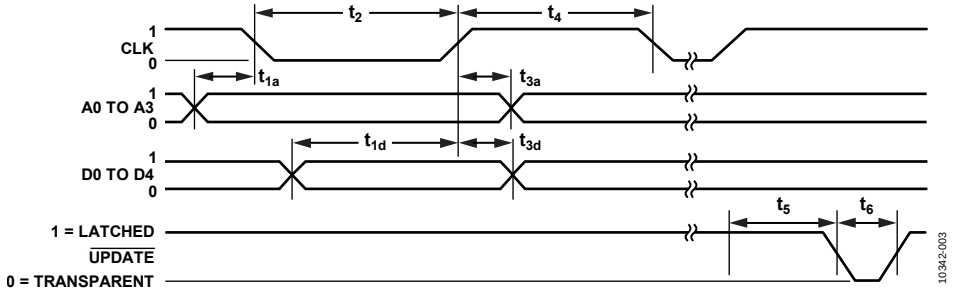


Figure 3. Timing Diagram, Parallel Mode

Table 5. Logic Levels

V_{IH}	V_{IL}	V_{OH}	V_{OL}	I_{IH}	I_{IL}	I_{OH}	I_{OL}
$\overline{\text{RESET}}$, $\overline{\text{SER}}$/PAR CLK, D0, D1, D2, D3, D4, A0, A1, A2, A3, $\overline{\text{CE}}$, $\overline{\text{UPDATE}}$	$\overline{\text{RESET}}$, $\overline{\text{SER}}$/PAR CLK, D0, D1, D2, D3, D4, A0, A1, A2, A3, $\overline{\text{CE}}$, $\overline{\text{UPDATE}}$	DATA OUT	DATA OUT	$\overline{\text{RESET}}$, $\overline{\text{SER}}$/PAR CLK, D0, D1, D2, D3, D4, A0, A1, A2, A3, $\overline{\text{CE}}$, $\overline{\text{UPDATE}}$	$\overline{\text{RESET}}$, $\overline{\text{SER}}$/PAR CLK, D0, D1, D2, D3, D4, A0, A1, A2, A3, $\overline{\text{CE}}$, $\overline{\text{UPDATE}}$	DATA OUT	DATA OUT
2.0 V min	0.8 V max	2.7 V min	0.5 V max	20 µA max	−400 µA min	−400 µA max	3.0 mA min

ABSOLUTE MAXIMUM RATINGS

Table 6.

Parameter	Rating
Analog Supply Voltage (AV_{CC} to AV_{EE})	12 V
Digital Supply Voltage (DV_{CC} to DGND)	6 V
Ground Potential Difference (AGND to DGND)	±0.5 V
Internal Power Dissipation[1]	3.1 W
Analog Input Voltage[2]	Maintain linear output
Digital Input Voltage	DV_{CC}
Output Voltage (Disabled Output)	(AV_{CC} − 1.5 V) to (AV_{EE} + 1.5 V)
Output Short-Circuit Duration	Momentary
Storage Temperature Range	−65°C to +125°C
Lead Temperature (Soldering 10 sec)	300°C

[1] Specification is for device in free air (T_A = 25°C): 100-lead plastic LQFP: θ_{JA} = 40°C/W.

[2] To avoid differential input breakdown, in no case should one-half the output voltage (1/2 V_{OUT}) and any input voltage be greater than 10 V potential differential. See the output voltage swing parameter in Table 1 for the linear output range.

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

POWER DISSIPATION

Packaged in a 100-lead LQFP, the ADV3205 junction-to-ambient thermal impedance (θ_{JA}) is 40°C/W. For long-term reliability, the maximum allowed junction temperature of the plastic encapsulated die should not exceed 150°C. Temporarily exceeding this limit may cause a shift in parametric performance due to a change in the stresses exerted on the die by the package. Exceeding a junction temperature of 175°C for an extended period can result in device failure.

The maximum ADV3205 power dissipation occurs when all outputs are enabled and driving loads. Supply current increases approximately linearly with the number of outputs that are enabled. Refer to the Theory of Operation section for more details regarding power dissipation calculations. Figure 4 indicates the maximum ADV3205 power dissipation as a function of ambient temperature.

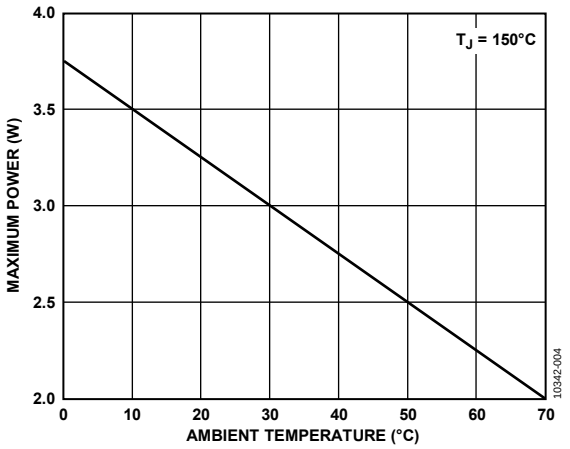


Figure 4. Maximum Power Dissipation vs. Ambient Temperature

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

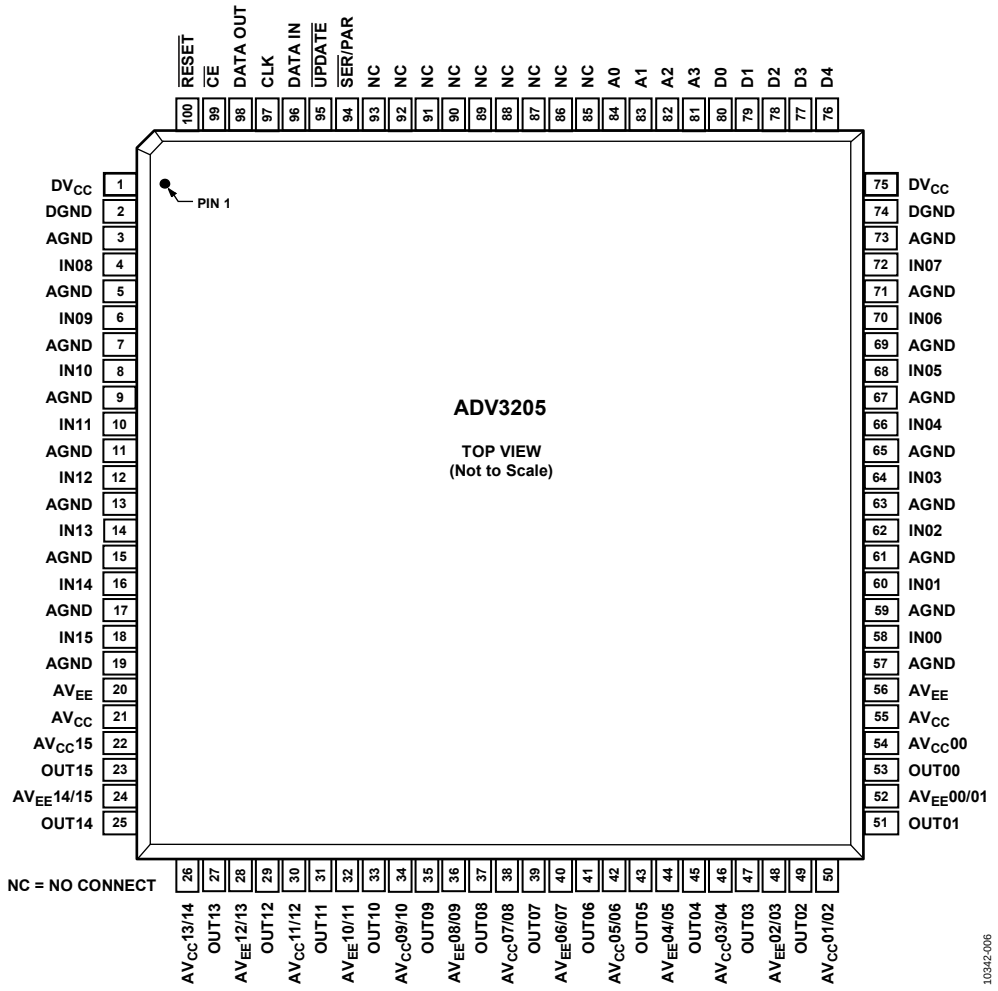


Figure 5. Pin Configuration

Table 7. Pin Function Descriptions

Pin Number	Mnemonic	Description
1, 75	DV_{CC}	5 V for Digital Circuitry.
2, 74	DGND	Ground for Digital Circuitry.
3, 5, 7, 9, 11, 13, 15, 17, 19, 57, 59, 61, 63, 65, 67, 69, 71, 73	AGND	Analog Ground for Inputs and Switch Matrix.
4, 6, 8, 10, 12, 14, 16, 18, 58, 60, 62, 64, 66, 68, 70, 72	INxx	Analog Inputs; xx = Channel Number 00 through Channel Number 15.
20, 56	AV_{EE}	−5 V for Inputs and Switch Matrix.
21, 55	AV_{CC}	5 V for Inputs and Switch Matrix.
22, 54	AV_{CC}xx	5 V for Output Amplifier that is used by Channel Number xx.
26, 30, 34, 38, 42, 46, 50	AV_{CC}xx/yy	5 V for Output Amplifier that is shared by Channel Number xx and Channel Number yy.
23, 25, 27, 29, 31, 33, 35, 37, 39, 41, 43, 45, 47, 49, 51, 53	OUTyy	Analog Outputs; yy = Channel Number 00 Through Channel Number 15.
24, 28, 32, 36, 40, 44, 48, 52	AV_{EE}xx/yy	−5 V for Output Amplifier that is shared by Channel Number xx and Channel Number yy.
76	D4	Parallel Data Input, TTL Compatible (Output Enable).
77	D3	Parallel Data Input, TTL Compatible (Input Select MSB).
78	D2	Parallel Data Input, TTL Compatible (Input Select).
79	D1	Parallel Data Input, TTL Compatible (Input Select).

Pin Number	Mnemonic	Description
80	D0	Parallel Data Input, TTL Compatible (Input Select LSB).
81	A3	Parallel Data Input, TTL Compatible (Output Select MSB).
82	A2	Parallel Data Input, TTL Compatible (Output Select).
83	A1	Parallel Data Input, TTL Compatible (Output Select).
84	A0	Parallel Data Input, TTL Compatible (Output Select LSB).
85 to 93	NC	No Connect. Do not connect to this pin.
94	$\overline{\text{SER}}$/PAR	Selects Serial Data Mode, Low or Parallel Data Mode, High.
95	$\overline{\text{UPDATE}}$	Enable (Transparent) Low. Allows serial register to connect directly to switch matrix. Data latched when high.
96	DATA IN	Serial Data Input, TTL Compatible.
97	CLK	Clock, TTL Compatible. Falling edge triggered.
98	DATA OUT	Serial Data Out, TTL Compatible.
99	$\overline{\text{CE}}$	Chip Enable, Enable Low. Must be low to clock in and latch data.
100	$\overline{\text{RESET}}$	Disable Outputs, Active Low.

TRUTH TABLE AND LOGIC DIAGRAM

Table 8. Operation Truth Table[1]

$\overline{CE}$	$\overline{UPDATE}$	CLK	DATA IN	DATA OUT	$\overline{RESET}$	$\overline{SER}$/PAR	Operation/Comment
1	X	X	X	X	X	X	No change in logic.
0	1	↓[2]	Data $_i$	Data $_{i-80}$	1	0	The data on the serial DATA IN line is loaded into the serial register. The first bit clocked into the serial register appears at DATA OUT 80 clocks later.
0	1	↓[3]	D0 ... D4, A0 ... A3	Not applicable in parallel mode	1	1	The data on the parallel data lines, D0 to D4, are loaded into the 80-bit serial shift register location addressed by A0 to A3.
0	0	X	X	X	1	X	Data in the 80-bit shift register transfers into the parallel latches that control the switch array. Latches are transparent.
X	X	X	X	X	0	X	Asynchronous operation. All outputs are disabled. Remainder of logic is unchanged.

[1] X = don't care, 0 = logic low, 1 = logic high, and ↓ = falling edge triggered.
[2] ↓ = falling edge triggered.
[3] ↓ = low level triggered.

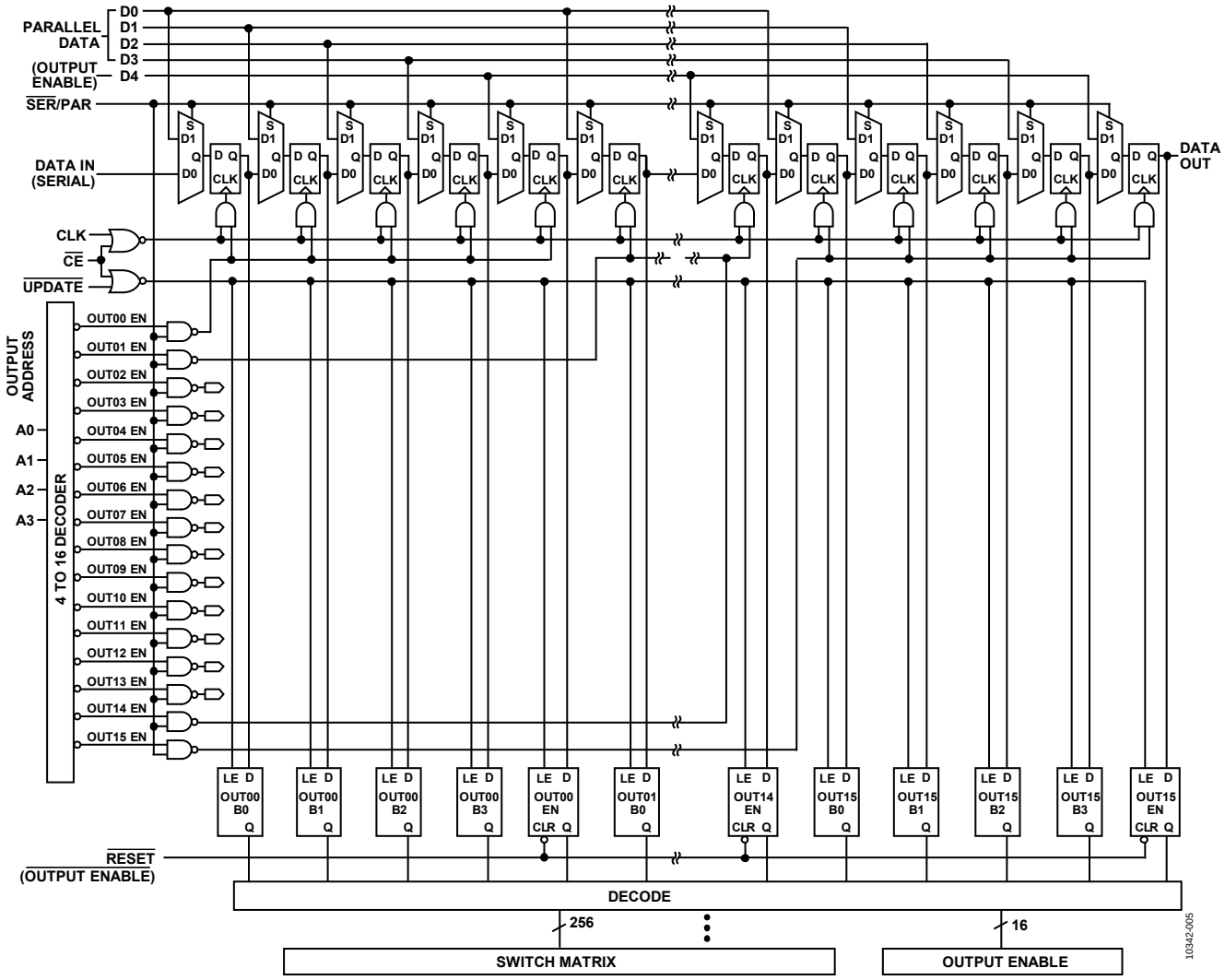


Figure 6. Logic Diagram

TYPICAL PERFORMANCE CHARACTERISTICS

T_A = 25°C, V_S = ±5 V, R_L = 150 Ω, unless otherwise noted.

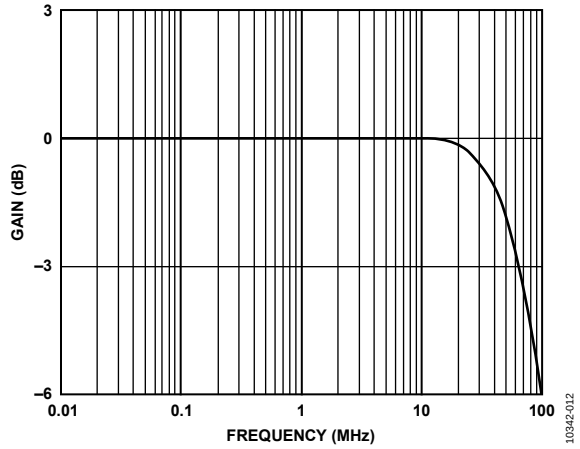


Figure 7. Small Signal Bandwidth, V_{OUT} = 200 mV p-p

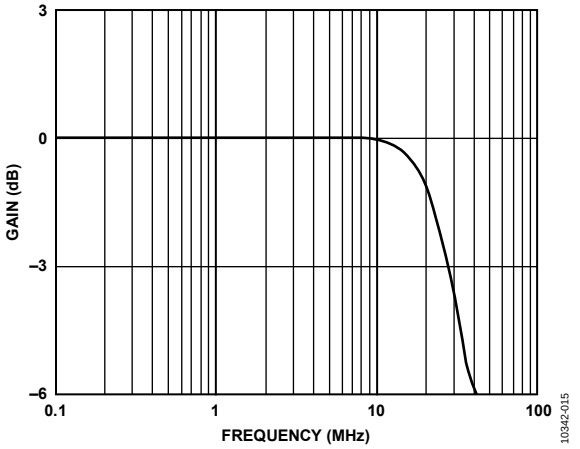


Figure 10. Large Signal Bandwidth, V_{OUT} = 2 V p-p

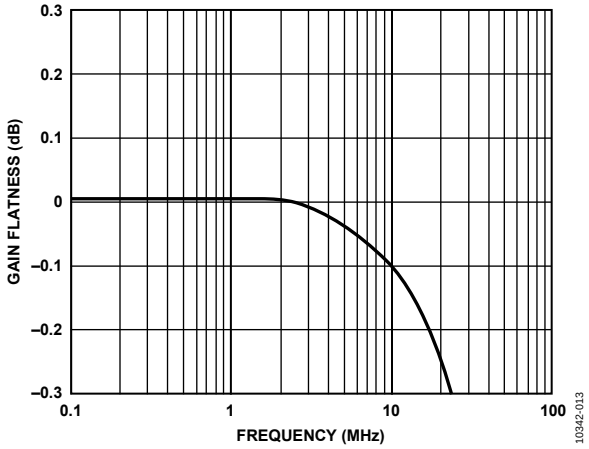


Figure 8. Small Signal Gain Flatness, V_{OUT} = 200 mV p-p

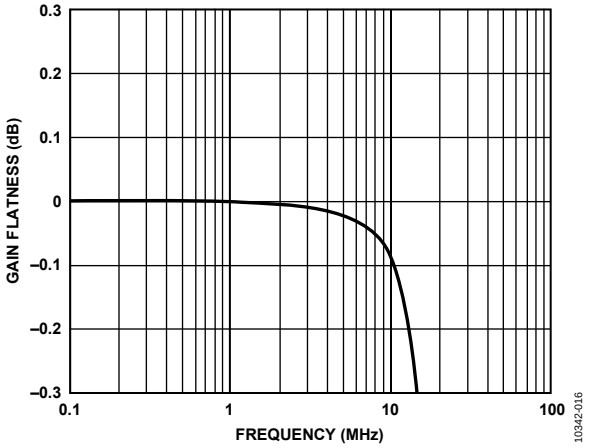


Figure 11. Large Signal Gain Flatness, V_{OUT} = 2 V p-p

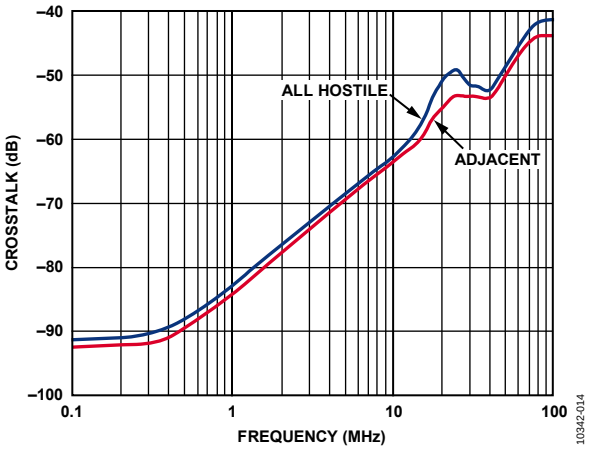


Figure 9. Crosstalk vs. Frequency, V_{OUT} = 2 V p-p

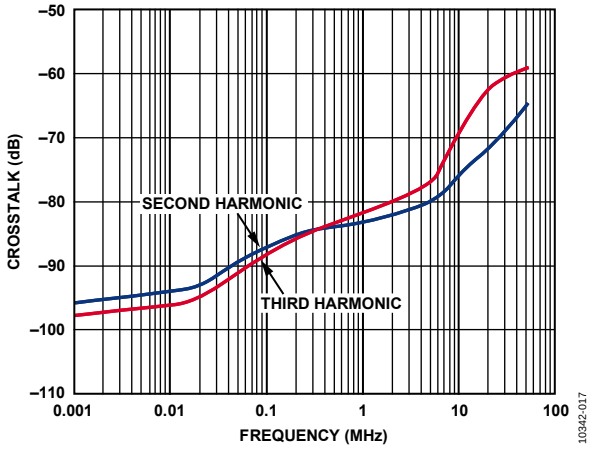


Figure 12. Distortion vs. Frequency, V_{OUT} = 2 V p-p

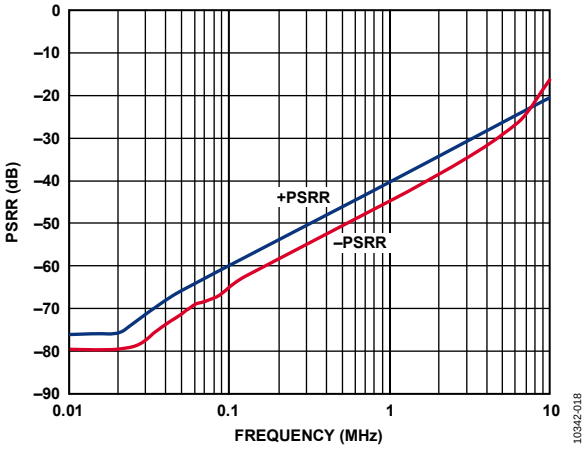


Figure 13. PSRR vs. Frequency

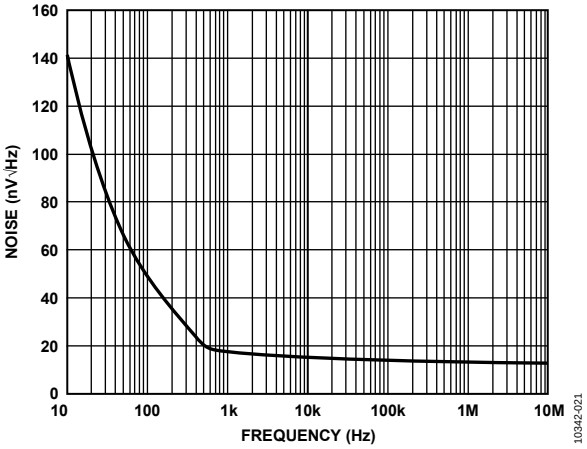


Figure 16. Noise vs. Frequency

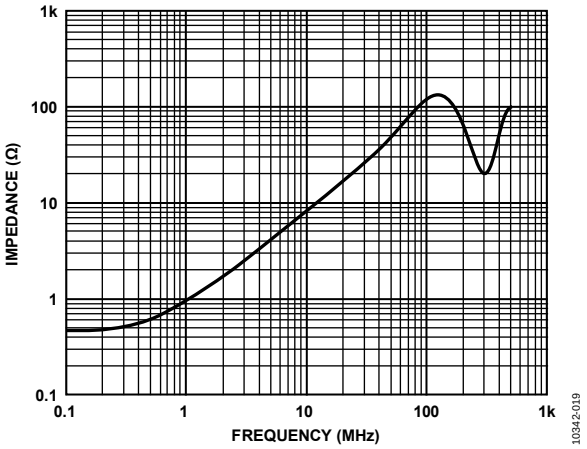


Figure 14. Enabled Output Impedance vs. Frequency

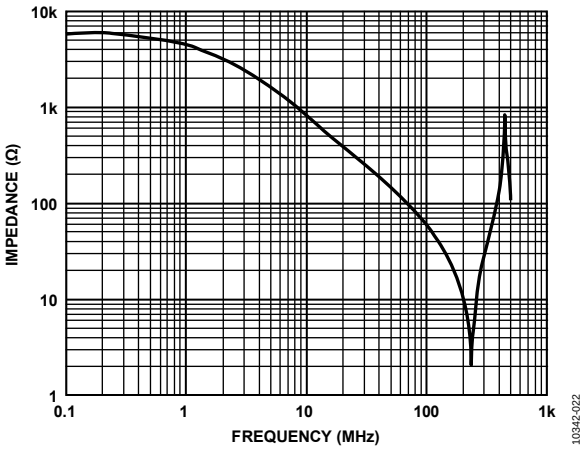


Figure 17. Disabled Output Impedance vs. Frequency

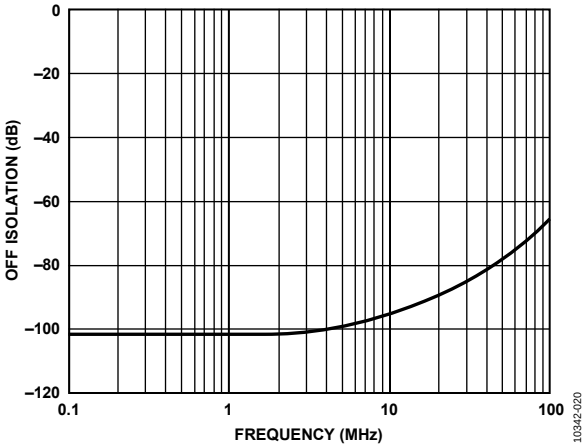


Figure 15. Off Isolation vs. Frequency, V_{OUT} = 2 V p-p

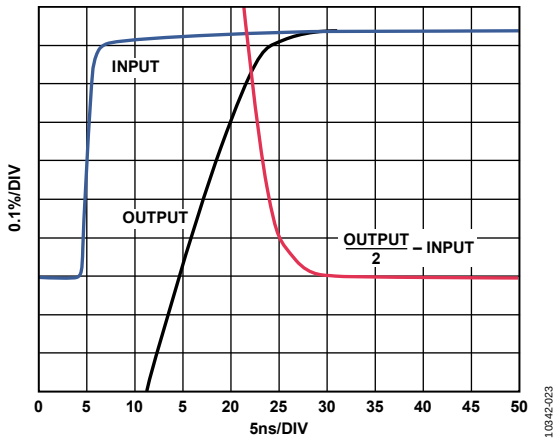


Figure 18. Settling Time to 0.1%, 2 V Output Step

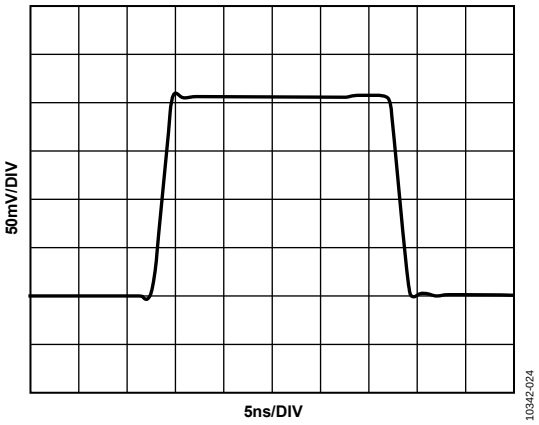


Figure 19. Small Signal Pulse Response

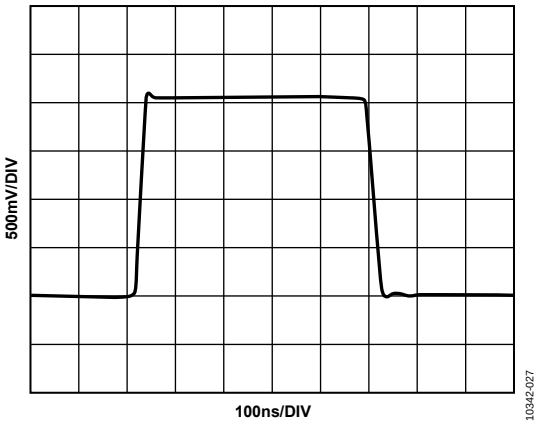


Figure 22. Large Signal Pulse Response

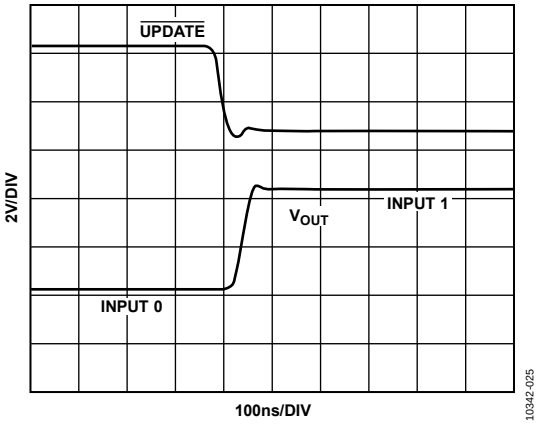


Figure 20. Switching Time

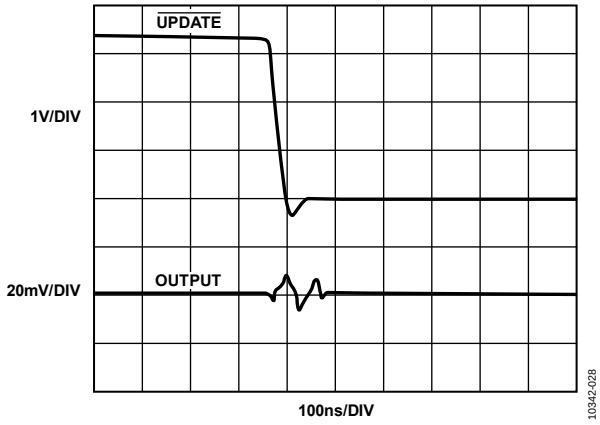


Figure 23. Switching Transient

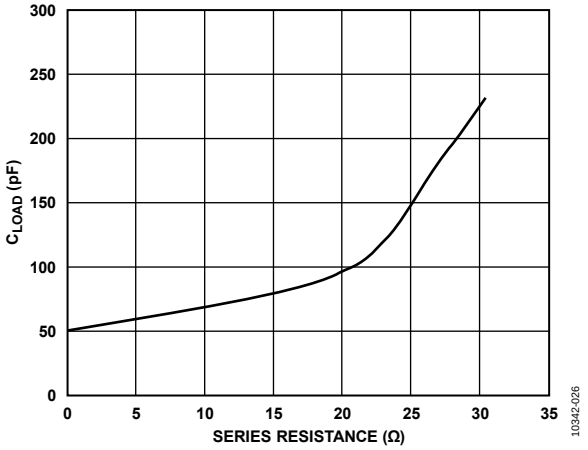


Figure 21. C_{LOAD} vs. Series Resistance for Less than 30% Overshoot

CIRCUIT DIAGRAMS

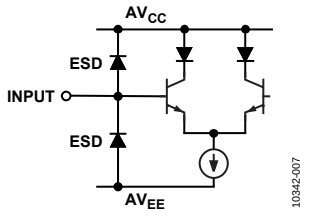


Figure 24. Analog Input

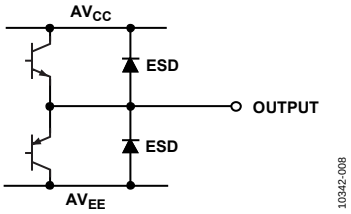


Figure 25. Analog Output

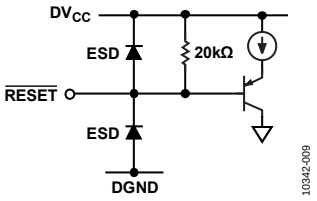


Figure 26. Reset Input

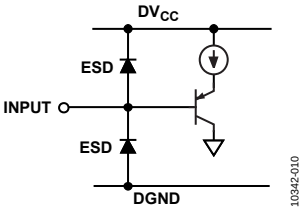


Figure 27. Logic Input

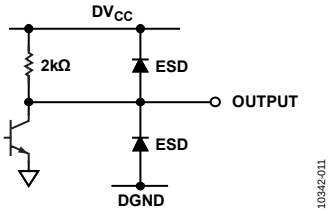


Figure 28. Logic Output

THEORY OF OPERATION

The ADV3205 is a gain-of-two crosspoint array with 16 outputs, each of which can be connected to any one of 16 inputs. Organized by output row, 16 switchable transconductance stages are connected to each output buffer in the form of a 16-to-1 multiplexer. Each of the 16 rows of transconductance stages are wired in parallel to the 16 input pins, for a total array of 256 transconductance stages. Decoding logic for each output selects one (or none) of the transconductance stages to drive the output stage. The transconductance stages are NPN input differential pairs, sourcing current into the folded cascode output stage. The compensation networks and emitter follower output buffers are in the output stage. Voltage feedback sets the gain at +2.

The ADV3205 can drive reverse-terminated video loads, swinging ±3.0 V into 150 Ω. Disabling unused outputs and transconductance stages minimizes on-chip power consumption.

Features of the ADV3205 facilitate the construction of larger switch matrices. The unused outputs can be disabled, leaving only a feedback network resistance of 4 kΩ on the output. This allows multiple ICs to be bused together, provided the output load impedance is greater than the minimum allowed values. Because no additional input buffering is necessary, high input resistance and low input capacitance are easily achieved without additional signal degradation.

The ADV3205 inputs have a unique bias current compensation scheme that overcomes a problem common to transconductance input array architectures. Typically, input bias current increases as more and more transconductance stages connected to the same input are turned on. Anywhere from 0 to 16 transconductance stages can be sharing one input pin, so there is a varying amount of bias current supplied through the source impedance driving the input. The ADV3205 samples and cancels the input bias current contributions from each transconductance stage so that the residual bias current is nominally zero, regardless of the number of enabled inputs.

The ADV3205 contains internal crosstalk isolation clamps that have variable bias levels. These levels were chosen to allow the necessary input range to accommodate the full output swing with a gain of +2. Overdriving the inputs beyond the linear range of the device eventually forward biases these clamps, increasing the power dissipation. The valid input range is ±1.5 V. When outputs are disabled and being driven externally, the voltage applied to them should not exceed the valid input swing range for the ADV3205.

A flexible TTL-compatible logic interface simplifies the programming of the matrix. Either parallel or serial loading into a first rank of latches programs each output. A global latch simultaneously updates all outputs. In serial mode, a serial data out pin (DATA OUT) allows devices to be daisy chained together for single pin programming of multiple ICs. A power-on reset function can be implemented to avoid bus conflicts by disabling all outputs.

The digital logic requires 5 V on the DV_{CC} pin with respect to DGND. Internal ESD protection diodes require that the DGND and AGND pins be at the same potential.

SHORT-CIRCUIT OUTPUT CONDITIONS

Although there is short-circuit current protection on the ADV3205 outputs, the short-circuit output current can reach levels that can result in device failure. Do not operate the ADV3205 with a sustained short to ground on any of its outputs.

APPLICATIONS INFORMATION

The ADV3205 has two options for changing the programming of the crosspoint matrix. In the first option, a serial word of 80 bits can be provided that updates the entire matrix in one serial operation. The second option allows for changing the programming of a single output via a parallel interface. The serial option requires fewer signals but more time (clock cycles) for changing the programming, whereas the parallel programming technique requires more signals, but can change a single output at a time, and requires fewer clock cycles to complete programming.

SERIAL PROGRAMMING

The serial programming mode uses the device pins: $\overline{CE}$, CLK, DATA IN, $\overline{UPDATE}$, and $\overline{SER}$/PAR. The first step is to assert a low on $\overline{SER}$/PAR to enable the serial programming mode. $\overline{CE}$ for the chip must be low to allow data to be clocked into the device. The $\overline{CE}$ signal can be used to address an individual device when devices are connected in parallel.

The $\overline{UPDATE}$ signal should be high during the time that data is shifted into the serial port of the device. Although the data still shifts in when $\overline{UPDATE}$ is low, the transparent, asynchronous latches allow the shifting data to reach the matrix. This causes the matrix to try to update to every intermediate state as defined by the shifting data.

The data at DATA IN is clocked in at every down edge of CLK. A total of 80 bits must be shifted into the shift register via the DATA IN input to complete the programming. For each of the 16 outputs, there are four bits (D0 to D3) that determine the source of its input followed by one bit (D4) that determines the enabled state of the output. If D4 is low (output disabled), the four associated bits (D0 to D3) do not matter because no input is switched to that output.

The most significant output address data is shifted into the shift register first, following in sequence until the least significant output address data is shifted in. At this point $\overline{UPDATE}$ can be taken low, which causes the programming of the device according to the data that was just shifted in. The $\overline{UPDATE}$ registers are asynchronous, and when $\overline{UPDATE}$ is low (and $\overline{CE}$ is low), the registers are transparent.

When more than one ADV3205 device is serially programmed in a system, the DATA OUT signal from one device can be connected to the DATA IN of the next device to form a serial chain. Connect all of the CLK, $\overline{CE}$, $\overline{UPDATE}$, and $\overline{SER}$/PAR pins in parallel and operate them as previously described. The serial data is input to the DATA IN pin of the first device of the chain, and it ripples through to the last. Therefore, the data for the last device in the chain should come at the beginning of the programming sequence. The length of the programming sequence is 80 bits times the number of devices in the chain.

PARALLEL PROGRAMMING

When using the parallel programming mode, it is not necessary to reprogram the entire device when making changes to the matrix. In fact, parallel programming allows for the modification of a single output at a time. Because this takes only one CLK/$\overline{UPDATE}$ cycle, significant time savings can be realized by using parallel programming.

One important consideration in using parallel programming is that the $\overline{RESET}$ signal does not reset all registers in the ADV3205. When taken low, the $\overline{RESET}$ signal only sets each output to the disabled state. This is helpful during power-up to ensure that two parallel outputs are not active at the same time.

After initial power-up, the internal registers in the device generally contain random data, even though the $\overline{RESET}$ signal has been asserted. If parallel programming is used to program one output, that output is properly programmed but the rest of the device has a random program state depending on the internal register content at power-up. Therefore, when using parallel programming, it is essential that all outputs be programmed to a desired state after power-up. This ensures that the programming matrix is always in a known state. From then on, parallel programming can be used to modify a single output at a time.

In similar fashion, if both $\overline{CE}$ and $\overline{UPDATE}$ are taken low after initial power-up, the random power-up data in the shift register is programmed into the matrix. Therefore, to prevent the crosspoint from being programmed into an unknown state, do not apply low logic levels to both $\overline{CE}$ and $\overline{UPDATE}$ after power is initially applied. Programming the full shift register one time to a desired state, by either serial or parallel programming after initial power-up, eliminates the possibility of programming the matrix to an unknown state.

To change the output's programming via parallel programming, take $\overline{SER}$/PAR and $\overline{UPDATE}$ high and take $\overline{CE}$ low. The CLK signal should be in the high state. Put the 4-bit address of the output to be programmed on the A0 to A3 pins. The first four data bits (D0 to D3) should contain the information that identifies the input that is programmed to the output that is addressed. The fifth data bit (D4) determines the enabled state of the output. If D4 is low (output disabled), the data on D0 to D3 does not matter.

After the desired address and data signals are established, they can be latched into the shift register by a high-to-low transition of the CLK signal. The matrix is not programmed, however, until the $\overline{UPDATE}$ signal is taken low. It is thus possible to latch in new data for several or all of the outputs first via successive negative transitions of CLK while $\overline{UPDATE}$ is held high and then have all of the new data take effect when $\overline{UPDATE}$ goes low. Use this technique when programming the device for the first time after power-up when using parallel programming.

POWER-ON RESET

When powering up the ADV3205, it is usually desirable to have the outputs start up in the disabled state. The $\overline{\text{RESET}}$ pin, when taken low, causes all outputs to be in the disabled state. However, the $\overline{\text{RESET}}$ signal does not reset all registers in the ADV3205. This is important when operating in parallel programming mode. Refer to the Parallel Programming section for information about programming internal registers after power-up. Serial programming programs the entire matrix each time; therefore, no special considerations apply.

Because the data in the shift register is random after power-up, do not use it to program the matrix or the matrix can enter unknown states. To prevent this, do not apply logic low signals to both $\overline{\text{CE}}$ and $\overline{\text{UPDATE}}$ initially after power-up. First, load the shift register with the desired data, and then take $\overline{\text{UPDATE}}$ low to program the device.

The $\overline{\text{RESET}}$ pin has a 20 kΩ pull-up resistor to DV_{CC} that can be used to create a simple power-up reset circuit. A capacitor from $\overline{\text{RESET}}$ to ground holds $\overline{\text{RESET}}$ low for some time while the rest of the device stabilizes. The low condition causes all outputs to be disabled. The capacitor then charges through the pull-up resistor to the high state, thus allowing full programming capability of the device.

MANAGING VIDEO SIGNALS

Video signals often use controlled impedance transmission lines that are terminated in their characteristic impedance. Although this is not always the case, there are some considerations when using the ADV3205 to route video signals with controlled impedance transmission lines. Figure 29 shows a schematic of an input and output treatment of a typical video channel.

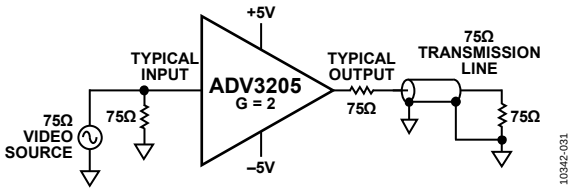


Figure 29. Video Signal Circuit

Video signals most often use 75 Ω transmission lines that need to be terminated with this value of resistance at each end. When such a source is delivered to one of the ADV3205 inputs, the high input impedance does not properly terminate these signals. Therefore, terminate the line with a 75 Ω shunt resistor to ground. Because video signals are limited in their peak-to-peak amplitude (typically no more than 1.5 V p-p), there is no need to attenuate video signals before they pass through the ADV3205.

The ADV3205 outputs are low impedance and do not properly terminate the source end of a 75 Ω transmission line. In these cases, insert a series 75 Ω resistor at an output that drives a video signal. Then terminate the 75 Ω transmission line with 75 Ω at its far end. This overall termination scheme divides the amplitude of the ADV3205 output by two. An overall unity-gain channel is produced because of the channel gain-of-two of the ADV3205.

CREATING LARGER CROSSPOINT ARRAYS

The ADV3205 is a high density building block for creating crosspoint arrays of dimensions larger than 16 × 16. Various features, such as output disable and chip enable, are useful for creating larger arrays.

The first consideration in constructing a larger crosspoint is to determine the minimum number of devices that are required. The 16 × 16 architecture of the ADV3205 contains 256 points, which is a factor of 64 greater than a 4 × 1 crosspoint (or multiplexer). The printed circuit board (PCB) area, power consumption, and design effort savings are readily apparent when compared to using these smaller devices.

For a nonblocking crosspoint, the number of points required is the product of the number of inputs multiplied by the number of outputs. Nonblocking requires that the programming of a given input to one or more outputs does not restrict the availability of that input to be a source for any other outputs.

Some nonblocking crosspoint architectures require more than this minimum as previously calculated. In addition, there are blocking architectures that can be constructed with fewer devices than this minimum. These systems have connectivity available on a statistical basis that is determined when designing the overall system.

The basic concept in constructing larger crosspoint arrays is to connect inputs in parallel in a horizontal direction and to wire-OR the outputs together in the vertical direction. The meaning of horizontal and vertical can best be understood by looking at a diagram. Figure 30 illustrates this concept for a 32 × 32 crosspoint array that uses four ADV3205 devices. Note that the 75 Ω source terminations are not shown on the outputs, but they are required when driving the 75 Ω transmission lines.

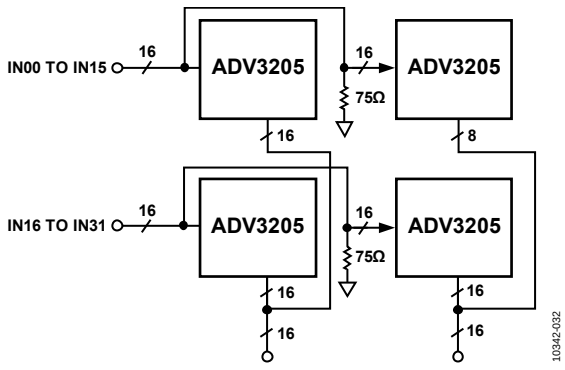


Figure 30. 32 × 32 Crosspoint Array Using Four ADV3205 Devices

The inputs are individually assigned to each of the 32 inputs of the two devices, and the shunt 75 Ω terminations are placed at the end of the transmission lines. The outputs are wire-OR'ed together in pairs. Only enable one of the outputs from a wire-ORed pair at any given time. The device programming software must be properly written to achieve this.

MULTICHANNEL VIDEO

The good video specifications of the ADV3205 make it an ideal candidate for creating composite video crosspoint switches. These switches can be made quite dense by taking advantage of the high level of integration of the ADV3205 and the fact that composite video requires only one crosspoint channel per system video channel. There are, however, other video formats that can be routed with the ADV3205, requiring more than one crosspoint channel per video channel.

Some systems use twisted pair wiring to carry video signals. These systems use differential signals and can lower costs because they use lower cost cables, connectors, and termination methods. They also have the ability to lower crosstalk and reject common-mode signals, which can be important for equipment that operates in noisy environments, or where common-mode voltages are present between transmitting and receiving equipment.

In such systems, the video signals are differential; there are positive and negative (or inverted) versions of the signals. These complementary signals are transmitted onto each of the two wires of the twisted pair, yielding a first-order zero common-mode voltage. At the receive end, the signals are differentially received and converted back into a single-ended signal.

When switching these differential signals, two channels are required in the switching element to handle the two differential signals that make up the video channel. Thus, one differential video channel is assigned to a pair of crosspoint channels, both input and output. For a single ADV3205, eight differential video channels can be assigned to the 16 inputs and 16 outputs. This effectively forms an 8 × 8 differential crosspoint switch.

Programming such a device requires that the inputs and outputs be programmed in pairs. This information can be deduced through inspection of the programming format of the ADV3205 and the requirements of the system.

There are other analog video formats requiring more than one analog circuit per video channel. One two-circuit format that is commonly being used in video systems is S-Video or Y/C Video. The Y/C Video format carries the brightness (luminance or Y) portion of the video signal on one channel and the color (chrominance, chroma, or C) on a second channel.

Because S-Video also uses two separate circuits for one video channel, creating a crosspoint system requires assigning one video channel to two crosspoint channels, as in the case of a differential video system. Aside from the nature of the video format, other aspects of these two systems are the same.

There are yet other video formats using three channels to carry the video information. Video cameras produce RGB (red, green, and blue) directly from the image sensors. RGB is also the usual format used by computers internally for graphics. RGB can also be converted to Y, R–Y, and B–Y format, sometimes called YUV format. These three circuit video standards are referred to as analog component video.

The analog component video standards require three crosspoint channels per video channel to handle the switching function. In a fashion similar to the two circuit video formats, the inputs and outputs are assigned in groups of three, and the appropriate logic programming is performed to route the video signals.

CROSSTALK

Many video systems have strict requirements for keeping the various signals from influencing any of the others in the system. Crosstalk is the term used to describe the coupling of the signals of other nearby channels to a given channel.

When there are many signals in proximity in a system, as is the case in a system that uses the ADV3205, the crosstalk issues can be quite complex. A good understanding of the nature of crosstalk and some definition of terms is required to specify a system that uses one or more ADV3205 devices.

Types of Crosstalk

Crosstalk can be propagated by means of any of three methods. These fall into the categories of electric field, magnetic field, and sharing of common impedances. This section explains these effects.

Every conductor can be both a radiator of electric fields and a receiver of electric fields. The electric field crosstalk mechanism occurs when the electric field created by the transmitter propagates across a stray capacitance (for example, free space) and couples with the receiver and induces a voltage. This voltage is an unwanted crosstalk signal in any channel that receives it.

Currents flowing in conductors create magnetic fields that circulate around the currents. These magnetic fields then generate voltages in any other conductors with whose paths they link. The undesired induced voltages in these other channels are crosstalk signals. The channels that crosstalk can be said to have a mutual inductance that couples signals from one channel to another.

The power supplies, grounds, and other signal return paths of a multichannel system are generally shared by the various channels. When a current from one channel flows in one of these paths, a voltage that is developed across the impedance becomes an input crosstalk signal for other channels that share the common impedance.

All these sources of crosstalk are vector quantities; therefore, the magnitudes cannot simply be added together to obtain the total crosstalk. In fact, there are conditions where driving additional circuits in parallel in a given configuration can actually reduce the crosstalk.

Areas of Crosstalk

A practical ADV3205 circuit must be mounted to some sort of circuit board to connect it to power supplies and measurement equipment. This, however, raises the issue that the crosstalk of a system is a combination of the intrinsic crosstalk of the devices in addition to the circuit board to which they are mounted. It is important to try to separate these two areas when attempting to minimize the effect of crosstalk.

In addition, crosstalk can occur among the inputs to a crosspoint and among the outputs. It can also occur from input to output. Techniques are presented in the following sections for diagnosing which part of a system is contributing to crosstalk, as well as minimizing crosstalk.

Measuring Crosstalk

Crosstalk is measured by applying a signal to one or more channels and measuring the relative strength of that signal on a desired selected channel. The measurement is usually expressed as dB down from the magnitude of the test signal. The crosstalk is expressed by

$$|XT| = 20\log_{10}(Asel(s)/Atest(s))$$

where:
$s = jw$, the Laplace transform variable.
Asel(s) is the amplitude of the crosstalk induced signal in the selected channel.
Atest(s) is the amplitude of the test signal.

It can be seen that crosstalk is a function of frequency, but not a function of the magnitude of the test signal (to the first order). In addition, the crosstalk signal has a phase relative to the test signal associated with it.

A network analyzer is most commonly used to measure crosstalk over a frequency range of interest. It can provide both magnitude and phase information about the crosstalk signal.

As a crosspoint system or device grows larger, the number of theoretical crosstalk combinations and permutations can become extremely large. For example, in the case of the 16 × 16 matrix of the ADV3205, note the number of crosstalk terms that can be considered for a single channel, such as the IN00 input. IN00 is programmed to connect to one of the ADV3205 outputs where the measurement can be made.

First, the crosstalk terms associated with driving a test signal into each of the other 15 inputs can be measured one at a time, while applying no signal to IN00. Then, the crosstalk terms associated with driving a parallel test signal into all 15 other inputs can be measured two at a time in all possible combinations, then three at a time, and so on, until finally, there is only one way to drive a test signal into all 15 other inputs in parallel.

Each of these cases is legitimately different from the others and may yield a unique value, depending on the resolution of the measurement system, but it is hardly practical to measure all these terms and then specify them. In addition, this describes the crosstalk matrix for just one input channel. A similar crosstalk matrix can be proposed for every other input. In addition, if the possible combinations and permutations for connecting inputs to the other outputs (not used for measurement) are taken into consideration, the numbers grow impractically large. If a larger crosspoint array of multiple ADV3205 devices is constructed, the numbers grow larger still.

Clearly, some subset of all these cases must be selected to be used as a guide for a practical measure of crosstalk. One common method is to measure all hostile crosstalk; this means that the crosstalk to the selected channel is measured while all other system channels are driven in parallel. In general, this yields the worst crosstalk number, but this is not always the case, due to the vector nature of the crosstalk signal.

Other useful crosstalk measurements are those that are created by one nearest neighbor or by the two nearest neighbors on either side. These crosstalk measurements are generally higher than those of more distant channels, so they can serve as a worst-case measure for any other 1-channel or 2-channel crosstalk measurements.

Input and Output Crosstalk

The flexible programming capability of the ADV3205 can be used to diagnose whether crosstalk is occurring more on the input side or the output side. Some examples are illustrative. A given input channel (IN07 in the middle for this example) can be programmed to drive OUT07 (also in the middle). The input to IN07 is just terminated to ground (via 50 Ω or 75 Ω) and no signal is applied.

All the other inputs are driven in parallel with the same test signal (provided by a distribution amplifier), with all other outputs except OUT07 disabled. Because grounded IN07 is programmed to drive OUT07, no signal should be present. Any signal that is present can be attributed to the other 15 hostile input signals because no other outputs are driven (they are all disabled). Thus, this method measures the all-hostile input contribution to crosstalk into IN07. Of course, the method can be used for other input channels and combinations of hostile inputs.

For output crosstalk measurement, a single input channel is driven (IN00, for example) and all outputs other than a given output (IN07 in the middle) are programmed to connect to IN00. OUT07 is programmed to connect to IN15 (far away from IN00), which is terminated to ground. Therefore, OUT07 should not have a signal present because it is listening to a quiet input. Any signal measured at OUT07 can be attributed to the output crosstalk of the other 16 hostile outputs. Again, this method can be modified to measure the other channels and the other crosspoint matrix combinations.

Effect of Impedances on Crosstalk

The input side crosstalk can be influenced by the output impedance of the sources that drive the inputs. The lower the impedance of the drive source, the lower the magnitude of the crosstalk. The dominant crosstalk mechanism on the input side is capacitive coupling. The high impedance inputs do not have significant current flow to create magnetically induced crosstalk. However, significant current can flow through the input termination resistors and the loops that drive them. Thus, the PCB on the input side can contribute to magnetically coupled crosstalk.

From a circuit standpoint, the input crosstalk mechanism is similar to a capacitor coupling to a resistive load. For low frequencies, the magnitude of the crosstalk is given by

$$|XT| = 20\log_{10}[(R_S C_M) \times s]$$

where:
R_S is the source resistance.
C_M is the mutual capacitance between the test signal circuit and the selected circuit.
s is the Laplace transform variable.

From the previous equation, it can be observed that this crosstalk mechanism has a high-pass nature; it can also be minimized by reducing the coupling capacitance of the input circuits and lowering the output impedance of the drivers. If the input is driven from a 75 Ω terminated cable, the input crosstalk can be reduced by buffering this signal with a low output impedance buffer.

On the output side, the crosstalk can be reduced by driving a lighter load. Although the ADV3205 is specified with excellent differential gain and phase when driving a standard 150 Ω video load, the crosstalk is higher than the minimum obtainable due to the high output currents. These currents induce crosstalk via the mutual inductance of the output pins and bond wires of the ADV3205.

From a circuit standpoint, this output crosstalk mechanism is similar to a transformer with a mutual inductance between the windings that drives a load resistor. For low frequencies, the magnitude of the crosstalk is given by

$$|XT| = 20\log_{10}(Mxy \times s/R_L)$$

where:
Mxy is the mutual inductance of Output X to Output Y.
R_L is the load resistance on the measured output.

This crosstalk mechanism can be minimized by keeping the mutual inductance low and increasing R_L. The mutual inductance can be kept low by increasing the spacing of the conductors and minimizing their parallel lengths.

PCB Layout

Extreme care must be exercised to minimize additional crosstalk generated by the system circuit board(s). The areas that must be carefully detailed are grounding, shielding, signal routing, and supply bypassing.

The packaging of the ADV3205 is designed to keep the crosstalk to a minimum. Each input is separated from every other input by an analog ground pin. Directly connect all AGND pins to the ground plane of the circuit board. These ground pins provide shielding, low impedance return paths, and physical separation for the inputs. All of these help to reduce crosstalk.

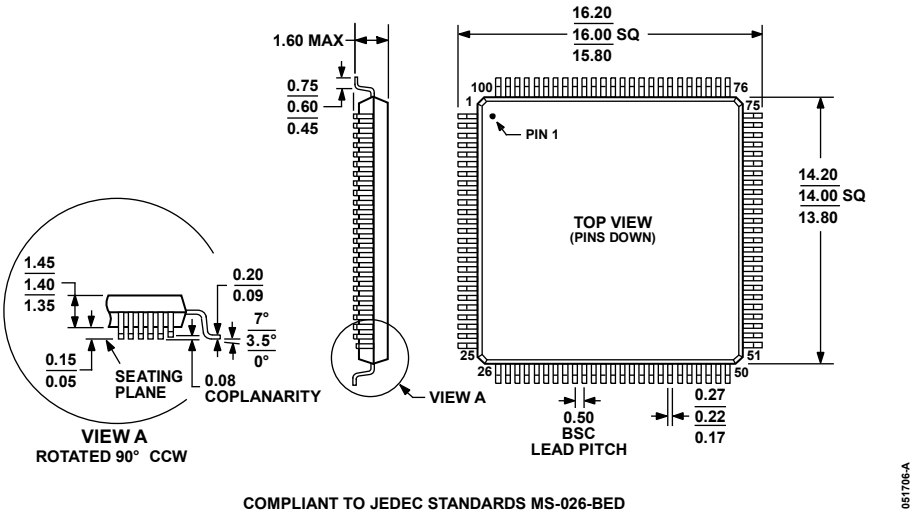
Each output is separated from its two neighboring outputs by an analog supply pin of one polarity or the other. Each of these analog supply pins provides power to the output stages of only the two nearest outputs. These supply pins provide shielding, physical separation, and a low impedance supply for the outputs. Individual bypassing of each of these supply pins with a 0.1 µF chip capacitor directly to the ground plane minimizes high frequency output crosstalk via the mechanism of shared common impedances.

Each output also has an on-chip compensation capacitor that is individually tied to the nearby analog ground pins. This technique reduces crosstalk by preventing the currents that flow in these paths from sharing a common impedance on the IC and in the package pins. Directly connect these AGND pins to the ground plane.

There are separate digital (logic) and analog supplies. DV_{CC} must be at 5 V to be compatible with the 5 V CMOS and TTL logic. AV_{CC} and AV_{EE} can range from ±5 V to ±12 V, depending on the application.

Locally decouple each power supply pin (or group of adjacent power supply pins) with a 0.1 µF capacitor. Use a 10 µF capacitor to decouple power supplies as they come onto the board.

OUTLINE DIMENSIONS



COMPLIANT TO JEDEC STANDARDS MS-026-BED

Figure 31. 100-Lead Low Profile Quad Flat Package [LQFP]
(ST-100-1)
Dimensions shown in millimeters

ORDERING GUIDE

Model[1]	Temperature Range	Package Description	Package Option
ADV3205JSTZ	0°C to 70°C	100-Lead Low Profile Quad Flat Package [LQFP]	ST-100-1
ADV3205-EVALZ		Evaluation Board	

[1] Z = RoHS Compliant Part.

D10342-0-12/11(0)

Mouser Electronics

Authorized Distributor

Click to View Pricing, Inventory, Delivery & Lifecycle Information:

Analog Devices Inc.:

ADV3205JSTZ