Dual Downconverter with DVGA and PLL/VCO, 450 MHz to 2700 MHz

Data Sheet

ADRF6650

FEATURES

Dual down-converter with integrated fractional-N PLL/VCO
RF: 450 MHz to 2700 MHz continuous
LO frequency: 450 MHz to 2900 MHz, high-side or low-side injection
43 dB gain control range
Gain control with up/down and SPI
Integrated RF balun for single-ended 50 Ω inputs
Power supply: 3.3 and 5 V
8 mm × 8 mm, 56-lead LFCSP package

APPLICATIONS

Multiband/multistandard cellular base station diversity receivers
Wideband radio link diversity downconverters
Multimode cellular extenders and picocells

GENERAL DESCRIPTION

The ADRF6650 is a highly integrated downconverter that integrates dual mixers, dual digital switched attenuators, dual digital variable gain amplifiers, a phase-locked loop (PLL), and voltage controlled oscillators (VCOs). In addition, the ADRF6650 integrates two radio frequency (RF) baluns, serial gain control (SGC) controls, and fast enable inputs for time division duplex (TDD) operation.

The on-chip RF baluns enable the ADRF6650 to support 50 Ω terminated RF inputs. The integrated passive mixer provides a highly linear downconversion for a 200 MHz, sliding, intermediate frequency (IF) window. The ADRF6650 uses broadband square wave limiting local oscillator (LO) amplifiers to achieve an RF bandwidth of 450 MHz to 2700 MHz. Unlike conventional narrow-band sine wave LO amplifier solutions, this amplifier permits the LO to be applied either above or below the RF input over an extremely wide bandwidth.

The ADRF6650 offers two alternatives for generating the differential LO input signal: internally via the on-chip fractional-N synthesizer with low phase noise VCOs, or externally via a low phase noise LO signal. The integrated PLL/VCO enables continuous LO coverage from 450 MHz to 2900 MHz. The PLL reference input supports a wide frequency range and includes integrated reference dividers before the phase frequency detector (PFD).

The ADRF6650 is fabricated using an advanced silicon-germanium (SiGe) bipolar complementary metal-oxide semiconductor (BiCMOS) process. It is available in a 56-lead, RoHS-compliant, 8 mm × 8 mm, lead frame chip scale package (LFCSP) package with an exposed pad. Performance is specified over the −40°C to +105°C maximum paddle temperature.

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REVISION HISTORY

11/2019—Revision A

FUNCTIONAL BLOCK DIAGRAM

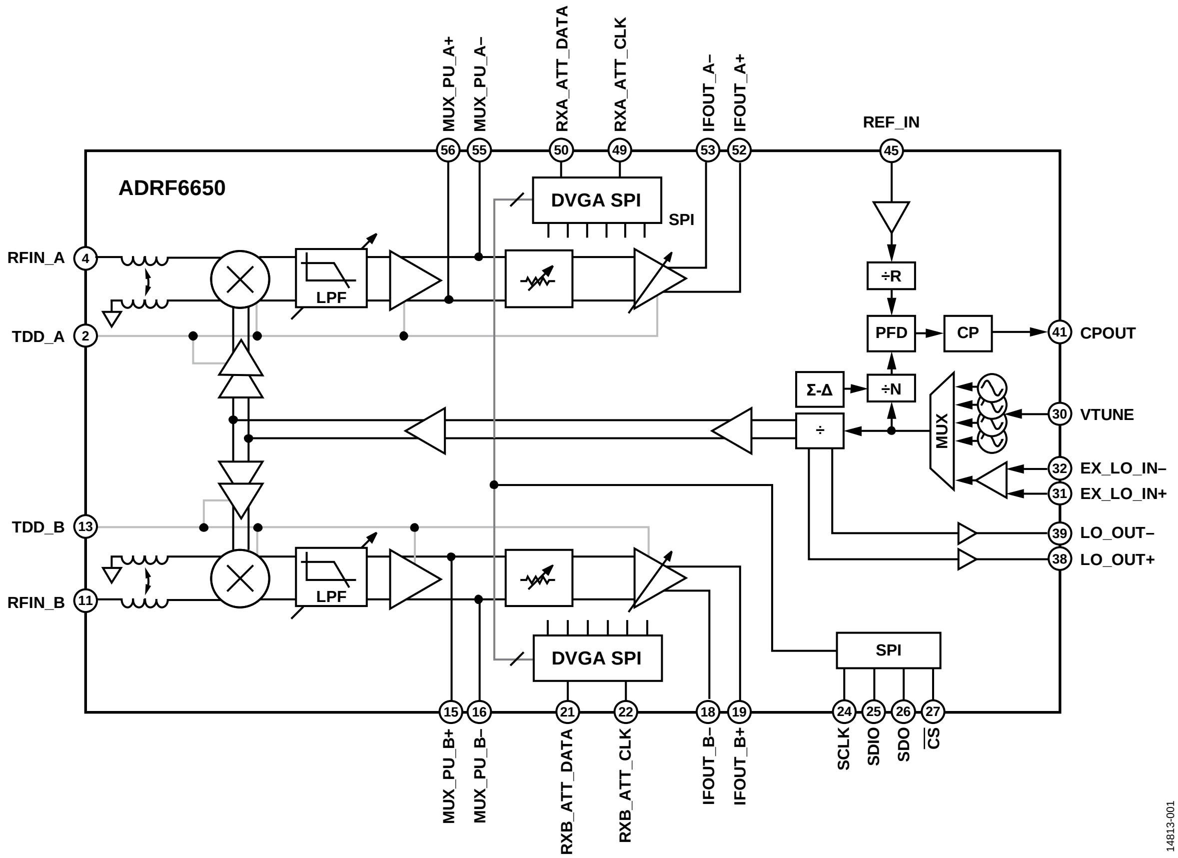

Figure 1.

SPECIFICATIONS

VCC_DVGA_A/VCC_DVGA_B = 5 V, remaining supplies = 3.3 V, T_A = 25°C, low-side LO injection, f_{IF} = 184 MHz, internal LO, maximum gain setting, 5 V high performance settings, unless otherwise noted. All losses from input and output traces and baluns are de-embedded from results.

Table 1.

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
RF INPUT INTERFACE					
Return Loss	RFIN_A/RFIN_B internally matched to 50 Ω		−10		dB
Input Impedance			50		Ω
RF Frequency Range		450		2700	MHz
IF OUTPUT INTERFACE					
Return loss	IF output with 100 Ω differential load (25 Ω external resistors are required on each differential output pin)		−10		dB
Output Impedance	Differential impedance		10		Ω
LO INPUT INTERFACE	External LO operation, differential				
Required Input Power		−6		+6	dBm
Input Impedance			100		Ω
Return Loss			−10		dB
Frequency Range	Low-side or high-side LO	450		2900	MHz
LO OUTPUT INTERFACE	Differential				
Power[1]	TRM_XLODRV_DRV_POUT = 01				
f_{LO} = 900 MHz			0		dBm
f_{LO} = 1800 MHz			1		dBm
f_{LO} = 2700 MHz			0		dBm
Output Impedance			50		Ω
Return Loss			−10		dB
Frequency Range	Low-side or high-side LO	450		2900	MHz
POWER SUPPLY					
VCC_DVGA_A and VCC_DVGA_B[2]	5 V mode	4.75	5.0	5.25	V
	3.3 V mode	3.1	3.3	3.5	V
PLL/VCO Supplies[3]		3.2	3.3	3.4	V
RF and IF Supplies		3.1	3.3	3.5	V
POWER CONSUMPTION	Total				
f_{LO} = 1050 MHz	Internal LO		2.6		W
	Internal LO, auxiliary LO output buffer disabled		2.4		W
f_{LO} = 1565 MHz	Internal LO		2.7		W
	Internal LO, auxiliary LO output buffer disabled		2.5		W
f_{LO} = 2350 MHz	Internal LO		2.6		W
	Internal LO, auxiliary LO output buffer disabled		2.47		W

[1] For details on LO output power setting, see the LO Generation Block section.
[2] For the 3.3 V DVGA supply option, see the Applications Information section.
[3] Design practices for the best noise performance are discussed in the Applications Information section.

RF INPUT TO IF OUTPUT SYSTEM SPECIFICATIONS

VCC_DVGA_A/VCC_DVGA_B = 5 V, remaining supplies = 3.3 V, T_A = 25°C, low-side LO injection, f_{IF} = 184 MHz, internal LO, maximum gain setting, 5 V high performance settings, unless otherwise noted. All losses from input and output traces and baluns are de-embedded from results.

Table 2.

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
DYNAMIC PERFORMANCE AT RF Frequency (f_{RF}) = 900 MHz	High-side LO				
Power Gain			30		dB
Output 1 dB Compression Point (OP1dB)	Maximum gain		16		dBm
	Gain = 1 dB		8		dBm
Output Third-Order Intercept Point (OIP3)	Output power (P_{OUT}) = −4 dBm/tone, 1 MHz to 40 MHz separation		44		dBm
	Maximum gain minus 16 dB, P_{OUT} = −4 dBm/tone, 1 MHz to 40 MHz separation		38		dBm
Noise Figure	Maximum gain and maximum gain minus 5 dB		9.5		dB
Noise Figure Under Blocker	Internal LO, 3 MHz offset blocking, P_{IN} = 0 dBm, P_{OUT} = 1 dBm		21		dB
Second Harmonic Distortion (HD2)	P_{IN} = 0 dBm, P_{OUT} = 1 dBm		−66.7		dBc
Third Harmonic Distortion (HD3)	P_{IN} = 0 dBm, P_{OUT} = 1 dBm		−58		dBc
LO to IF Leakage			−22.5		dBm
LO to RF Leakage			−54		dBm
RF to IF Leakage			−46		dBc
Isolation	Channel to channel		52		dBc
DYNAMIC PERFORMANCE AT f_{RF} = 1800 MHz	Low-side LO				
Power Gain			29		dB
OP1dB	Maximum gain		16		dBm
	Gain = 1 dB		9		dBm
OIP3	P_{OUT} = −4 dBm/tone, 1 MHz to 40 MHz separation		43		dBm
	Maximum gain minus 16 dB, P_{OUT} = −4 dBm/tone, 1 MHz to 40 MHz separation		41		dBm
Noise Figure	Maximum gain and maximum gain minus 5 dB		11		dB
Noise Figure Under Blocker	Internal LO, 3 MHz offset blocking, input power (P_{IN}) = 0 dBm, P_{OUT} = 1 dBm		22.5		dB
HD2	P_{IN} = 0 dBm, P_{OUT} = 1 dBm		−75		dBc
HD3	P_{IN} = 0 dBm, P_{OUT} = 1 dBm		−67		dBc
LO to IF Leakage			−37.5		dBm
LO to RF Leakage			−55		dBm
RF to IF Leakage			−68		dBc
Isolation	Channel to channel		50		dBc
DYNAMIC PERFORMANCE AT f_{RF} = 2700 MHz	High-side LO				
Power Gain			29		dB
OP1dB	Maximum gain		16		dBm
	Gain = 1 dB		9		dBm
OIP3	P_{OUT} = −4 dBm/tone, 1 MHz to 40 MHz separation		43.5		dBm
	Maximum gain minus 16 dB, P_{OUT} = −4 dBm/tone, 1 MHz to 40 MHz separation		40		dBm
Noise Figure	Maximum gain and maximum gain minus 5 dB		11.5		dB
Noise Figure Under Blocker	Internal LO, 3 MHz offset blocking, P_{IN} = 0 dBm, P_{OUT} = 1 dBm		23.5		dB
HD2	P_{IN} = 0 dBm, P_{OUT} = 1 dBm		−59		dBc
HD3	P_{IN} = 0 dBm, P_{OUT} = 1 dBm		−63		dBc
LO to IF Leakage			−43		dBm
LO to RF Leakage			−46		dBm
RF to IF Leakage			−81		dBc
Isolation	Channel to channel		57		dBc

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
MxN SPURS	See the Spurious Performance section				
RF TO IF DELAY DIFFERENCE BETWEEN CHANNELS	Channel A = 5 dB attenuation, Channel B sweep attenuation from 0 dB to 40 dB		1		ns
TDD SWITCH TIME	Level sensitive, from effective level of control signal to 99%/1% of final RF signal level; the amplitude response, phase response, and group delay must all be settled in this time interval		1	2	µs

GAIN CONTROL SPECIFICATIONS

Table 3.

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
GAIN ADJUSTMENT					
Range			43		dB
Step			1		dB
Gain Step Error	Between any two adjacent steps		±0.2		dB
Cumulative Gain Error	Error vs. line (maximum gain reference)		1		dB
Phase Error	f_{RF} = 200 MHz and with 20 dB gain change		10		Degrees
Gain Adjustment Setting Time	At any gain settings, this specification must be met with any gain adjustment between 1 dB to 16 dB and the output power settled within ±1 dB of the final value		15		ns
Gain Adjustment Setting Time	At any gain settings, this specification must be met with any gain adjustment between 1 dB to 16 dB and the output power settled within ±0.1 dB of the final value		70		ns

PLL/VCO SPECIFICATIONS

VCC_x and VCC_DVGA_A/VCC_DVGA_B = 5 V, remaining supplies = 3.3 V, T_A = 25°C, f_{REF} = 122.88 MHz, f_{REF} power = 2.5 V p-p, PFD frequency (f_{PFD}) = 30.72 MHz, charge pump current setting of 7, and loop filter bandwidth = 20 kHz, unless otherwise noted.

Table 4.

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
PLL REFERENCE					
PLL Reference Frequency		10	30.72	250	MHz
PLL Reference Level	For PLL lock condition, 50 Ω to ground required close to REF_IN pin	0.7		3.3	V p-p
Step Size			240		kHz
Lock Time			0.4		ms
PFD FREQUENCY			30.72	61.44	MHz
INTERNAL VCO RANGE		4000		8000	MHz
OPEN-LOOP VCO PHASE NOISE					
VCO Frequency (f_{VCO}) = 4200 MHz	10 kHz offset		−86		dBc/Hz
	100 kHz offset		−112		dBc/Hz
	1 MHz offset		−133		dBc/Hz
	10 MHz offset		−153		dBc/Hz
f_{VCO} = 4700 MHz	10 kHz offset		−84		dBc/Hz
	100 kHz offset		−112		dBc/Hz
	1 MHz offset		−134		dBc/Hz
	10 MHz offset		−154		dBc/Hz
f_{VCO} = 5440 MHz	10 kHz offset		−83		dBc/Hz
	100 kHz offset		−110		dBc/Hz
	1 MHz offset		−132		dBc/Hz
	10 MHz offset		−152		dBc/Hz

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
f_{VCO} = 6260 MHz	10 kHz offset		−82		dBc/Hz
	100 kHz offset		−108		dBc/Hz
	1 MHz offset		−130		dBc/Hz
	10 MHz offset		−150		dBc/Hz
f_{VCO} = 7060 MHz	10 kHz offset		−80		dBc/Hz
	100 kHz offset		−106		dBc/Hz
	1 MHz offset		−127		dBc/Hz
	10 MHz offset		−147		dBc/Hz
SYNTHESIZER SPECIFICATIONS					
Fractional Figure of Merit (FOM)			−227		dBc/Hz
Flicker FOM			−262		dBc/Hz
f_{PFD} Spurs[1]	At the input of internal mixer and daisy-chained ADRF6650 mixer				
$f_{PFD} \times 1$			−90		dBc
$f_{PFD} \times 2$			−95		dBc
$f_{PFD} \times 3$ and Higher			−95		dBc
Unwanted Spurs (Other Than PFD and Harmonics)[1]	At the input of internal mixer and daisy-chained ADRF6650 mixer		−70		dBc
LO Frequency (f_{LO}) = 1050 MHz, f_{VCO} = 4200 MHz					
Closed-Loop Phase Noise	1 kHz offset		−110		dBc/Hz
	10 kHz offset		−107		dBc/Hz
	100 kHz offset		−122		dBc/Hz
	600 kHz offset		−141		dBc/Hz
	800 kHz offset		−143		dBc/Hz
	1.6 MHz offset		−149		dBc/Hz
	3 MHz offset		−153		dBc/Hz
	10 MHz offset		−157		dBc/Hz
	100 MHz offset		−159		dBc/Hz
Integrated Phase Noise and Spurs	100 Hz to 10 MHz integration bandwidth		0.08		°rms
f_{LO} = 1565 MHz, f_{VCO} = 6260 MHz					
Closed-Loop Phase Noise	1 kHz offset		−106		dBc/Hz
	10 kHz offset		−102		dBc/Hz
	100 kHz offset		−119		dBc/Hz
	600 kHz offset		−137		dBc/Hz
	800 kHz offset		−140		dBc/Hz
	1.6 MHz offset		−145		dBc/Hz
	3 MHz offset		−151		dBc/Hz
	10 MHz offset		−156		dBc/Hz
	100 MHz offset		−157		dBc/Hz
Integrated Phase Noise and Spurs	100 Hz to 10 MHz integration bandwidth		0.13		°rms
f_{LO} = 1765 MHz, f_{VCO} = 7060 MHz					
Closed-Loop Phase Noise	1 kHz offset		−102		dBc/Hz
	10 kHz offset		−97		dBc/Hz
	100 kHz offset		−117		dBc/Hz
	950 kHz offset		−138		dBc/Hz
	2.1 MHz offset		−145		dBc/Hz
	3.5 MHz offset		−149		dBc/Hz
	7.5 MHz offset		−153		dBc/Hz
	10 MHz offset		−156		dBc/Hz
	100 MHz offset		−158		dBc/Hz
Integrated Phase Noise and Spurs	100 Hz to 10 MHz integration bandwidth		0.2		°rms

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
f_{LO} = 2350 MHz, f_{VCO} = 4700 MHz					
Closed-Loop Phase Noise	1 kHz offset		−103		dBc/Hz
	10 kHz offset		−101		dBc/Hz
	100 kHz offset		−116		dBc/Hz
	950 kHz offset		−140		dBc/Hz
	2.1 MHz offset		−147		dBc/Hz
	3.5 MHz offset		−151		dBc/Hz
	7.5 MHz offset		−156		dBc/Hz
	10 MHz offset		−156		dBc/Hz
	100 MHz offset		−157		dBc/Hz
Integrated Phase Noise and Spurs	100 Hz to 10 MHz integration bandwidth		0.16		°rms
f_{LO} = 2720 MHz, f_{VCO} = 5440 MHz					
Closed-Loop Phase Noise	1 kHz offset		−102		dBc/Hz
	10 kHz offset		−99		dBc/Hz
	100 kHz offset		−114		dBc/Hz
	950 kHz offset		−137		dBc/Hz
	2.1 MHz offset		−144		dBc/Hz
	3.5 MHz offset		−148		dBc/Hz
	7.5 MHz offset		−153		dBc/Hz
	10 MHz offset		−155		dBc/Hz
	100 MHz offset		−156		dBc/Hz
Integrated Phase Noise and Spurs	100 Hz to 10 MHz integration bandwidth		0.2		°rms

[1] Auxiliary LO output measurements are performed under daisy-chain configuration with another ADRF6650 device. Measurements are taken from the auxiliary LO output of the daisy-chained ADRF6650.

DIGITAL LOGIC SPECIFICATIONS

Table 5.

Parameter	Symbol	Test Conditions/Comments	Min	Typ	Max	Unit
ALL DIGITAL INPUTS/OUTPUTS						
Input Voltage						
Logic Low	V_{IL}		0		0.5	V
Logic High	V_{IH}		1.2		3.6	V
Input Current						
Logic High	I_{IH}		−100		+100	µA
Logic Low	I_{IL}		−100		+100	µA
Output Voltage						
Logic Low	V_{OL}		0		0.4	V
Logic High	V_{OH}	When driving loads with complementary metal-oxide semiconductor (CMOS) 1.8 V interface	1.4		1.8	V
		When driving loads with CMOS 3.3 V interface	2.4		3.3	V
Output Driving Current						
Logic High	I_{OH}			1	2	mA
Logic Low	I_{OL}			1	2	mA

Serial Peripheral Interface (SPI) Timing

Table 6.

Parameter	Description	Min	Typ	Max	Unit
t_{DS}	SDI to SCLK rising edge setup	8			ns
t_{DH}	SCLK rising edge to SDI hold	8			ns
t_{CLK}	Period of SCLK	50			ns
t_{HIGH}	High width of SCLK	25			ns
t_{LOW}	Low width of SCLK	25			ns
t_S	$\overline{CS}$ falling edge to SCLK rising edge, setup time	10			ns
t_C	SCLK rising edge to $\overline{CS}$ rising edge, hold time	30			ns
t_{DV}	SCLK falling edge to valid readback data, SDIO/SDO; not shown in Figure 2	18			ns

SPI Timing Diagram

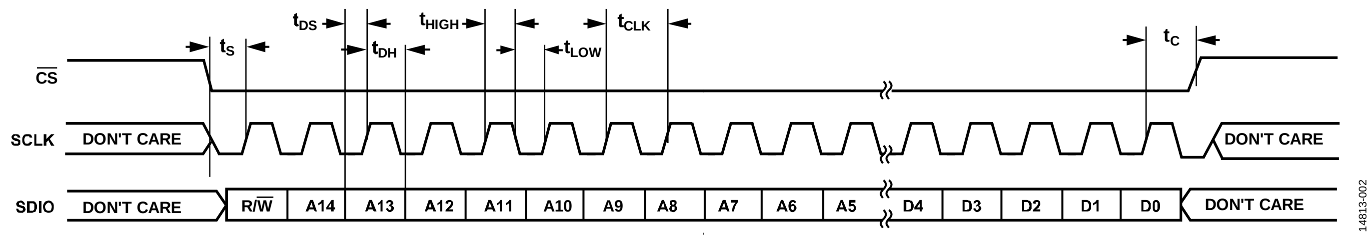

Figure 2. Serial Control Port Write Timing—MSB First, 16-Bit Instruction

ABSOLUTE MAXIMUM RATINGS

Table 7.

Parameter	Rating
VCC_MIX_A, VCC_LOA_S2, VCC_LOA_S1, VCC_LOB_S1, VCC_LOB_S2, VCC_MIX_B, MIX_PU_A+, MIX_PU_A−, MIX_PU_B+, MIX_PU_B−	−0.3 V to +3.6 V
VCC_DVGA_B, VCC_DVGA_A	−0.3 V to +5.4 V
VCCVCO_3V3, VCCDIV_3V3, VCCFBDIV_3V3, VCCLO_MIX_3V3, VCCLO_AUX_3V3, VCCCP_3V3, VCCPFD_3V3, VCCREF_3V3, VBAT_DIG_3V3	−0.3 V to +3.6 V
RF Input Power (RFIN_A, RFIN_B)	20 dBm
External LO Input Power	10 dBm differential
VTUNE, CPOUT, REF_IN, DCL_BIAS	−0.3 V to +3.6 V
TDD_A, TDD_B, RXA_ATT_CLK, RXA_ATT_DATA, RXB_ATT_CLK, RXB_ATT_DATA	−0.3 V to +3.6 V
SCLK, SDIO, SDO, $\overline{\text{CS}}$	−0.3 V to +3.6 V
Maximum Junction Temperature	125°C
Operating Temperature Range (Measured at Pad)	−40°C to +105°C
Storage Temperature Range	−65°C to +150°C

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

THERMAL RESISTANCE

Thermal performance is directly linked to printed circuit board (PCB) design and operating environment. Careful attention to PCB thermal design is required.

Typical θ_{JA} and θ_{JC} are specified vs. the number of PCB layers. The use of appropriate thermal management techniques is recommended to ensure that the maximum junction temperature does not exceed the limits shown in Table 7.

Table 8. Thermal Resistance

Package Type	θ_{JA}	θ_{JC}	Unit
CP-56-16[1]			
JEDEC 1s0p Board[2]	N/A[4]	3.3	°C/W
Cold Plate Only, No PCB[3]	N/A[4]	2.8	°C/W
JEDEC 2s2p Board[2]	29.3	N/A	°C/W

[1] The maximum junction temperature of 125°C cannot be exceeded.
[2] Per JEDEC JESD51-12.
[3] For nonstandardized testing where the paddle of the device is directly connected to a cold plate. This approach can be useful to estimate junction temperature when the exact paddle temperature is known in the application.
[4] N/A means not applicable.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

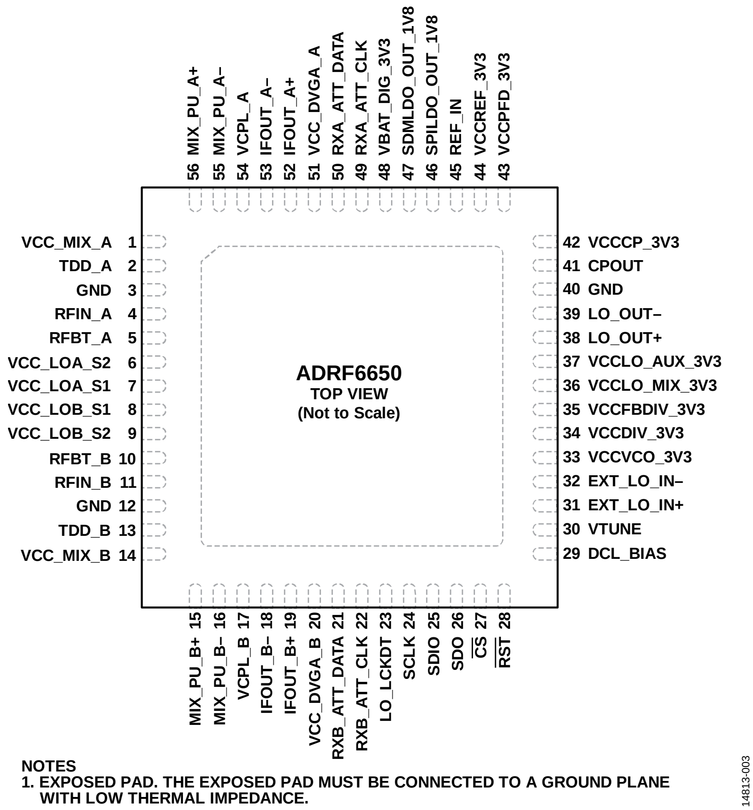

Figure 3. Pin Configuration

Table 9. Pin Function Descriptions

Pin No.	Mnemonic	Description
1	VCC_MIX_A	Channel A Mixer IF Amplifier V_{CC}.
2	TDD_A	TDD Enable, Channel A.
3	GND	Ground.
4	RFIN_A	Channel A Single-Ended, RF, 50 Ω Input.
5	RFBT_A	Channel A RF Balun Low Frequency Inductor Connection.
6	VCC_LOA_S2	Channel A LO Path V_{CC} (Stage 3 and Stage 4).
7	VCC_LOA_S1	Channel A LO Path V_{CC} (Stage 1 and Stage 2).
8	VCC_LOB_S1	Channel B LO Path V_{CC} (Stage 1 and Stage 2).
9	VCC_LOB_S2	Channel B LO Path V_{CC} (Stage 3 and Stage 4).
10	RFBT_B	Channel B RF Balun Low Frequency Inductor Connection.
11	RFIN_B	Channel B Single-Ended, RF, 50 Ω Input.
12	GND	Ground.
13	TDD_B	TDD Enable, Channel B.
14	VCC_MIX_B	Channel B Mixer IF Amplifier V_{CC}.
15	MIX_PU_B+	Channel B Mixer IF Amplifier Positive Output Pull-Up.
16	MIX_PU_B–	Channel B Mixer IF Amplifier Negative Output Pull-Up.
17	VCPL_B	Channel B Variable Gain Amplifier (VGA) Decouple Output.
18	IFOUT_B–	Channel B VGA Negative Output.
19	IFOUT_B+	Channel B VGA Positive Output.
20	VCC_DVGA_B	Channel B Digital Step Attenuator (DSA) and VGA V_{CC}.
21	RXB_ATT_DATA	Channel B VGA Serial Gain Control (Up/Down) Data.
22	RXB_ATT_CLK	Channel B VGA Serial Gain Control (Up/Down) Clock.
23	LO_LCKDT	LO Lock Detect.
24	SCLK	SPI Clock.

Pin No.	Mnemonic	Description
25	SDIO	SPI Data Input/Output (3-Wire Mode); Input Only (4-Wire Mode).
26	SDO	SPI Data Output (4-Wire Mode); Not Used (3-Wire Mode).
27	$\overline{\text{CS}}$	SPI Chip Select (Active Low).
28	$\overline{\text{RST}}$	Reset (Active Low).
29	DCL_BIAS	VCO Core Bias Decouple Output.
30	VTUNE	Tuning Voltage (V_{TUNE}) Input.
31	EXT_LO_IN+	External LO Positive Input.
32	EXT_LO_IN−	External LO Negative Input.
33	VCCVCO_3V3	VCO 3.3 V Supply.
34	VCCDIV_3V3	LO Chain and Divider 3.3 V Supply.
35	VCCFBDIV_3V3	PLL Feedback Divider 3.3 V Supply.
36	VCCLO_MIX_3V3	LO Mixer Output Buffer 3.3 V Supply.
37	VCCLO_AUX_3V3	LO External Output Buffer 3.3 V Supply.
38	LO_OUT+	External LO Positive Output.
39	LO_OUT−	External LO Negative Output.
40	GND	Charge Pump GND.
41	CPOUT	Charge Pump Output.
42	VCCCP_3V3	Charge Pump 3.3 V Supply.
43	VCCPFD_3V3	PFD 3.3 V Supply.
44	VCCREF_3V3	Reference Input Buffer 3.3 V Supply.
45	REF_IN	Reference Input Buffer.
46	SPILDO_OUT_1V8	SPI 1.8 V LDO External Decouple Output.
47	SDMLDO_OUT_1V8	SDM 1.8 V LDO External Decouple Output.
48	VBAT_DIG_3V3	SPI and SDM LDO 3.3 V Supply.
49	RXA_ATT_CLK	Channel A VGA Serial Gain Control (Up/Down) Clock.
50	RXA_ATT_DATA	Channel A VGA Serial Gain Control (Up/Down) Data.
51	VCC_DVGA_A	Channel A DSA and VGA V_{CC}.
52	IFOUT_A+	Channel A VGA Positive Output.
53	IFOUT_A−	Channel A VGA Negative Output.
54	VCPL_A	Channel A VGA Decouple Output.
55	MIX_PU_A−	Channel A Mixer Amplifier Negative Output Pull-Up.
56	MIX_PU_A+	Channel A Mixer Amplifier Positive Output Pull-Up.
	EPAD	Exposed Pad. The exposed pad must be connected to a ground plane with low thermal impedance.

TYPICAL PERFORMANCE CHARACTERISTICS

VCC_DVGA_x = 5 V, VCCx = 3.3 V, T_A = 27°C, f_{IF} = 184 MHz, internal LO, digital variable gain amplifier (DVGA) attenuation = 0 dB, L_{TUNE} = 1 nH, L_{SHUNT} = 150 nH, and 25 Ω external resistors on each differential leg, 5 V high power mode, low-pass filter setting = 7, unless otherwise noted. The LO is high-side for RF frequencies lower than 1 GHz and higher than 2.5 GHz, and LO is low-side for the remaining RF frequencies. For two-tone measurements, IF output power is −4 dBm/tone and 10 MHz tone spacing, unless otherwise noted. All losses from input and output traces and baluns are de-embedded from results.

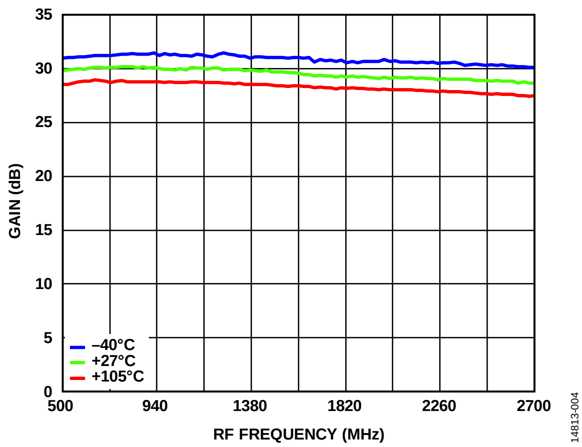

Figure 4. Gain vs. RF Frequency

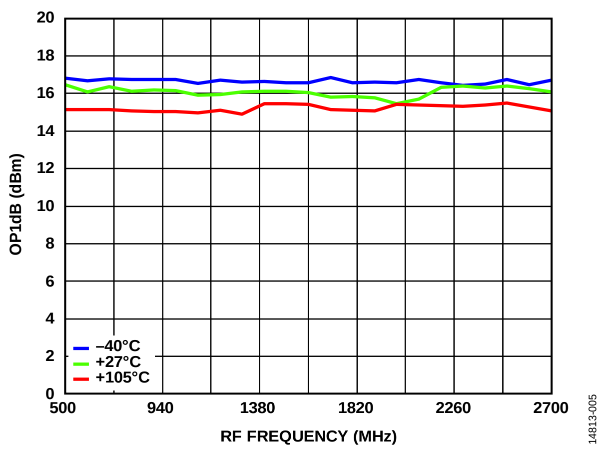

Figure 5. OP1dB vs. RF Frequency

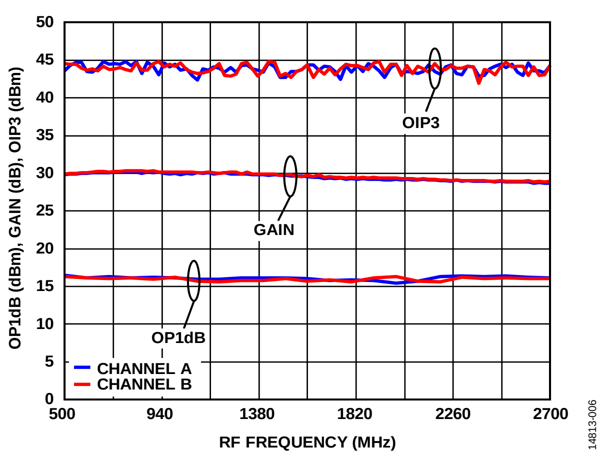

Figure 6. OP1dB, Gain, and OIP3 vs. RF Frequency, Channel Comparison

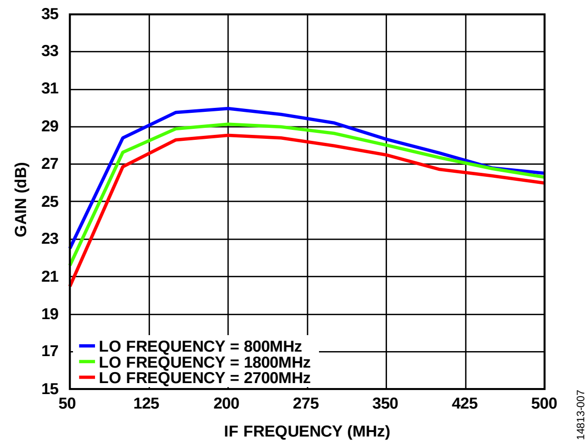

Figure 7. Gain vs. IF Frequency; RF Sweep with Fixed LO, $L_{SHUNT}x$ = 150 nH

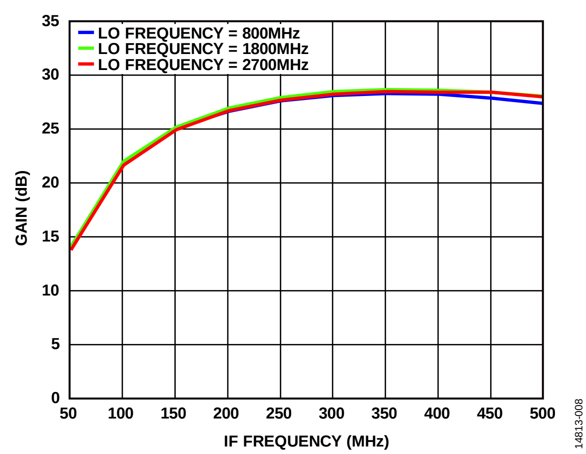

Figure 8. Gain vs. IF Frequency; RF Sweep with Fixed LO, $L_{SHUNT}x$ = 47 nH

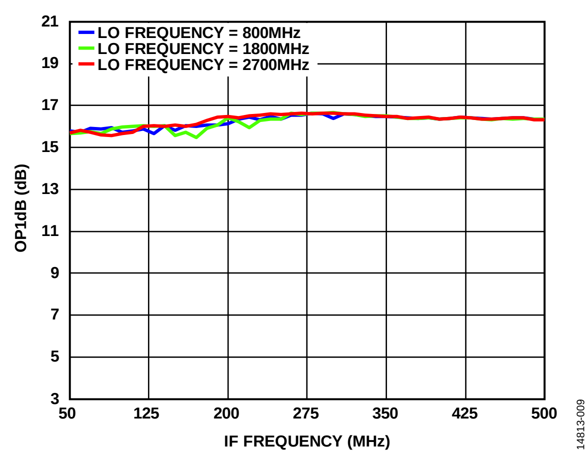

Figure 9. OP1dB vs. IF Frequency; RF Sweep with Fixed LO

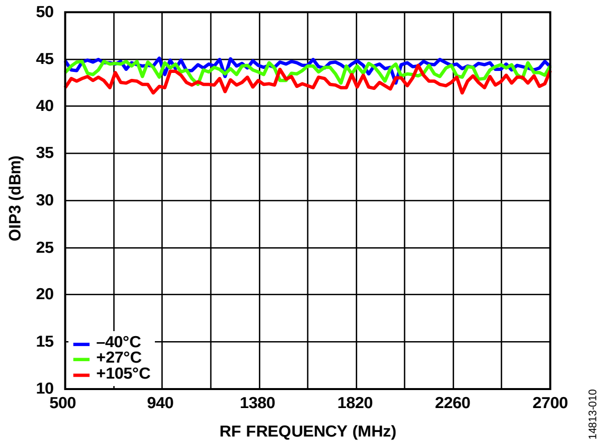

Figure 10. OIP3 vs. RF Frequency; Maximum Gain, $L_{SHUNT}X$ = 150 nH

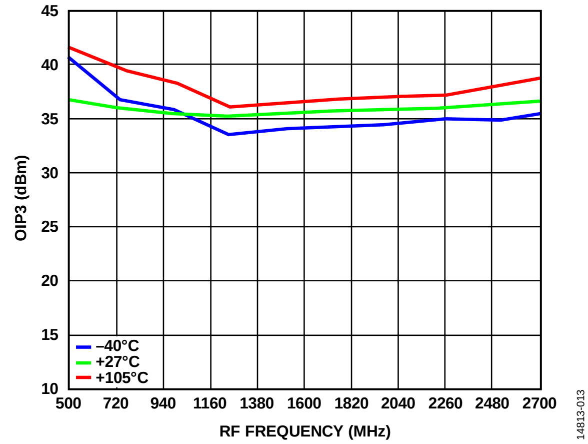

Figure 13. OIP3 vs. RF Frequency; Maximum Gain – 16 dB, $L_{SHUNT}X$ = 47 nH, IF = 368 MHz

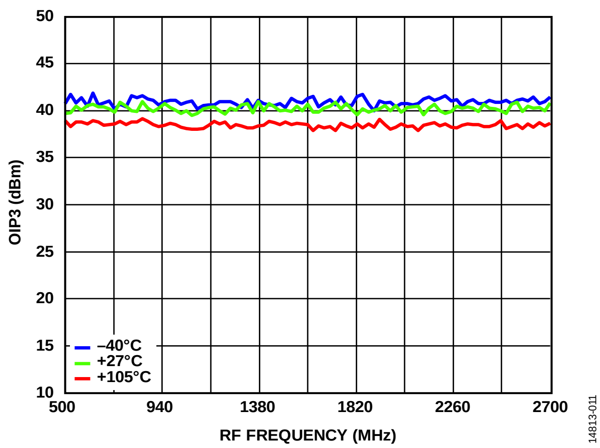

Figure 11. OIP3 vs. RF Frequency; Maximum Gain, $L_{SHUNT}X$ = 47 nH, IF = 368 MHz

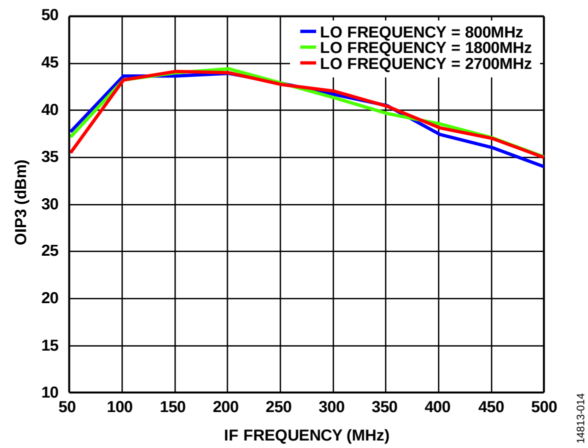

Figure 14. OIP3 vs. IF Frequency; RF Sweep with Fixed LO, Maximum Gain, $L_{SHUNT}X$ = 150 nH

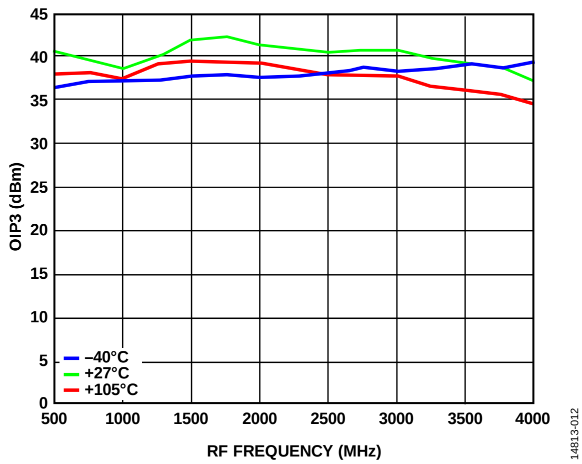

Figure 12. OIP3 vs. RF Frequency; Maximum Gain – 16 dB, $L_{SHUNT}X$ = 150 nH

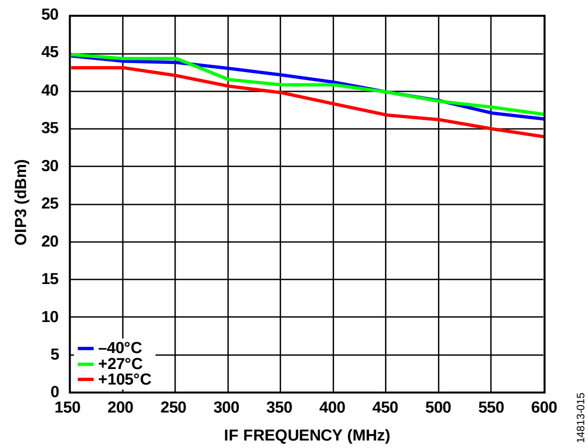

Figure 15. OIP3 vs. IF Frequency; RF Sweep with Fixed LO, Maximum Gain, $L_{SHUNT}X$ = 47 nH, IF = 368 MHz

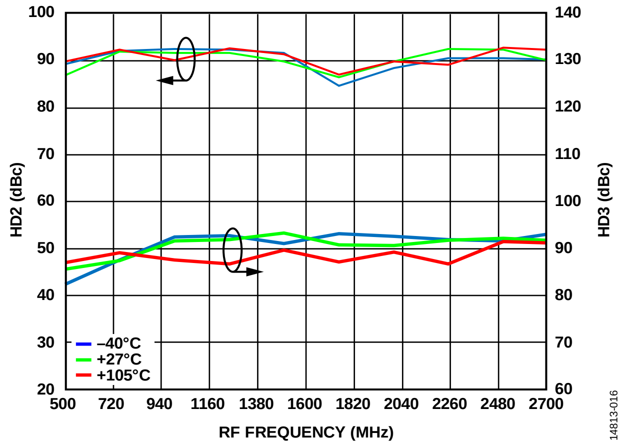

Figure 16. HD2 and HD3 vs. RF Frequency, Maximum Gain

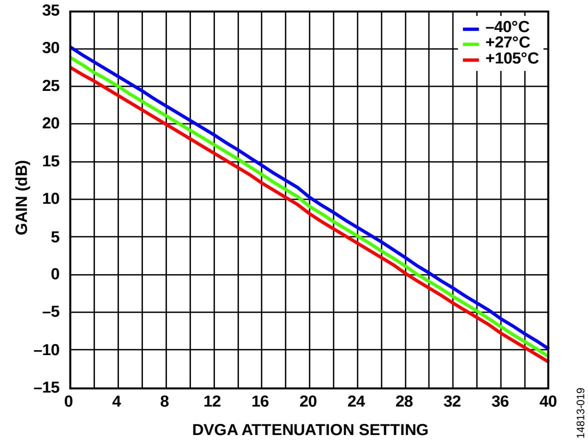

Figure 19. Gain vs. DVGA Attenuation Setting, RF = 2700 MHz

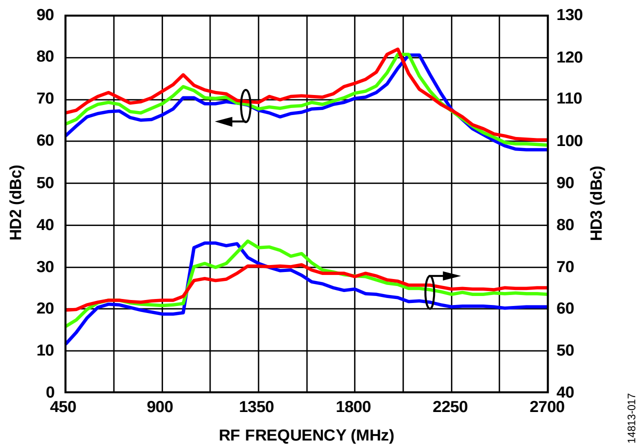

Figure 17. HD2 and HD3 vs. RF Frequency, Gain = 1 dB

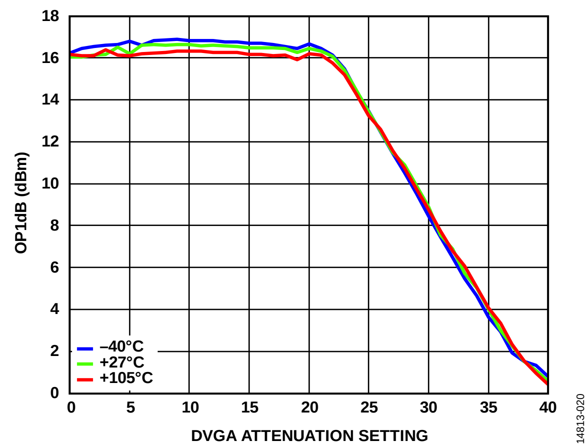

Figure 20. OP1dB vs. DVGA Attenuation Setting, RF = 2700 MHz

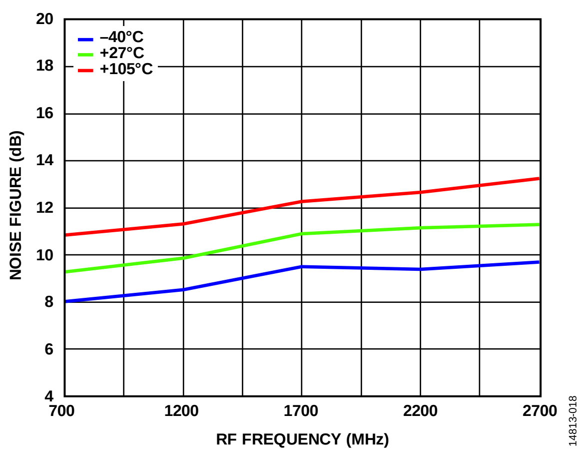

Figure 18. Noise Figure vs. RF Frequency; Maximum Gain

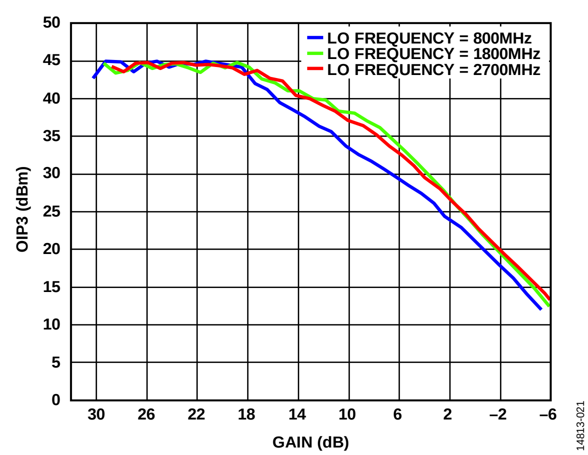

Figure 21. OIP3 vs. Gain for Various LO Frequencies

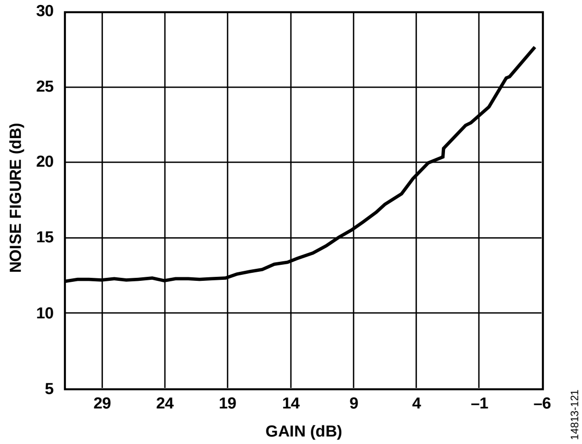

Figure 22. Noise Figure vs. Gain, RF = 2100 MHz

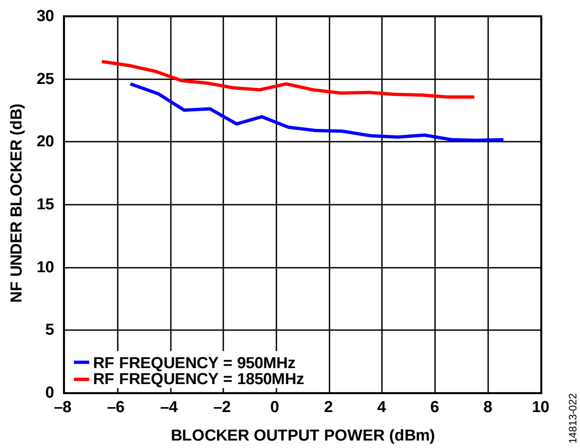

Figure 23. Noise Figure Under Blocker vs. Blocker Output Power, P_{IN} = 0 dBm, Internal LO

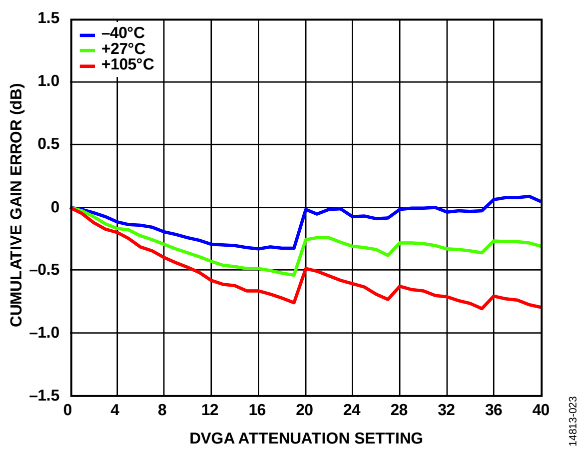

Figure 24. Cumulative Gain Error vs. DVGA Attenuation Setting, RF = 2700 MHz

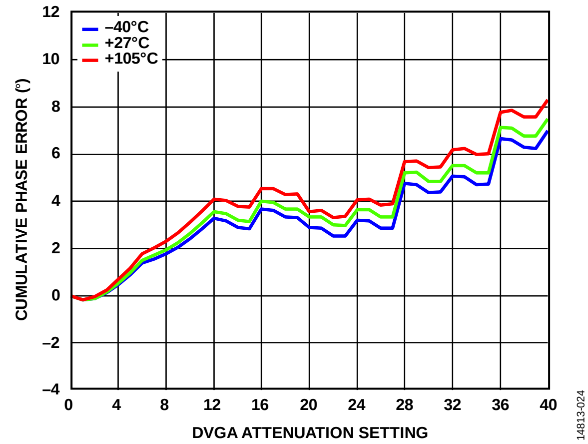

Figure 25. Cumulative Phase Error vs. DVGA Attenuation Setting, RF = 2700 MHz

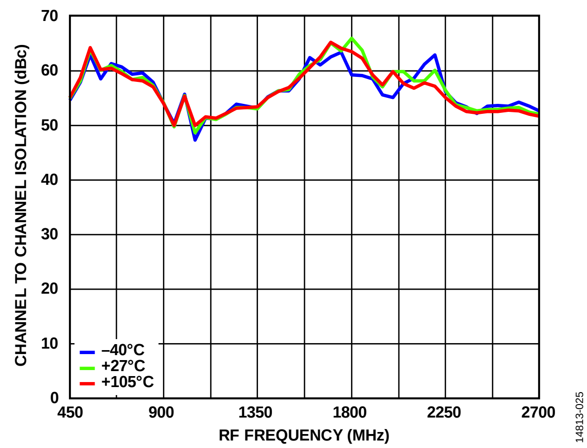

Figure 26. Channel to Channel Isolation vs. RF Frequency

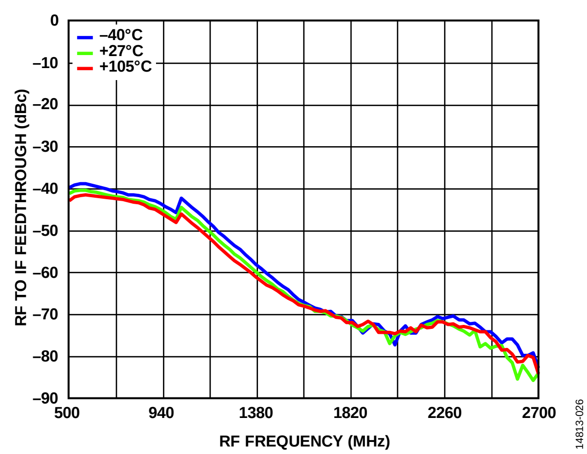

Figure 27. RF to IF Feedthrough vs. RF Frequency

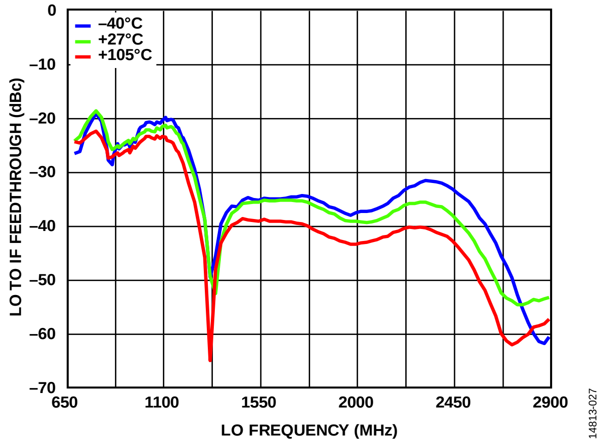

Figure 28. LO to IF Feedthrough vs. LO Frequency

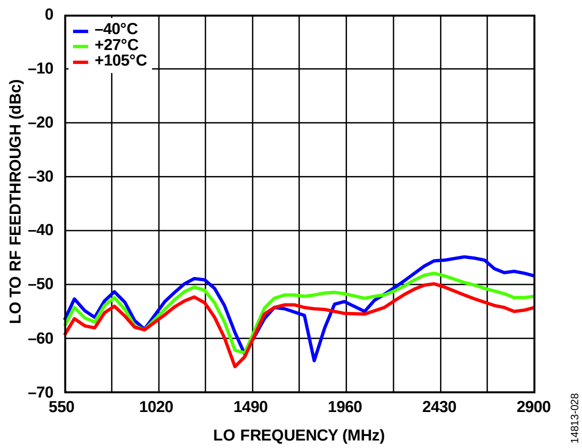

Figure 29. LO to RF Feedthrough vs. LO Frequency

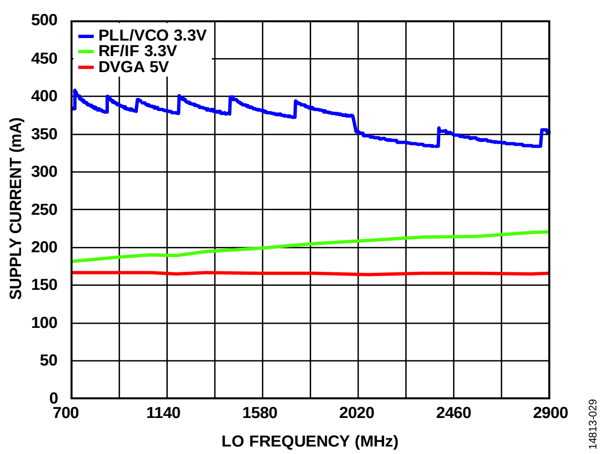

Figure 30. RF/IF 3.3 V, DVGA 5 V, and PLL/VCO 3.3 V Supply Currents vs. LO Frequency

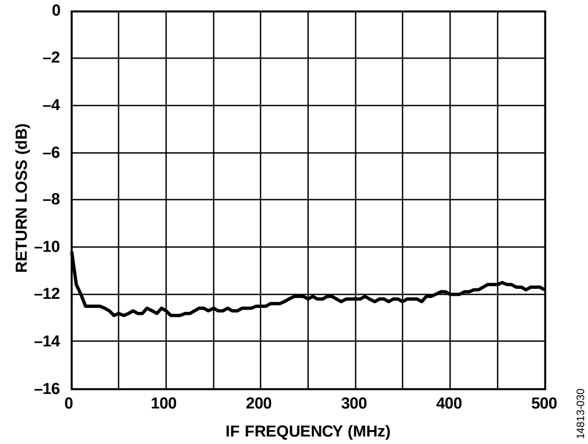

Figure 31. IF Output Return Loss , External 25 Ω on Each Differential Leg

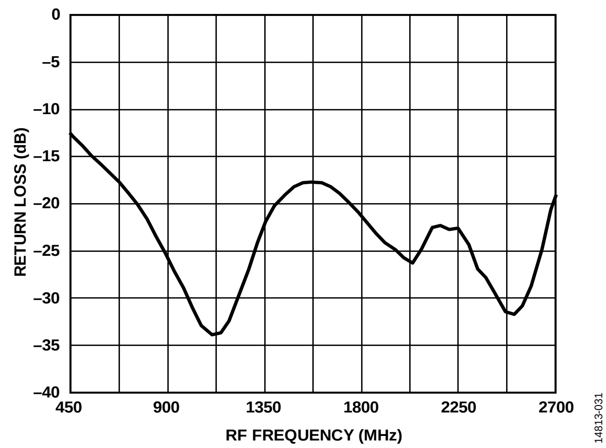

Figure 32. RF Input Return Loss

PHASE-LOCKED LOOP (PLL)

VCC_DVGA_x = 5 V, VCCx = 3.3 V, T_A = 27°C, f_{PFD} = 30.72 MHz, f_{REF} = 122.88 MHz, 20 kHz loop filter, measured at the LO output, unless otherwise noted. All losses from input and output traces and baluns are de-embedded from results.

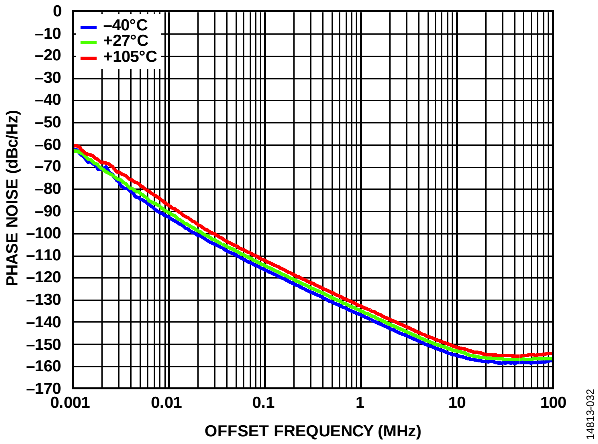

Figure 33. Open-Loop VCO Phase Noise vs. Offset Frequency, f_{LO} = 2350 MHz, f_{VCO} = 4700 MHz

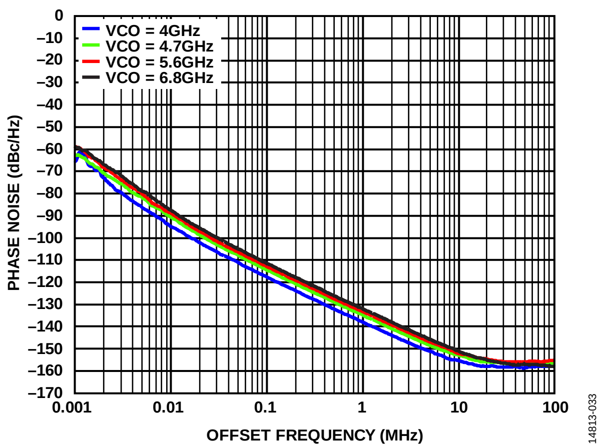

Figure 34. Open-Loop VCO Phase Noise vs. Offset Frequency, for Various VCO Frequencies, Divide by 2 Selected

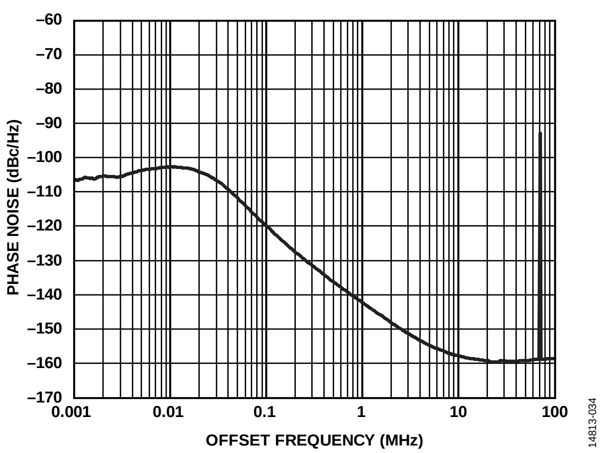

Figure 35. Closed-Loop Phase Noise vs. Offset Frequency for f_{LO} = 1565 MHz

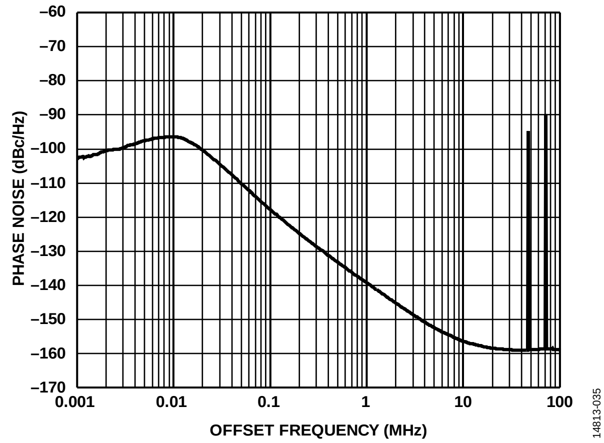

Figure 36. Closed-Loop Phase Noise vs. Offset Frequency for f_{LO} = 1765 MHz

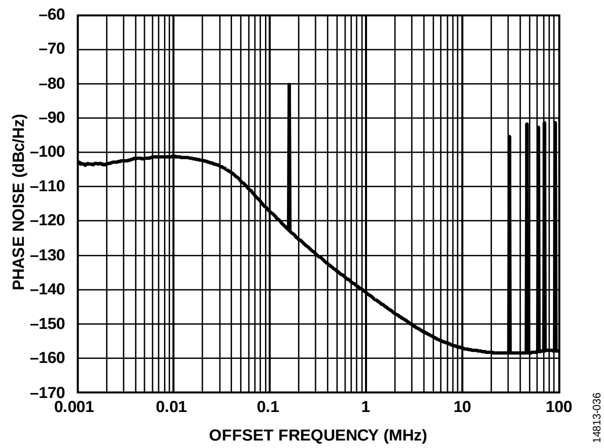

Figure 37. Closed-Loop Phase Noise vs. Offset Frequency for f_{LO} = 2350 MHz

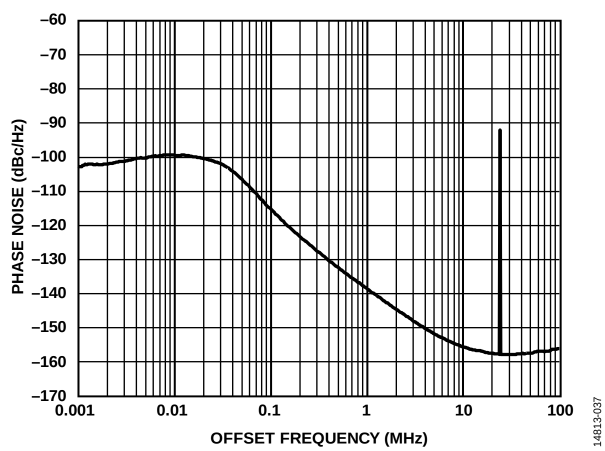

Figure 38. Closed-Loop Phase Noise vs. Offset Frequency for f_{LO} = 2720 MHz

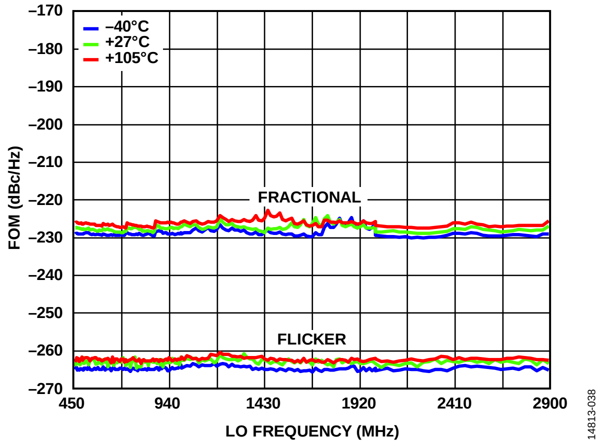

Figure 39. PLL Figure of Merit (FOM) vs. LO Frequency

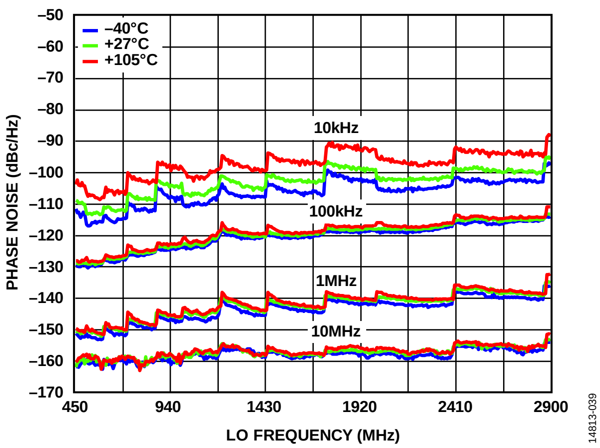

Figure 40. Closed-Loop LO Phase Noise vs. LO Frequency for Various Offset Frequencies

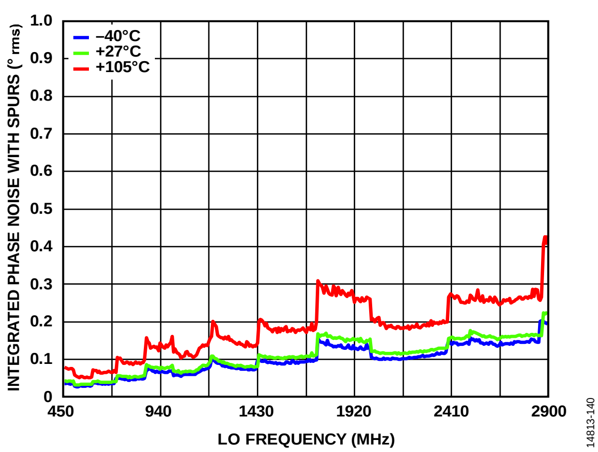

Figure 41. 100 Hz to 10 MHz Integrated Phase Noise vs. LO Frequency

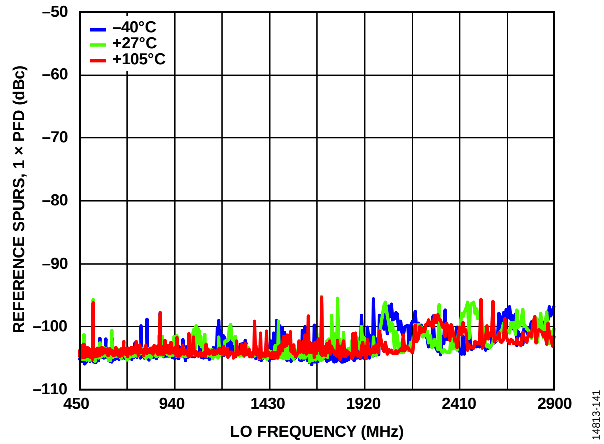

Figure 42. Reference Spurs vs. LO Frequency, 1 × f_{PFD} Offset, Daisy-Chain Measurement

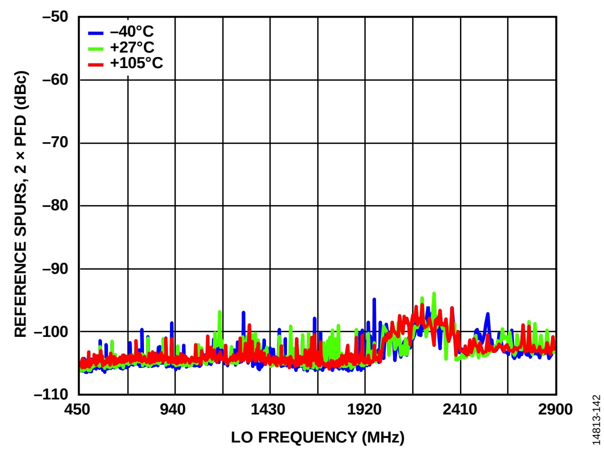

Figure 43. Reference Spurs vs. LO Frequency, 2 × f_{PFD} Offset, Daisy-Chain Measurement

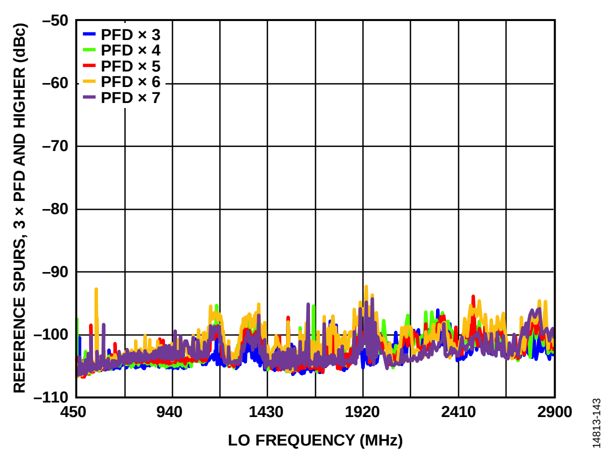

Figure 44. Reference Spurs vs. LO Frequency, 3 and Higher × f_{PFD} Offset, Daisy-Chain Measurement

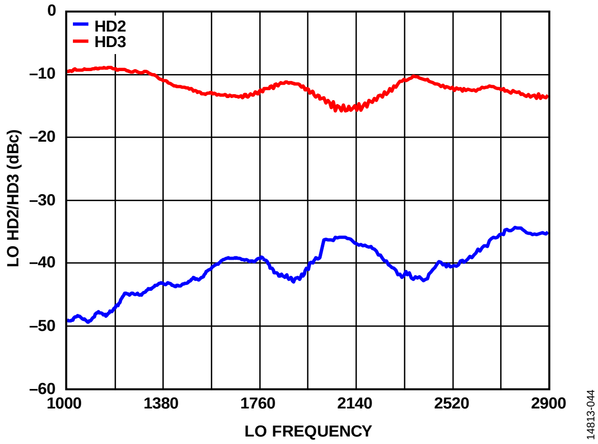

Figure 45. LO HD2/HD3 vs. LO Frequency

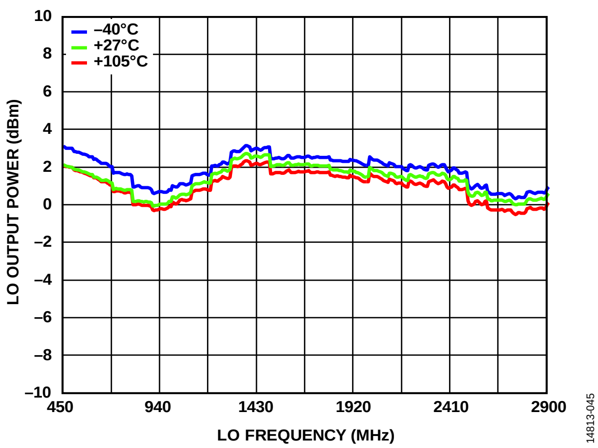

Figure 46. LO Output Power vs. LO Frequency

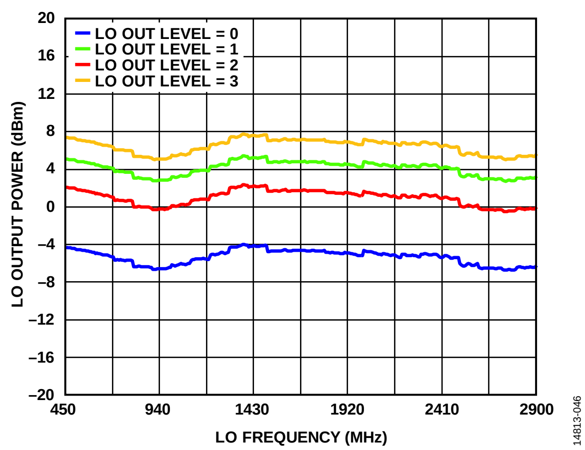

Figure 47. LO Output Power vs. LO Frequency, for Various Output Power Level Settings

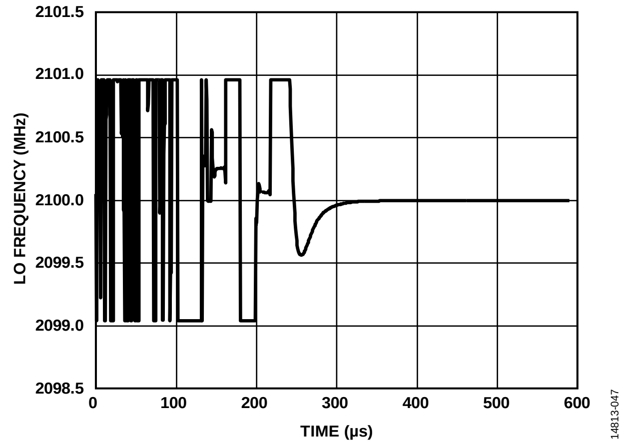

Figure 48. LO Frequency Settling Time, f_{LO} = 2.1 GHz

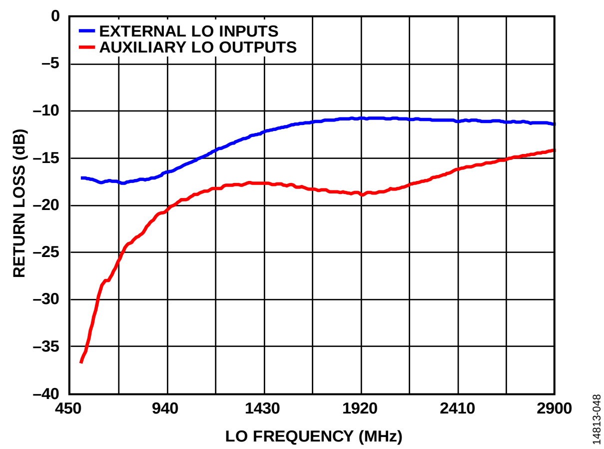

Figure 49. Auxiliary Output Return Loss, External LO Input Return Loss vs. LO Frequency

SPURIOUS PERFORMANCE

($N \times f_{RF}$) − ($M \times f_{LO}$) spur measurements were made using the standard evaluation board. Mixer spurious products were measured in decibels (dB) relative to the carrier (dBc) from the IF output power level. IF = 184 MHz, and RF spur frequency is found with the formula; $f_{RF\_SPUR} = ((M \times f_{LO}) + f_{IF}))/N$. Data is shown for all spurious components greater than −115 dBc and frequencies of less than 2.7 GHz.

Table 10. 900 MHz Spurious Performance

N	M = 1	M = 2	M = 3	M = 4	M = 5	M = 6
1	Not applicable	−53	−10.5	−49	−17	Not applicable
2	Not applicable	−84	Not applicable	Not applicable	Not applicable	Not applicable
3	Not applicable	Not applicable	−115	Not applicable	−115	Not applicable
4	Not applicable	Not applicable	Not applicable	Not applicable	Not applicable	Not applicable
5	Not applicable	Not applicable	Not applicable	Not applicable	Not applicable	Not applicable
6	Not applicable	Not applicable	Not applicable	Not applicable	Not applicable	Not applicable

THEORY OF OPERATION

The ADRF6650 is a wideband, highly integrated, dual-channel downconverter ideally suited for multiple input, multiple output (MIMO) applications. Additionally, the ADRF6650 integrates an LO generation block consisting of a synthesizer and a multicore VCO with an octave range and low phase noise. The synthesizer uses a fractional-N PLL to enable continuous LO coverage from 450 MHz to 2900 MHz. The wideband frequency response and flexible frequency programming simplifies the receiver design, saves on-board space, and minimizes the need for external components.

The RF subsystem of the ADRF6650 consists of an integrated, wideband, low loss RF balun; a double balanced, passive metal-oxide semiconductor field-effect transistor (MOSFET) mixer; a tunable filter; a fixed gain IF amplifier; a DVGA, and fractional synthesizer with on-chip VCO.

RF BALUN

The ADRF6650 integrates a wideband balun operating over a frequency range from 450 MHz to 2700 MHz. The RF balun offers the benefit of ease of drivability from a single-ended 50 Ω RF input, and the single-ended to differential conversion of the balun optimizes common-mode rejection. The balun uses an external compensation inductor to improve the balance for low RF frequency. See the RF Frequency and IF Bandwidth Optimization section for details.

MIXERS

The output of the balun is applied to a passive mixer that commutates the RF input in accordance with the output of the LO subsystem. The passive mixer is essentially a balanced, low loss switch that adds minimum noise to the frequency translation. The only noise contribution from the mixer is due to the resistive loss of the switches, which is in the order of a few ohms.

LOW-PASS FILTERS

Because the mixer is inherently broadband and bidirectional, it is necessary to properly terminate all idler (M × N product) frequencies generated by the mixing process. Terminating the mixer avoids the generation of unwanted intermodulation products and reduces the level of unwanted signals at the input of the IF amplifier, where high peak signal levels can compromise the compression and intermodulation performance of the system. This termination is accomplished by the addition of a programmable low-pass filter (LPF) network between the IF amplifier and the mixer and in the feedback elements in the IF amplifier. The LPF filter has programmable filter bandwidths and is tuned by switching parallel capacitances on the primary and secondary sides by writing to the LPF_OVERRIDE register (Register 0x0300). Therefore, selecting the proper combination of LPF1_OVERRIDE (Register 0x0300, Bits[3:1]) and LPF2_OVERRIDE (Register 0x0300, Bits[6:4]) sets the desired bandwidth. It is recommended to set the LPF1_OVERRIDE and LPF2_OVERRIDE bit fields to the same value.

In addition, the input side of the LPF has a series 50 Ω resistor on each differential leg which improves the mixer termination for low RF frequencies (<1 GHz). The resistors can be bypassed by DPLX_EN_OVERRIDE (Register 0x0300, Bit 0).

IF AMPLIFIERS

The IF amplifier following the LPF is a fixed gain, balanced feedback design that simultaneously provides the desired gain, noise figure, and input impedance that is required to achieve the overall performance. The balanced open-collector output of the IF amplifier, with an impedance modified by the feedback within the amplifier, connects internally to the DSA stage, but requires external pull-up inductors of approximately 220 nH. It is also possible to use a tuned load to improve the filtering of unwanted mixing products but can limit the signal bandwidth for wide bandwidth applications.

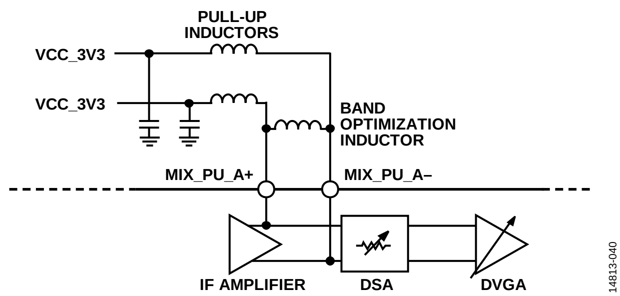

Figure 50. External Pull-Up Inductor Connection

The IP3 performance can be optimized by adjusting the low-pass filter between the mixer and the IF amplifier. Further optimization can be made, via SPI control, by adjusting the IF main bias current, IFMAIN_BIAS_OVERRIDE (Register 0x0301, Bits[3:0]), and a linearizing optimization current, IFLIN_BIAS_OVERRIDE (Register 0x0302, Bits[3:0]). The linearization current generally maintains the same IP3 for a given IF frequency but may need to be adjusted for different IF frequencies.

DVGA

The ADRF6650 integrates a differential variable gain amplifier consisting of a differential, digitally controlled passive attenuator (DSA) followed by a DVGA. The total attenuation range is 43 dB, in 1 dB steps, with the first 12 dB of attenuation provided by the DVGA and the remaining 31 dB provided by the DSA. The 12 dB of attenuation from the DVGA has less than 1 dB degradation of the ADRF6650 noise figure for the entire 12 dB range. The OIP3 also remains nearly constant over that attenuation range, as shown in Figure 21. The input digitally controlled binary weighted attenuator has a 31 dB range in 1 dB steps. The noise figure for this attenuator increases 1 dB for each dB of attenuation of this 31 dB attenuation range.

Output Impedance and Matching

The differential output impedance of each channel of the ADRF6650 is 10 Ω. External series resistors are required to increase the output impedance for matching considerations, but reduce the maximum output power of the ADRF6650. A series resistor of 25 Ω on each differential leg of each output provides a −10 dB return loss for a 100 Ω differential load and the maximum output power.

Power Supply and Common Mode

The DVGA in each channel of the ADRF6650 can be powered either at 3.3 V or 5.0 V through the VCC_DVGA_A and VCC_DVGA_B pins. A 5.0 V supply provides increased performance, mainly in OIP3 and in OP1dB but results in increased power consumption. The current consumption of the DVGA is maintained at the same level for each power voltage (approximately 75 mA) and is controlled by DVGA_5V_SEL (Register 0x0103, Bit 7). If desired, the current can be reduced for lower power consumption and reduced performance. The performance mode select is controlled by DVGA_HP_SEL (Register 0x0104, Bit 6).

TheADRF6650 is also flexible in terms of input/output coupling. It can be ac-coupled or dc-coupled at the outputs within the specified output common-mode levels of 1.2 V to 2.8 V, depending on the supply voltage. The output common-mode voltage can be set by VCPL_A and VCPL_B, which allows the driving of an analog-to-digital converter (ADC) directly without external components. If no external output common-mode voltage is applied, the output common mode is $V_{CC}/2$.

Gain Control Modes

The attenuation of the DVGA can be controlled by several different modes:

- SPI mode through a dedicated register for each channel in the main SPI.
- Up/down mode through the serial gain control 2-wire SPI port for each channel.

The mode is set by DVGA_GAIN_MODE (Register 0x0103, Bits[2:0]) as shown in Table 11. The attenuation setting at any configuration can be read from the ATTEN_READBACK_CH1 register (Register 0x003C) and ATTEN_READBACK_CH2 register (Register 0x003D) for Channel A and Channel B, respectively. When the gain control mode is changed between different modes, a reset needs to be issued through DVGA_CH1_RSTB (Register 0x0021, Bit 1) and DVGA_CH2_RSTB (Register 0x0021, Bit 0) to the Channel A DVGA and Channel B DVGA, respectively. See the description details for the DVGA_CH1_RSTB and DVGA_CH2_RSTB registers.

Table 11. DVGA Gain Modes

DVGA_GAIN_MODE (Register 0x0103, Bits[2:0])	DVGA Mode
01	SPI
11	Up/down

SPI Mode

In SPI mode, the DVGA gain is controlled by DVGA_GAIN1 (Register 0x0104, Bits[5:0]) and DVGA_GAIN2 (Register 0x0104, Bits[5:0]), as shown in Table 12.

Table 12. DVGA Attenuation Setting

DVGA_GAIN_CH1 (Register 0x0104, Bits[5:0]) and DVGA_GAIN_CH2 (Register 0x0105, Bits[5:0])	Attenuation
000000	0
000001	1
…	…
101010	42
101011	43

Up/Down Mode

The up/down interface reuses the RXx_ATT_DATA and RXx_ATT_CLK pins to control the gain. Gain is increased by a clock pulse on RXx_ATT_CLK (rising edges) when RXx_ATT_DATA is low. Gain is decreased by a clock pulse on RXx_ATT_CLK when RXx_ATT_DATA is high. Reset is detected by a rising edge latching data having one polarity with the falling edge latching the opposite polarity. Reset results in minimum gain code 111111 (binary).

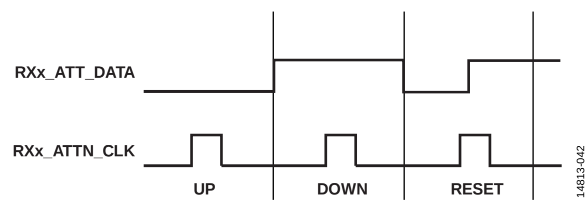

Figure 51. Up/Down Data and Clock Bit Sequence

The step size is selectable via DVGA_UPDN_STEP (Register 0x0103, Bits[4:3]), as shown in Table 13. The default step size is 1 dB. The gain code count rails at the top and bottom of the control range.

Table 13. Up/Down Step Size

DVGA_UPDN_STEP (Register 0x0103, Bits[4:3])	Step Size
00	1
01	2
10	4
11	8

TDD OPERATION

The ADRF6650 provides two separate pins to control the channels (enable/disable) in TDD operation. When the TDD_A (Pin 2) and TDD_B (Pin 13) pins are pulled low, Channel A and Channel B are active, respectively. When TDD_A and TDD_B are pulled high, the channels are disabled.

The ADRF6650 also provides TDD enable masks to enable/disable certain blocks during TDD operation. The TDD enable masks select which blocks are disabled during TDD off time. The EN_MASK register (Register 0x0102) includes the mask bits for the LO stages, the IF amplifiers, the DVGAs, and the PLL. When set to 1, the bits shown in Table 14 disable the related block during TDD off time. The enable mask bits for the LO Stage 23, the IF amplifiers, and the DVGA disable the related block (when set to 1) when either one of the TDD_A and TDD_B pins is set to high. Alternatively, the LO_STG1_ENB_MASK bit (Register 0x0102, Bit 0) disables the LO stage amplifier only when both TDD_A and TDD_B are high. In the same manner, the PLL_ENB_CH12_MASK bit (Register 0x0102, Bit 7) disables the PLL/VCO only when both TDD_A and TDD_B are high.

Table 14. TDD Enable Mask Register (Register 0x0102)

TDD Enable Mask Bit	Default	Block
LO_STG1_ENB_MASK	0	LO Stage 1
LO_STG23_ENB_CH1_MASK	1	Channel A LO Stage 23
LO_STG23_ENB_CH2_MASK	1	Channel B LO Stage 23
IF_ENB_CH1_MASK	1	Channel A IF amplifier
IF_ENB_CH2_MASK	1	Channel B IF amplifier
DVGA_ENB_CH1_MASK	1	Channel A DVGA
DVGA_ENB_CH1_MASK	1	Channel B DVGA
PLL_ENB_CH12_MASK	0	PLL

LO GENERATION BLOCK

The ADRF6650 supports the use of both internal and external LO signals for the mixers. The internal LO is generated by an on-chip VCO, which is tunable over a frequency range of 4000 MHz to 8000 MHz. The output of the VCO is phase-locked to an external reference clock through a fractional-N PLL that is programmable through the SPI control registers. To produce LO signals over the 450 MHz to 2900 MHz frequency range to drive the mixers, the VCO outputs passes through an output divider. Alternatively, an external signal can be used to supply the LO signals to the mixers.

Internal LO Mode

For internal LO mode, the ADRF6650 uses the on-chip PLL and VCO to synthesize the frequency of the LO signal. The PLL, shown in Figure 52, consists of a reference path, phase and frequency detector (PFD), charge pump, and a programmable integer divider with a prescaler. The reference path takes in a reference clock and divides it down by a value calculated with the R divider together with doubler bit and prescaler bit. Then the divided down reference signal passes to the PFD. The PFD compares this signal to the divided down signal from the VCO. The PFD sends an up/down signal to the charge pump if the VCO signal is slow/fast compared to the reference frequency. The charge pump sends a current pulse to the off-chip loop filter to increase or decrease the tuning voltage (V_{TUNE}).

The ADRF6650 integrates a multicore VCO covering an octave range of 4 GHz to 8 GHz. The suitable VCO is selected with the autotune functionality built in the chip. After the user determines the necessary register values, a write to the INT_L register (Register 0x1200) initiates the autotune process.

LO Frequency and Dividers

The signal originating from the VCO or the external LO inputs goes through a series of dividers before it is buffered to drive the mixer. The programmable divide by two stages divide the frequency of the incoming signal by 1, 2, 4, 8, and 16 before reaching to the mixers. The control bits (Register 0x1414, Bits[4:0]) needed to select the different LO frequency ranges are listed in Table 15.

Table 15. Output Divide Ratio for Frequency Ranges

LO Frequency (MHz)	OUT_DIVRATIO (Register 0x1414, Bits[4:0])	VCO Frequency (MHz)
450 to 500	10000	LO × 16
500 to 1000	01000	LO × 8
1000 to 2000	00100	LO × 4
2000 to 2900	00010	LO × 2

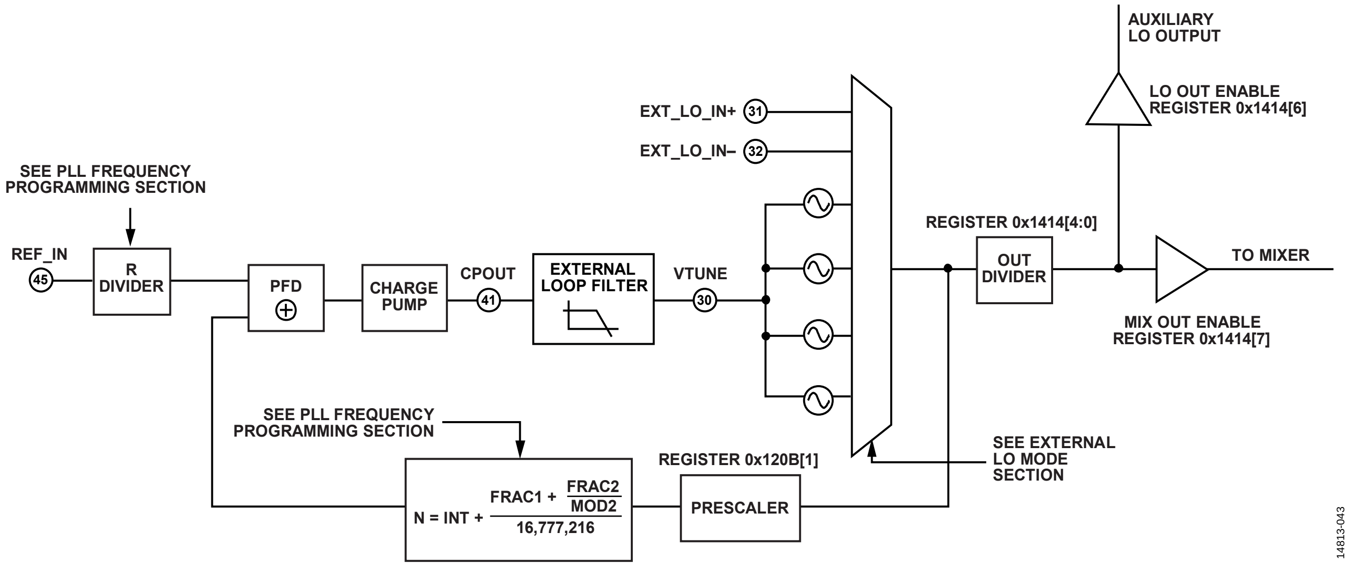

Figure 52. PLL/VCO Block Diagram

PLL Frequency Programming

The INT, FRAC1, FRAC2, and MOD values, in conjunction with the R counter, make it possible to generate output frequencies that are spaced by fractions of the PFD frequency (f_{PFD}). Calculate the VCO frequency (VCOOUT) by

$$VCOOUT = f_{PFD} \times N \quad (1)$$

where:
VCOOUT is the output frequency of the VCO (without using the output divider).
f_{PFD} is the frequency of the phase frequency detector.
N is the desired value of the feedback counter.

Calculate f_{PFD} by

$$f_{PFD} = REF_{IN} \times ((1 + D)/(R \times (1 + T))) \quad (2)$$

where:
REF_{IN} is the reference input frequency.
D is the reference doubler bit (Register 0x120E, Bit 3).
R is the preset divide ratio of the binary 7-bit programmable reference counter (1 to 255) (Register 0x120C, Bits[6:0]).
T is the reference divide by 2 bit (0 or 1) (Register 0x120E, Bit 0).

N comprises

$$N = INT + \frac{FRAC1 + \frac{FRAC2}{MOD}}{16{,}777{,}216} \quad (3)$$

where:
INT is the 16-bit integer value (23 to 32,767 for the 4/5 prescaler, 75 to 65,535 for the 8/9 prescaler) referenced with Register 0x1201 and Register 0x1200.
FRAC1 is the 24-bit numerator of the primary modulus (0 to 16,777,215) with Register 0x1204, Register 0x1203, and Register 0x1202.
FRAC2 is the numerator of the 14-bit auxiliary modulus (0 to 16,383) with Register 0x1234, Bits[5:0] and Register 0x1233.
MOD is the programmable, 14-bit auxiliary fractional modulus (2 to 16,383), referenced with Register 0x1209, Bits[5:0] and Register 0x1208.

Equation 3 results in a very fine frequency resolution with no residual frequency error. To apply this formula, take the following steps:

1. Calculate N by VCOOUT/f_{PFD}. The integer value of this number forms INT.
2. Subtract the INT value from the full N value.
3. Multiply the remainder by 2^{24}. The integer value of this number forms FRAC1.
4. Calculate MOD based on the channel spacing (f_{CHSP}) by

   $$MOD = f_{PFD}/\mathrm{GCD}(f_{PFD}, f_{CHSP}) \quad (4)$$

   where:
   $\mathrm{GCD}(f_{PFD}, f_{CHSP})$ is the greatest common divider of the PFD frequency and the channel spacing frequency.
   f_{CHSP} is the desired channel spacing frequency.
5. Calculate FRAC2 by the following equation:

   $$FRAC2 = (N - INT) \times 224 - FRAC1)) \times MOD \quad (5)$$

The FRAC2 and MOD fraction results in outputs with zero frequency error for channel spacings when

$$f_{PFD}/\mathrm{GCD}(f_{PFD}/f_{CHSP}) < 16{,}383 \quad (6)$$

where:
f_{PFD} is the frequency of the phase frequency detector.
GCD is a greatest common denominator function.
f_{CHSP} is the desired channel spacing frequency.

After determining the necessary register values for PLL, also set the SD_EN_FRAC0 bit (Register 0x122A, Bit 4) to 1.

It is recommended to set the charge pump current to be 2.4 mA by setting the CP_CURRENT bit (Register 0x122E, Bits[3:0]) to 7. Together with a 20 kHz loop filter, the charge pump current setting results in an optimized performance.

Bleed Setting

The PFD circuitry compares the PFD and divided down VCO signals. The ADRF6650 employs a bleed circuit to put the PFD circuit in the linear operation region. The bleed circuit introduces a delay to the incoming PFD signal, indicated as PFD_OFFSET in Equation 7. Calculate the bleed current, BICP (Register 0x122F, Bits[7:0]), from the desired PFD_OFFSET, as shown in Equation 7.

$$BICP = \mathrm{integer}(\mathrm{round}(\mathrm{float}(I_{CP} \times PFD\_OFFSET \times f_{PFD})/960)/255)) \quad (7)$$

where:
I_{CP} is the charge pump current.
The recommended *PFD_OFFSET* for the 20 kHz loop filter is 2 ns.

PLL Lock Time

The time it takes to lock the PLL after the last register is written breaks down into two parts: VCO band calibration and loop settling.

After writing to the last register, the PLL automatically performs a VCO band calibration to choose the correct VCO band. This calibration requires approximately 200 µs. After calibration completes, the feedback action of the PLL causes the VCO to lock to the correct frequency eventually. The speed with which this lock occurs depends on the small signal settling of the loop. Settling time, after calibration, depends on the PLL loop filter bandwidth. With a 20 kHz loop filter bandwidth, the settling time is approximately 200 µs.

Lock Detection Control

The ADRF6650 provides two ways of observing lock detection. Lock detection can be monitored from a dedicated register, LOCK_DETECT (Register 0x124D, Bit 0). Lock detection can also be monitored through the dedicated LO_LCKDT pin (Pin 23). The SD_SM_2 bit (Register 0x122A, Bit 1) must be set to 0 to observe lock detection.

Required PLL/VCO Settings and Register Write Sequence

Configure the PLL registers accordingly to achieve the desired frequency, and the last write must be to Register 0x1200 (INT_L). When Register 0x1200 is programmed, an internal VCO calibration initiates, which is the last step to locking the PLL. After the PLL locks, enable the buffer to the mixer via the MIX_OE bit (Register 0x1414, Bit 7) to provide the LO signal to the mixer.

External LO Mode

The external LO frequency range is 450 MHz to 2900 MHz, and the applied LO signal is fed to the mixers after passing through the divide by 1 block. To configure for external LO mode, write the following register sequence Table 16 and apply the differential LO signals to Pin 31 (EXT_LO_IN+) and Pin 32 (EXT_LO_IN−).

Table 16. Register Settings for External LO Mode

Register	Required Value	Description
0x120B	0x00	Disable feedback divider
0x122D	0x00	Disable PFD and CP
0x1240	0x03	Disable VCO adjust
0x1217	0x00	Set VCO select to a low value
0x121F	0x40	Disable calibration
0x1021	0xD8	Disable PLL blocks
0x1414	0xA1	Use external LO

The EXT_LO_IN+ and EXT_LO_IN− input pins must be ac-coupled. When not in use, leave the EXT_LO_IN+ and EXT_LO_IN− pins unconnected.

In external LO mode of operation, the ADRF6650 consumes approximately 0.5 W less of power compared to the internal LO mode of operation.

SERIAL PORT INTERFACE

The SPI of the ADRF6650 allows the user to configure the device for specific functions or operations through a structured register space provided inside the chip. This interface provides the user with added flexibility and customization. Addresses are accessed via the serial port interface and can be written to or read from the serial port interface.

The serial port interface consists of four control lines: SCLK, SDIO, SDO, and $\overline{CS}$. The SPI supports both 3-wire (default) and 4-wire modes of operation. Enable SDOACTIVE (Register 0x0000, Bit 4) and SDOACTIVE (Register 0x0000, Bit 3) for 4-wire mode. SCLK (serial clock) is the serial shift clock, and it synchronizes the serial interface reads and writes. SDIO is the serial data input or the serial data output depending on the instruction sent and the relative position in the timing frame. $\overline{CS}$ is an active low control that gates the read and write cycles. The falling edge of $\overline{CS}$, in conjunction with the rising edge of SCLK, determines the start of the frame. When $\overline{CS}$ is high, all SCLK and SDIO activity is ignored. See Table 6 for the serial timing and its definitions.

The ADRF6650 protocol consists of a read/write followed by 16 register address bits and 8 data bits. Both the address and data fields are organized with the MSB first and end with the LSB.

SPI and GPIO 1.8 V/3.3 V Compatibility

The SPI and general-purpose input/output (GPIO) interfaces of the ADRF6650 provide two options for the logic voltage levels, namely 1.8 V and 3.3 V. The interfaces use 1.8 V logic levels as the default. Enable SPI_18_33_SEL (Register 0x0101, Bit 0) and SPI_1P8_3P3_CTRL (Register 0x1401, Bit 4) for 3.3 V-compatible logic levels. See Table 5 for the SPI and GPIO specifications.

APPLICATIONS INFORMATION

BASIC CONNECTIONS

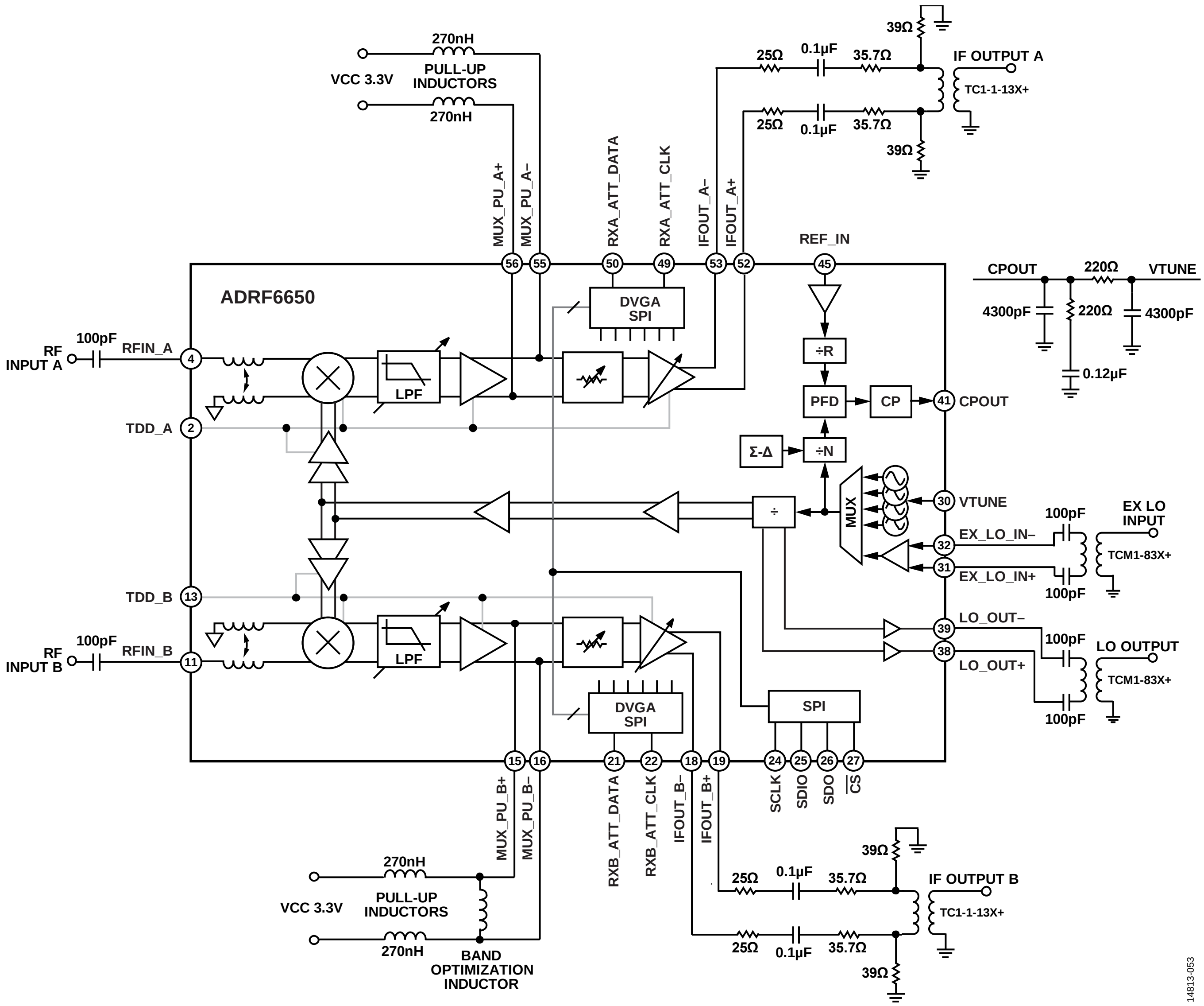

Figure 53. Basic Connections Diagram

Table 17. Basic Connections

Pin No.	Mnemonic	Description	Basic Connection
RF Inputs			The single-ended RF inputs have a 50 Ω impedance. These pins must be ac-coupled. Terminate unused RF inputs with a dc blocking capacitor to GND to improve isolation. See the Layout section for the recommended PCB layout.
4, 11	RFIN_A, RFIN_B	RF inputs	
RF Balun Optimization			Connect the balun tuning inductors (L_{TUNE}x) to ground. See the RF Frequency and IF Bandwidth Optimization section for L_{TUNE}x values.
5, 10	RFBT_A, RFBT_B	RF balun tuning inductor	
TDD_x Pins			Active high. 1.8 V and 3.3 V logic level compatible. See the TDD Operation section for details about TDD pin use.
2, 13	TDD_A, TDD_B	TDD enable control pins	
Serial VGA Control			Follow the layout considerations given under the Layout section.
21, 50	RXB_ATT_DATA, RXA_ATT_DATA	DVGA data pins	
22, 49	RXB_ATT_CLK, RXA_ATT_CLK	DVGA clock pins	

Pin No.	Mnemonic	Description	Basic Connection
3.3 V RF/IF Power			Decouple all power supply pins to ground using 100 pF and 0.1 µF capacitors. Place the decoupling capacitors close to the pins.
1, 14	VCC_MIX_A, VCC_MIX_B	Mixer IF amplifier supply	
6, 9	VCC_LOA_S2, VCC_LOB_S2	LO path supply for Stage 3 and Stage 4	
7, 8	VCC_LOA_S1, VCC_LOB_S1	LO path supply for Stage 1 and Stage 2	
Mixer Supply Pull-Up		IF amplifier pull-up connections	Connect the pull-up pins to 3.3 V RF/IF power supply rail with 270 nH pull-up inductors on each leg. Place the decoupling capacitors of 100 pF and 0.1 µF between the supply rail and the pull-up inductors. Place the inductor to optimize the IF bandwidth ($L_{SHUNT}x$) in between the negative and positive pins. See the RF Frequency and IF Bandwidth Optimization section for $L_{SHUNT}x$ values.
15, 16, 55, 56	MIX_PU_B+, MIX_PU_B−, MIX_PU_A−, MIX_PU_A+		
DVGA Decoupling			Decouple the DVGA decoupling pins to ground using 100 pF and 0.1 µF capacitors and connect to the DVGA power supply rail (5 V). Place the decoupling capacitors close to the pins. Place a resistor divider to divide the power supply for the DVGA into two. Use 5.1 kΩ (or similar) for resistor divider component values.
17, 54	VCPL_B, VCPL_A	DVGA decoupling pins	
5 V Power			Decouple all power supply pins to ground using 100 pF and 0.1 µF capacitors. Place the decoupling capacitors close to the pins.
20, 51	VCC_DVGA_B, VCC_DVGA_A	DVGA power supply	
IF Outputs			Place 25 Ω in series for each differential leg. The differential IF output impedance, together with the series 25 Ω, becomes 60 Ω. For optimized performance, the 60 Ω output impedance must be terminated with a 100 Ω load.
18, 19, 52, 53	IFOUT_A−, IFOUT_B+, IFOUT_A+, IFOUT_A−	IF outputs	
3.3 V PLL/VCO Power			Decouple all power supply pins to ground using 100 pF and 0.1 µF capacitors. Place the decoupling capacitors close to the pins. Employ ferrite beads to provide isolation between the PLL/VCO supply pins. Beware of the series resistance of the ferrite beads and try to minimize the voltage drop.
33	VCCVCO_3V3	VCO 3.3 V supply	
34	VCCDIV_3V3	LO chain and divider 3.3 V supply	
35	VCCFBDIV_3V3	PLL feedback divider 3.3 V supply	
36	VCCLO_MIX_3V3	LO mixer output buffer 3.3 V supply	
37	VCCLO_AUX_3V3	LO external output buffer 3.3 V supply	
42	VCCCP_3V3	Charge pump 3.3 V supply	
43	VCCPFD_3V3	PFD 3.3 V supply	
44	VCCREF_3V3	Reference input buffer 3.3 V supply	
48	VBAT_DIG_3V3	SPI and SDM LDO 3.3 supply V supply	
PLL/VCO			
29	DCL_BIAS	VCO core bias decouple	Decouple this pin to ground using 0.1 µF capacitor.
30	VTUNE	VTUNE input	This pin is driven by the output of the loop filter; its nominal input voltage range is 1.5 V to 2.5 V.
41	CPOUT	Charge pump output	Connect this pin to the VTUNE pin through the loop filter.
45	REF_IN	Reference input buffer	The nominal input level of this pin is 1 V p-p. The input range is 10 MHz to 250 MHz. This pin is internally biased and must be ac-coupled and terminated externally with a 50 Ω resistor. Place the ac coupling capacitor between the pin and the resistor.
46	SPILDO_OUT_1V8	SPI 1.8 V LDO external decouple output	Decouple the decoupling pins to ground using 100 pF and 0.1 µF capacitors. Place the decoupling capacitors close to the pins.
47	SDMLDO_OUT_1V8	SDM 1.8 V LDO external decouple output	Decouple the decoupling pins to ground using 100 pF and 0.1 µF capacitors. Place the decoupling capacitors close to the pins.
23	LO_LCKDT	LO lock detect	This pin has1.8 V/3.3 V logic levels.
Auxiliary LO Output			The differential output impedance of the LO output buffer is 100 Ω.
38, 39	LO_OUT+, LO_OUT−	LO output	

Pin No.	Mnemonic	Description	Basic Connection
External LO Inputs			The differential input impedance of the external LO input buffer is 100 Ω.
31, 32	EXT_LO_IN+, EXT_LO_IN−	External LO input	
Serial Port Interface			
24	SCLK	SPI clock	This pin has1.8 V/3.3 V logic levels.
25	SDIO	SPI data input/output (3-wire mode), input only for 4-wire mode	This pin has 1.8 V/3.3 V logic levels.
26	SDO	SPI data output (4-wire mode), not used for 3-wire mode	This pin has 1.8 V/3.3 V logic levels.
27	$\overline{\text{CS}}$	SPI chip select	Active low. This pin has 1.8 V/3.3 V logic levels.
Reset			
28	$\overline{\text{RST}}$	Reset	Active low. This pin has 1.8 V/3.3 V logic levels.
Ground			
3, 12	GND	Ground	Connect these pins to the ground of the PCB.
40	GND	Charge pump ground	Do not connect this pin to the pad ground; connect this pin to the PCB ground.
Exposed Pad		Exposed pad	The exposed thermal pad is on the bottom of the package. The exposed pad must be soldered to ground.

RF FREQUENCY AND IF BANDWIDTH OPTIMIZATION

The ADRF6650 incorporates a wideband balun at its RF inputs for each channel. The wideband balun requires a tuning inductor (L_{TUNE}x) for optimized performance for various RF frequencies of operation. Optimized L_{TUNE}x provides optimized gain, noise figure, and OIP3. Table 18 provides the L_{TUNE}x values required for some of the popular RF frequency points. As shown in Table 18, the lower the RF frequency, the higher the L_{TUNE}x inductor. Figure 54 incorporates the ADRF6650 RF balun and the tuning inductor.

Table 18. L_{TUNE}x Values for Various RF frequencies

RF Frequency (MHz)	L_{TUNE}x (nH)
450	15
900	3.9
1800	3.9
2700	1

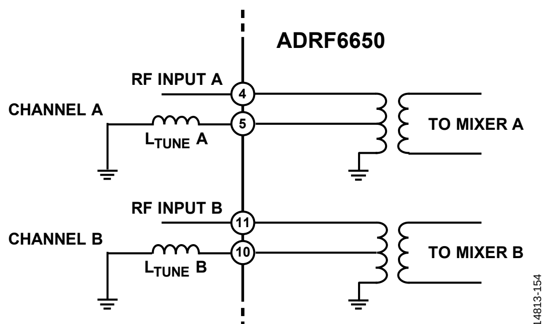

Figure 54. Block Diagram Incorporating L_{TUNE}x

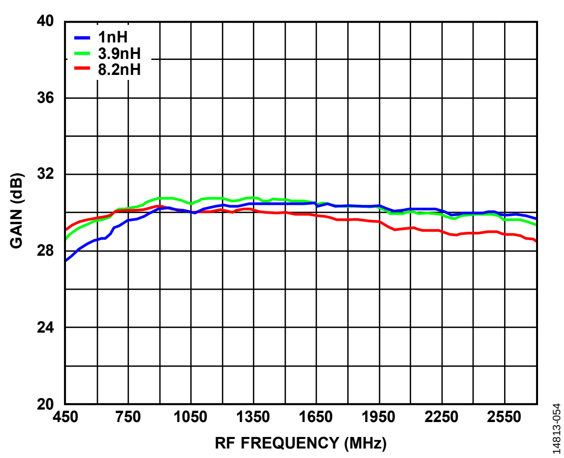

Figure 55. RF Gain Roll-Off for Various L_{TUNE}x Values

The IF amplifier employed within the ADRF6650 requires pull-up inductors tied to a 3.3 V power supply. In addition to these pull-up inductors, an IF band optimization inductor (L_{SHUNT}x) is used for each of the channels, as shown in Figure 54. L_{SHUNT}x places the center of the IF with a 200 MHz bandwidth. Complete coverage of 500 MHz IF bandwidth is achieved by shifting the 200 MHz IF window, as shown in Figure 56. The IF band optimization inductor provides optimized gain flatness and OIP3.

Table 19. IF Band Optimization Inductor Values for Various IF Center Frequencies

IF Center Frequency (MHz)	IF Band Optimization Inductor, L_{SHUNT}x (nH)
120	Open
180	150
270	100
360	47

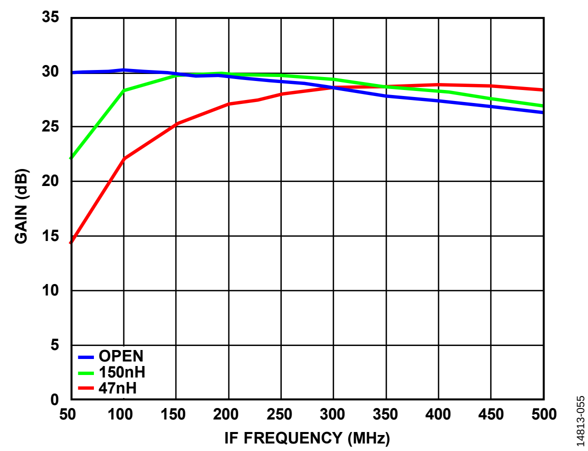

Figure 56. Centering the IF Bandwidth with L_{TUNE}x Gain vs. IF Frequency

IF DVGA VS. LOAD

By design, the ADRF6650 has an output impedance of 10 Ω. The ADRF6650 is optimized to perform with external 25 Ω in each differential leg. External resistors are employed to increase the output impedance. Together with the external 25 Ω, the total differential output impedance equals 60 Ω. With a 100 Ω differential load, the return loss is below −10 dB for a wide range of IF frequency.

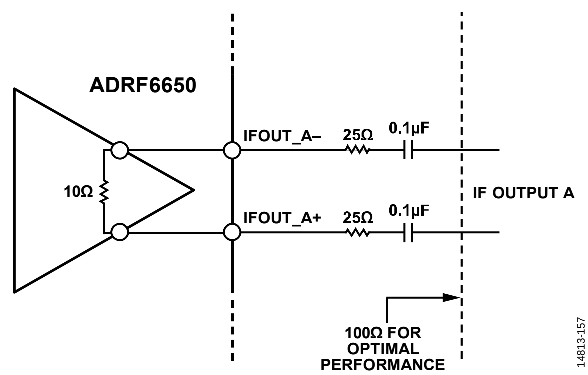

Figure 57. IF Output Schematic, Channel A Output Shown

Different application circuits may require various loading conditions for the IF outputs. Therefore it is important to understand the effect of IF output loading on the performance characteristics, such as OP1dB, gain, OIP3, and OIP2.

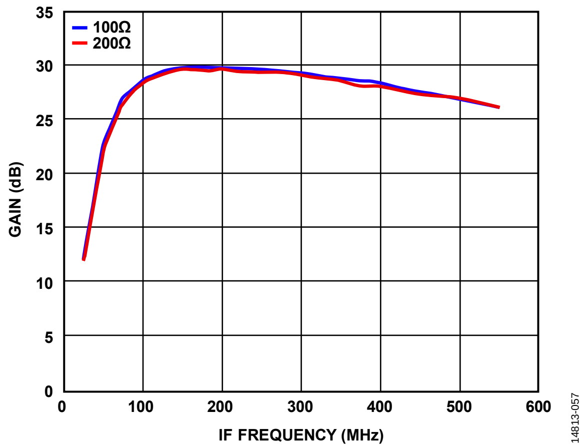

Figure 58. IF Gain vs. IF Frequency for Various Loads

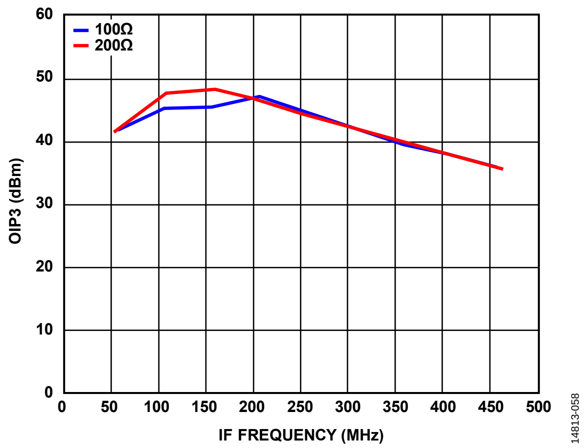

Figure 59. OIP3 vs. IF Frequency for Various Loads

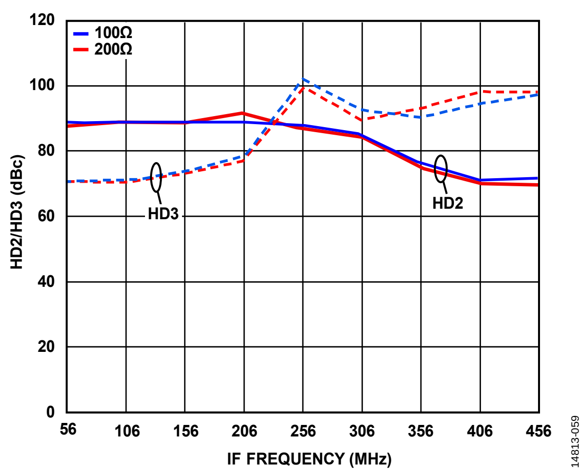

Figure 60. HD2/HD3 vs. IF Frequency for Various Loads

As mentioned previously in this section, the IF outputs are optimized for a load of 100 Ω; however, this may not be the most readily available load impedance. As a result, load vs. performance trade-offs must be considered. Use Figure 58 through Figure 60 as guides only; do not interpret them in the absolute sense. The results are obtained for one chip under nominal voltage and supply.

ADC INTERFACING

The integrated IF DVGA of the ADRF6650 provides variable and sufficient drive capability for both buffered and unbuffered ADCs. The DVGA also provides isolation between the sampling edges of the ADC and the mixer core. As result, only a selective band-pass filter is required when interfacing with an ADC.

The filter resides between the ADRF6650 and the ADC. The band-pass filter eliminates all out-of-band signals that might degrade the performance of the ADRF6650 and ADC pair. The band-pass filter center and bandwidth are selected for the specific application, that is, the topology, system requirements, signal bandwidth, ADC type, and sampling rate. The type and the order of the filter are chosen by taking into account the trade-off between the amount of rejection required and the insertion loss. In this section, a filter design is explained for a band-pass sampling use case with a step by step analysis.

Band-pass sampling is a popular way of reconstructing the information from the received signals, especially for wireless communication standards with high dynamic range requirements. Band-pass sampling relies on the idea that the sampling rate required to completely represent an analog signal is twice the highest frequency of signal bandwidth of interest. With this fact, a signal at a high IF frequency can be reconstructed by accurately placing the signal of interest to one of the Nyquist zones. To better illustrate the idea, a case for IF center frequency of 187.5 MHz with a signal bandwidth of 30 MHz is considered. To place the signal bandwidth to the first Nyquist zone, a sampling rate of 250 MSPS is adequate, which puts the center frequency of the retrieved signal to 62.5 MHz. One important consideration for the band-pass sampling is that all of the Nyquist zones fold on top of each other, which reduces the available dynamic range. To overcome excessive noise due to folding, employ a sharp antialiasing filter between the ADRF6650 and the ADC.

To determine a proper candidate for the ADC, consider the signal-to-noise ratio (SNR)/spurious-free dynamic range (SFDR) and analog input bandwidth requirements. The SNR/SFDR requirements are provided for a given input power. Considering a standard LTE uplink signal with a peak-to-average power ratio (PAPR) of 8 dB to 10 dB, the average input signal power is backed off at least 10 dB from the full scale. The SNR/SFDR of the ADC at the backed off level allows a dynamic range compatible with the system requirements. The analog input specification, alternatively, must be able to cope with the high IF frequency signal (centered at 187.5 MHz). With these requirements in mind, the AD9694 14-bit, 500 MSPS ADC or the AD6684 135 MHz quad IF receiver are proper candidates with an SNR of 68 dBFS and SFDR of 97 dBFS at 10 dB back-off from full scale.

The IF center frequency of the received signal (187.5 MHz) is on the second Nyquist zone for a sampling rate of 250 MSPS. The antialiasing filter provides enough rejection on other Nyquist zones so that inherent folding of the zones does not degrade the SNR and SFDR of the ADC. Considering that there are RF filters (diplexer, SAW, BAW, and others) at the front end of the signal chain, the major spurious contents result from the HD2 and HD3 products of the ADRF6650. As shown in Figure 17, for an ADRF6650 gain of 1 dB, the HD2 and HD3 products are −60 dBc. To avoid degrading the SFDR performance of the AD9694 or AD6684, the antialiasing filter must reject the HD2 and HD3 products by 37 dB (97 dBFS − 60 dBc = 37 dB). Considering the tolerances of the filter components, a filter with a bandwidth of 36 MHz and a rejection of at least 40 dB at second and third harmonic zones is sufficient.

When designing the band-pass filter, it is important to consider the IF output impedance of the ADRF6650 and the input impedance of the ADC. As mentioned in the IF DVGA vs. Load section, the ADRF6650 IF outputs have an impedance of 60 Ω (together with the external 25 Ω on each differential leg) and are optimized for a 100 Ω differential load.

Figure 61 shows a band-pass filter designed around 187.5 MHz with a bandwidth of 36 MHz. Figure 62 shows the return loss of the filter. Figure 63 shows the performance of the filter with and without the ADRF6650.

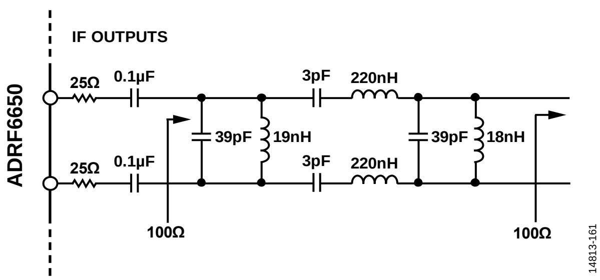

Figure 61. Antialiasing Band-Pass Filter Schematic

Table 20. Component Values for Band Pass Filter Design (Center at 184 MHz and Bandwidth 75 MHz)

Value	Type	Manufacturer
39 pF	0402, NPO	Murata
3 pF	0402, NPO	Murata
18 nH	0402HP	Coilcraft
19 nH	0402HP	Coilcraft
220 nH	0402HP	Coilcraft

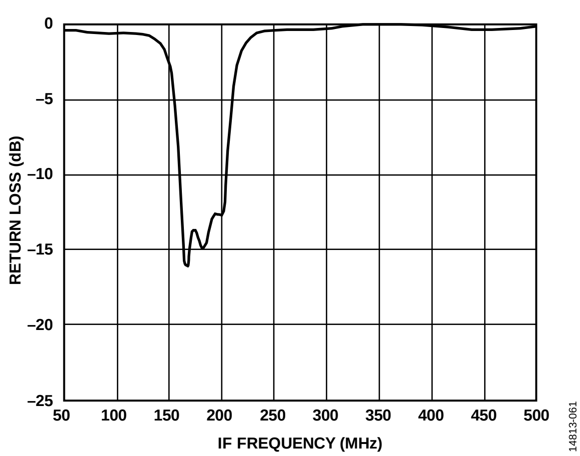

Figure 62. Standalone Return Loss Response

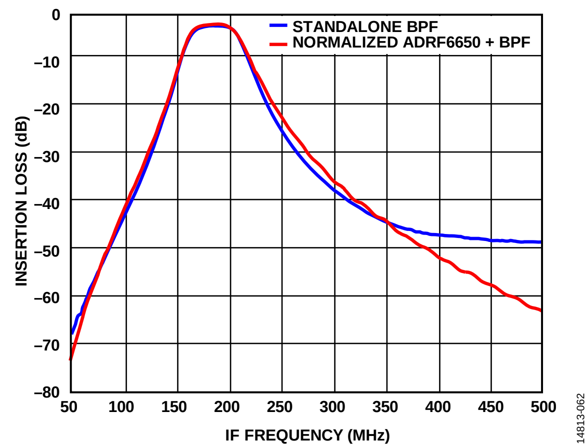

Figure 63. Standalone BPF and Normalized ADRF6650 and Band-Pass Filter Insertion Loss Response

POWER MODES

The ADRF6650 incorporates dual DVGAs that are compatible with either a 5 V or 3.3 V supply. The specifications are given under the 5 V supply condition. However, it is possible to use the DVGA with a 3.3 V supply with decreased gain and OP1dB, whereas a 3.3 V supply consumes the same amount of current, which in turn saves power consumption.

The ADRF6650 allows the user to select between two power modes for each supply voltage: high performance and low power. The 5 V high performance mode achieves the best linearity given in the Specifications section. Alternatively, low power mode enables power consumption savings in return of decreased linearity.

To summarize, the ADRF6650 has four power modes, as outlined in Table 21.

Table 21. Power Mode Bit Settings

Power Mode	DVGA_5V_SEL (Register 0x0103, Bit 7)	DVGA_HP_SEL (Register 0x0104, Bit 6)
DVGA 5 V and High Performance	1	1
DVGA 5 V and Low Power	1	0
DVGA 3.3 V and High Performance	0	1
DVGA 3.3 V and Low Power	0	0

To provide insight on the various power modes of the ADRF6650, Figure 64 to Figure 66 display OP1dB, OIP3, and gain vs. IF frequency.

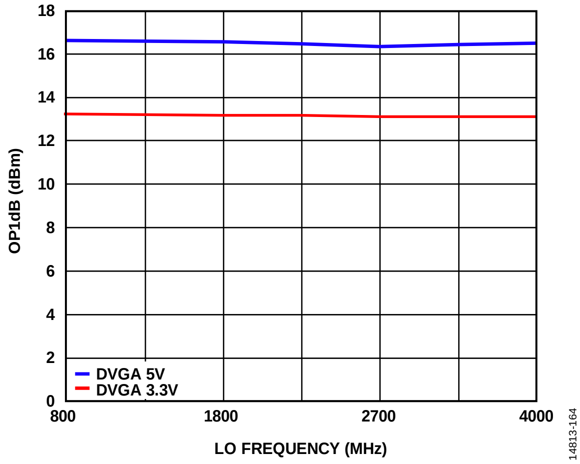

Figure 64. OP1dB vs. LO Frequency for Various Power Modes

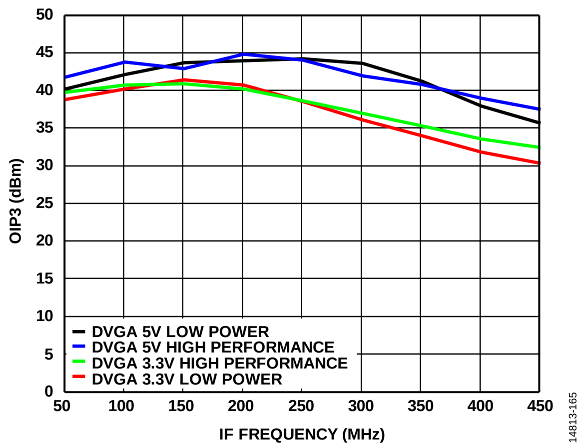

Figure 65. OIP3 vs. IF Frequency for Various Power Modes, f_{LO} = 1800 MHz

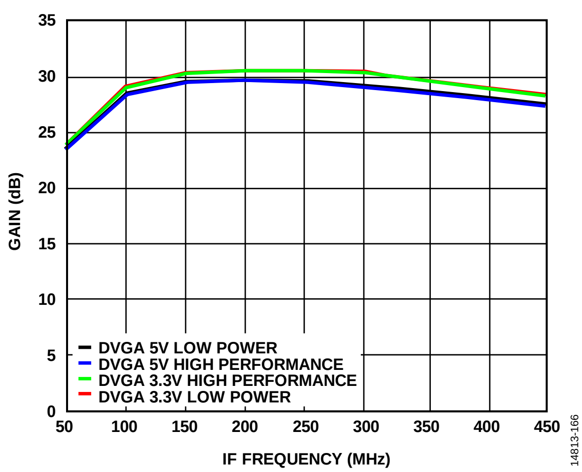

Figure 66. Gain vs. IF Frequency for Various Power Modes, f_{LO} = 1800 MHz

POWER SUPPLY CONFIGURATION

The ADRF6650 employs high performance mixers, IF amplifiers, DVGAs, PLL, and VCOs. To achieve the best performance, especially in terms of spurs and phase noise, the power supply configuration must be dealt with great care.

There are three main supply domains for the ADRF6650, namely, DVGA (5 V), RF/IF (3.3 V), and PLL/VCO (3.3 V). For the best performance, each of the supply domains requires specific attention in the power supply design.

DVGA (5 V) Supply Domain

DVGAs on each channel are supplied thorough the same linear regulator, taking into account the total amount of current drawn. The linear regulator must have high power supply rejection ratio (PSRR) and low noise to avoid spur injection from the supply circuitry. Another consideration is the transient response, which is important for the TDD operation. If the DVGAs are set to turn on and off during TDD cycles, the transient response of the power supply IC may affect the settling time of the ADRF6650. Take care to avoid long transient times. The ADM7170/ADM7171 are ultralow noise, high PSRR, and fast transient response LDOs that are suitable for the DVGA (5 V) supply domain. Their fast transient response ensures that the ADRF6650 settling time is not affected by variations in supply.

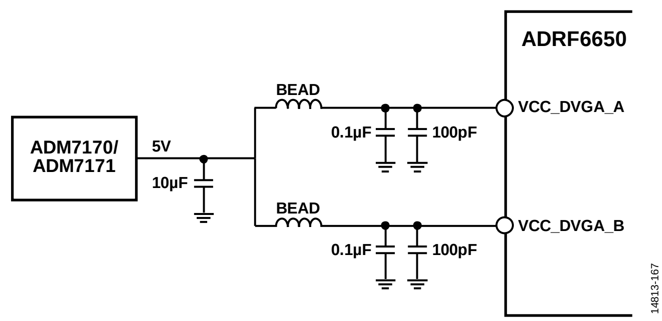

Figure 67. DVGA (5 V) Supply Domain with the ADM7170/ADM7171

RF/IF (3.3 V) Supply Domain

The RF/IF supply domain includes all of the supplies related to RF and IF blocks within the ADRF6650, namely mixers, IF amplifiers, and LO path to the mixers. All of the RF/IF supply domain pins are supplied with the same linear regulator with beads separating each individual pin. Each pin requires its own decoupling capacitors, placed close to the pin.

The linear regulator must have high PSRR and low noise to avoid spur injection from the supply circuitry. Another consideration is the transient response, which becomes important for the TDD operation. If the RF/IF blocks are set to turn on and off during TDD cycles, transient response of the power supply IC can affect the settling time of the ADRF6650. Take care to avoid long transient times. The ADM7170/ADM7171 are ultralow noise, high PSRR, and fast transient response LDOs that are suitable for the RF/IF (3.3 V) supply domain. Their fast transient response ensures that the ADRF6650 settling time is not affected by variations in supply.

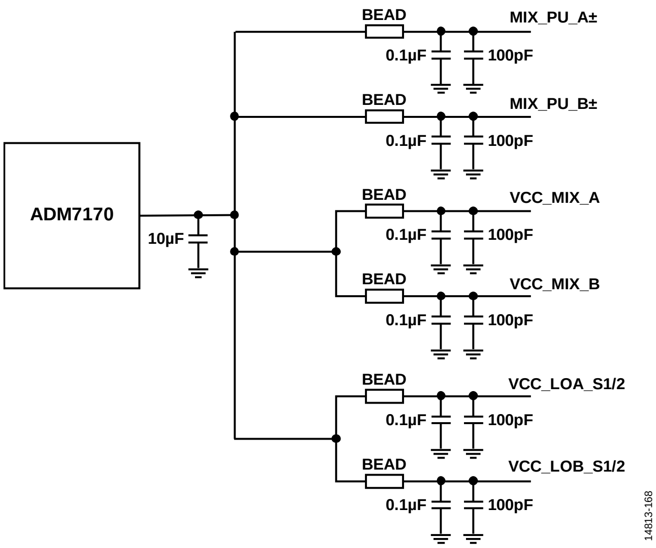

Figure 68. RF/IF (3.3 V) Supply Domain with the ADM7170

Note that if the DVGA is supplied through 3.3 V, the two supply domains can be tied together to reduce the number of power supply ICs. Take care for the increased current drawn from the power supply IC when the DVGA and RF/IF supply domains are connected together.

PLL/VCO (3.3 V) Supply Domain

The PLL/VCO supply domain requires specific attention, which can otherwise result in performance degradation. The ADRF6650 incorporates an ultralow noise PLL/VCO, which is sensitive to any noise and/or frequency component at the supply pins. These unwanted noise and frequency components degrade the performance of the overall system. To avoid performance degradation, the ADRF6650-EVALZ evaluation board employs the PLL/VCO supply domain circuit given in Figure 69, which uses the HMC1060, an ultralow noise LDO with four isolated outputs. Noise performance and isolated outputs makes the HMC1060 the perfect solution for the PLL/VCO supply domain. For more configurability options, see the ADRF6650-EVALZ evaluation board user guide.

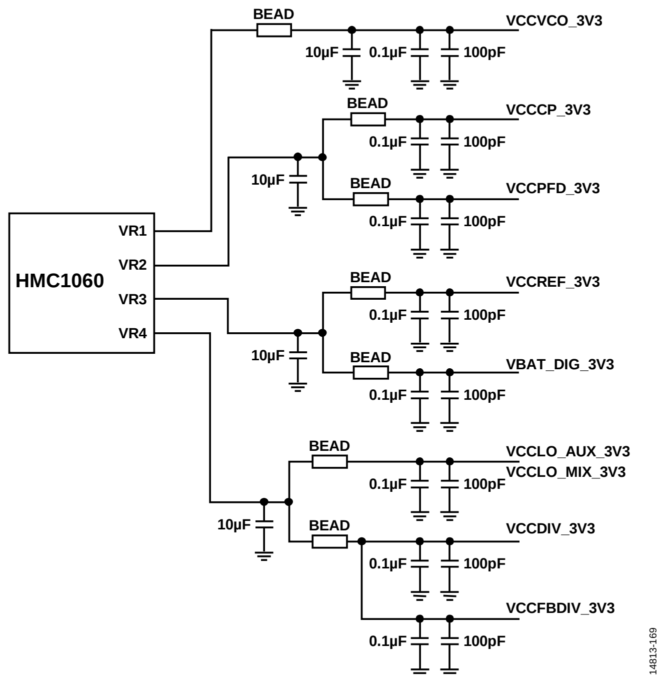

Figure 69. PLL/VCO Domain Power Supply Circuit

LAYOUT

Careful layout of the ADRF6650 is necessary to optimize performance and minimize stray parasitics. Because the ADRF6650 supports two channels, the layout of the RF section is critical in achieving isolation between channels. Figure 70 shows the recommended layout for the RF inputs. The best layout approach is to keep the traces short and direct. In addition, for improved isolation, do not route the RF input traces in parallel to each other and spread the traces immediately after each one leaves the pins. Keep the traces as far away from each other as possible (and at an angle, if possible) to prevent cross coupling.

The input impedance of the RF inputs is 50 Ω, and the traces leading to the pin must also have a 50 Ω characteristic impedance. Terminate the unused RF inputs with a dc blocking capacitor to ground.

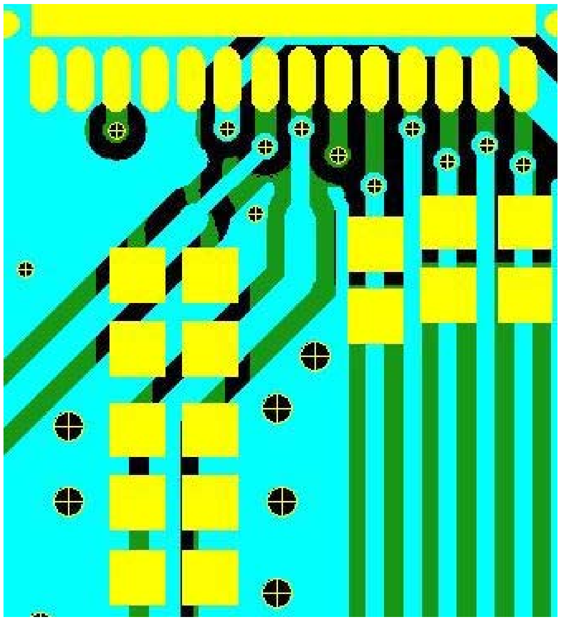

Figure 70. Serial Gain Control Clock and Data Routing (Green is Top Layer, Blue is Inner Layer, Yellow is Component Placement)

The ADRF6650 incorporates a very low noise PLL/VCO, and care must be taken when designing the PCB routing around the PLL/VCO pins. It is required to place the decoupling capacitors for the supply pins as close as possible. If 0402 capacitors are used, placing all of the decoupling capacitors close to the pin becomes problematic. In such a case, place the smaller value decoupling capacitor as close as possible to the pin. It is a good practice to keep the first capacitor of the loop filter close to the CPOUT pin, and the last capacitor close to the VTUNE pin, as shown in Figure 71.

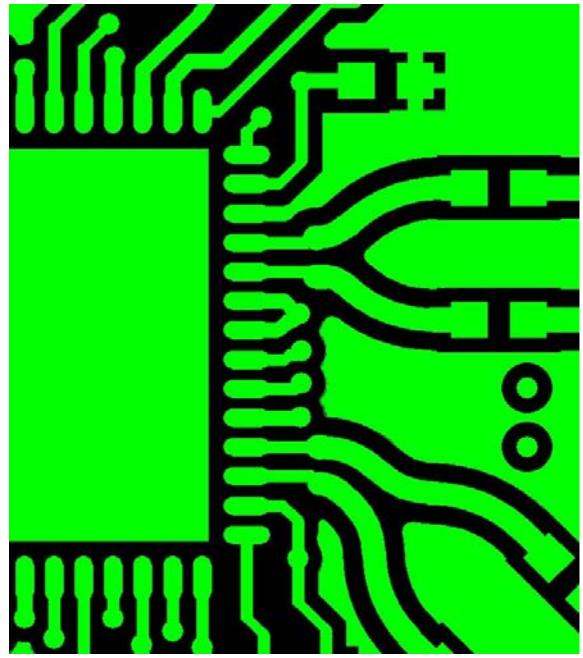

Figure 71. PLL/VCO Pin Connections

REGISTER MAP

Table 22. Register Details

Reg	Name	Bits	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Reset	RW
0x0000	ADI_SPI_CONFIG	[7:0]	SOFTRESET_	LSB_FIRST_	ENDIAN_	SDOACTIVE_	SDOACTIVE	ENDIAN	LSB_FIRST	SOFTRESET	0x00	R/W
0x0001	SPI_CONFIG_B	[7:0]	SINGLE_INSTRUCTION	CSB_STALL	MASTER_SLAVE_RB	RESERVED		SOFT_RESET		MASTER_SLAVE_TRANSFER	0x00	R/W
0x0002	DEVICE_CONFIG	[7:0]	RESERVED				OPERATING_MODE		POWER_MODE		0x00	R/W
0x0003	CHIP_TYPE	[7:0]	CHIPTYPE								0x00	R
0x0004	PRODUCT_ID_1	[7:0]	PRODUCT_ID[7:0]								0x12	R
0x0005	PRODUCT_ID_2	[7:0]	PRODUCT_ID[15:8]								0x00	R
0x000A	SCRATCH	[7:0]	SCRATCHPAD								0x00	R/W
0x000B	SPI_REVISON	[7:0]	SPI_VER								0x00	R
0x000C	VENDOR_ID_L	[7:0]	VENDOR_ID[7:0]								0x56	R
0x000D	VENDOR_ID_H	[7:0]	VENDOR_ID[15:8]								0x04	R
0x0021	BLOCK_RESETS	[7:0]	RESERVED						DVGA_CH2_RSTB	DVGA_CH1_RSTB	0x1F	R/W
0x003C	ATTEN_READBACK_CH1	[7:0]	ATTEN_READBACK_CH1								0x00	R
0x003D	ATTEN_READBACK_CH2	[7:0]	ATTEN_READBACK_CH2								0x00	R
0x003E	DVGA_TRIM_READBACK_CH1	[7:0]	DVGA_TRIM_READBACK_CH1								0x00	R
0x003F	DVGA_TRIM_READBACK_CH2	[7:0]	DVGA_TRIM_READBACK_CH2								0x00	R
0x0100	TDD_BYPASS	[7:0]	DVGA_ENB_CH2	DVGA_ENB_CH1	IF_ENB_CH2	IF_ENB_CH1	LO_STG23_ENB_CH2	LO_STG23_ENB_CH1	LO_STG1_ENB	BYPASS_TDD	0xFE	R/W
0x0101	CONFIG	[7:0]	Reserved	Reserved	IFLIN_BIAS_EN	IFMAIN_BIAS_EN	RESERVED			SPI_18_33_SEL	0x38	R/W
0x0102	EN_MASK	[7:0]	PLL_ENB_CH12_MASK	DVGA_ENB_CH2_MASK	DVGA_ENB_CH1_MASK	IF_ENB_CH2_MASK	IF_ENB_CH1_MASK	LO_STG23_ENB_CH2_MASK	LO_STG23_ENB_CH1_MASK	LO_STG1_ENB_MASK	0x7E	R/W
0x0103	DVGA_MODE	[7:0]	DVGA_5V_SEL	DVGA_FA_STEP		DVGA_UPDN_STEP		DVGA_GAIN_MODE			0x80	R/W
0x0104	DVGA_GAIN1	[7:0]	RESERVED	DVGA_HP_SEL	DVGA_GAIN_CH1						0x68	R/W
0x0105	DVGA_GAIN2	[7:0]	RESERVED		DVGA_GAIN_CH2						0x28	R/W
0x0300	LPF_OVERRIDE	[7:0]	RESERVED	LPF2_OVERRIDE			LPF1_OVERRIDE			LPF_DPLX_EN_OVERRIDE	0x7F	R/W
0x0301	IFMAIN_OVERRIDE	[7:0]	RESERVED				IFMAIN_BIAS_OVERRIDE				0x15	R/W
0x0302	IFLIN_OVERRIDE	[7:0]	RESERVED				IFLIN_BIAS_OVERRIDE				0x1F	R/W
0x0303	VGS_OVERRIDE	[7:0]	RESERVED				VGS_OVERRIDE				0x04	R/W
0x0304	DVGA_TRIM1_LP3V_OVERRIDE	[7:0]	RESERVED			DVGA_TRIM_LP_3V_CH1_OVERRIDE					0x10	R/W
0x0305	DVGA_TRIM1_HP3V_OVERRIDE	[7:0]	RESERVED			DVGA_TRIM_HP_3V_CH1_OVERRIDE					0x10	R/W
0x0306	DVGA_TRIM1_LP5V_OVERRIDE	[7:0]	RESERVED			DVGA_TRIM_LP_5V_CH1_OVERRIDE					0x10	R/W
0x0307	DVGA_TRIM1_HP5V_OVERRIDE	[7:0]	RESERVED			DVGA_TRIM_HP_5V_CH1_OVERRIDE					0x10	R/W
0x0308	DVGA_TRIM2_LP3V_OVERRIDE	[7:0]	RESERVED			DVGA_TRIM_LP_3V_CH2_OVERRIDE					0x10	R/W
0x0309	DVGA_TRIM2_HP3V_OVERRIDE	[7:0]	RESERVED			DVGA_TRIM_HP_3V_CH2_OVERRIDE					0x10	R/W
0x030A	DVGA_TRIM2_LP5V_OVERRIDE	[7:0]	RESERVED			DVGA_TRIM_LP_5V_CH2_OVERRIDE					0x10	R/W
0x030B	DVGA_TRIM2_HP5V_OVERRIDE	[7:0]	RESERVED			DVGA_TRIM_HP_5V_CH2_OVERRIDE					0x10	R/W

Reg	Name	Bits	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Reset	RW
0x0310	OVERRIDE_SELECT	[7:0]	SPARE2_OVERRIDE_SEL	SPARE1_OVERRIDE_SEL	DVGA_TRIM_CH2_OVERRIDE_SEL	DVGA_TRIM_CH1_OVERRIDE_SEL	VGS_OVERRIDE_SEL	IFLIN_TRIM_OVERRIDE_SEL	IFMAIN_TRIM_OVERRIDE_SEL	LPF_TRIM_OVERRIDE_SEL	0x00	R/W
0x1021	BLOCK_RESETS	[7:0]	RESERVED	ARSTB_BLOCK_LKD	ARSTB_BLOCK_AUTOCAL	ARSTB_BLOCK_NDIV	ARSTB_BLOCK_RDIV	ARSTB_BLOCK_DSMOSTG	ARSTB_BLOCK_DSMCORE	ARSTB_BLOCK_DSMALL	0xFF	R/W
0x1032	GPO1_CONTROL	[7:0]	RESERVED	GPO1_BLK_SEL				RESERVED		GPO1_ENABLE	0x02	R/W
0x1033	GPO1_SELECT	[7:0]	GPO1_SGNL_SEL								0x00	R/W
0x1109	SIG_PATH_9_NORMAL	[7:0]	RESERVED			TRM_MIXLODRV_DRV_POUT		TRM_XLODRV_DRV_POUT		RESERVED	0x0A	R/W
0x1200	INT_L	[7:0]	INT_DIV[7:0]								0x89	R/W
0x1201	INT_H	[7:0]	INT_DIV[15:8]								0x01	R/W
0x1202	FRAC1_L	[7:0]	FRAC[7:0]								0x00	R/W
0x1203	FRAC1_M	[7:0]	FRAC[15:8]								0x00	R/W
0x1204	FRAC1_H	[7:0]	FRAC[23:16]								0x00	R/W
0x1205	SD_PHASE_L_0	[7:0]	PHASE[7:0]								0x00	R/W
0x1206	SD_PHASE_M_0	[7:0]	PHASE[15:8]								0x00	R/W
0x1207	SD_PHASE_H_0	[7:0]	PHASE[23:16]								0x00	R/W
0x1208	MOD_L	[7:0]	MOD2[7:0]								0x00	R/W
0x1209	MOD_H	[7:0]	RESERVED		MOD2[13:8]						0x00	R/W
0x120B	SYNTH	[7:0]	RESERVED						PRE_SEL	EN_FBDIV	0x01	R/W
0x120C	R_DIV	[7:0]	RESERVED	R_DIV							0x03	R/W
0x120E	SYNTH_0	[7:0]	RESERVED				DOUBLER_EN	RESERVED		RDIV2_SEL	0x04	R/W
0x1214	MULTI_FUNC_SYNTH_CTRL_0214	[7:0]	LD_BIAS		LDP			RESERVED			0x48	R/W
0x1217	SI_VCO_SEL	[7:0]	RESERVED				SI_VCO_SEL				0x00	R/W
0x121F	VCO_FSM	[7:0]	RESERVED	DISABLE_CAL	RESERVED						0x00	R/W
0x122A	SD_CTRL	[7:0]	RESERVED		SD_EN_FRAC0	SD_EN_OUT_OFF	RESERVED		SD_SM_2	RESERVED	0x02	R/W
0x122C	MULTI_FUNC_SYNTH_CTRL_022C	[7:0]	RESERVED						CP_HIZ		0x03	R/W
0x122D	MULTI_FUNC_SYNTH_CTRL_022D	[7:0]	EN_PFD_CP	BLEED_POL	RESERVED			INT_ABP	RESERVED	BLEED_EN	0x81	R/W
0x122E	CP_CURR	[7:0]	RESERVED				CP_CURRENT				0x0F	R/W
0x122F	BICP	[7:0]	BICP								0x08	R/W
0x1233	FRAC2_L	[7:0]	FRAC2[7:0]								0x00	R/W
0x1234	FRAC2_H	[7:0]	RESERVED		FRAC2[13:8]						0x00	R/W
0x1235	MULTI_FUNC_SYNTH_CTRL_0235	[7:0]	RESERVED						PHASE_ADJ_EN	RESERVED	0x00	R/W
0x1240	VCO_LUT_CTRL	[7:0]	RESERVED			SI_VCO_FORCE_CAPSVCOI	RESERVED		SI_VCO_FORCE_VCO	SI_VCO_FORCE_CAPS	0x00	R/W
0x124D	LOCK_DETECT	[7:0]	RESERVED							LOCK_DETECT	0x00	R
0x1401	MULTI_FUNC_CTRL	[7:0]	RESERVED			SPI_1P8_3P3_CTRL	RESERVED				0x00	R/W
0x140E	LO_CNTRL2	[7:0]	EN_BIAS_R	RESERVED	REFBUF_EN	RESERVED					0xB3	R/W
0x1414	LO_CNTRL8	[7:0]	MIX_OE	LO_OE	USEEXT_LOI	OUT_DIVRATIO					0x02	R/W
0x1541	FRAC2_L_SLAVE	[7:0]	FRAC2_SLV[7:0]								0x00	R
0x1542	FRAC2_H_SLAVE	[7:0]	RESERVED		FRAC2_SLV[13:8]						0x00	R
0x1543	FRAC_L_SLAVE	[7:0]	FRAC_SLV[7:0]								0x00	R
0x1544	FRAC_M_SLAVE	[7:0]	FRAC_SLV[15:8]								0x00	R

Reg	Name	Bits	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Reset	RW
0x1545	FRAC_H_SLAVE2	[7:0]	FRAC_SLV[23:16]								0x00	R
0x1546	PHASE_L_SLAVE	[7:0]	PHASE_SLV[7:0]								0x00	R
0x1547	PHASE_M_ SLAVE2	[7:0]	PHASE_SLV[15:8]								0x00	R
0x1548	PHASE_H_ SLAVE3	[7:0]	PHASE_SLV[23:16]								0x00	R
0x1549	INT_DIV_L_ SLAVE	[7:0]	INT_DIV_SLV[7:0]								0x89	R
0x154A	INT_DIV_H_ SLAVE	[7:0]	INT_DIV_SLV[15:8]								0x01	R
0x154B	R_DIV_SLAVE	[7:0]	RESERVED	R_DIV_SLV							0x03	R
0x154C	RDIV2_SEL_ SLAVE	[7:0]	RESERVED							RDIV2_SEL_ SLV	0x00	R
0x1583	DISABLE_CFG	[7:0]	RESERVED			DSM_LAUNCH_DLY		DISABLE_ FREQHOP	DISABLE_ DBLBUFFERING	DISABLE_ PHASEADJ	0x00	R/W

REGISTER DETAILS

Address: 0x0000, Reset: 0x00, Name: ADI_SPI_CONFIG

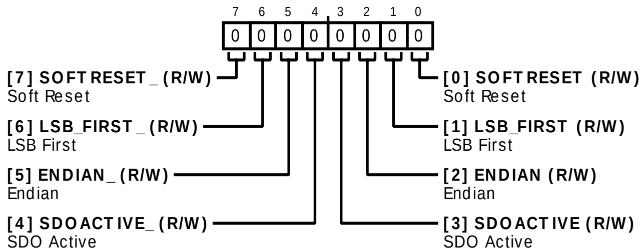

Table 23. Bit Descriptions for ADI_SPI_CONFIG

Bits	Bit Name	Settings	Description	Reset	Access
7	SOFTRESET_		Soft Reset	0x0	R/W
6	LSB_FIRST_		LSB First	0x0	R/W
5	ENDIAN_		Endian	0x0	R/W
4	SDOACTIVE_		SDO Active	0x0	R/W
3	SDOACTIVE		SDO Active	0x0	R/W
2	ENDIAN		Endian	0x0	R/W
1	LSB_FIRST		LSB First	0x0	R/W
0	SOFTRESET		Soft Reset	0x0	R/W

Address: 0x0001, Reset: 0x00, Name: SPI_CONFIG_B

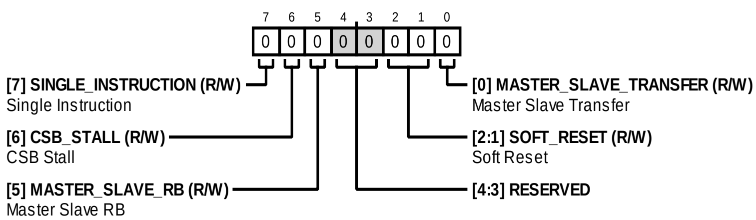

Table 24. Bit Descriptions for SPI_CONFIG_B

Bits	Bit Name	Settings	Description	Reset	Access
7	SINGLE_INSTRUCTION		Single Instruction	0x0	R/W
6	CSB_STALL		CSB Stall	0x0	R/W
5	MASTER_SLAVE_RB		Master Slave RB	0x0	R/W
[4:3]	RESERVED		Reserved	0x0	R/W
[2:1]	SOFT_RESET		Soft Reset	0x0	R/W
0	MASTER_SLAVE_TRANSFER		Master Slave Transfer	0x0	R/W

Address: 0x0002, Reset: 0x00, Name: DEVICE_CONFIG

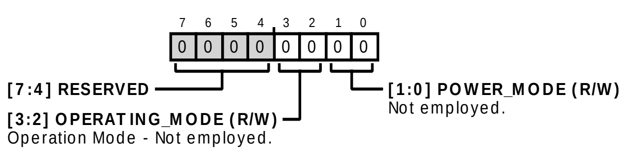

Table 25. Bit Descriptions for DEVICE_CONFIG

Bits	Bit Name	Settings	Description	Reset	Access
[7:4]	RESERVED		Reserved.	0x0	R
[3:2]	OPERATING_MODE		Operation Mode - Not employed.	0x0	R/W
[1:0]	POWER_MODE		Not employed.	0x0	R/W

Address: 0x0003, Reset: 0x00, Name: CHIP_TYPE

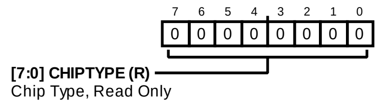

Table 26. Bit Descriptions for CHIP_TYPE

Bits	Bit Name	Settings	Description	Reset	Access
[7:0]	CHIPTYPE		Chip Type, Read Only	0x0	R

Address: 0x0004, Reset: 0x12, Name: Product_ID_1

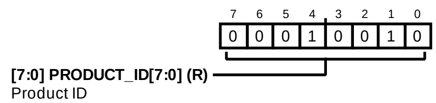

Table 27. Bit Descriptions for Product_ID_1

Bits	Bit Name	Settings	Description	Reset	Access
[7:0]	PRODUCT_ID[7:0]		Product ID	0x12	R

Address: 0x0005, Reset: 0x00, Name: Product_ID_2

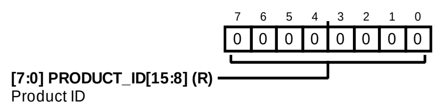

Table 28. Bit Descriptions for Product_ID_2

Bits	Bit Name	Settings	Description	Reset	Access
[7:0]	PRODUCT_ID[15:8]		Product ID	0x12	R

Address: 0x000A, Reset: 0x00, Name: Scratch

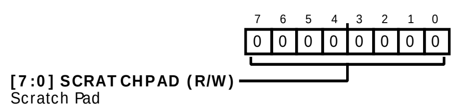

Table 29. Bit Descriptions for Scratch

Bits	Bit Name	Settings	Description	Reset	Access
[7:0]	SCRATCHPAD		Scratch Pad	0x0	R/W

Address: 0x000B, Reset: 0x00, Name: SPI_Revision

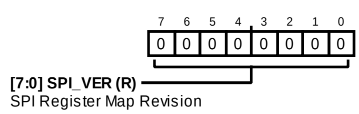

Table 30. Bit Descriptions for SPI_Revision

Bits	Bit Name	Settings	Description	Reset	Access
[7:0]	SPI_VER		SPI Register Map Revision	0x0	R

Address: 0x000C, Reset: 0x56, Name: VENDOR_ID_L

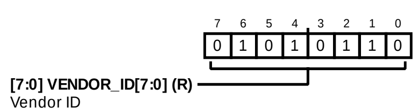

Table 31. Bit Descriptions for VENDOR_ID_L

Bits	Bit Name	Settings	Description	Reset	Access
[7:0]	VENDOR_ID[7:0]		Vendor ID	0x456	R

Address: 0x000D, Reset: 0x04, Name: VENDOR_ID_H

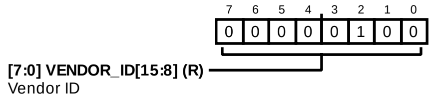

Table 32. Bit Descriptions for VENDOR_ID_H

Bits	Bit Name	Settings	Description	Reset	Access
[7:0]	VENDOR_ID[15:8]		Vendor ID	0x456	R

Address: 0x0021, Reset: 0x1F, Name: BLOCK_RESETS

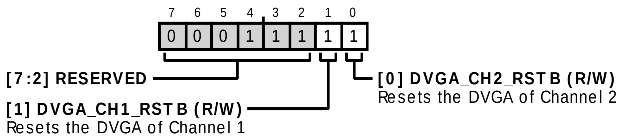

Table 33. Bit Descriptions for BLOCK_RESETS

Bits	Bit Name	Settings	Description	Reset	Access
[7:2]	RESERVED		Reserved.	0x7	R
1	DVGA_CH1_RSTB		Resets the DVGA of Channel 1	0x1	R/W
0	DVGA_CH2_RSTB		Resets the DVGA of Channel 2	0x1	R/W

Address: 0x003C, Reset: 0x00, Name: ATTEN_READBACK_CH1

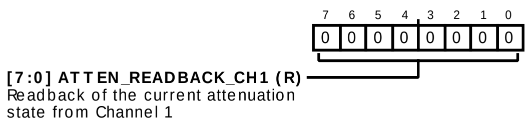

Table 34. Bit Descriptions for ATTEN_READBACK_CH1

Bits	Bit Name	Settings	Description	Reset	Access
[7:0]	ATTEN_READBACK_CH1		Readback of the current attenuation state from Channel 1	0x0	R

Address: 0x003D, Reset: 0x00, Name: ATTEN_READBACK_CH2

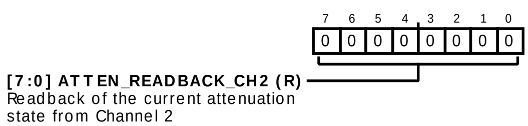

Table 35. Bit Descriptions for ATTEN_READBACK_CH2

Bits	Bit Name	Settings	Description	Reset	Access
[7:0]	ATTEN_READBACK_CH2		Readback of the current attenuation state from Channel 2	0x0	R

Address: 0x003E, Reset: 0x00, Name: DVGA_TRIM_READBACK_CH1

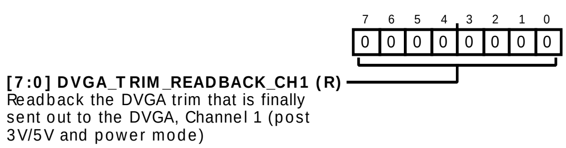

Table 36. Bit Descriptions for DVGA_TRIM_READBACK_CH1

Bits	Bit Name	Settings	Description	Reset	Access
[7:0]	DVGA_TRIM_READBACK_CH1		Readback the DVGA trim that is finally sent out to the DVGA, Channel 1 (post 3 V/5 V and power mode)	0x0	R

Address: 0x003F, Reset: 0x00, Name: DVGA_TRIM_READBACK_CH2

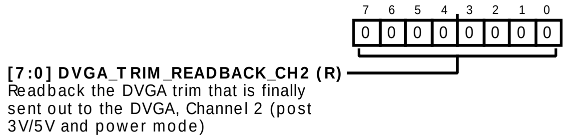

Table 37. Bit Descriptions for DVGA_TRIM_READBACK_CH2

Bits	Bit Name	Settings	Description	Reset	Access
[7:0]	DVGA_TRIM_READBACK_CH2		Readback the DVGA trim that is finally sent out to the DVGA, Channel 2 (post 3 V/5 V and power mode)	0x0	R

Address: 0x0100, Reset: 0xFE, Name: TDD_BYPASS

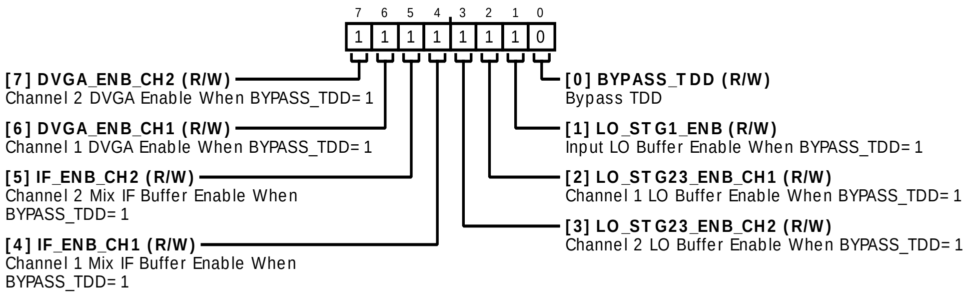

Table 38. Bit Descriptions for TDD_BYPASS

Bits	Bit Name	Settings	Description	Reset	Access
7	DVGA_ENB_CH2		Channel 2 DVGA Enable When BYPASS_TDD = 1	0x1	R/W
6	DVGA_ENB_CH1		Channel 1 DVGA Enable When BYPASS_TDD = 1	0x1	R/W
5	IF_ENB_CH2		Channel 2 Mix IF Buffer Enable When BYPASS_TDD = 1	0x1	R/W
4	IF_ENB_CH1		Channel 1 Mix IF Buffer Enable When BYPASS_TDD = 1	0x1	R/W
3	LO_STG23_ENB_CH2		Channel 2 LO Buffer Enable When BYPASS_TDD = 1	0x1	R/W
2	LO_STG23_ENB_CH1		Channel 1 LO Buffer Enable When BYPASS_TDD = 1	0x1	R/W
1	LO_STG1_ENB		Input LO Buffer Enable When BYPASS_TDD = 1	0x1	R/W
0	BYPASS_TDD		Bypass TDD	0x0	R/W

Address: 0x0101, Reset: 0x38, Name: CONFIG

Table 39. Bit Descriptions for CONFIG

Bits	Bit Name	Settings	Description	Reset	Access
5	IFLIN_BIAS_EN		Enable Internal Bias Adjustment for IF Amplifier Linearization	0x1	R/W
4	IFMAIN_BIAS_EN		Enable Internal Bias Adjustment for IF Amplifier	0x1	R/W
[3:1]	RESERVED		Reserved	0x4	R/W
0	SPI_18_33_SEL		SPI Tristate Buffer Output Voltage Level, 0 = 1.8 V, 1 = 3.3 V	0x0	R/W

Address: 0x0102, Reset: 0x7E, Name: EN_MASK

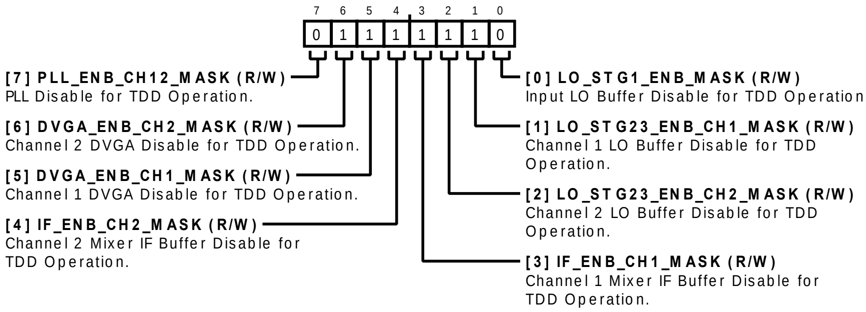

Table 40. Bit Descriptions for EN_MASK

Bits	Bit Name	Settings	Description	Reset	Access
7	PLL_ENB_CH12_MASK		PLL Disable for TDD Operation. Pass PLL disable to PLL when TDD_A and TDD_B are both high. PLL Blocks disable according to PLL register setting	0x0	R/W
6	DVGA_ENB_CH2_MASK		Channel 2 DVGA Disable for TDD Operation. 1 = disable when TDD_A is high (active low), 0 = enable.	0x1	R/W
5	DVGA_ENB_CH1_MASK		Channel 1 DVGA Disable for TDD Operation. 1 = disable when TDD_A is high (active low), 0 = enable.	0x1	R/W
4	IF_ENB_CH2_MASK		Channel 2 Mixer IF Buffer Disable for TDD Operation. 1 = disable when TDD_A is high (active low), 0 = enable.	0x1	R/W
3	IF_ENB_CH1_MASK		Channel 1 Mixer IF Buffer Disable for TDD Operation. 1 = disable when TDD_A is high (active low), 0 = enable.	0x1	R/W
2	LO_STG23_ENB_CH2_MASK		Channel 2 LO Buffer Disable for TDD Operation. 1 = disable when TDD_A is high (active low), 0 = enable.	0x1	R/W
1	LO_STG23_ENB_CH1_MASK		Channel 1 LO Buffer Disable for TDD Operation. 1 = disable when TDD_A is high (active low), 0 = enable.	0x1	R/W
0	LO_STG1_ENB_MASK		Input LO Buffer Disable for TDD Operation. 1 = disable when TDD_A is high (active low), 0 = enable.	0x0	R/W

Address: 0x0103, Reset: 0x80, Name: DVGA_MODE

Table 41. Bit Descriptions for DVGA_MODE

Bits	Bit Name	Settings	Description	Reset	Access
7	DVGA_5V_SEL		5 V Power Supply Select for DVGA. 1 = 5 V mode.	0x1	R/W
[4:3]	DVGA_UPDN_STEP		VGA Up-Down Gain Step Size for Both Channels.	0x0	R/W
		0	1 dB		
		1	2 dB		
		10	4 dB		
		11	8 dB		
[2:0]	DVGA_GAIN_MODE		VGA Gain Mode for Both Channels.	0x0	R/W
		1	SPI		
		11	Up/Down		

Address: 0x0104, Reset: 0x68, Name: DVGA_GAIN1

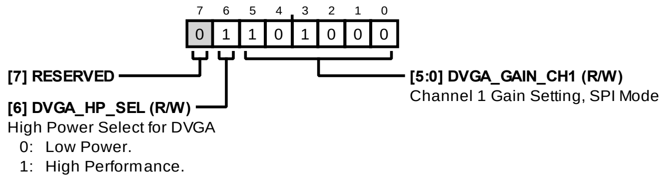

Table 42. Bit Descriptions for DVGA_GAIN1

Bits	Bit Name	Settings	Description	Reset	Access
7	RESERVED		Reserved	0x0	R
6	DVGA_HP_SEL		High Power Select for DVGA	0x1	R/W
		0	Low Power		
		1	High Performance		
[5:0]	DVGA_GAIN_CH1		Channel 1 Gain Setting, SPI Mode	0x28	R/W

Address: 0x0105, Reset: 0x28, Name: DVGA_GAIN2

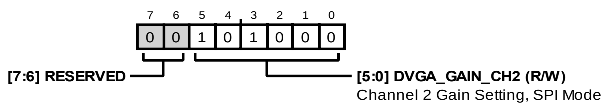

Table 43. Bit Descriptions for DVGA_GAIN2

Bits	Bit Name	Settings	Description	Reset	Access
[7:6]	RESERVED		Reserved	0x0	R
[5:0]	DVGA_GAIN_CH2		Channel 2 Gain Setting, SPI Mode	0x28	R/W

Address: 0x0300, Reset: 0x7F, Name: LPF_OVERRIDE

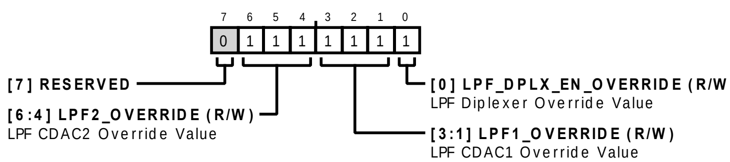

Table 44. Bit Descriptions for LPF_OVERRIDE

Bits	Bit Name	Settings	Description	Reset	Access
7	RESERVED		Reserved	0x0	R
[6:4]	LPF2_OVERRIDE		LPF CDAC2 Override Value	0x7	R/W
[3:1]	LPF1_OVERRIDE		LPF CDAC1 Override Value	0x7	R/W
0	LPF_DPLX_EN_OVERRIDE		LPF Diplexer Override Value	0x1	R/W

Address: 0x0301, Reset: 0x15, Name: IFMAIN_OVERRIDE

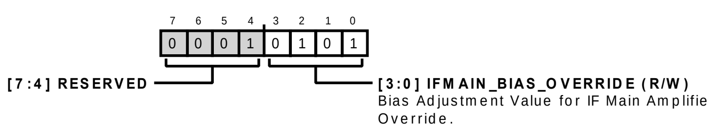

Table 45. Bit Descriptions for IFMAIN_OVERRIDE

Bits	Bit Name	Settings	Description	Reset	Access
[7:4]	RESERVED		Reserved	0x1	R/W
[3:0]	IFMAIN_BIAS_OVERRIDE		Bias Adjustment for IF Main Amplifier Override Value	0x5	R/W

Address: 0x0302, Reset: 0x1F, Name: IFLIN_OVERRIDE

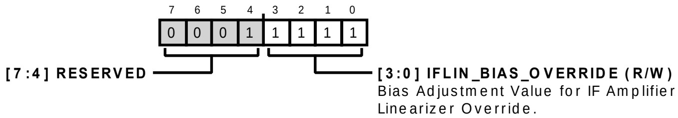

Table 46. Bit Descriptions for IFLIN_OVERRIDE

Bits	Bit Name	Settings	Description	Reset	Access
[7:4]	RESERVED		Reserved	0x1	R/W
[3:0]	IFLIN_BIAS_OVERRIDE		Bias Adjustment Value for IF Amplifier Linearizer Override	0xF	R/W

Address: 0x0303, Reset: 0x04, Name: VGS_OVERRIDE

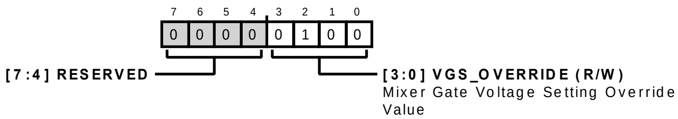

Table 47. Bit Descriptions for VGS_OVERRIDE

Bits	Bit Name	Settings	Description	Reset	Access
[7:4]	RESERVED		Reserved.	0x0	R/W
[3:0]	VGS_OVERRIDE		Mixer Gate Voltage Setting Override Value	0x4	R/W

Address: 0x0304, Reset: 0x10, Name: DVGA_TRIM1_LP3V_OVERRIDE

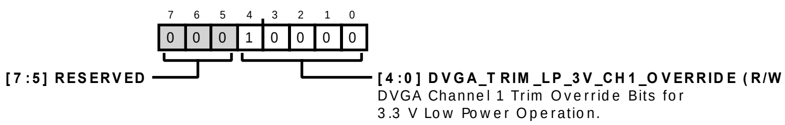

Table 48. Bit Descriptions for DVGA_TRIM1_LP3V_OVERRIDE

Bits	Bit Name	Settings	Description	Reset	Access
[7:5]	RESERVED		Reserved.	0x0	R
[4:0]	DVGA_TRIM_LP_3V_CH1_OVERRIDE		DVGA Channel 1 Trim Override Bits for 3.3 V Low Power Operation. When DVGA_5V_SEL = 0 and DVGA_HP_SEL = 0.	0x10	R/W

Address: 0x0305, Reset: 0x10, Name: DVGA_TRIM1_HP3V_OVERRIDE

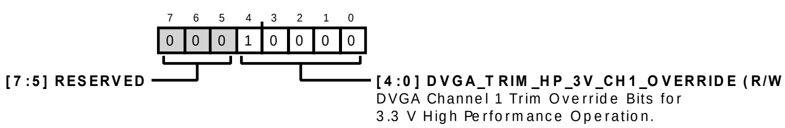

Table 49. Bit Descriptions for DVGA_TRIM1_HP3V_OVERRIDE

Bits	Bit Name	Settings	Description	Reset	Access
[7:5]	RESERVED		Reserved.	0x0	R
[4:0]	DVGA_TRIM_HP_3V_CH1_OVERRIDE		DVGA Channel 1 Trim Override Bits for 3.3 V High Performance Operation. When DVGA_5V_SEL = 0 and DVGA_HP_SEL = 1.	0x10	R/W

Address: 0x0306, Reset: 0x10, Name: DVGA_TRIM1_LP5V_OVERRIDE

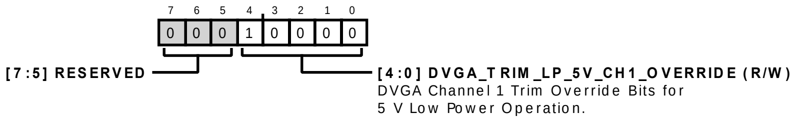

Table 50. Bit Descriptions for DVGA_TRIM1_LP5V_OVERRIDE

Bits	Bit Name	Settings	Description	Reset	Access
[7:5]	RESERVED		Reserved.	0x0	R
[4:0]	DVGA_TRIM_LP_5V_CH1_OVERRIDE		DVGA Channel 1 Trim Override Bits for 5 V Low Power Operation. When DVGA_5V_SEL = 1 and DVGA_HP_SEL = 0.	0x10	R/W

Address: 0x0307, Reset: 0x10, Name: DVGA_TRIM1_HP5V_OVERRIDE

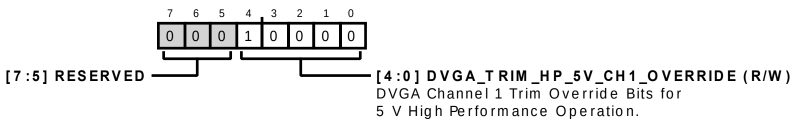

Table 51. Bit Descriptions for DVGA_TRIM1_HP5V_OVERRIDE

Bits	Bit Name	Settings	Description	Reset	Access
[7:5]	RESERVED		Reserved.	0x0	R
[4:0]	DVGA_TRIM_HP_5V_CH1_OVERRIDE		DVGA Channel 1 Trim Override Bits for 5 V High Performance Operation. When DVGA_5V_SEL = 1 and DVGA_HP_SEL = 1	0x10	R/W

Address: 0x0308, Reset: 0x10, Name: DVGA_TRIM2_LP3V_OVERRIDE

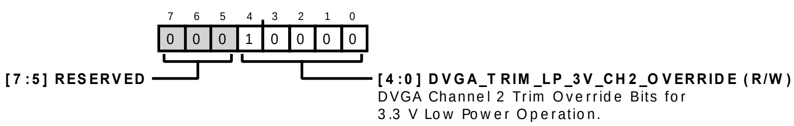

Table 52. Bit Descriptions for DVGA_TRIM2_LP3V_OVERRIDE

Bits	Bit Name	Settings	Description	Reset	Access
[7:5]	RESERVED		Reserved.	0x0	R
[4:0]	DVGA_TRIM_LP_3V_CH2_OVERRIDE		DVGA Channel 2 Trim Override Bits for 3.3 V Low Power Operation. When DVGA_5V_SEL = 0 and DVGA_HP_SEL = 0.	0x10	R/W

Address: 0x0309, Reset: 0x10, Name: DVGA_TRIM2_HP3V_OVERRIDE

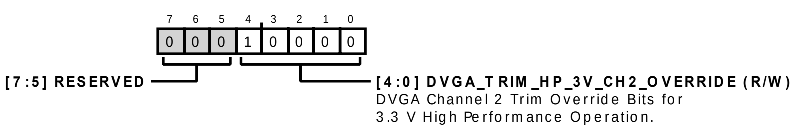

Table 53. Bit Descriptions for DVGA_TRIM2_HP3V_OVERRIDE

Bits	Bit Name	Settings	Description	Reset	Access
[7:5]	RESERVED		Reserved.	0x0	R
[4:0]	DVGA_TRIM_HP_3V_CH2_OVERRIDE		DVGA Channel 2 Trim Override Bits for 3.3 V High Performance Operation. When DVGA_5V_SEL = 0 and DVGA_HP_SEL = 1.	0x10	R/W

Address: 0x0310, Reset: 0x00, Name: OVERRIDE_SELECT

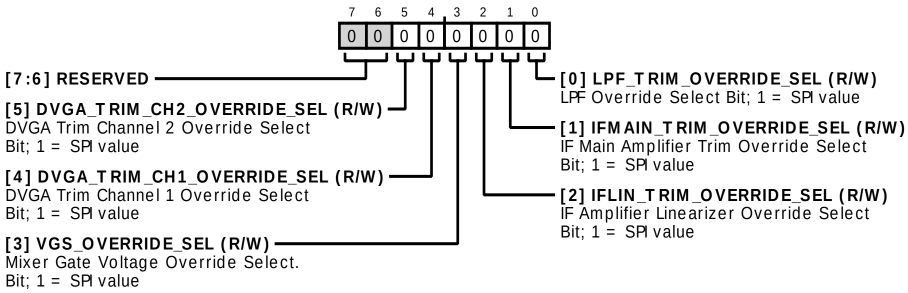

Table 56. Bit Descriptions for OVERRIDE_SELECT

Bits	Bit Name	Settings	Description	Reset	Access
[7:6]	RESERVED		Reserved.	0x0	R/W
5	DVGA_TRIM_CH2_OVERRIDE_SEL		DVGA Trim Channel 2 Override Select Bit; 1 = SPI value	0x0	R/W
4	DVGA_TRIM_CH1_OVERRIDE_SEL		DVGA Trim Channel 1 Override Select Bit; 1 = SPI value	0x0	R/W
3	VGS_OVERRIDE_SEL		Mixer Gate Voltage Override Select. Bit; 1 = SPI value	0x0	R/W
2	IFLIN_TRIM_OVERRIDE_SEL		IF Amplifier Linearizer Override Select Bit; 1 = SPI value	0x0	R/W
1	IFMAIN_TRIM_OVERRIDE_SEL		IF Main Amplifier Trim Override Select Bit; 1 = SPI value	0x0	R/W
0	LPF_TRIM_OVERRIDE_SEL		LPF Override Select Bit; 1 = SPI value	0x0	R/W

Address: 0x1021, Reset: 0xFF, Name: BLOCK_RESETS

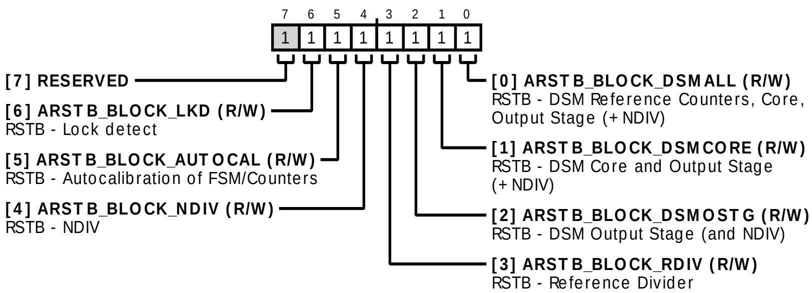

Table 57. Bit Descriptions for BLOCK_RESETS

Bits	Bit Name	Settings	Description	Reset	Access
7	RESERVED		Reserved.	0x1	R/W
6	ARSTB_BLOCK_LKD		RSTB - Lock detect	0x1	R/W
5	ARSTB_BLOCK_AUTOCAL		RSTB - Autocalibration of FSM/Counters	0x1	R/W
4	ARSTB_BLOCK_NDIV		RSTB - NDIV	0x1	R/W
3	ARSTB_BLOCK_RDIV		RSTB - Reference Divider	0x1	R/W
2	ARSTB_BLOCK_DSMOSTG		RSTB - DSM Output Stage (and NDIV)	0x1	R/W
1	ARSTB_BLOCK_DSMCORE		RSTB - DSM Core and Output Stage (+NDIV)	0x1	R/W
0	ARSTB_BLOCK_DSMALL		RSTB - DSM Reference Counters, Core, Output Stage (+NDIV)	0x1	R/W

Address: 0x1032, Reset: 0x02, Name: GPO1_CONTROL

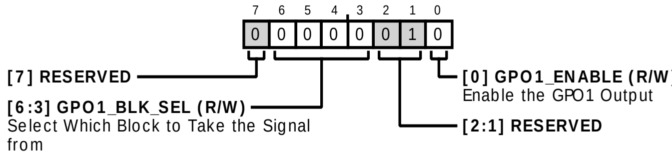

Table 58. Bit Descriptions for GPO1_CONTROL

Bits	Bit Name	Settings	Description	Reset	Access
7	RESERVED		Reserved.	0x0	R/W
[6:3]	GPO1_BLK_SEL		Select Which Block to Take the Signal from	0x0	R/W
[2:1]	RESERVED		Reserved.	0x0	R/W
0	GPO1_ENABLE		Enable the GPO1 Output	0x0	R/W

Address: 0x1033, Reset: 0x00, Name: GPO1_SELECT

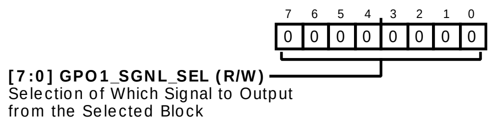

Table 59. Bit Descriptions for GPO1_SELECT

Bits	Bit Name	Settings	Description	Reset	Access
[7:0]	GPO1_SGNL_SEL		Selection of Which Signal to Output from the Selected Block	0x0	R/W

Address: 0x1109, Reset: 0x0A, Name: SIG_PATH_9_NORMAL

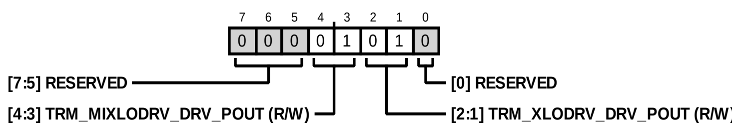

Table 60. Bit Descriptions for SIG_PATH_9_NORMAL

Bits	Bit Name	Settings	Description	Reset	Access
[7:5]	RESERVED		Reserved	0x0	R
[4:3]	TRM_MIXLODRV_DRV_POUT		LO Output to Mixer Power Level	0x1	R/W
[2:1]	TRM_XLODRV_DRV_POUT		Auxiliary LO output Power Level	0x1	R/W
0	RESERVED		Reserved	0x0	R

Address: 0x1200, Reset: 0x89, Name: INT_L

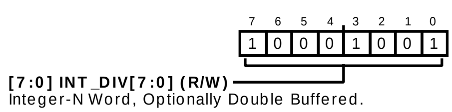

Table 61. Bit Descriptions for INT_L

Bits	Bit Name	Settings	Description	Reset	Access
[7:0]	INT_DIV[7:0]		Integer-N Word, Optionally Double Buffered. Writing the LSB of the integer word normally causes an autotune event.	0x189	R/W

Address: 0x1201, Reset: 0x01, Name: INT_H

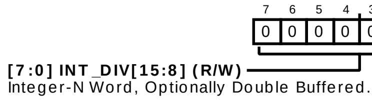

Table 62. Bit Descriptions for INT_H

Bits	Bit Name	Settings	Description	Reset	Access
[7:0]	INT_DIV[15:8]		Integer-N Word, Optionally Double Buffered. Writing the LSB of the integer word normally causes an autotune event.	0x189	R/W

Address: 0x1202, Reset: 0x00, Name: FRAC1_L

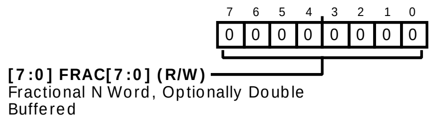

Table 63. Bit Descriptions for FRAC1_L

Bits	Bit Name	Settings	Description	Reset	Access
[7:0]	FRAC[7:0]		Fractional-N Word, Optionally Double Buffered. Lower 8 bits of 24-bit FRAC value.	0x0	R/W

Address: 0x1203, Reset: 0x00, Name: FRAC1_M

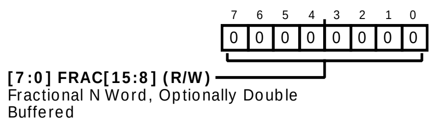

Table 64. Bit Descriptions for FRAC1_M

Bits	Bit Name	Settings	Description	Reset	Access
[7:0]	FRAC[15:8]		Fractional-N Word, Optionally Double Buffered. Lower 8 bits of 24-bit FRAC value.	0x0	R/W

Address: 0x1204, Reset: 0x00, Name: FRAC1_H

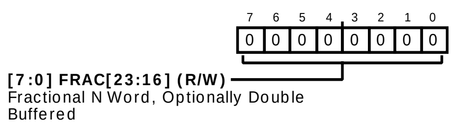

Table 65. Bit Descriptions for FRAC1_H

Bits	Bit Name	Settings	Description	Reset	Access
[7:0]	FRAC[23:16]		Fractional-N Word, Optionally Double Buffered. Lower 8 bits of 24-bit FRAC value.	0x0	R/W

Address: 0x1205, Reset: 0x00, Name: SD_PHASE_L_0

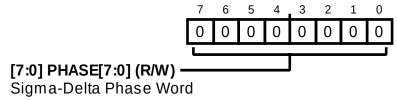

Table 66. Bit Descriptions for SD_PHASE_L_0

Bits	Bit Name	Settings	Description	Reset	Access
[7:0]	PHASE[7:0]		Sigma-Delta Phase Word. Lower bits. If phase adjust mode is enabled (PHASE_ADJ_EN = 1), the phase in the DSM is incremented by this amount on each phase adjustment trigger. The phase adjustment trigger can be caused from SPI, via a write to the LSB of this register (provided DISABLE_PHASEADJ = 0), or from the GPI port. The value is represented as an unsigned 24-bit fractional-Number, in units of VCO cycles. It therefore has a resolution of 21 μ°. For example, to adjust the phase by 5° of the fundamental VCO, program this word to $(5°/360°) \times 2^{24} = 233{,}017$. This process can be done repetitively to effectively recede by multiple VCO cycles, or to embed the PLL itself inside phase or frequency control loops under some other supervisory control. The phase adjust feature must not be done any faster than once every 5 PFD cycles, and by no more than 180° on any individual adjustment.	0x0	R/W

Address: 0x1206, Reset: 0x00, Name: SD_PHASE_M_0

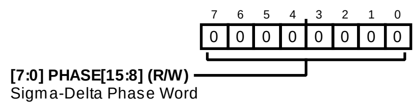

Table 67. Bit Descriptions for SD_PHASE_M_0

Bits	Bit Name	Settings	Description	Reset	Access
[7:0]	PHASE[15:8]		Sigma-Delta Phase Word. Middle bits. See description for SD_PHASE_L_0.	0x0	R/W

Address: 0x1207, Reset: 0x00, Name: SD_PHASE_H_0

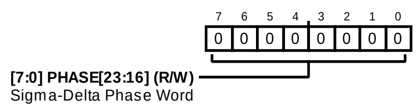

Table 68. Bit Descriptions for SD_PHASE_H_0

Bits	Bit Name	Settings	Description	Reset	Access
[7:0]	PHASE[23:16]		Sigma-Delta Phase Word. Upper bits. See description for SD_PHASE_L_0.	0x0	R/W

Address: 0x1208, Reset: 0x00, Name: MOD_L

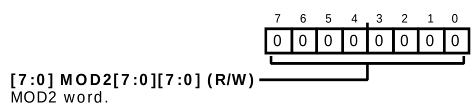

Table 69. Bit Descriptions for MOD_L

Bits	Bit Name	Settings	Description	Reset	Access
[7:0]	MOD2[7:0][7:0]		MOD2 word. Upper bits.	0x0	R/W

Address: 0x1209, Reset: 0x00, Name: MOD_H

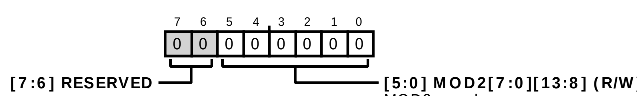

Table 70. Bit Descriptions for MOD_H

Bits	Bit Name	Settings	Description	Reset	Access
[7:6]	RESERVED		Reserved	0x0	R
[5:0]	MOD2[7:0][13:8]		MOD2 word. Upper bits.	0x0	R/W

Address: 0x120B, Reset: 0x01, Name: SYNTH

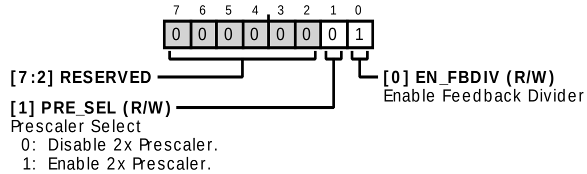

Table 71. Bit Descriptions for SYNTH

Bits	Bit Name	Settings	Description	Reset	Access
[7:2]	RESERVED		Reserved.	0x0	R
1	PRE_SEL		Prescaler Select	0x0	R/W
		0	Disable 2x Prescaler.		
		1	Enable 2x Prescaler.		
0	EN_FBDIV		Enable Feedback Divider	0x1	R/W

Address: 0x120C, Reset: 0x03, Name: R_DIV

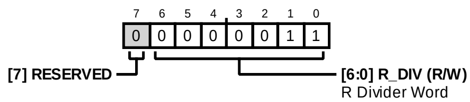

Table 72. Bit Descriptions for R_DIV

Bits	Bit Name	Settings	Description	Reset	Access
7	RESERVED		Reserved.	0x0	R
[6:0]	R_DIV		R Divider Word. Lower 8 bits of 10-bit reference R divider word.	0x3	R/W

Address: 0x120E, Reset: 0x04, Name: SYNTH_0

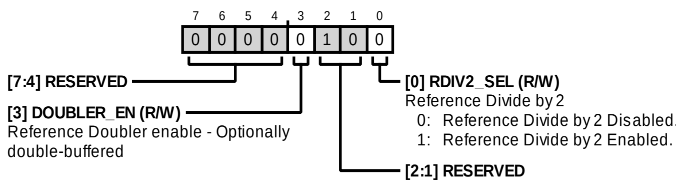

Table 73. Bit Descriptions for SYNTH_0

Bits	Bit Name	Settings	Description	Reset	Access
[7:4]	RESERVED		Reserved	0x0	R
3	DOUBLER_EN		Reference Doubler Enable, Optionally Double-Buffered	0x0	R/W
[2:1]	RESERVED		Reserved	0x2	R/W
0	RDIV2_SEL		Reference Divide by 2	0x0	R/W
		0	Reference Divide by 2 Disabled		
		1	Reference Divide by 2 Enabled		

Address: 0x1214, Reset: 0x48, Name: MULTI_FUNC_SYNTH_CTRL_0214

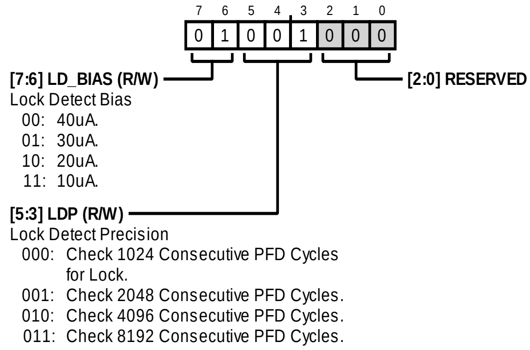

Table 74. Bit Descriptions for MULTI_FUNC_SYNTH_CTRL_0214

Bits	Bit Name	Settings	Description	Reset	Access
[7:6]	LD_BIAS		Lock Detect Bias	0x1	R/W
		00	40 μA		
		01	30 μA		
		10	20 μA		
		11	10 μA		
[5:3]	LDP		Lock Detect Precision	0x1	R/W
		000	Check 1024 Consecutive PFD Cycles for Lock		
		001	Check 2048 Consecutive PFD Cycles		
		010	Check 4096 Consecutive PFD Cycles		
		011	Check 8192 Consecutive PFD Cycles		
[2:0]	RESERVED		Reserved	0x0	R/W

Address: 0x1217, Reset: 0x00, Name: SI_VCO_SEL

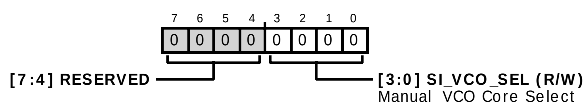

Table 75. Bit Descriptions for SI_VCO_SEL

Bits	Bit Name	Settings	Description	Reset	Access
[7:4]	RESERVED		Reserved	0x0	R
[3:0]	SI_VCO_SEL		Manual VCO Core Select	0x0	R/W

Address: 0x121F, Reset: 0x00, Name: VCO_FSM

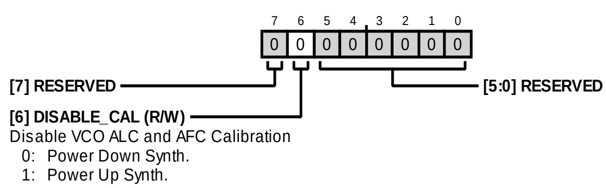

Table 76. Bit Descriptions for VCO_FSM

Bits	Bit Name	Settings	Description	Reset	Access
7	RESERVED		Reserved.	0x0	R
6	DISABLE_CAL		Disable VCO ALC and AFC Calibration. The PLL does not reset the calibration machine, or trigger a new calibration if set to 1 on a frequency hop to maintain ALC and capacitor positions.	0x0	R/W
		0	Power Down Synth.		
		1	Power Up Synth.		
[5:0]	RESERVED		Reserved.	0x0	R/W

Address: 0x122A, Reset: 0x02, Name: SD_CTRL

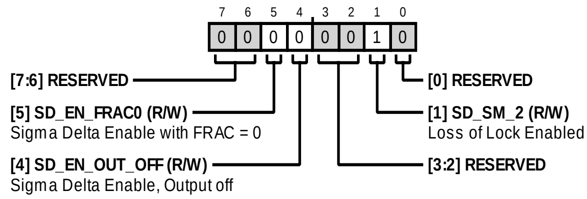

Table 77. Bit Descriptions for SD_CTRL

Bits	Bit Name	Settings	Description	Reset	Access
[7:6]	RESERVED		Reserved.	0x0	R/W
5	SD_EN_FRAC0		Sigma-Delta Enable with FRAC = 0. The DSM normally recognizes a FRAC value of all 0, and disables itself. Setting this mode can keep the DSM running even when a zero fractional is presented.	0x0	R/W
4	SD_EN_OUT_OFF		Sigma-Delta Enable, Output Off. Keeps the DSM core enabled and clocking, but ignores the output of the DSM and instead muxes the N divider setpoint from the double-buffer data directly.	0x0	R/W
[3:2]	RESERVED		Reserved.	0x0	R
1	SD_SM_2		Loss of Lock Enabled. Enables the CSP/LOL circuit. Recommend reserved 1.	0x1	R/W
0	RESERVED		Reserved.	0x0	R/W

Address: 0x122C, Reset: 0x03, Name: MULTI_FUNC_SYNTH_CTRL_022C

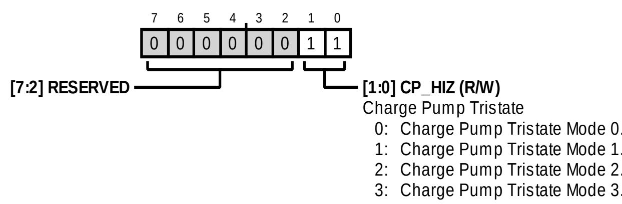

Table 78. Bit Descriptions for MULTI_FUNC_SYNTH_CTRL_022C

Bits	Bit Name	Settings	Description	Reset	Access
[7:2]	RESERVED		Reserved	0x0	R
[1:0]	CP_HIZ		Charge Pump Tristate	0x3	R/W
		0	Charge Pump Tristate Mode 0		
		1	Charge Pump Tristate Mode 1		
		2	Charge Pump Tristate Mode 2		
		3	Charge Pump Tristate Mode 3		

Address: 0x122D, Reset: 0x81, Name: MULTI_FUNC_SYNTH_CTRL_022D

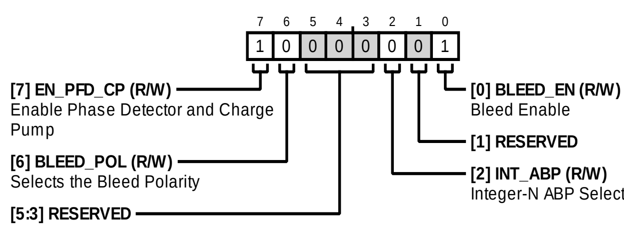

Table 79. Bit Descriptions for MULTI_FUNC_SYNTH_CTRL_022D

Bits	Bit Name	Settings	Description	Reset	Access
7	EN_PFD_CP		Enable Phase Detector and Charge Pump.	0x1	R/W
6	BLEED_POL		Selects the Bleed Polarity.	0x0	R/W
[5:3]	RESERVED		Reserved.	0x0	R
2	INT_ABP		Integer-N ABP Select. Shortens the reset delay of the PFD by 4 inverters.	0x0	R/W
1	RESERVED		Reserved.	0x0	R
0	BLEED_EN		Bleed Enable.	0x1	R/W

Address: 0x122E, Reset: 0x0F, Name: CP_CURR

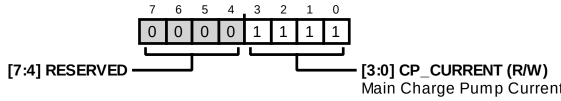

Table 80. Bit Descriptions for CP_CURR

Bits	Bit Name	Settings	Description	Reset	Access
[7:4]	RESERVED		Reserved	0x0	R
[3:0]	CP_CURRENT		Main Charge Pump Current	0xF	R/W

Address: 0x122F, Reset: 0x08, Name: BICP

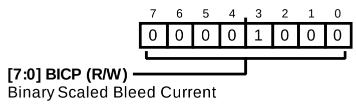

Table 81. Bit Descriptions for BICP

Bits	Bit Name	Settings	Description	Reset	Access
[7:0]	BICP		Binary Scaled Bleed Current	0x8	R/W

Address: 0x1233, Reset: 0x00, Name: FRAC2_L

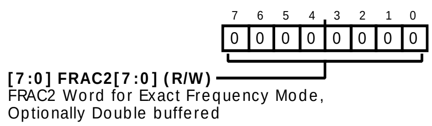

Table 82. Bit Descriptions for FRAC2_L

Bits	Bit Name	Settings	Description	Reset	Access
[7:0]	FRAC2[7:0]		FRAC2 Word for Exact Frequency Mode, Optionally Double Buffered	0x0	R/W

Address: 0x1234, Reset: 0x00, Name: FRAC2_H

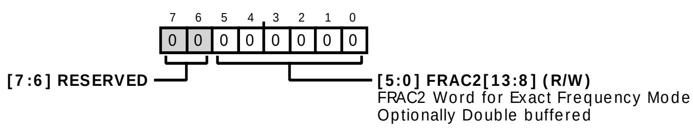

Table 83. Bit Descriptions for FRAC2_H

Bits	Bit Name	Settings	Description	Reset	Access
[7:6]	RESERVED		Reserved.	0x0	R
[5:0]	FRAC2[13:8]		FRAC2 Word for Exact Frequency Mode, Optionally Double Buffered	0x0	R/W

Address: 0x1235, Reset: 0x00, Name: MULTI_FUNC_SYNTH_CTRL_0235

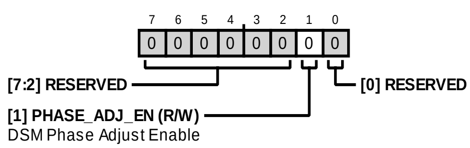

Table 84. Bit Descriptions for MULTI_FUNC_SYNTH_CTRL_0235

Bits	Bit Name	Settings	Description	Reset	Access
[7:2]	RESERVED		Reserved.	0x0	R
1	PHASE_ADJ_EN		DSM Phase Adjust Enable. If set to 1, a phase adjust trigger causes a phase shift in the delta-sigma by the amount programmed in the phase word. The phase trigger is either caused by a write to the LSB of the phase word or through a GPI trigger.	0x0	R/W
0	RESERVED		Reserved.	0x0	R

Address: 0x1240, Reset: 0x00, Name: VCO_LUT_CTRL

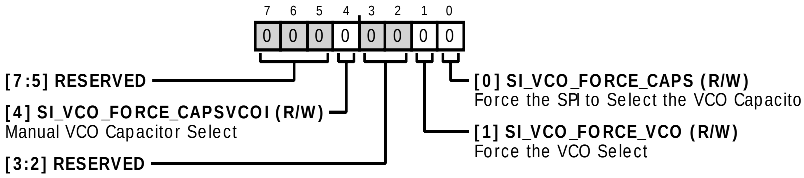

Table 85. Bit Descriptions for VCO_LUT_CTRL

Bits	Bit Name	Settings	Description	Reset	Access
[7:5]	RESERVED		Reserved	0x0	R
4	SI_VCO_FORCE_CAPSVCOI		Manual VCO Capacitor Select	0x0	R/W
[3:2]	RESERVED		Reserved	0x0	R/W
1	SI_VCO_FORCE_VCO		Force the VCO Select	0x0	R/W
0	SI_VCO_FORCE_CAPS		Force the SPI to Select the VCO Capacitor	0x0	R/W

Address: 0x124D, Reset: 0x00, Name: LOCK_DETECT

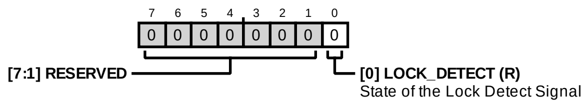

Table 86. Bit Descriptions for LOCK_DETECT

Bits	Bit Name	Settings	Description	Reset	Access
[7:1]	RESERVED		Reserved	0x0	R
0	LOCK_DETECT		State of the Lock Detect Signal	0x0	R

Address: 0x1401, Reset: 0x00, Name: MULTI_FUNC_CTRL

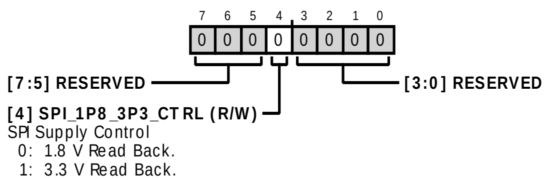

Table 87. Bit Descriptions for MULTI_FUNC_CTRL

Bits	Bit Name	Settings	Description	Reset	Access
[7:5]	RESERVED		Reserved	0x0	R
4	SPI_1P8_3P3_CTRL		SPI Supply Control	0x0	R/W
		0	1.8 V Read Back		
		1	3.3 V Read Back		
[3:0]	RESERVED		Reserved	0x0	R

Address: 0x140E, Reset: 0xB3, Name: LO_CNTRL2

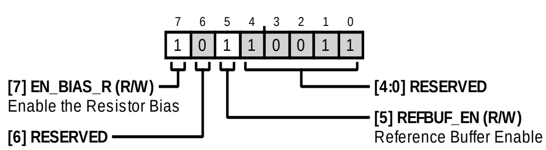

Table 88. Bit Descriptions for LO_CNTRL2

Bits	Bit Name	Settings	Description	Reset	Access
7	EN_BIAS_R		Enable the Resistor Bias. Selects the resistor bias instead of bandgap-based bias for the LO path.	0x1	R/W
6	RESERVED		Reserved.	0x0	R/W
5	REFBUF_EN		Reference Buffer Enable.	0x1	R/W
[4:0]	RESERVED		Reserved.	0x13	R/W

Address: 0x1414, Reset: 0x02, Name: LO_CNTRL8

Recommended register for use to control the LO path from a single spot. By programming this register, all of the individual block enables and configuration bits are set appropriately.

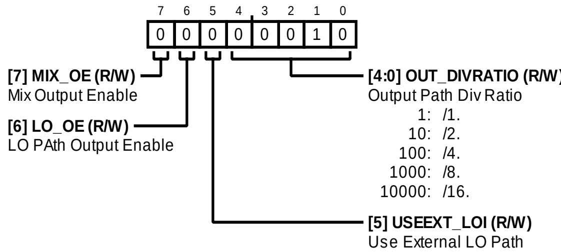

Table 89. Bit Descriptions for LO_CNTRL8

Bits	Bit Name	Settings	Description	Reset	Access
7	MIX_OE		Mix Output Enable. When disabled (MIX_OE = 0), MUTE = 1, or DIVRATIO = 0, the mute depth is selected via GEN_MUTE_DEPTH. Note that the mute depth may be artificially restricted if the other output path is still enabled and relies on a shared branch of the LO chain.	0x0	R/W
6	LO_OE		LO Path Output Enable. When disabled (LO_OE = 0), MUTE = 1, or DIVRATIO = 0, the mute depth is selected via GEN_MUTE_DEPTH. Note that the mute depth may be artificially restricted if the other output path is still enabled and relies on a shared branch of the LO chain.	0x0	R/W
5	USEEXT_LOI		Use External LO Path.	0x0	R/W
[4:0]	OUT_DIVRATIO		Output Path Divide Ratio. Sets the divide ratio from the fundamental VCOs or external input path to the output paths. Nominally, the internal VCO range is 4 GHz to 8 GHz. 0 = mute.	0x2	R/W
		1	/1.		
		10	/2.		
		100	/4.		
		1000	/8.		
		10000	/16.		

Address: 0x1541, Reset: 0x00, Name: FRAC2_L_SLAVE

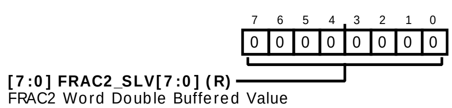

Table 90. Bit Descriptions for FRAC2_L_SLAVE

Bits	Bit Name	Settings	Description	Reset	Access
[7:0]	FRAC2_SLV[7:0]		FRAC2 Word Double Buffered Value	0x0	R

Address: 0x1542, Reset: 0x00, Name: FRAC2_H_SLAVE

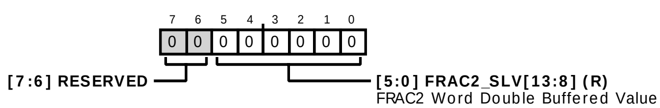

Table 91. Bit Descriptions for FRAC2_H_SLAVE

Bits	Bit Name	Settings	Description	Reset	Access
[7:6]	RESERVED		Reserved	0x0	R
[5:0]	FRAC2_SLV[13:8]		FRAC2 Word Double Buffered Value	0x0	R

Address: 0x1543, Reset: 0x00, Name: FRAC_L_SLAVE

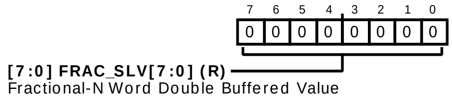

Table 92. Bit Descriptions for FRAC_L_SLAVE

Bits	Bit Name	Settings	Description	Reset	Access
[7:0]	FRAC_SLV[7:0]		Fractional-N Word Double Buffered Value. Lower 8 bits of 24-bit FRAC value.	0x0	R

Address: 0x1544, Reset: 0x00, Name: FRAC_M_SLAVE

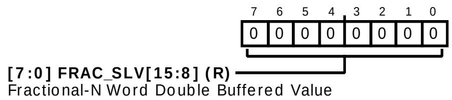

Table 93. Bit Descriptions for FRAC_M_SLAVE

Bits	Bit Name	Settings	Description	Reset	Access
[7:0]	FRAC_SLV[15:8]		Fractional-N Word Double Buffered Value. Middle 8 bits of 24-bit FRAC value.	0x0	R

Address: 0x1545, Reset: 0x00, Name: FRAC_H_SLAVE2

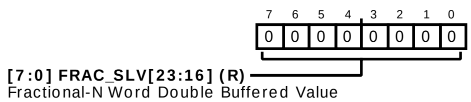

Table 94. Bit Descriptions for FRAC_H_SLAVE2

Bits	Bit Name	Settings	Description	Reset	Access
[7:0]	FRAC_SLV[23:16]		Fractional-N Word Double Buffered Value. Higher 8 bits of 24-bit FRAC value.	0x0	R

Address: 0x1546, Reset: 0x00, Name: PHASE_L_SLAVE

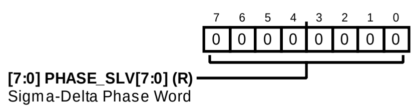

Table 95. Bit Descriptions for PHASE_L_SLAVE

Bits	Bit Name	Settings	Description	Reset	Access
[7:0]	PHASE_SLV[7:0]		Sigma-Delta Phase Word. Lower 8 bits of 24-bit SD phase word.	0x0	R

Address: 0x1547, Reset: 0x00, Name: PHASE_M_SLAVE2

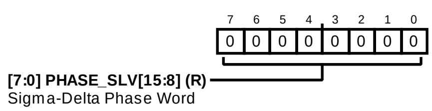

Table 96. Bit Descriptions for PHASE_M_SLAVE2

Bits	Bit Name	Settings	Description	Reset	Access
[7:0]	PHASE_SLV[15:8]		Sigma-Delta Phase Word. Middle 8 bits of 24-bit SD phase word.	0x0	R

Address: 0x1548, Reset: 0x00, Name: PHASE_H_SLAVE3

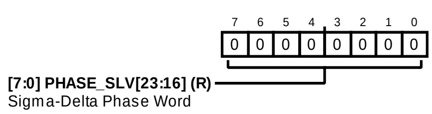

Table 97. Bit Descriptions for PHASE_H_SLAVE3

Bits	Bit Name	Settings	Description	Reset	Access
[7:0]	PHASE_SLV[23:16]		Sigma-Delta Phase Word. Lower Higher 8 bits of 24-bit SD phase word.	0x0	R

Address: 0x1549, Reset: 0x89, Name: INT_DIV_L_SLAVE

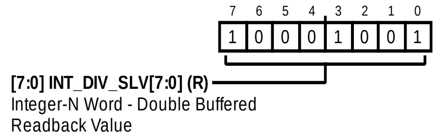

Table 98. Bit Descriptions for INT_DIV_L_SLAVE

Bits	Bit Name	Settings	Description	Reset	Access
[7:0]	INT_DIV_SLV[7:0]		Integer-N Word, Double Buffered Readback Value. Readback data from the N setpoint double buffer output.	0x189	R

Address: 0x154A, Reset: 0x01, Name: INT_DIV_H_SLAVE

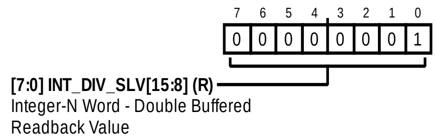

Table 99. Bit Descriptions for INT_DIV_H_SLAVE

Bits	Bit Name	Settings	Description	Reset	Access
[7:0]	INT_DIV_SLV[15:8]		Integer-N Word, Double Buffered Readback Value. Readback data from the N setpoint double buffer output.	0x189	R

Address: 0x154B, Reset: 0x03, Name: R_DIV_SLAVE

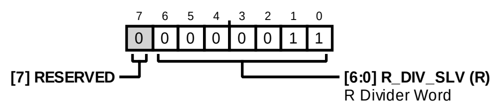

Table 100. Bit Descriptions for R_DIV_SLAVE

Bits	Bit Name	Settings	Description	Reset	Access
7	RESERVED		Reserved.	0x0	R
[6:0]	R_DIV_SLV		R Divider Word. Lower 8 bits of 10-bit reference R divider word.	0x3	R

Address: 0x154C, Reset: 0x00, Name: RDIV2_SEL_SLAVE

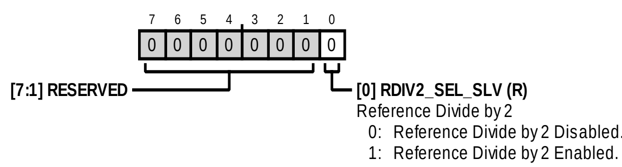

Table 101. Bit Descriptions for RDIV2_SEL_SLAVE

Bits	Bit Name	Settings	Description	Reset	Access
[7:1]	RESERVED		Reserved	0x0	R
0	RDIV2_SEL_SLV		Reference Divide by 2	0x0	R
		0	Reference Divide by 2 Disabled		
		1	Reference Divide by 2 Enabled		

Address: 0x1583, Reset: 0x00, Name: DISABLE_CFG

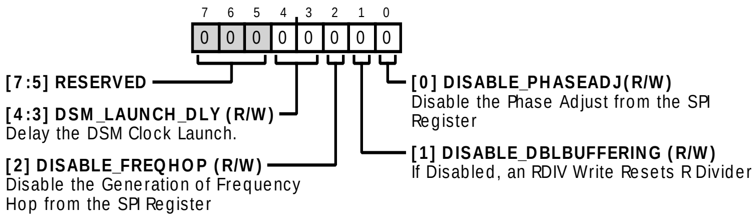

Table 102. Bit Descriptions for DISABLE_CFG

Bits	Bit Name	Settings	Description	Reset	Access
[7:5]	RESERVED		Reserved.	0x0	R
[4:3]	DSM_LAUNCH_DLY		Delay the DSM Clock Launch.	0x0	R/W
2	DISABLE_FREQHOP		Disable the Generation of Frequency Hop from the SPI Register	0x0	R/W
1	DISABLE_DBLBUFFERING		If Disabled, an RDIV Write Resets R Divider	0x0	R/W
0	DISABLE_PHASEADJ		Disable the Phase Adjust from the SPI Register	0x0	R/W

OUTLINE DIMENSIONS

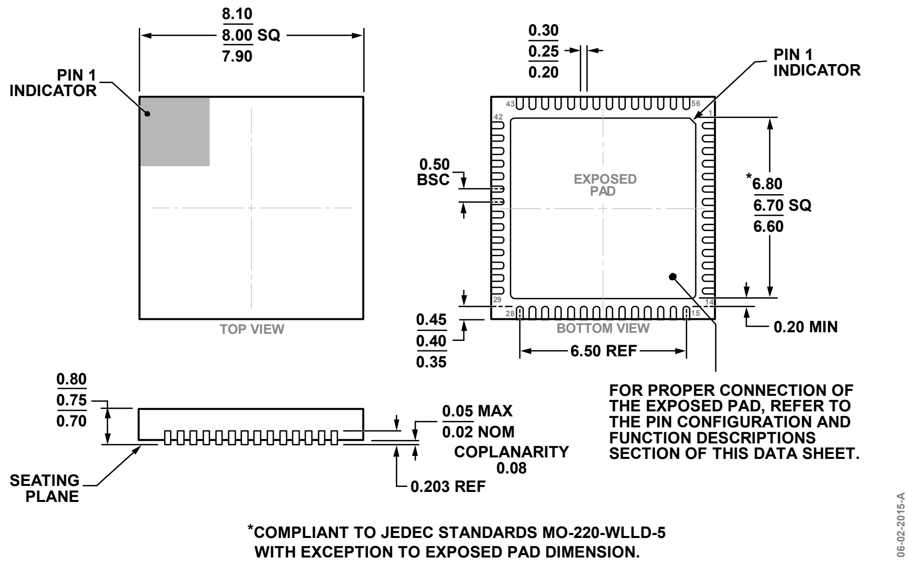

Figure 72. 56-Lead Lead Frame Chip Scale Package [LFCSP]
8 mm × 8 mm Body and 0.75 mm Package Height
(CP-56-16)
Dimensions shown in millimeters

ORDERING GUIDE

Model[1]	Temperature Range	Package Description	Package Option
ADRF6650ACPZ	−40°C to +105°C	56-Lead Lead Frame Chip Scale Package [LFCSP]	CP-56-16
ADRF6650ACPZ-RL7	−40°C to +105°C	56-Lead Lead Frame Chip Scale Package [LFCSP]	CP-56-16
ADRF6650-EVALZ		Evaluation Board	

[1] Z = RoHS Compliant Part.