18 GHz to 44 GHz, GaAs, pHEMT, 32 dBm (>1 W), MMIC Power Amplifier

Data Sheet **ADPA7005**

FEATURES

Output P1dB: up to 31 dBm typical
P_{SAT}: up to 32 dBm typical
Gain: up to 15.5 dB typical
Output IP3: up to 42.5 dBm typical
Supply voltage: 5 V at 1400 mA
50 Ω matched input/output
18-terminal, 7 mm × 7 mm LCC_HS package
Integrated power detector

APPLICATIONS

Military and space
Test instrumentation
Communications

FUNCTIONAL BLOCK DIAGRAM

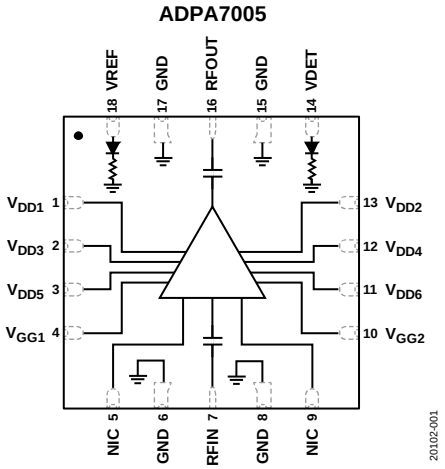

Figure 1.

GENERAL DESCRIPTION

The ADPA7005 is a gallium arsenide (GaAs), pseudomorphic high electron mobility transfer (pHEMT), monolithic microwave integrated circuit (MMIC), 32 dBm saturated output power (>1 W) power amplifier, with an integrated temperature compensated, on-chip power detector that operates between 18 GHz and 44 GHz. The ADPA7005 provides 15.5 dB of small signal gain and approximately 32 dBm of saturated output power at 32 GHz from a 5 V supply (see Figure 26). The ADPA7005 has an IP3 of 40 dBm and is ideal for linear applications such as electronic countermeasure and instrumentation applications requiring >30 dBm of efficient saturated output power. The RF input/outputs are internally matched and dc blocked for ease of integration into higher level assemblies. The ADPA7005 is packaged in a 7 mm × 7 mm, 18-terminal ceramic leadless chip carrier with heat sink (LCC_HS) that exhibits low thermal resistance and is compatible with surface-mount manufacturing techniques.

Rev. 0 **Document Feedback**

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REVISION HISTORY

11/2019—Revision 0: Initial Version

SPECIFICATIONS

18 GHz TO 20 GHz FREQUENCY RANGE

T_A = 25°C, drain bias voltage (V_{DD}) = 5 V, and quiescent drain current (I_{DQ}) = 1400 mA for nominal operation, unless otherwise noted. 50 Ω matched input/output.

Table 1.

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions/Comments
FREQUENCY RANGE		18		20	GHz	
GAIN			14.5		dB	
Gain Flatness			±1		dB	
Gain Variation over Temperature			0.021		dB/°C	
NOISE FIGURE			11		dB	
RETURN LOSS						
Input			18		dB	
Output			12.5		dB	
OUTPUT						
Output Power for 1 dB Compression	P1dB		29		dBm	
Saturated Output Power	P_{SAT}		30		dBm	
Output Third-Order Intercept	IP3		37.5		dBm	Measurement taken at output power (P_{OUT}) per tone = 16 dBm
POWER ADDED EFFICIENCY	PAE		11		%	Measured at P_{SAT}
SUPPLY						Adjust V_{GGx} from −1.5 V up to 0 V to achieve the desired I_{DQ}, V_{GGx} = −0.685 V typical to achieve I_{DQ} = 1400 mA
Quiescent Drain Current	I_{DQ}		1400		mA	
Drain Bias Voltage	V_{DD}	4	5		V	

20 GHz TO 24 GHz FREQUENCY RANGE

T_A = 25°C, V_{DD} = 5 V, and I_{DQ} = 1400 mA for nominal operation, unless otherwise noted. 50 Ω matched input/output.

Table 2.

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions/Comments
FREQUENCY RANGE		20		24	GHz	
GAIN		13	15.5		dB	
Gain Flatness			±0.5		dB	
Gain Variation over Temperature			0.018		dB/°C	
NOISE FIGURE			8		dB	
RETURN LOSS						
Input			12		dB	
Output			12.5		dB	
OUTPUT						
Output Power for 1 dB Compression	P1dB	27.5	30		dBm	
Saturated Output Power	P_{SAT}		30.5		dBm	
Output Third-Order Intercept	IP3		39		dBm	Measurement taken at P_{OUT} per tone = 16 dBm
POWER ADDED EFFICIENCY	PAE		13		%	Measured at P_{SAT}
SUPPLY						Adjust V_{GGx} from −1.5 V up to 0 V to achieve the desired I_{DQ}, V_{GGx} = −0.685 V typical to achieve I_{DQ} = 1400 mA
Current	I_{DQ}		1400		mA	
Voltage	V_{DD}	4	5		V	

24 GHz TO 34 GHz FREQUENCY RANGE

T_A = 25°C, V_{DD} = 5 V, and I_{DQ} = 1400 mA for nominal operation, unless otherwise noted. 50 Ω matched input/output.

Table 3.

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions/Comments
FREQUENCY RANGE		24		34	GHz	
GAIN		13.5	15.5		dB	
Gain Flatness			±0.5		dB	
Gain Variation over Temperature			0.015		dB/°C	
NOISE FIGURE			7		dB	
RETURN LOSS						
Input			10		dB	
Output			12		dB	
OUTPUT						
Output Power for 1 dB Compression	P1dB	28.5	31		dBm	
Saturated Output Power	P_{SAT}		32		dBm	
Output Third-Order Intercept	IP3		40		dBm	Measurement taken at P_{OUT} per tone = 16 dBm
POWER ADDED EFFICIENCY	PAE		13		%	Measured at P_{SAT}
SUPPLY						Adjust V_{GGx} from −1.5 V up to 0 V to achieve the desired I_{DQ}, V_{GGx} = −0.685 V typical to achieve I_{DQ} = 1400 mA
Current	I_{DQ}		1400		mA	
Voltage	V_{DD}	4	5		V	

34 GHz TO 44 GHz FREQUENCY RANGE

T_A = 25°C, V_{DD} = 5 V, and I_{DQ} = 1400 mA for nominal operation, unless otherwise noted. 50 Ω matched input/output.

Table 4.

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions/Comments
FREQUENCY RANGE		34		44	GHz	
GAIN		12	14.5		dB	
Gain Flatness			±1		dB	
Gain Variation over Temperature			0.021		dB/°C	
NOISE FIGURE			6		dB	
RETURN LOSS						
Input			10		dB	
Output			14		dB	
OUTPUT						
Output Power for 1 dB Compression	P1dB	28.5	30.5		dBm	
Saturated Output Power	P_{SAT}		31		dBm	
Output Third-Order Intercept	IP3		42.5		dBm	Measurement taken at P_{OUT} per tone = 16 dBm
POWER ADDED EFFICIENCY	PAE		8		%	Measured at P_{SAT}
SUPPLY						Adjust V_{GGx} from −1.5 V up to 0 V to achieve the desired I_{DQ}, V_{GGx} = −0.685 V typical to achieve I_{DQ} = 1400 mA
Current	I_{DQ}		1400		mA	
Voltage	V_{DD}	4	5		V	

ABSOLUTE MAXIMUM RATINGS

Table 5.

Parameter	Rating
Drain Bias Voltage (V_{DDx})	6.0 V
Gate Bias Voltage (V_{GGx})	−1.6 to 0 V
Radio Frequency Input Power (RFIN)	27 dBm
Continuous Power Dissipation (P_{DISS}), T = 85°C (Derate 137 mW/°C Above 85°C)	12.33 W
Storage Temperature Range	−55°C to +150°C
Operating Temperature Range	−40°C to +85°C
Junction Temperature to Maintain 1,000,000 Hour Mean Time to Failure (MTTF)	175°C
Nominal Junction Temperature (T = 85°C, V_{DD} = 5 V, I_{DQ} = 1400 mA)	136.1°C
Peak Reflow Temperature (Moisture Sensitivity Level 3 (MSL3))[1]	260°C
Moisture Sensitivity Level	MSL3
Electrostatic Discharge (ESD) Sensitivity Human Body Model (HBM)	Class 1B (passed 500 V)

[1] See the Ordering Guide for additional information.

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

THERMAL RESISTANCE

Thermal performance is directly linked to system design and operating environment. Careful attention to the printed circuit board (PCB) thermal design is required.

θ_{JC} is the channel to case thermal resistance, channel to bottom of die using die attach epoxy.

Table 6. Thermal Resistance

Package Type	θ_{JC}	Unit
EH-18-1[1]	7.3	°C/W

[1] θ_{JC} is determined by simulation under the following conditions: the heat transfer is due solely to thermal conduction from the channel, through the ground pad, to the PCB. The ground pad is held constant at the operating temperature of 85°C.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

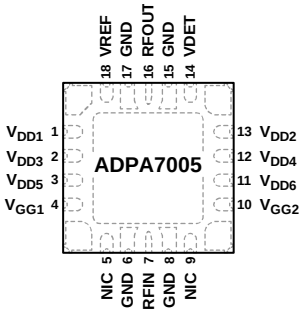

Figure 2. Pin Configuration

Table 7. Pin Function Descriptions

Pin No.	Mnemonic	Description
1, 2, 3, 11, 12, 13	V_{DD1}, V_{DD3}, V_{DD5}, V_{DD6}, V_{DD4}, V_{DD2}	Drain Bias for the Amplifier.
4, 10	V_{GG1}, V_{GG2}	Amplifier Gate Control. ESD protection diodes are included and turn on below −1.5 V.
5, 9	NIC	Not Internally Connected. Note that data shown herein was measured with these pins externally connected to RF and dc ground.
6, 8, 15, 17	GND	Ground Pins. Connect these pins and the exposed pad to RF and dc ground.
7	RFIN	RF Signal Input. This pin is ac-coupled and internally matched to 50 Ω.
14	VDET	Detector Diode Used for Measuring the RF Output Power. Detection via this pin requires the application of a dc bias voltage through an external series resistor. Used in combination with VREF, the difference voltage, VREF − VDET, is a temperature compensated dc voltage proportional to the RF output power.
16	RFOUT	RF Signal Output. This pin is ac-coupled and internally matched to 50 Ω.
18	VREF	Reference Diode Used for Temperature Compensation of VDET RF Output Power Measurements. Detection via this pin requires the application of a dc bias voltage through an external series resistor. Used in combination with VDET, this voltage provides temperature compensation to VDET RF output power measurements.
	EPAD	Exposed Pad. The exposed pad must be connected to RF and dc ground.

INTERFACE SCHEMATICS

Figure 3. GND Interface Schematic

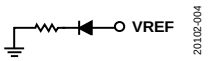

Figure 4. VREF Interface Schematic

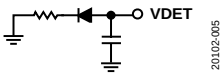

Figure 5. VDET Interface Schematic

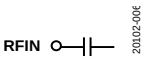

Figure 6. RFIN Interface Schematic

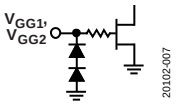

Figure 7. V_{GG1}, V_{GG2} Interface Schematic

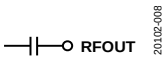

Figure 8. RFOUT Interface Schematic

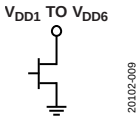

Figure 9. V_{DD1} to V_{DD6} Interface Schematic

TYPICAL PERFORMANCE CHARACTERISTICS

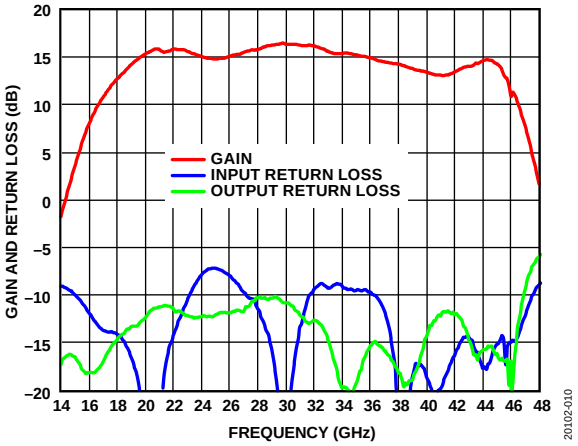

Figure 10. Gain and Return Loss vs. Frequency, V_{DD} = 5 V, I_{DQ} = 1400 mA

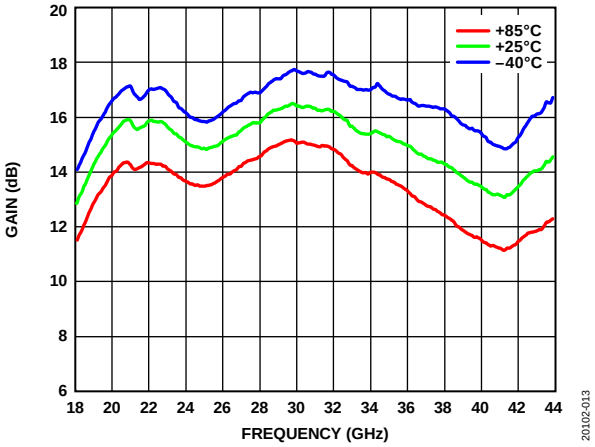

Figure 13. Gain vs. Frequency for Various Temperatures, V_{DD} = 5 V, I_{DQ} = 1400 mA

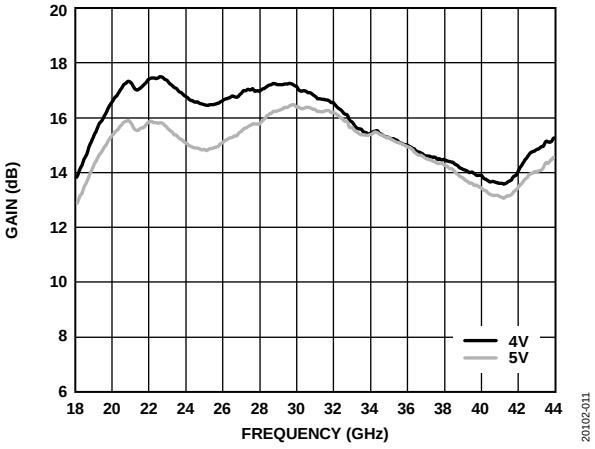

Figure 11. Gain vs. Frequency for Various V_{DD}, I_{DQ} = 1400 mA

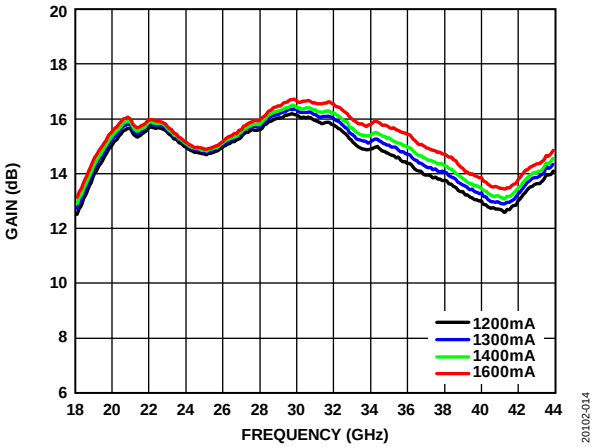

Figure 14. Gain vs. Frequency for Various I_{DQ}, V_{DD} = 5 V

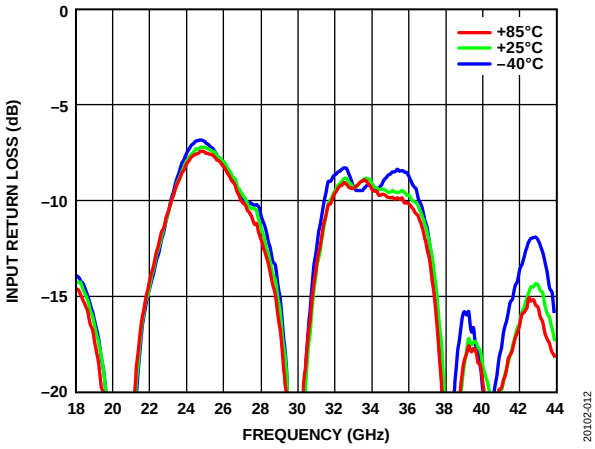

Figure 12. Input Return Loss vs. Frequency for Various Temperatures, V_{DD} = 5 V, I_{DQ} = 1400 mA

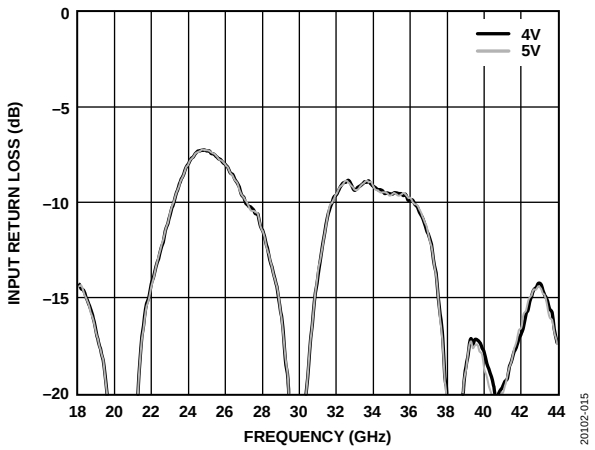

Figure 15. Input Return Loss vs. Frequency for Various V_{DD}, I_{DQ} = 1400 mA

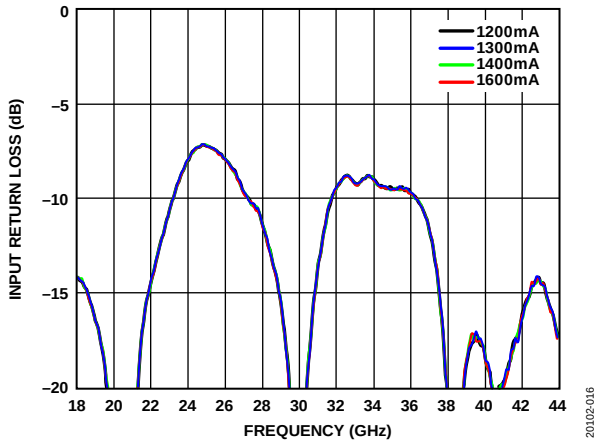

Figure 16. Input Return Loss vs. Frequency for Various I_{DQ}, V_{DD} = 5 V

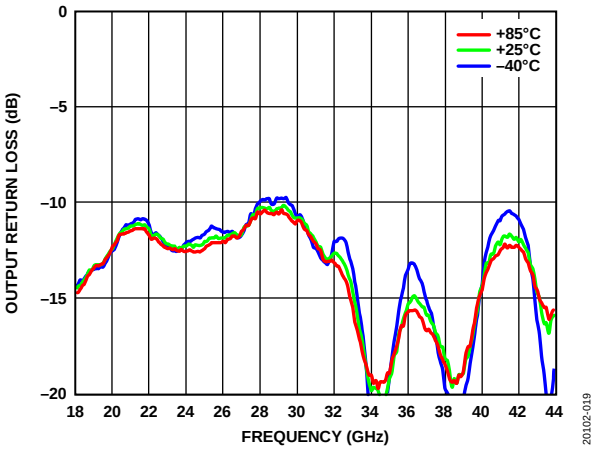

Figure 19. Output Return Loss vs. Frequency for Various Temperatures, V_{DD} = 5 V, I_{DQ} = 1400 mA

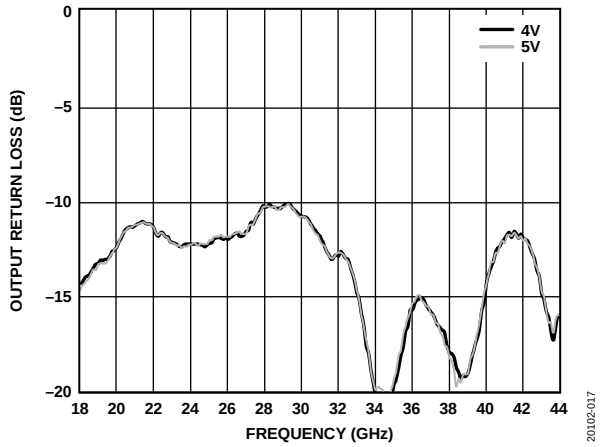

Figure 17. Output Return Loss vs. Frequency for Various V_{DD}, I_{DQ} = 1400 mA

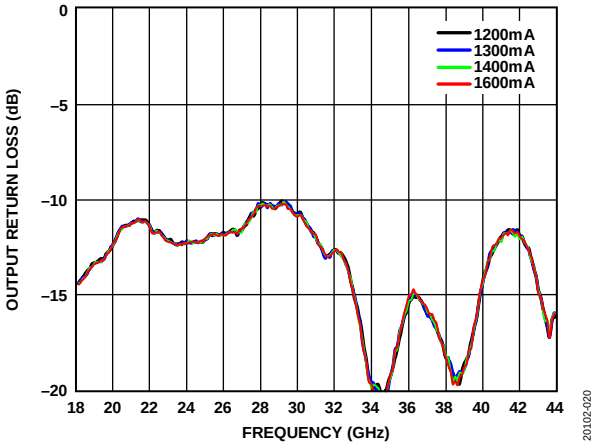

Figure 20. Output Return Loss vs. Frequency for Various I_{DQ}, V_{DD} = 5 V

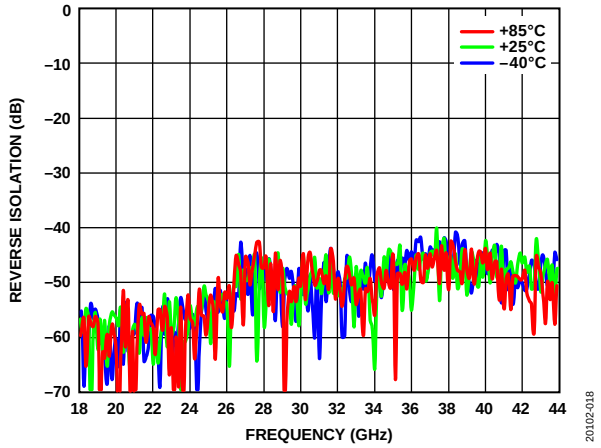

Figure 18. Reverse Isolation vs. Frequency for Various Temperatures, V_{DD} = 5 V, I_{DQ} = 1400 mA

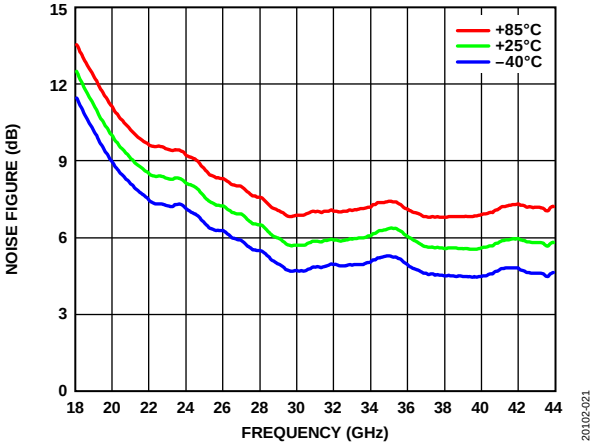

Figure 21. Noise Figure vs. Frequency for Various Temperatures, V_{DD} = 5 V, I_{DQ} = 1400 mA

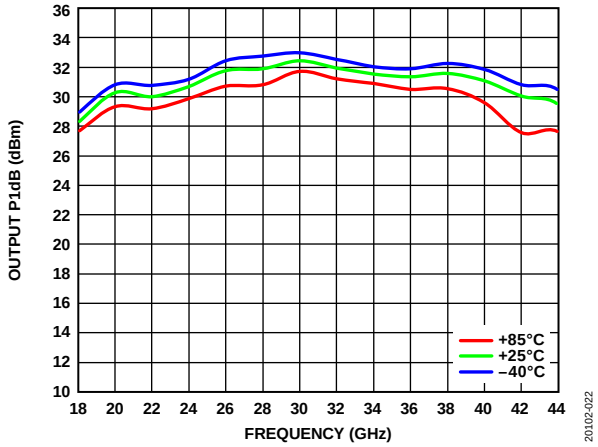

Figure 22. Output P1dB vs. Frequency for Various Temperatures, V_{DD} = 5 V, I_{DQ} = 1400 mA

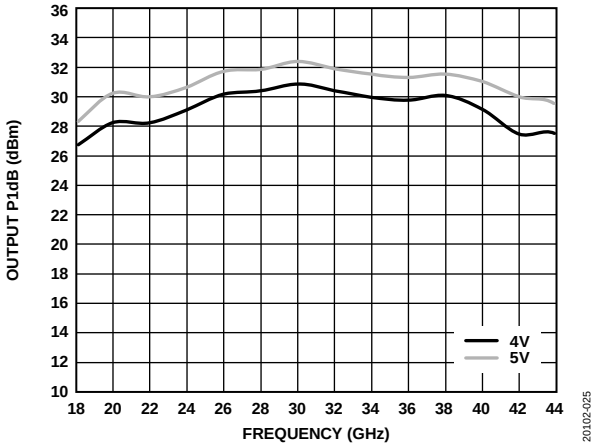

Figure 25. Output P1dB vs. Frequency for Various V_{DD}, I_{DQ} = 1400 mA

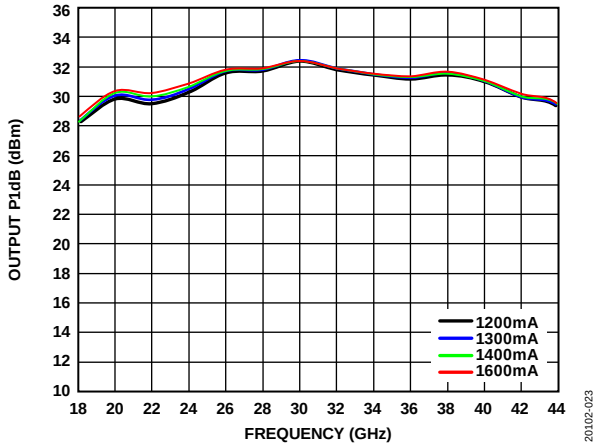

Figure 23. Output P1dB vs. Frequency for Various I_{DQ}, V_{DD} = 5 V

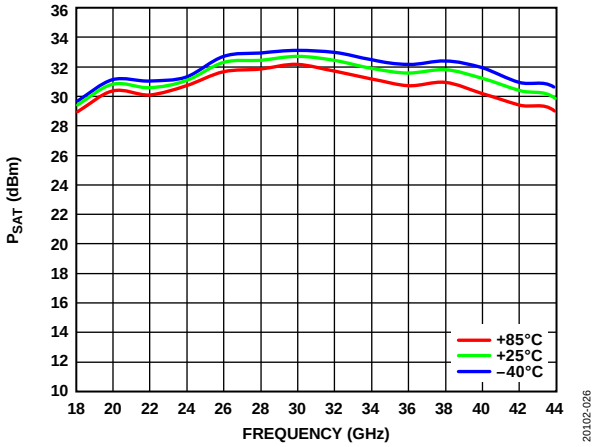

Figure 26. P_{SAT} vs. Frequency for Various Temperatures, V_{DD} = 5 V, I_{DQ} = 1400 mA

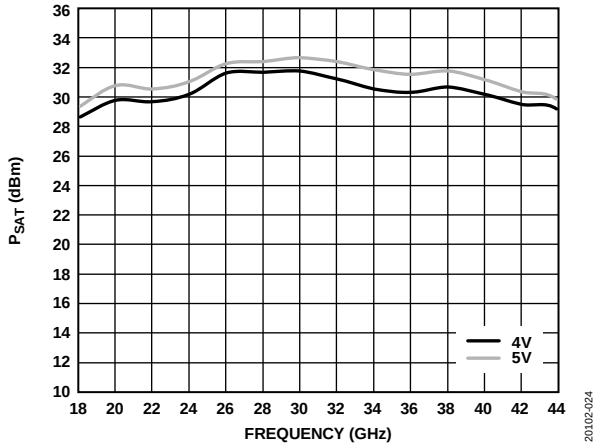

Figure 24. P_{SAT} vs. Frequency for Various V_{DD}, I_{DQ} = 1400 mA

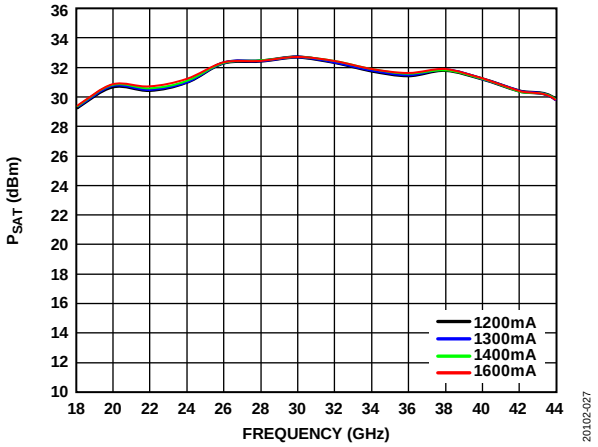

Figure 27. P_{SAT} vs. Frequency for Various I_{DQ}, V_{DD} = 5 V

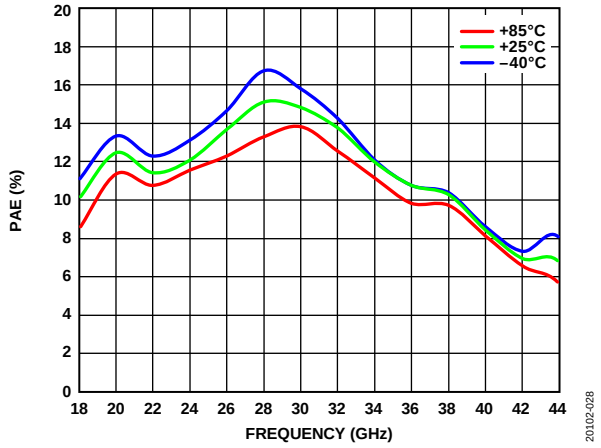

Figure 28. Power Added Efficiency (PAE) vs. Frequency for Various Temperatures, V_{DD} = 5 V, I_{DQ} = 1400 mA, PAE Measured at P_{SAT}

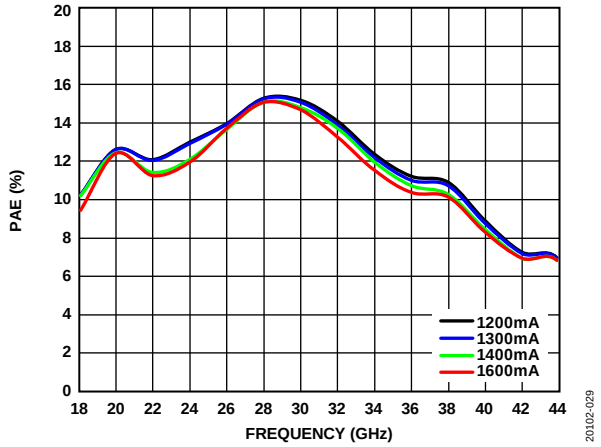

Figure 29. PAE vs. Frequency for Various I_{DQ}, V_{DD} = 5 V, I_{DQ} = 1400 mA, PAE Measured at P_{SAT}

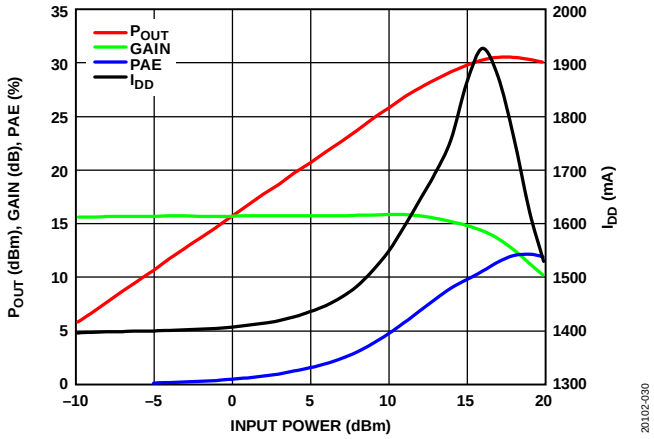

Figure 30. P_{OUT}, Gain, PAE, and Drain Current with RF Applied (I_{DD}) vs. Input Power, 22 GHz, V_{DD} = 5 V, I_{DQ} = 1400 mA

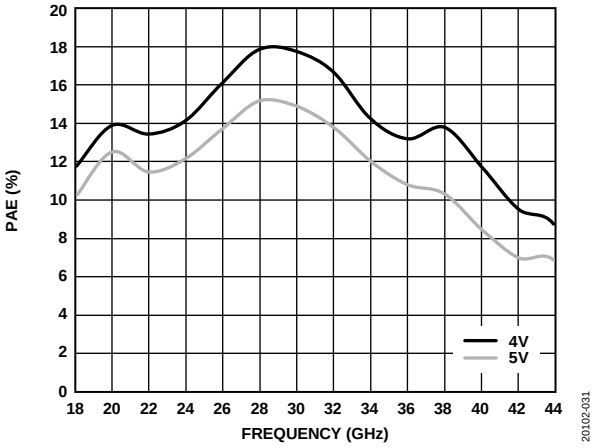

Figure 31. PAE vs. Frequency for Various V_{DD}, I_{DQ} = 1400 mA, PAE Measured at P_{SAT}

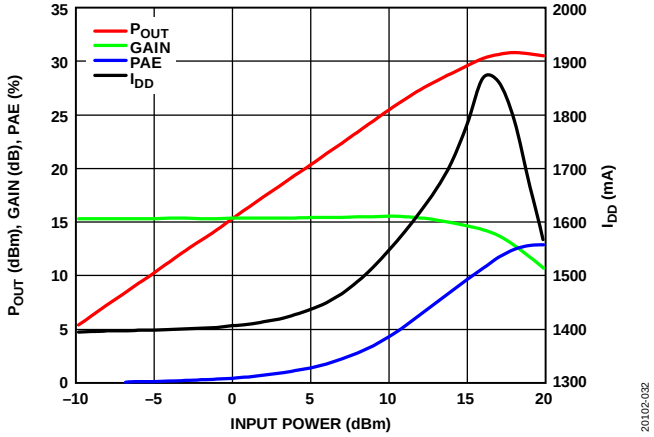

Figure 32. P_{OUT}, Gain, PAE, and I_{DD} vs. Input Power, 20 GHz, V_{DD} = 5 V, I_{DQ} = 1400 mA

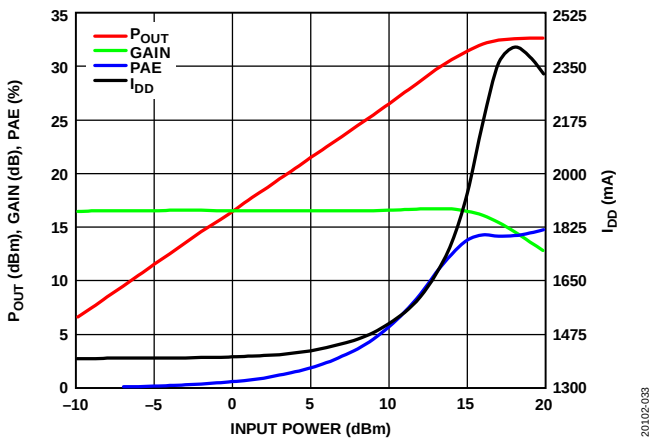

Figure 33. P_{OUT}, Gain, PAE, and I_{DD} vs. Input Power, 30 GHz, V_{DD} = 5 V, I_{DQ} = 1400 mA

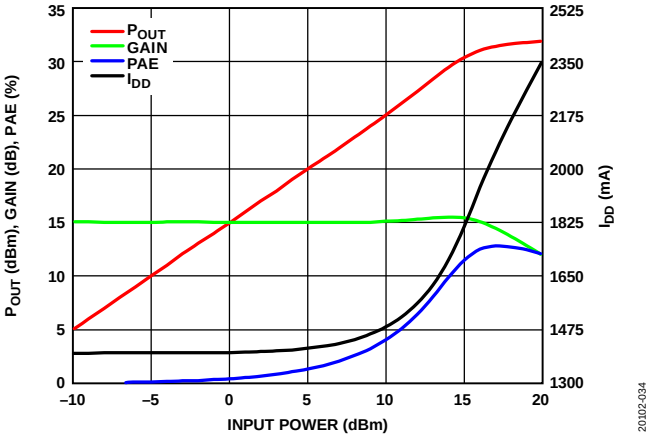

Figure 34. P_{OUT}, Gain, PAE, and I_{DD} vs. Input Power, 34 GHz, V_{DD} = 5 V, I_{DQ} = 1400 mA

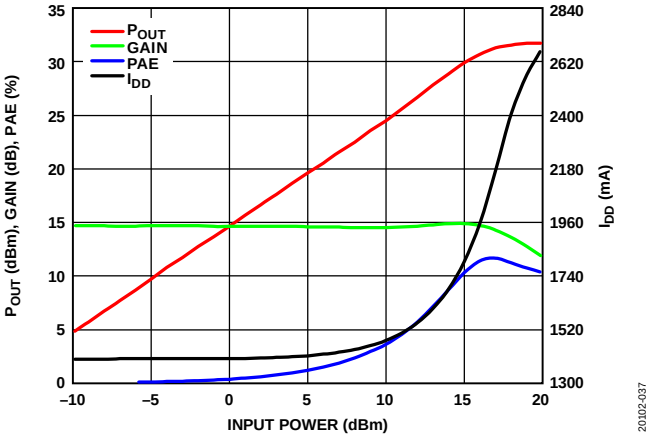

Figure 37. P_{OUT}, Gain, PAE, and I_{DD} vs. Input Power, 38 GHz, V_{DD} = 5 V, I_{DQ} = 1400 mA

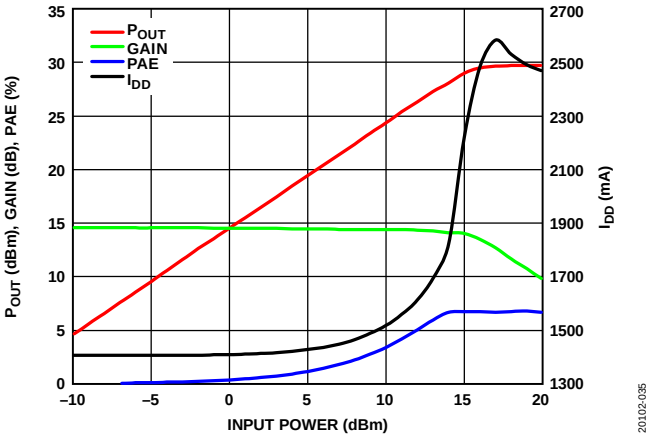

Figure 35. P_{OUT}, Gain, PAE, and I_{DD} vs. Input Power, 44 GHz, V_{DD} = 5 V, I_{DQ} = 1400 mA

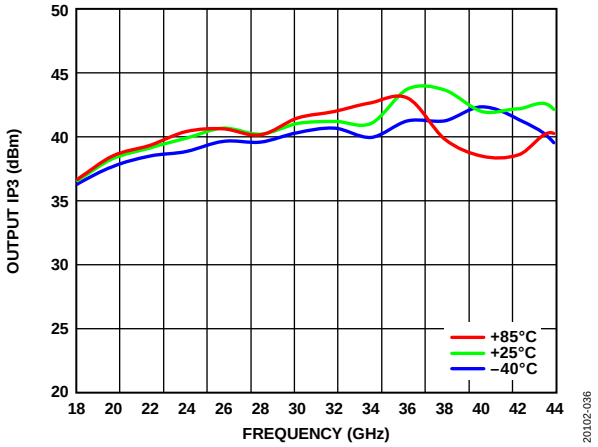

Figure 38. Output IP3 vs. Frequency for Various Temperatures, P_{OUT} per Tone = 16 dBm, V_{DD} = 5 V, I_{DQ} = 1400 mA

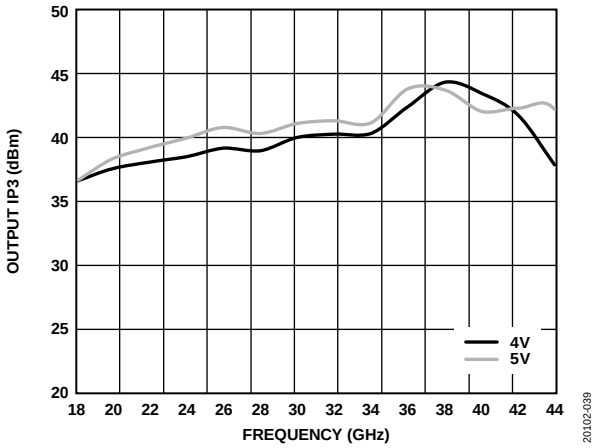

Figure 36. Output IP3 vs. Frequency for Various V_{DD}, P_{OUT} per Tone = 16 dBm, V_{DD} = 5 V, I_{DQ} = 1400 mA

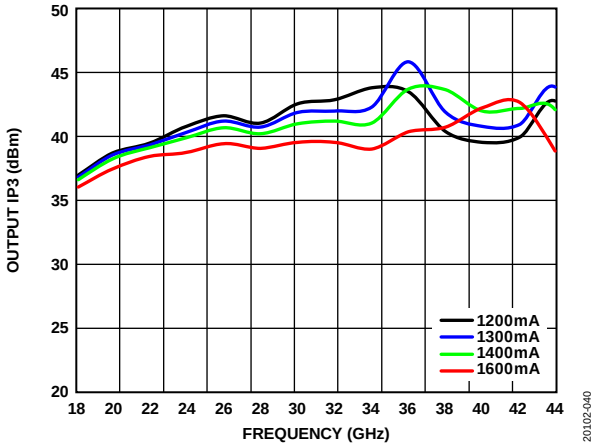

Figure 39. Output IP3 vs. Frequency for Various I_{DQ}, P_{OUT} per Tone = 16 dBm, V_{DD} = 5 V

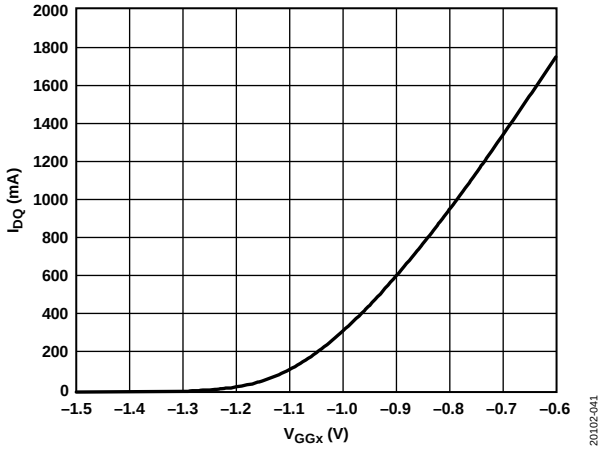

Figure 40. I_{DQ} vs. V_{GGx}

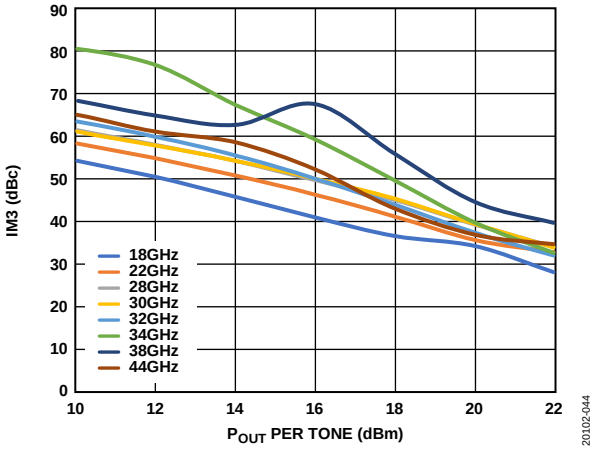

Figure 43. Third-Order Intermodulation Distortion (IM3) vs. P_{OUT} per Tone, V_{DD} = 5 V, I_{DQ} = 1400 mA

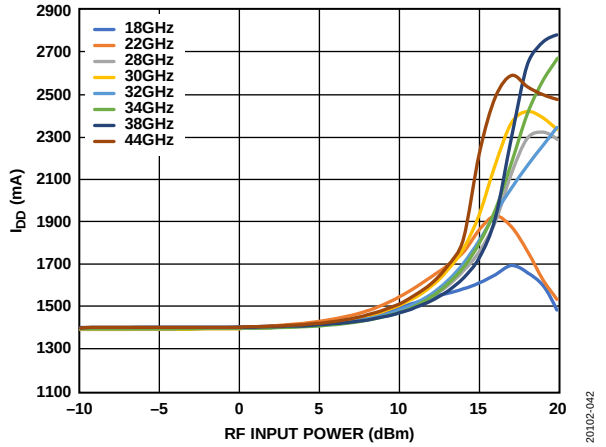

Figure 41. I_{DD} vs. RF Input Power at Various Frequencies, V_{DD} = 5 V, I_{DQ} = 1400 mA

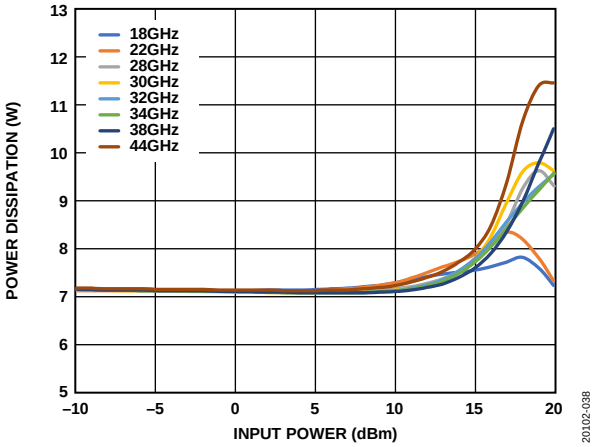

Figure 44. Power Dissipation vs. Input Power at T = 85°C, V_{DD} = 5 V, I_{DQ} = 1400 mA

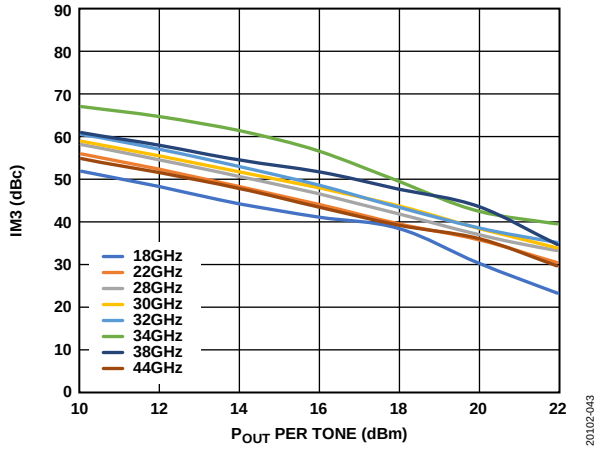

Figure 42. Third-Order Intermodulation Distortion (IM3) vs. P_{OUT} per Tone, V_{DD} = 4 V, I_{DQ} = 1400 mA

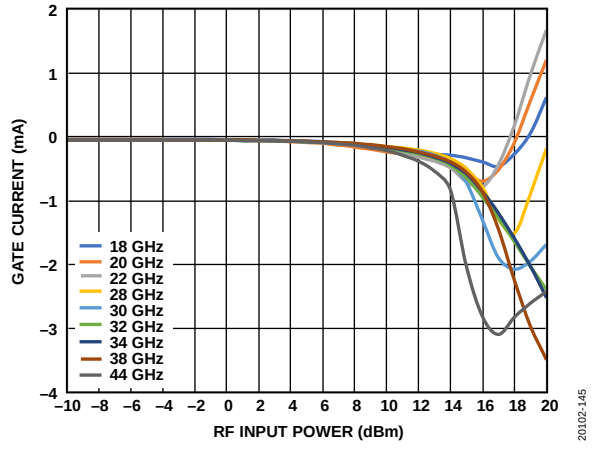

Figure 45. Gate Current (I_{GG}) vs. RF Input Power at Various Frequencies, V_{DD} = 5 V, I_{DQ} = 1400 mA

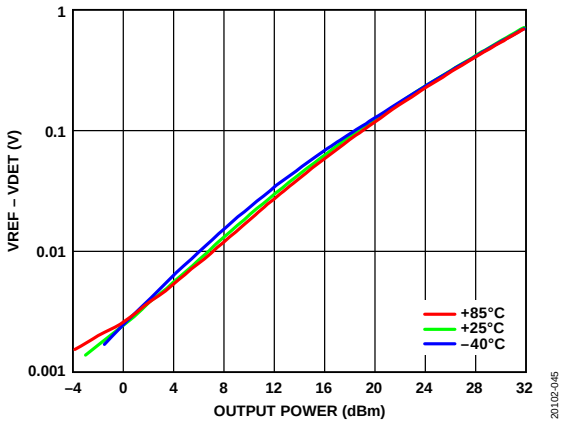

Figure 46. VREF – VDET vs. Output Power for Various Temperatures at 30 GHz

CONSTANT I_{DD} OPERATION

Biased with HMC980LP4E active bias controller (see Figure 53), T_A = 25°C, V_{DD} = 5 V, and I_{DD} = 1800 mA for nominal operation, unless otherwise noted.

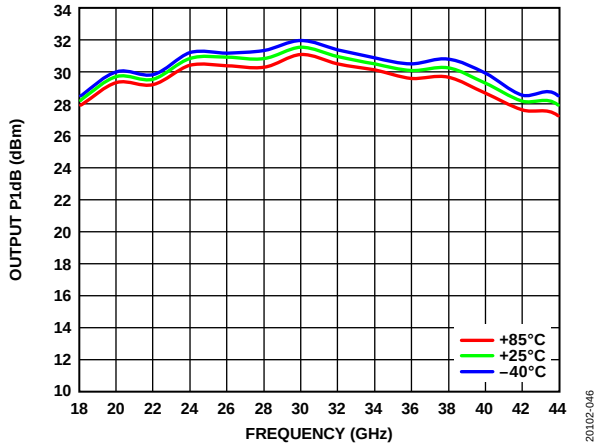

Figure 47. Output P1dB vs. Frequency for Various Temperatures, V_{DD} = 5 V, Data Measured with Constant I_{DD}

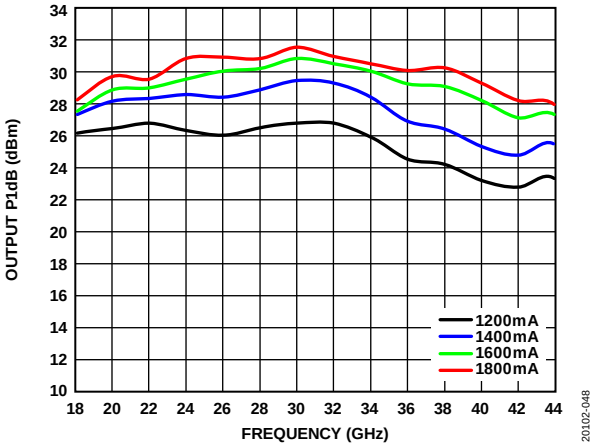

Figure 49. Output P1dB vs. Frequency for Various I_{DQ}, V_{DD} = 5 V, Data Measured with Constant I_{DD}

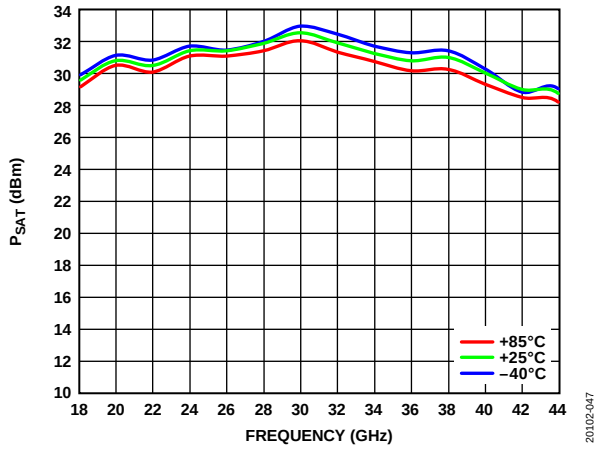

Figure 48. P_{SAT} vs. Frequency for Various Temperatures, V_{DD} = 5 V, Data Measured with Constant I_{DD}

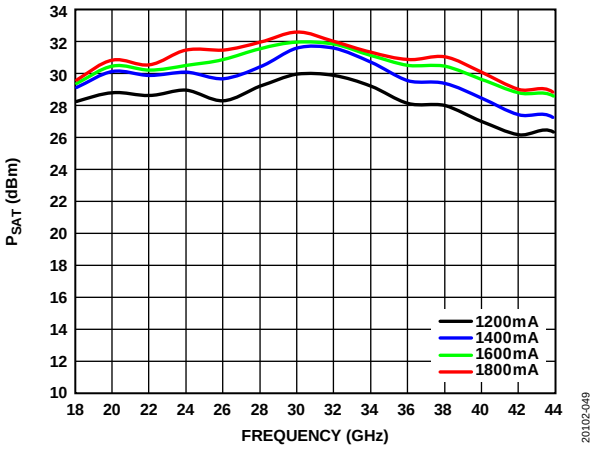

Figure 50. P_{SAT} vs. Frequency for Various I_{DQ}, V_{DD} = 5 V, Data Measured with Constant I_{DD}

THEORY OF OPERATION

The simplified architecture of the ADPA7005 power amplifier is shown in Figure 51. The ADPA7005 is a cascaded, three-stage amplifier with a combined gain of 15.5 dB and a P_{SAT} value of 32 dBm.

The drain current is controlled by the voltage on the V_{GG1} and V_{GG2} pins. These pins must be connected together and driven by a negative voltage in the −1.5 V to 0 V range (typical gate bias voltage for a quiescent drain current bias of 1400 mA is −0.685 V). Simplified bias pin connections to the dedicated gain stages are shown in Figure 51.

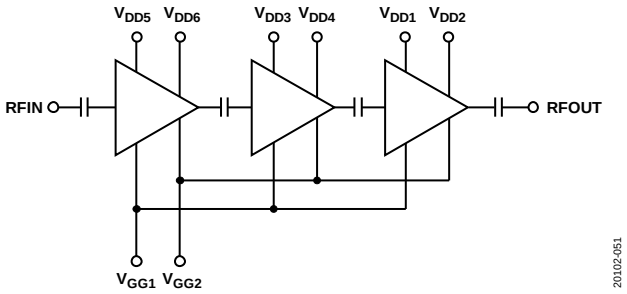

Figure 51. Simplified Architecture of ADPA7005

A portion of the RF output signal is directionally coupled to a diode for detection of the RF output power. When the diode is dc biased, the diode rectifies the RF power and makes the RF power available for measurement as a dc voltage at VDET. To allow temperature compensation of VDET, an identical and symmetrically located circuit (minus the coupled RF power) is available via VREF. The difference of VREF − VDET provides a temperature compensated signal that is proportional to the RF output.

To obtain optimal performance from the ADPA7005 and avoid damaging the device, follow the recommended biasing sequences described in the Applications Information section.

APPLICATIONS INFORMATION

Figure 52 shows the basic connections for operating the ADPA7005. All measurements for this device were taken using the typical application circuit shown in Figure 52.

Capacitive bypassing is required for all V_{GGx} and V_{DDx} pins. V_{GG1} and V_{GG2} are the gate bias pins, and V_{DD1} to V_{DD6} are the drain bias pins to the cascaded amplifier.

The power supply and gate voltage decoupling capacitors shown in Figure 52 represent the configuration that was used to characterize and qualify the device. There may be scopes to reduce the number of capacitors, but scopes vary from system to system. It is recommended to first remove or combine the largest capacitors that are farthest from the device. The following is the recommended bias sequence during power-up:

1. Connect the power supply ground to circuit ground (GND).
2. Set the gate bias voltages, V_{GG1} and V_{GG2}, to −1.5 V.
3. Set all drain bias voltages (V_{DDx}) to 5 V.
4. Increase the gate bias voltage to achieve the quiescent supply current and set I_{DQ} = 1400 mA.
5. Apply the RF signal.

The following is the recommended bias sequence during power-down:

1. Turn off the RF signal.
2. Decrease the gate bias voltages, V_{GG1} and V_{GG2}, to −1.5 V to achieve an I_{DQ} = 0 mA (approximately).
3. Decrease all drain bias voltages to 0 V.
4. Increase the V_{GGx} gate bias voltage to 0 V.

The V_{DD} = 5 V and I_{DQ} = 1400 mA bias conditions are recommended to optimize overall performance when the gate voltage is being held at a fixed value (note that with the gate voltage held at a fixed value, the drain current, I_{DD}, increases as the RF input power level is increased, as shown in Figure 41). Unless otherwise noted, the data shown was taken using the recommended bias conditions. Operation of the ADPA7005 at different bias conditions can result in different performance. Biasing the ADPA7005 for higher quiescent drain current typically results in higher gain and output P1dB at the expense of increased power dissipation (see Table 8).

Table 8. Power Selection[1, 2]

I_{DQ} (mA)	Gain (dB)	Output P1dB (dBm)	Output IP3 (dBm)	P_{DISS} (W)	V_{GGx} (V)
1200	15.80	31.89	42.90	6	−0.73
1400	16.20	31.93	41.30	7	−0.68
1600	16.50	31.95	39.55	8	−0.63

[1] Data taken at the following nominal bias conditions: V_{DD} = 5 V, T_A = 25°C, frequency = 32 GHz.
[2] Adjust V_{GG1} and V_{GG2} from −1.5 V to 0 V to achieve the desired quiescent drain current, I_{DQ}.

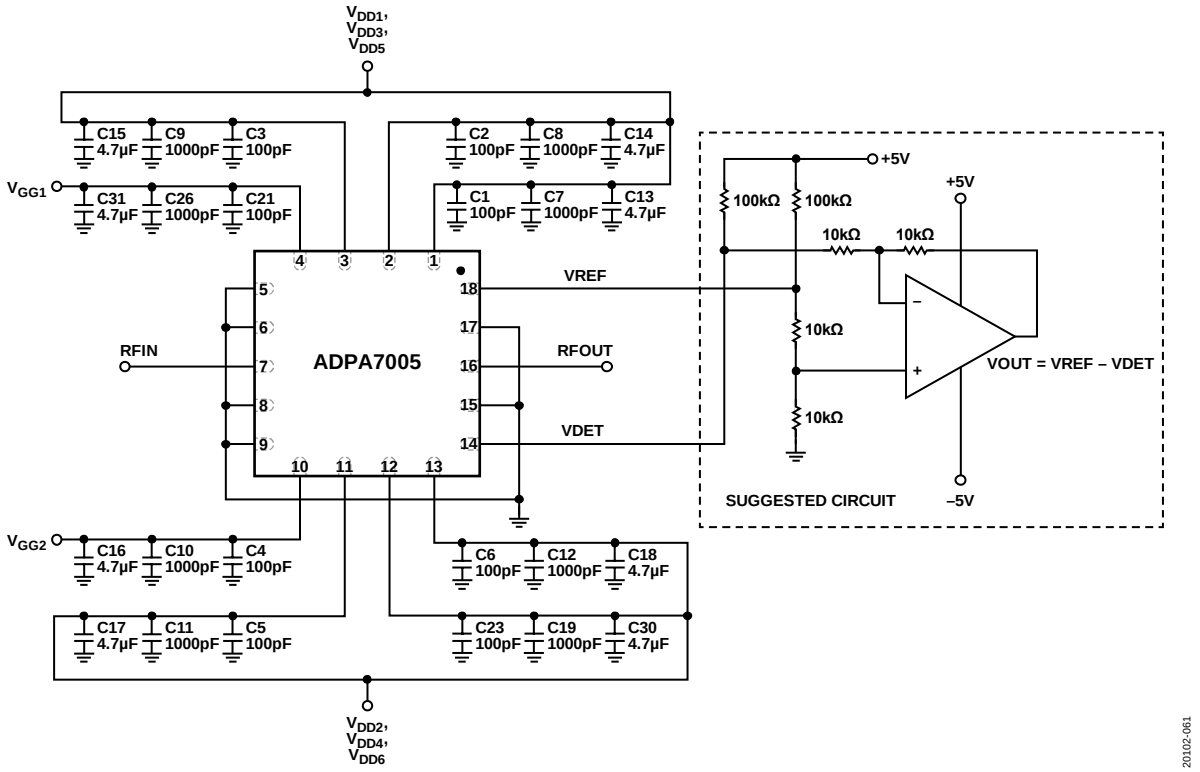

Figure 52. Typical Application Circuit

BIASING ADPA7005 WITH THE HMC980LP4E

The HMC980LP4E is an active bias controller that measures and regulates drain current by automatically adjusting the gate voltage. The HMC980LP4E can control the biasing of RF amplifiers with drain voltages up to 16.5 V and currents up to 1.6 A. The controller provides constant drain current biasing over temperature and device to device variation, and properly sequences gate and drain voltages to ensure the safe operation of the amplifier.

The HMC980LP4E offers self protection in the event of a short circuit, as well as an internal charge pump that generates the negative voltage required on the gate of the ADPA7005. The HMC980LP4E also provides the option to use an external negative voltage source. The HMC980LP4E is also available in die form as the HMC980-DIE.

APPLICATION CIRCUIT SETUP

Figure 53 shows a schematic of an application circuit using the two HMC980LP4E devices to control the ADPA7005. When using an external negative supply for VNEG, refer to the schematic in Figure 54.

Although the ADPA7005 is specified with a quiescent drain current of 1400 mA, the operational drain current, I_{DRAIN}, required to achieve the maximum output power from the ADPA7005 must be set closer to 1800 mA. The I_{DRAIN} current increases to approximately 1800 mA when the RF input power is 15 dBm, the approximate input compression point (see Figure 41). As a result, a target I_{DRAIN} of 1800 mA is chosen.

Two HMC980LP4E devices are needed to support current levels at 1800 mA because a single HMC980LP4E device can support a maximum current of 1600 mA. In the application circuit shown in Figure 53 and Figure 54, the ADPA7005 drain voltage and drain current are set by the following equations:

$$VDRAIN = V_{DD} - I_{DRAIN} \times 0.85\ \Omega \quad (1)$$

where:
$VDRAIN$ = 5 V, the drain voltage from Pin 17 and Pin 18 of the HMC980LP4E.
V_{DD} = 5.765 V, the supply voltage to the HMC980LP4E.
I_{DRAIN} = 1800 mA, the constant drain current from Pin 17 and Pin 18 on the HMC980LP4E.

$$R10 = \frac{150\ \Omega}{I_{DRAIN}} \quad (2)$$

where:
I_{DRAIN} = 900 mA (for each HMC980LP4E, per the dual bias setup in Figure 53).
$R10$ = 166.66 Ω.

LIMITING VGATE AND VNEG FOR ADPA7005 V_{GGX} ABSOLUTE MAXIMUM RATING REQUIREMENT

When using the HMC980LP4E to control the ADPA7005, set the minimum voltages for the VNEG and VGATE pins of the HMC980LP4E to −1.5 V to keep these voltages within the absolute maximum rating limits for the V_{GGx} pins of the ADPA7005. To set the minimum voltages, use the R15 and R16 resistors shown in Figure 53 and Figure 54. Refer to the AN-1363 Application Note, *Meeting Biasing Requirements of Externally Biased RF/Microwave Amplifiers with Active Bias Controllers*, for more information and calculations for R15 and R16.

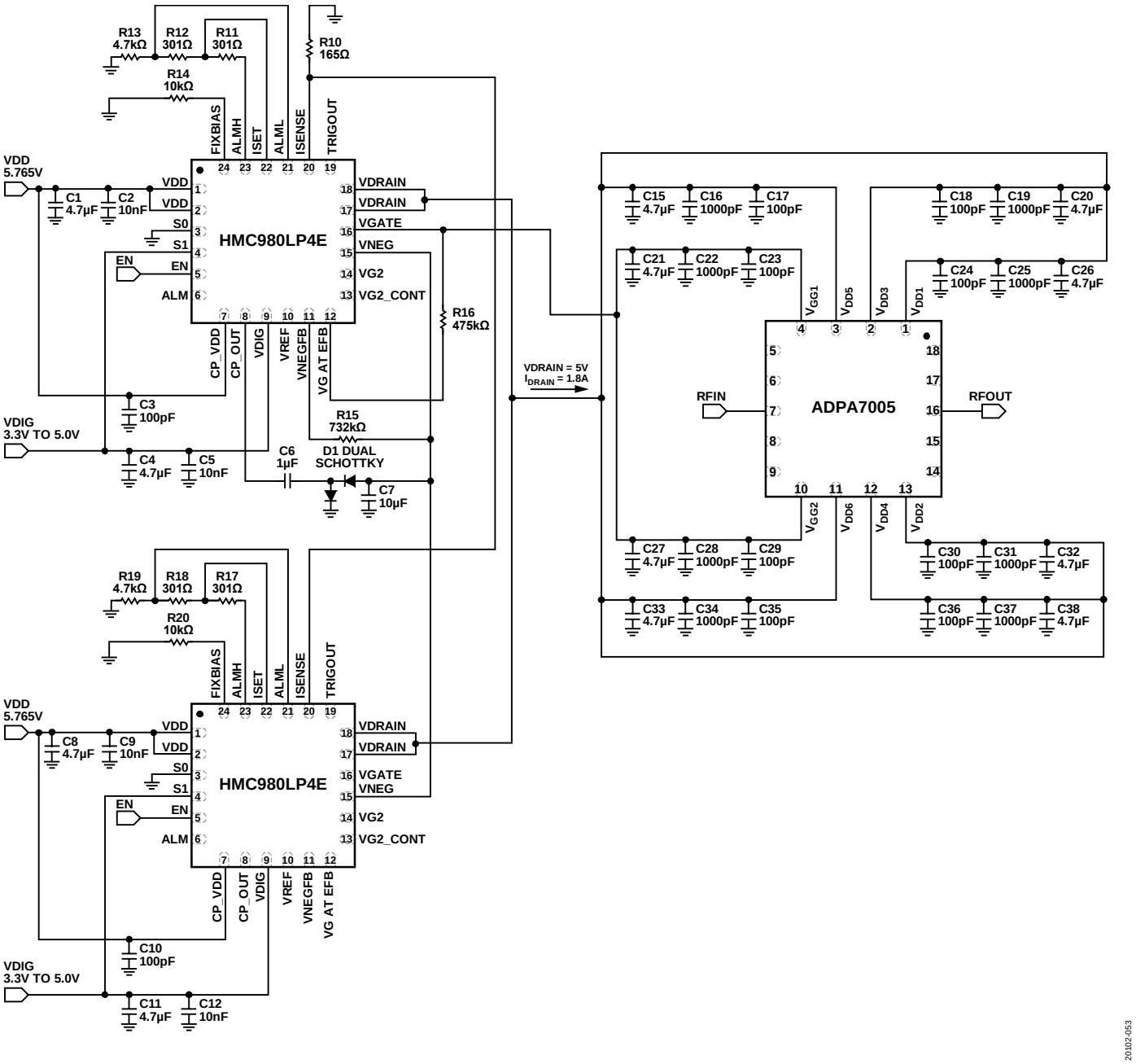

Figure 53. Application Circuit Using Dual HMC980LP4E with ADPA7005

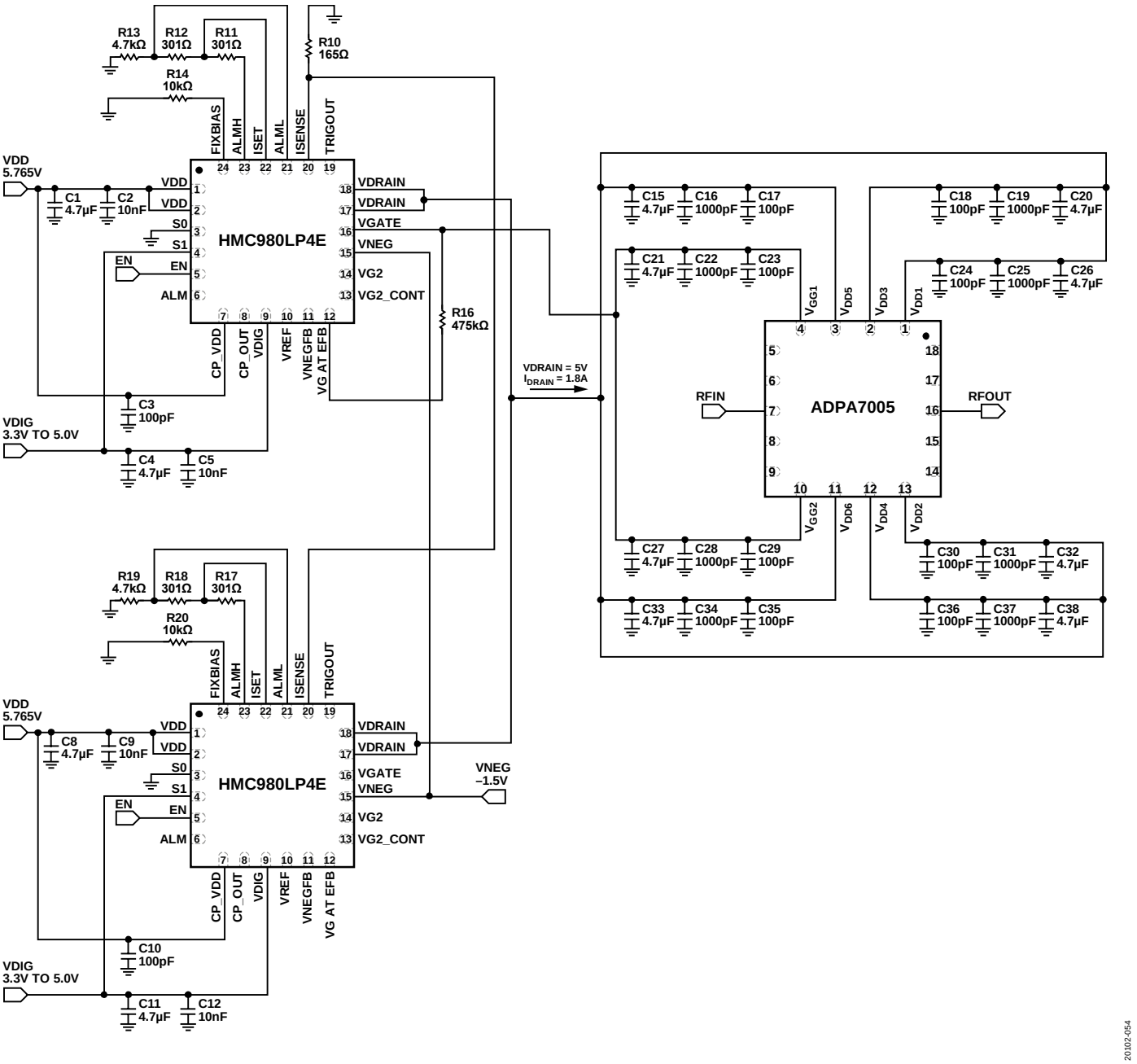

Figure 54. Application Circuit Using Dual HMC980LP4E with ADPA7005 and External Negative Voltage Source

HMC980LP4E BIAS SEQUENCE

The dc supply sequencing in the Power-Up Sequence section and the Power-Down Sequence section is required to prevent damage to the HMC980LP4E when using it to control the ADPA7005.

Power-Up Sequence

The power-up sequence is as follows:

1. Set VDIG (Pin 9) of both HMC980LP4E devices to 3.3 V.
2. Set the VDD pins of both HMC980LP4E devices to 5.765 V.
3. Set VNEG (Pin 15) of both HMC980LP4E devices to −1.5 V. This step is not needed if using an internally generated voltage.
4. Set EN (Pin 5) of both HMC980LP4E devices to 3.3 V (transitioning from 0 V to 3.3 V turns on VGATE and VDRAIN).

Power-Down Sequence

The power-down sequence is as follows:

1. Set EN (Pin 5 of both HMC980LP4E devices) to 0 V (transitioning from 3.3 V to 0 V turns off VDRAIN and VGATE).
2. Set VNEG (Pin 15 of both HMC980LP4E devices) to 0 V. This step is not needed if using an internally generated voltage.
3. Set the VDD pins of both HMC980LP4E devices to 0 V.
4. Set VDIG (Pin 9 of both HMC980LP4E devices) to 0 V.

When the HMC980LP4E bias control circuit is set up, toggle the bias to the ADPA7005 on or off by applying 3.3 V or 0 V, respectively, to the EN pin of the HMC980LP4E. At EN = 3.3 V, the VGATE pin of the HMC980LP4E drops to −1.5 V and the VDRAIN pin of the HMC980LP4E turns on at 5 V. VGATE then rises until I_{DRAIN} = 1800 mA, and the closed control loop regulates I_{DRAIN} at 1800 mA. When EN = 0 V, VGATE is set to −1.5 V, and VDRAIN is set to 0 V (see Figure 55 and Figure 56).

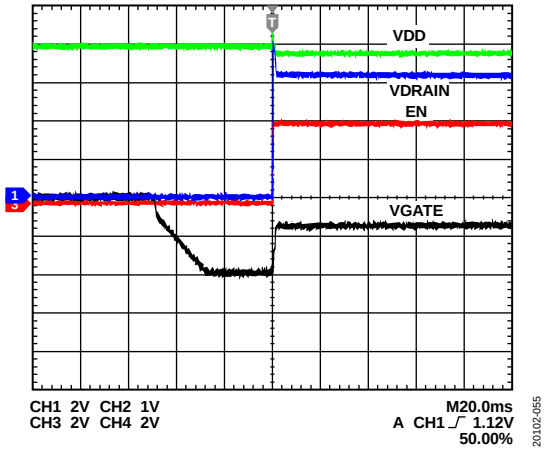

Figure 55. Turn On HMC980LP4E Outputs to ADPA7005

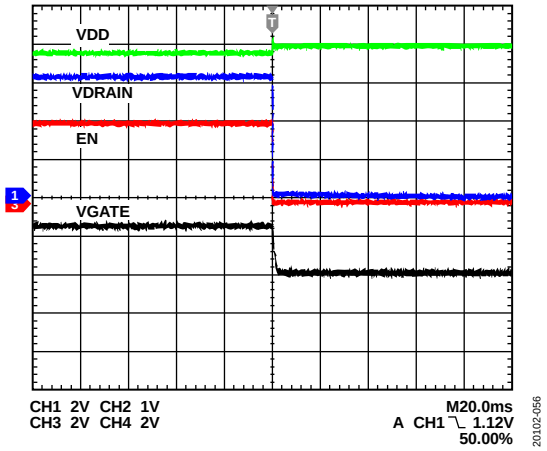

Figure 56. Turn Off HMC980LP4E Outputs to ADPA7005

CONSTANT DRAIN CURRENT BIASING vs. CONSTANT GATE VOLTAGE BIASING

The HMC980LP4E uses a feedback loop to continuously adjust VGATE to maintain a constant drain current over dc supply variation, temperature, RF input/output level, and device to device variation. Constant drain current bias is the preferred method for reducing time in calibration procedures and for maintaining consistent performance over time.

In comparison to a constant gate voltage bias, where the current increases when RF power is applied, a constant drain current has a slightly lower output P1dB. This output P1db is shown in Figure 60, where the RF performance is slightly lower than constant gate bias voltage operation due to a lower drain current at high input power (see Figure 57) as the HMC980LP4E reaches 1 dB compression.

The output P1dB performance for constant drain current bias can be increased toward constant gate voltage bias performance by increasing the set current toward the I_{DD} value it reaches under RF drive in the constant gate voltage bias condition (see Figure 60).

The limit of increasing drain current under the constant current operation is set by the thermal limitations found in Table 5 with the maximum power dissipation specification. As the I_{DD} increase continues, the actual output P1dB does not continue to increase indefinitely but the power dissipation increases linearly. Therefore, take the trade-off between the power dissipation and output P1dB performance into consideration when using constant drain current biasing.

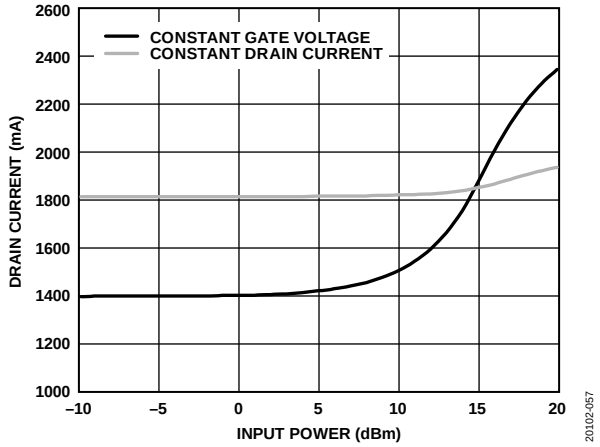

Figure 57. Drain Current vs. Input Power, V_{DD} = 5 V, Frequency = 32 GHz, Constant Drain Current Bias (I_{DRAIN} Setpoint = 1.8 A) and Constant Gate Voltage Bias (V_{GGx} ≈ –0.68 V)

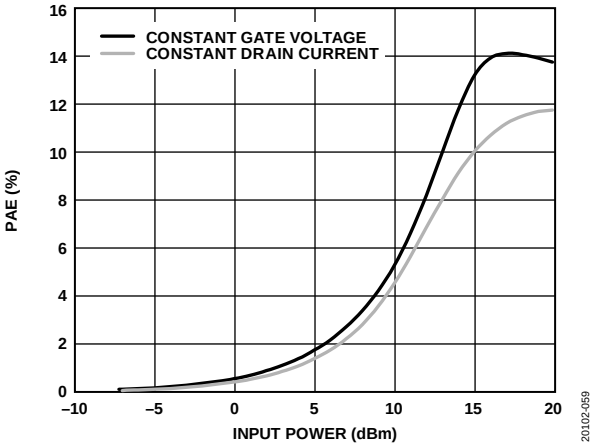

Figure 59. PAE vs. Input Power, V_{DD} = 5 V, Frequency = 32 GHz, Constant Drain Current Bias (I_{DRAIN} Setpoint = 1.8 A) and Constant Gate Voltage Bias (V_{GGx} ≈ –0.68 V)

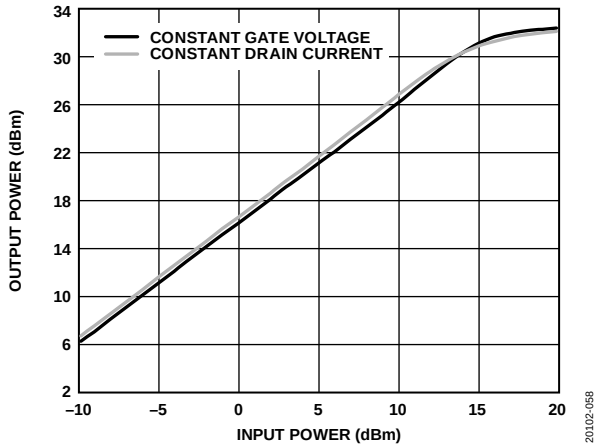

Figure 58. Output Power vs. Input Power, V_{DD} = 5 V, Frequency = 32 GHz, Constant Drain Current Bias (I_{DRAIN} Setpoint = 1.8 A) and Constant Gate Voltage Bias (V_{GGx} ≈ –0.68 V)

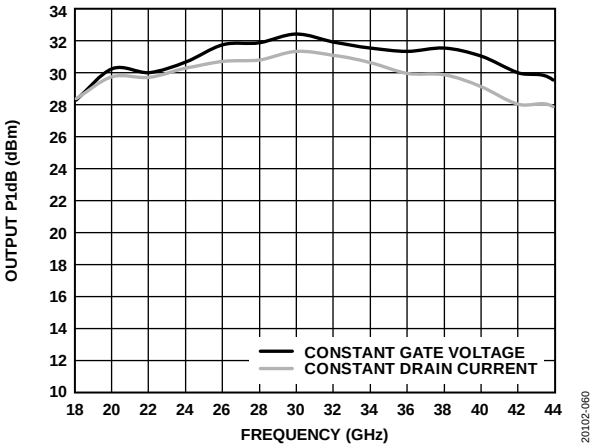

Figure 60. Output P1dB vs. Frequency, V_{DD} = 5 V, Constant Drain Current Bias (I_{DRAIN} Setpoint = 1.8 A) and Constant Gate Voltage Bias (V_{GGx} ≈ –0.68 V))

OUTLINE DIMENSIONS

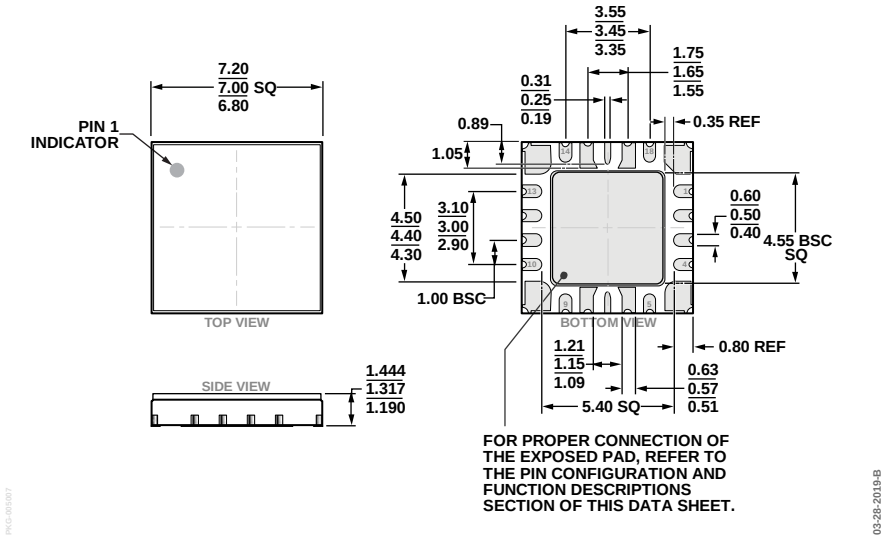

Figure 61. 18-Terminal Ceramic Leadless Chip Carrier with Heat Sink [LCC_HS]
(EH-18-1)
Dimensions shown in millimeters

ORDERING GUIDE

Model[1]	Temperature Range	MSL Rating[2]	Package Description	Package Option
ADPA7005AEHZ	−40°C to +85°C	MSL3	18-Terminal Ceramic Leadless Chip Carrier with Heat Sink [LCC_HS]	EH-18-1
ADPA7005AEHZ-R7	−40°C to +85°C	MSL3	18-Terminal Ceramic Leadless Chip Carrier with Heat Sink [LCC_HS]	EH-18-1
ADPA7005-EVALZ				

[1] Z = RoHS Compliant Part.
[2] See the Absolute Maximum Ratings section for additional information.

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