

## Evaluating the ADP1032 Two-Channel, Isolated Micropower Management Unit

### EVALUATION BOARD FEATURES

Input voltage range: 4.5 V to 60 V

Output voltage for  $V_{OUT1}$ : 24 V or 6 V to 28 V

Output voltage for  $V_{OUT2}$ : 3.3 V, 5.0 V, or 5.15 V

Enable and disable controls

Slew rate controls

Access to SYNC pin for oscillator synchronization

Access to all seven data channels

### EVALUATION KIT CONTENTS

ADP1032CP-x-EVALZ

### SUPPORTED ADP1032 MODELS

ADP1032ACPZ-1, ADP1032ACPZ-2, ADP1032ACPZ-3,  
ADP1032ACPZ-4, and ADP1032ACPZ-5

### ADDITIONAL EQUIPMENT NEEDED

DC power supplies

Multimeters for voltage and current measurements

Electronic or resistive loads

Function generator or alternative digital driver

Oscilloscope

### GENERAL DESCRIPTION

The ADP1032CP-x-EVALZ (where x represents the device model number of 1 through 5) can be used to demonstrate the functionality of the ADP1032 dc-to-dc converters and the isolated data channels.

Simple device measurements, such as line regulation, load regulation, and efficiency can be evaluated with the board. The performance of the isolated digital channels can also be evaluated. Device features, including oscillator synchronization, soft start, power good monitoring, sequencing and slew rate control may be demonstrated.

For more details about the dc-to-dc converters and the isolated data channels, refer to the ADP1032 data sheet.

### ADP1032CP-x-EVALZ PHOTOGRAPH

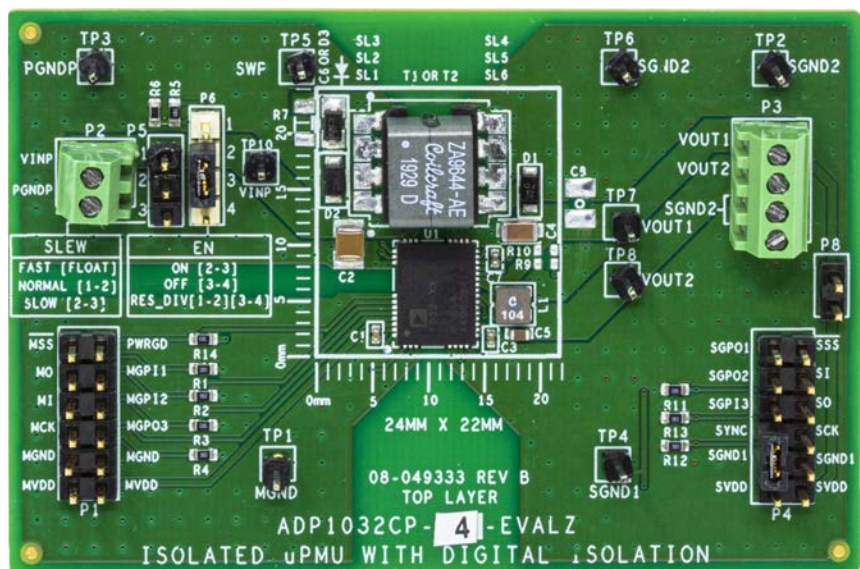


Figure 1.

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REVISION HISTORY

1/2020—Revision 0: Initial Version

## EVALUATION BOARD HARDWARE

### EVALUATION BOARD CONFIGURATIONS

The evaluation board is configured for 4.5 V to 60 V input voltage and 24 V or 6 V to 28 V output voltage for  $V_{OUT1}$ , and 3.3 V, 5.0 V, or 5.15 V output voltage for  $V_{OUT2}$ . The board is designed so that the end user can customize the design if desired, and alternative component values can be obtained from the [ADP1032](#) data sheet.

Figure 2 outlines the board features available to the user and Figure 3 highlights the [ADP1032](#) and supporting components, including locations for optional components if the user wants to modify the design.

The [ADP1032](#) evaluation board was designed to accommodate two transformers: Coilcraft ZA9644-AE (T2) and Würth Elektronik 750317986 (T1).

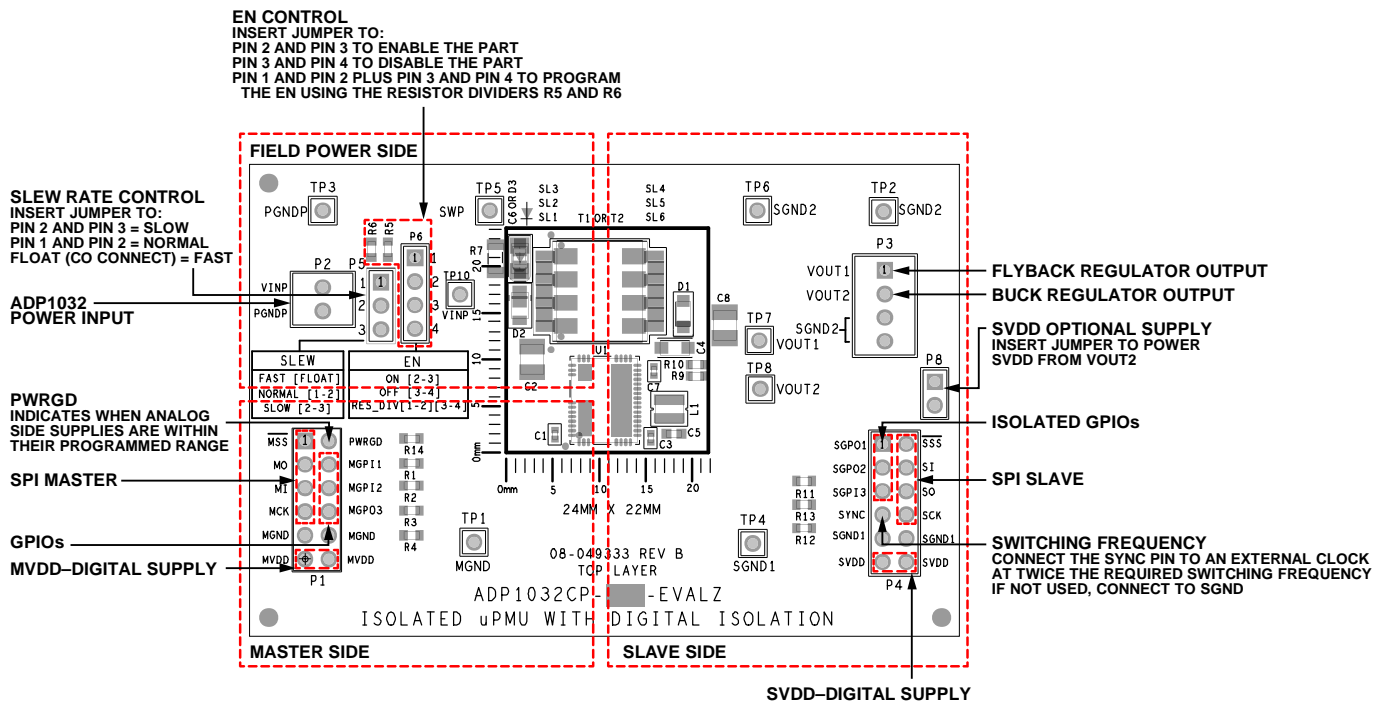


Figure 2. Outline of ADP1032CP-x-EVALZ Features

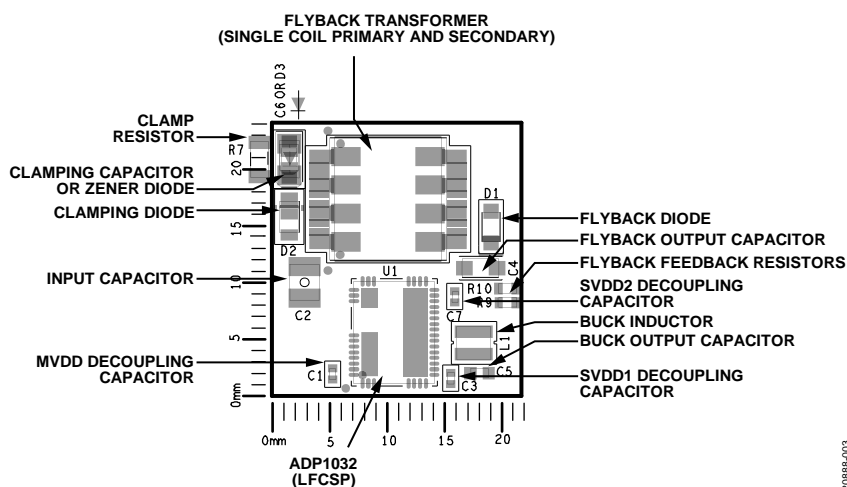


Figure 3. ADP1032CP-x-EVALZ Top Component Detail

Table 1. Evaluation Board Function Descriptions

Jumper/Connector Designation	Jumper/Connector Mnemonic	Description
P1	MVDD	Master side power input. This is between 2.3 V and 5.5 V.
	MCK	Serial peripheral interface (SPI) clock input from the master controller. Drives SCK on slave side.
	MI	SPI data output from the slave to the master master input, slave output (MISO) line. Driven by SO on slave side.
	MO	SPI data input from the master output, slave input (MOSI) line. Drives SI on slave side.
	$\overline{\text{MSS}}$	SPI slave select input from the master. This signal uses an active low logic. Drives $\overline{\text{SSS}}$ on slave side.
	PWRGD	Indicates when secondary side supplies on slave side are within their programmed range.
	MGPI1	General-Purpose Input 1. Used to send a low speed logic signal to the slave side. Paired with SGPO1.
	MGPI2	General-Purpose Input 2. Used to send a low speed logic signal to the slave side. Paired with SGPO2.
P2	MGPO3	General-Purpose Output 3. Used to receive a low speed logic signal from the slave side. Paired with SGPI3.
	MGND	Master side ground connection.
P3	VINP	Power input to <a href="#">ADP1032</a> . This is between 4.5 V and 60 V.
	PGNDP	Power side ground connection.
P4	VOUT1	Output from flyback regulator.
	VOUT2	Output from buck regulator.
	SGND2	Slave Side Ground 2 connection.
P5	SVDD	Slave side power input. This is between 1.8 V and 5.5 V.
	SCK	SPI slave clock output. Paired with MCK.
	SO	SPI slave data output. Paired with MI.
	SI	SPI slave data input. Paired with MO.
	$\overline{\text{SSS}}$	SPI slave select output. Paired with $\overline{\text{MSS}}$ . Driven by $\overline{\text{MSS}}$ on the master side.
	SGPO1	General Purpose Output 1. Paired with MGPI1.
	SGPO2	General Purpose Output 2. Paired with MGPI2.
	SGPI3	General Purpose Input 3. Paired with MGPO3.
	SYNC	Frequency setting and synchronization input. Connect the SYNC pin to an external clock. This is between 350 kHz and 750 kHz. The switching frequency of the flyback regulator is half of the external clock frequency. If not used, connect to SGND1.
	SGND1	Slave Side Ground 1 connection.
P6	SLEW	Flyback regulator slew rate control. The SLEW pin sets the slew rate for the SWP pin driver. For the fastest slew rate (best efficiency), leave the SLEW pin open. For the normal slew rate, connect the SLEW pin to VINP with Pin 1 and Pin 2 shorted. For the slowest slew rate (best electromagnetic interference (EMI) performance), connect the SLEW pin to PGNDP with Pin 2 and Pin 3 shorted.
	EN	Precision enable control. The EN pin is compared to an internal precision reference to enable the flyback regulator output. Connect a jumper to Pin 2 and Pin 3 to turn on the flyback regulator. Connect a jumper to Pin 3 and Pin 4 to turn off the flyback regulator. Connect a jumper to Pin 1 and Pin 2 together with another jumper to Pin 3 and Pin 4 to use the input as a programmable undervoltage lockout (UVLO) through the R5 resistive divider and R6 resistive divider.
P8	SVDD Optional Supply	Option for VOUT2 to power SVDD. Connect a jumper to P8 to power the SVDD from VOUT2.
TP1	MGND	MGND test point.
TP2, TP6	SGND2	SGND2 test points. Connected to SGND1.
TP3	PGNDP	PGNDP test point.
TP4	SGND1	SGND1 test point. Connected to SGND2.
TP5	SWP	Flyback regulator switching node test point.
TP7	VOUT1	VOUT1 test point.
TP8	VOUT2	VOUT2 test point.

## MEASUREMENT SETUP

### FLYBACK OUTPUT MEASUREMENTS

Figure 4 shows the recommended setup to evaluate the flyback regulator of the ADP1032CP-x-EVALZ.

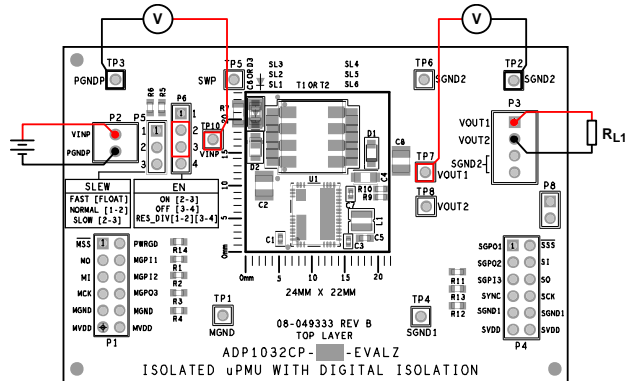


Figure 4. Flyback Regulator Measurement Setup

### BUCK OUTPUT MEASUREMENTS

Figure 5 shows the recommended setup to evaluate the buck regulator of the ADP1032CP-x-EVALZ.

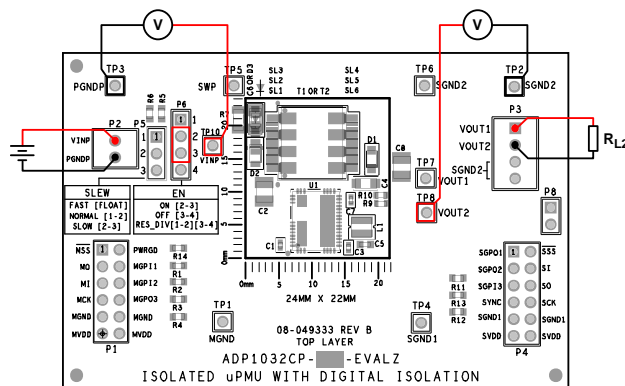


Figure 5. Buck Regulator Measurement Setup

### POWER DOMAIN EFFICIENCY MEASUREMENT

For overall efficiency measurements, the actual input and output voltages and currents must be measured. Figure 6 shows the setup for the overall efficiency measurement for the ADP1032CP-x-EVALZ.

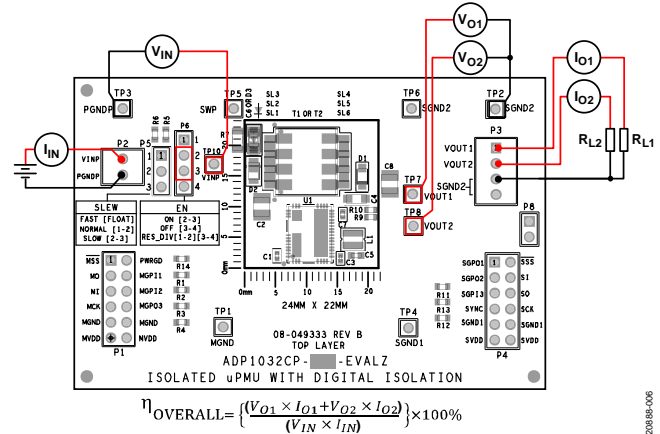


Figure 6. Overall Efficiency Measurement Setup

### DATA INPUT/OUTPUT (I/O) MEASUREMENT

Each data channel, and the associated power supply input, is accessed through the P1 and P4 header connectors. Each side of the ADP1032CP-x-EVALZ isolator requires an off board power source. The power sources must be independent from each other if users want to apply common-mode voltages across the isolation barrier. Sharing a single power supply for MVDD and SVDD does not harm the isolator. Sharing a power supply is also useful for testing the ADP1032 digital isolators when common-mode voltages are not present.

A 100 kΩ pull-down resistor to ground is installed on each digital input. A 100 kΩ pull-up resistor is installed across the PWRGD output and MVDD.

To properly operate the SPI channels and the GPIO channels, refer to the ADP1032 data sheet.

### HIGH VOLTAGE CAPABILITY

Take appropriate care when using the evaluation board at high voltages. Do not rely on the printed circuit board (PCB) for safety functions because the PCB has not been high potential tested (also known as HIPOT tested or dielectric withstanding voltage tested) nor certified for safety.

## OUTPUT VOLTAGE MEASUREMENTS

For basic output voltage accuracy measurements, connect the evaluation board to a voltage source and a voltmeter. Use a resistor as the load for the regulator.

Ensure that the resistor has an adequate power rating to handle the expected power dissipation. Use an electronic load as an alternative. Ensure that the voltage source supplies enough current for the expected load levels, considering the device efficiency.

Use the following steps to connect to a voltage source and voltmeter:

1. Connect the negative terminal (–) of the voltage source to the PGNDP terminal of the power input connector (P2) on the left side of the evaluation board.
2. Connect the positive terminal (+) of the voltage source to the VINP terminal of the power input connector (P2) on the left side of the evaluation board.
3. Connect a voltmeter across the VINP input terminal at TP10, and connect PGNDP at TP3 to monitor the actual input voltage supplied to the ADP1032.
4. Connect a load between the VOUT1 or VOUT2 terminal and the SGND2 terminal at the output connector (P3) on the right side of the evaluation board.
5. Connect the voltmeter across the selected output terminal and ground in parallel with the load resistor.

Turn on the voltage source for VINP. If the EN jumper is in Pin 2 and Pin 3, the regulator powers up.

If the load current is large, the user needs to connect the voltmeter as close as possible to the output capacitor to reduce the effects of the voltage drops across the resistor (IR).

If long power leads are used from the power supply, especially at higher loads, it is recommended to connect a large capacitor (100  $\mu$ F or more) across the VINP terminals to prevent losses from lead inductance. Likewise, adjust the power supply output voltage to ensure that the supply voltage measured at VINP test point TP10 is within the user specified target range. A power supply with a 4-wire supply and sense arrangement can be used as an alternative to manually adjust the supply voltage to be within the user specified range.

## LINE REGULATION

For line regulation measurements, the output of the regulator is monitored while its input is varied. For optimal line regulation, the output must change as little as possible with varying input levels. This measurement can be repeated under different load conditions. During line regulation tests, ensure that the leads to the power supply are short and remove any additional input capacitor. Figure 7 shows the typical line regulation performance of the ADP1032 flyback regulator output.

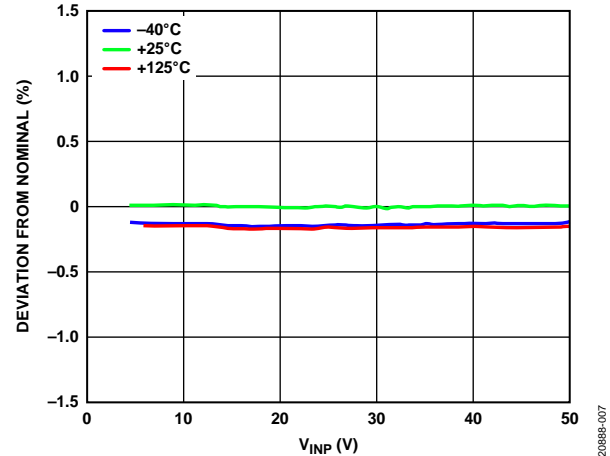


Figure 7. Flyback Regulator Line Regulation,  $V_{OUT1} = 24$  V, 80 mA Load,  $T_A = 25^\circ\text{C}$ , Nominal Condition:  $V_{OUT1} = 24$  V with Input Voltage ( $V_{INP}$ ) = 24 V

## LOAD REGULATION

For load regulation measurements, monitor the regulator output while the load is varied. For optimal load regulation, the output must change as little as possible with varying loads. The input voltage must be held constant during this measurement. Figure 8 and Figure 9 show the typical load regulation performance of the ADP1032 at the flyback regulator output and buck regulator output, respectively. Keep power leads short during this test and ensure that the supply voltage is constant under all load conditions or use a power supply with remote sense.

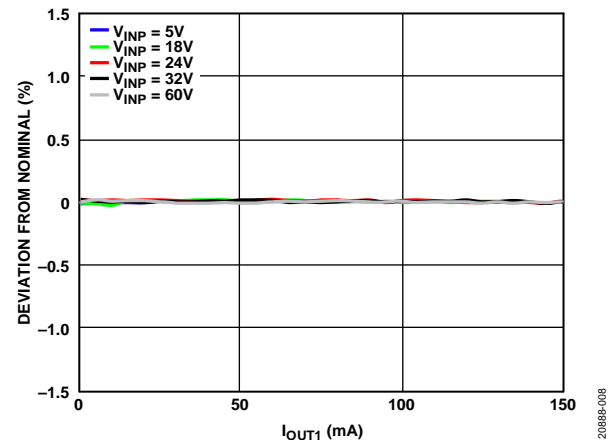


Figure 8. Flyback Regulator Load Regulation over Various  $V_{INP}$ , Using Adjustable Version,  $V_{OUT1} = 24$  V,  $V_{OUT2} = 3.3$  V, Buck Regulator Output Current ( $I_{OUT2}$ ) = 0 mA,  $T_A = 25^\circ\text{C}$ , Nominal Condition:  $V_{OUT1}$  at 20 mA Load



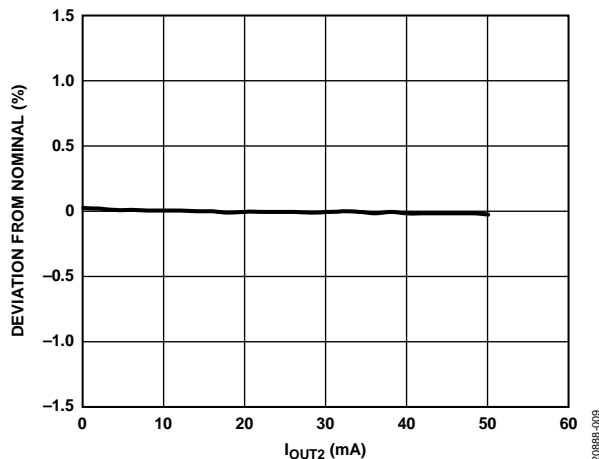


Figure 9. Buck Regulator Load Regulation,  $V_{OUT1} = 24\text{ V}$ ,  $V_{OUT2} = 3.3\text{ V}$ ,  $T_A = 25^\circ\text{C}$ , Nominal Condition:  $V_{OUT2}$  at 10 mA Load

## EFFICIENCY

For efficiency measurements, monitor the regulator input supply and output voltages while the load is varied. Keep power leads short during this test and use a power supply with remote sense. Connect ammeters in series with the input supply and the loads. Connect voltmeters to the test points provided for the input and output of the regulators. For the highest possible efficiency results, measure the voltage across the input and output capacitors. If possible, particularly at a low current, trigger the meters simultaneously and set to average readings for a period of a few hundred milliseconds or more. Figure 10 shows a typical overall efficiency curve for the ADP1032 with varying output load on the flyback regulator and a constant load on the buck regulator.

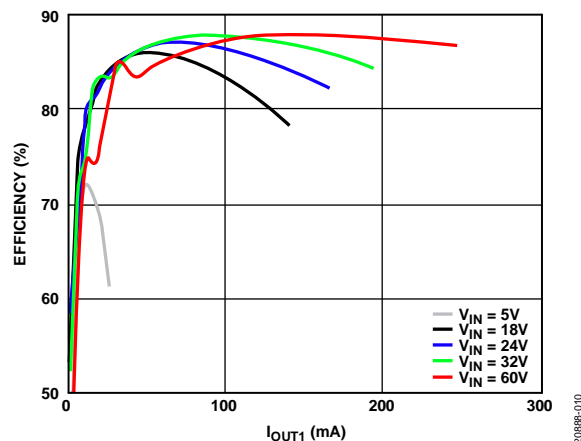


Figure 10. ADP1032 Overall Efficiency with Various Input Voltages,  $V_{OUT1} = 24\text{ V}$ ,  $V_{OUT2} = 3.3\text{ V}$ ,  $I_{OUT2} = 30\text{ mA}$ ,  $T_A = 25^\circ\text{C}$

## TRANSFORMER CONFIGURATIONS

The ADP1032CP-x-EVALZ is designed to accommodate two transformers: the Coilcraft ZA9644-AE as T2 and the Würth Elektronik 750317986 as T1. These transformers are chosen due to their smaller size and performance. See the ADP1032 data sheet for the size and efficiency performance comparisons. When ZA9644-AE (T2) is used, do not connect any solder link (SLx) as shown in Figure 1. When the 750317986 (T1) is used, connect solder links SL2, SL4, and SL6. Refer to Figure 11 if the 750317986 (T1) transformer is used.

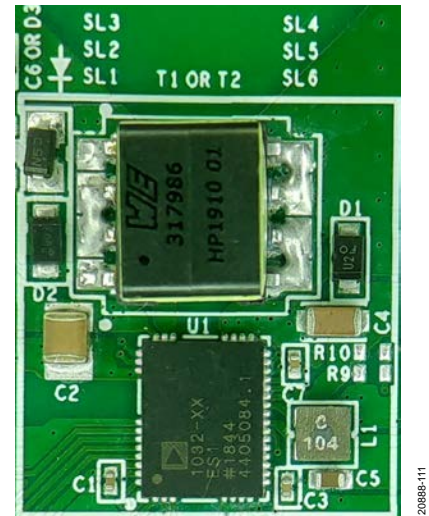


Figure 11. Solder Link Connections when Using T1

**OPTION TO USE RCD CLAMP**

SNUB  
R7 22K DNI  
C6 C0805\_R1206\_COMBO DNI  
VINP

**FIELD POWER**  
4.5V TO 60V  
VINP  
PGNDP  
282834-2  
PGNDP

TP10  
VINP  
TP5 (1)  
PGND  
C2 4.7UF  
PGNDP

EN 31  
SLEW 32  
GNDP 33  
PGNDP 28  
PAD 28  
TP3  
PGNDP

PWRGD 35  
MGPI1 36  
MGPI2 37  
MGPO3 38  
MCK 40  
MO 41  
MI 1  
MSSB 2  
MVDD 39

C1 0.1UF 16V  
MGND  
TP1 MGND  
MGND

U1 ADP1032ACPZ-1

VOUT1 18  
FB1 19  
VOUT2 15  
SW2 17  
DNC 13  
DNC 12  
DNC 11  
SYNC 14  
SGPO1 23  
SGPO2 22  
SGPI3 21  
SCK 9  
SI 8  
SO 7  
SSSB 6  
SVDD1 10  
SVDD2 20

D1 US1DWF-7  
C4 10UF  
C8 10UF  
SGND2  
TP7  
VOUT1  
TP8  
VOUT2  
R10 3.48MEG  
R9 120K  
SGND2  
L1 100UH  
C5 4.7UF  
SGND2

TP6  
SGND2  
TP4  
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Figure 12. ADP1032CP-x-EVALZ Schematic



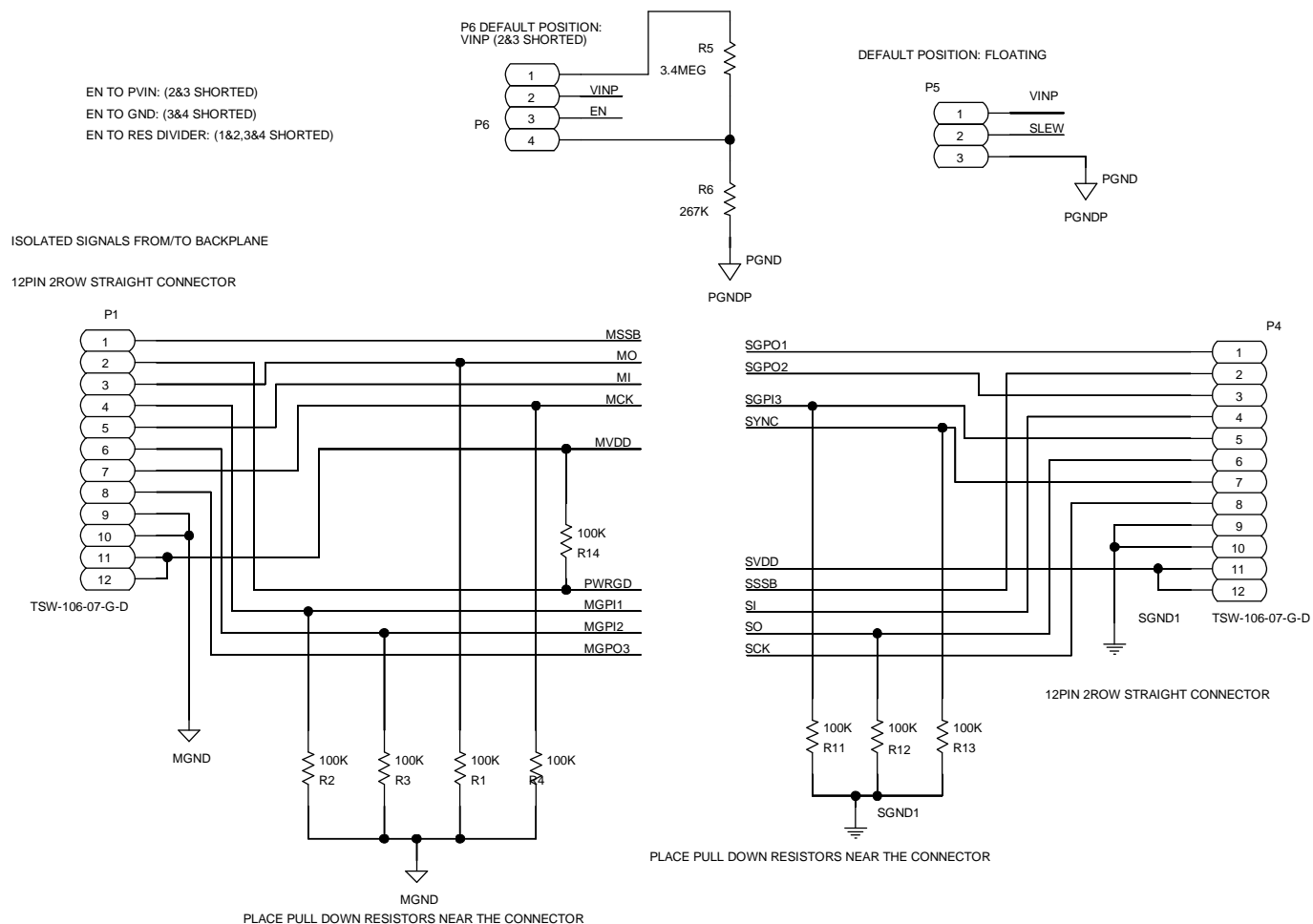


Figure 13. ADP1032CP-x-EVALZ Schematic, Connectors and Peripherals

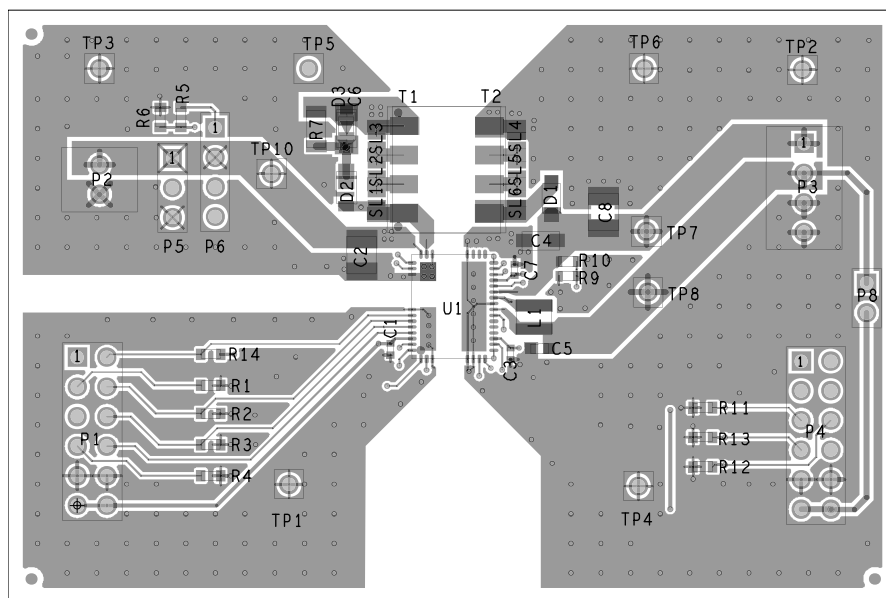


Figure 14. ADP1032CP-x-EVALZ Top Layer

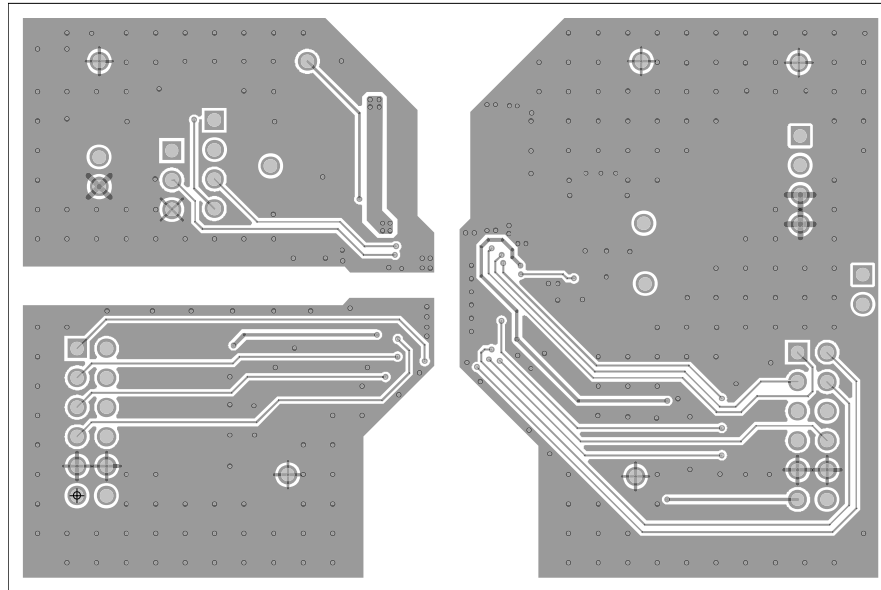


Figure 15. ADP1032CP-x-EVALZ Bottom Layer

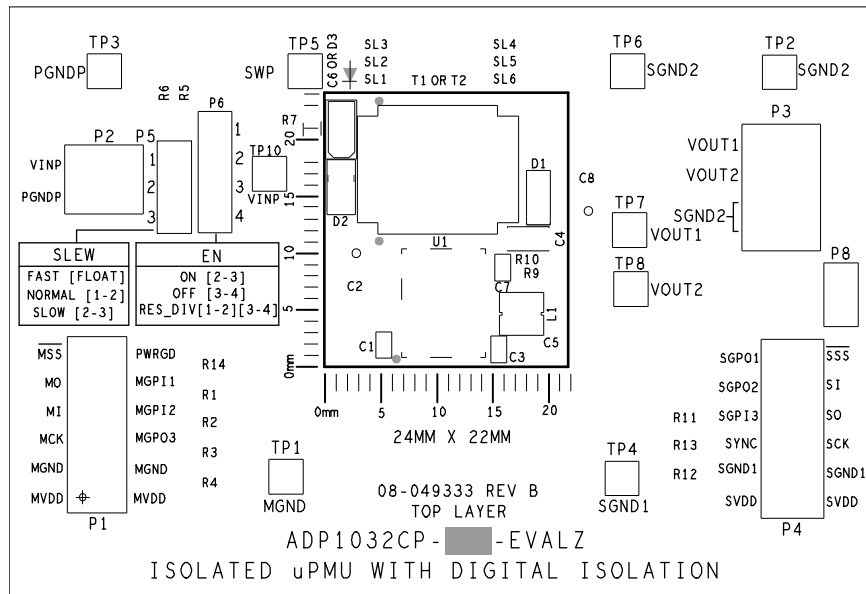


Figure 16. ADP1032CP-x-EVALZ Silkscreen (Top)

## ORDERING INFORMATION

## BILL OF MATERIALS

Table 2.

Quantity	Reference Designator	Description	Manufacturer/Part Number
3	C1, C3, C7	Capacitors multilayer ceramic capacitor (MLCC), 0.1 $\mu$ F, 16 V, 0402, X7R	Determined by the user
1	C2	Capacitor MLCC, 4.7 $\mu$ F, 100 V, 1210, X7S	Murata/GCM32DC72A475KE02L
1	C4	Capacitor MLCC, 10 $\mu$ F, 50 V, 1206, X7R	Samsung/CL31B106KBHNNNE
1	C5	Capacitor MLCC, 4.7 $\mu$ F, 10 V, 0603, X7S	TDK/C1608X7S1A475K080AC
1	D1	Diode, ultrafast rectifier, 1 A, 200 V, SMD	Diodes Incorporated/US1DWF-7
1	D2	Diode, Schottky rectifier, 1 A, 200 V, SMD	Diodes Incorporated/DFLS1200Q-7
1	D3	Diode, Zener voltage regulator, 62 V, 0.5 W	On Semiconductor/MMSZ5265BT1G
1	L1	Inductor, shielded, 100 $\mu$ H, 0.39 A	Coilcraft/XFL3012-104MEB
2	P1, P4	Headers, 12-pin	Samtec/TSW-106-07-G-D
1	P2	Terminal block, 2-pin	TE Connectivity/282834-2
1	P3	Terminal block, 4-pin	TE Connectivity/282834-4
1	P5	Header, 3-pin	Samtec/TSW-103-07-F-S
1	P6	Header, 4-pin	Samtec/TSW-104-07-G-S
9	TP1 to TP8, TP10	Headers, 1-pin	Samtec/TSW-101-07-G-S
1	P8	Header, 2-pin	Samtec/TSW-101-07-G-D
8	R1 to R4, R11 to R14	Resistors, 100 k $\Omega$ , 1/10 W, 1%, 0603, SMD	Determined by the user
1	R5	Resistor, 3.4 M $\Omega$ , 1/10 W, 1%, 0603, SMD	Determined by the user
1	R6	Resistor, 267 k $\Omega$ , 1/10 W, 1%, 0603, SMD	Determined by the user
1	R9	Resistor, 120 k $\Omega$ , 1/10 W, 1%, 0603, SMD	Determined by the user
1	R10	Resistor, 3.48 M $\Omega$ , 1/10 W, 1%, 0603, SMD	Determined by the user
1	T2	Transformer, 1:1 turn ratio, 470 $\mu$ H	Coilcraft/ZA9644-AE
1	U1	Two-channel isolated $\mu$ PMU with 7-channel digital isolators	Analog Devices/ADP1032

**ESD Caution**

**ESD (electrostatic discharge) sensitive device.** Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

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