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Evaluation Board for ADP1031 Three-Channel, Isolated Micropower Management Unit with Seven Digital Isolators

FEATURES

Input voltage range: 4.5 V to 60 V
Output voltage V_{OUT1}: 24 V or 21 V
Output voltage V_{OUT2}: 5.15 V
Output voltage V_{OUT3}: −15 V
Enable and disable controls
Slew rate controls
Access to SYNC pin for oscillator synchronization
Access to all seven data channels

EVALUATION KIT CONTENTS

ADP1031CP-1-EVALZ, ADP1031CP-2-EVALZ, ADP1031CP-3-EVALZ, ADP1031CP-4-EVALZ, or ADP1031CP-5-EVALZ evaluation board

SUPPORTED ADP1031 GENERICS

ADP1031ACPZ-1, ADP1031ACPZ-2, ADP1031ACPZ-3, ADP1031ACPZ-4, and ADP1031ACPZ-5

EQUIPMENT NEEDED

DC power supplies
Multimeters for voltage and current measurements
Electronic load or resistive loads
Function generator or alternative digital driver
Oscilloscope

DOCUMENTS NEEDED

ADP1031 data sheet

GENERAL DESCRIPTION

The ADP1031CP-EVALZ is a fully featured evaluation board that demonstrates the functionality of the ADP1031 dc-to-dc converters and the isolated data channels.

Users can evaluate ADP1031 device measurements, such as line regulation, load regulation, and efficiency with the evaluation board. The board also assists in evaluating the functionality of the isolated digital channels. Device features including oscillator synchronization, soft start, power good monitoring, sequencing, and slew rate control can be demonstrated on the evaluation board.

Each board model in the evaluation kit has a different output configuration. Only one board model is included in the kit but users can order from five different board models to fit their application needs.

Refer to the ADP1031 data sheet for more details about the dc-to-dc converters and isolated data channels.

EVALUATION BOARD PHOTOGRAPH

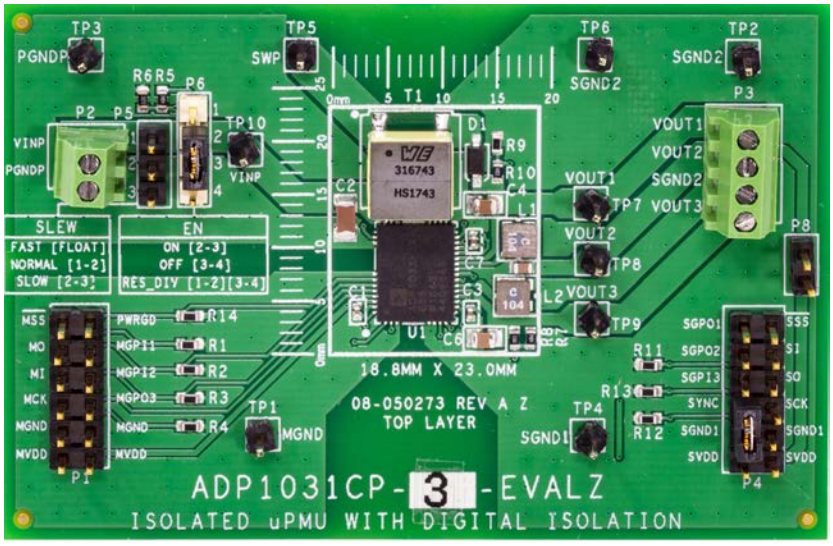

Figure 1.

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REVISION HISTORY

1/2019—Revision 0: Initial Version

EVALUATION BOARD HARDWARE

EVALUATION BOARD CONFIGURATIONS

The evaluation board is preconfigured to the output voltages described in Table 1.

Table 1. Evaluation Board Output Voltage Configurations

Model	V_{OUT1}[1]	V_{OUT2}	V_{OUT3}[1]
ADP1031CP-1-EVALZ	24 V (ADJ)	5.15 V	−15 V (ADJ)
ADP1031CP-2-EVALZ	24 V (ADJ)	5 V	−15 V (ADJ)
ADP1031CP-3-EVALZ	24 V (ADJ)	3.3 V	−15 V (ADJ)
ADP1031CP-4-EVALZ	24 V	5.15 V	−15 V (ADJ)
ADP1031CP-5-EVALZ	21 V	5.15 V	−15 V (ADJ)

[1] ADJ means that the output is adjusted to the specified voltage. If only the voltage is specified, without the ADJ, the output is fixed or factory programmed.

The board is designed so that if desired, the user can customize the converter design to obtain up to 60 V between the VOUT1 and VOUT3 terminals on the board. The user is responsible for ensuring that the board is suitably configured and that appropriate safety precautions are taken.

Figure 2 outlines the evaluation board features available for the user. Figure 3 provides information about both the ADP1031 and locations for optional components, which the user can use to modify the converter design.

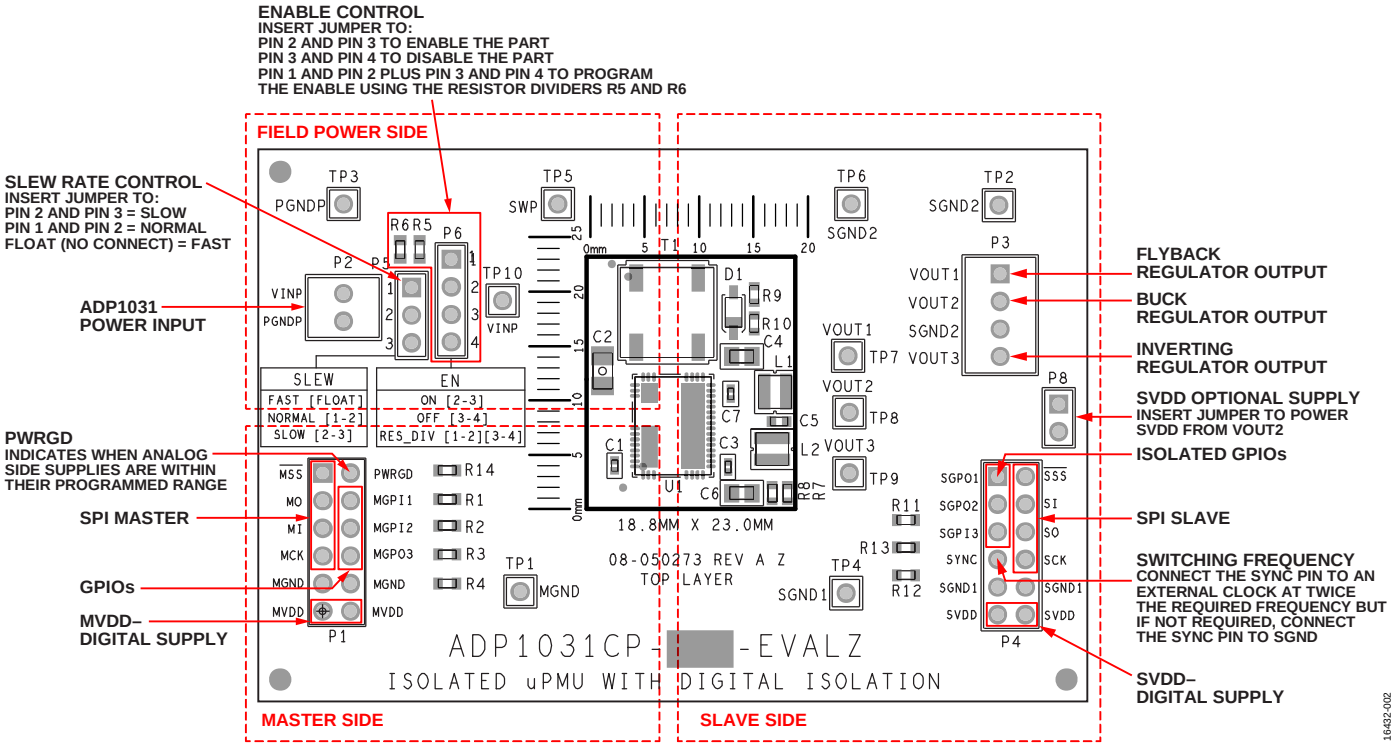

Figure 2. Outline of ADP1031CP-EVALZ Evaluation Board Features

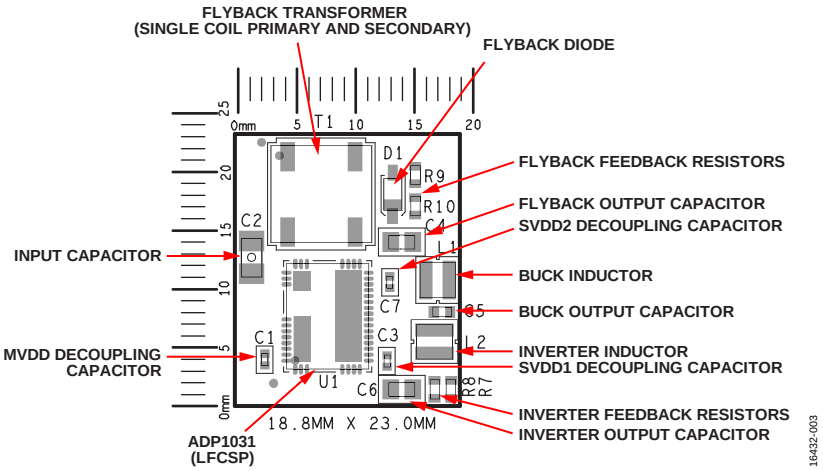

Figure 3. ADP1031CP-EVALZ Top Component Detail

Table 2. Evaluation Board Function Descriptions

Jumper/Connector Designation	Jumper/Connector Mnemonic	Description
P1	MVDD	Master side power input. The input voltage is between 2.3 V and 5.5 V.
	MCK	SPI clock input from the master controller. Drives SCK on the slave side.
	MI	SPI data output from the slave MI/SO line. Driven by SO on the slave side.
	MO	SPI data input to the slave MO/SI line. Drives SI on the slave side.
	$\overline{\text{MSS}}$	SPI slave select input from the master controller. This signal uses an active low logic. Drives $\overline{\text{SSS}}$ on the slave side.
	PWRGD	Power good. Indicates when secondary side supplies are within the programmed range.
	MGPI1	General purpose Input 1. Paired with SGPO1.
	MGPI2	General purpose Input 2. Paired with SGPO2.
	MGPO3	General purpose Output 3. Paired with SGPI3.
P2	VINP	Power input to the ADP1031 flyback regulator. The input voltage is between 4.5 V and 60 V.
P3	VOUT1	Output from the flyback regulator. Set to 24 V in default configuration.
	VOUT2	Output from the buck regulator. Factory set to 5.15 V in default configuration.
	VOUT3	Output from the inverting regulator. Set to −15 V in default configuration.
P4	SVDD	Slave side power input. This is between 1.8 V and 5.5 V.
	SCK	SPI clock output from the master MCK/SCK line. Paired with MCK. Driven by MCK on the master side.
	SO	SPI data input to the master MI/SO line. Paired with MI. Drives MI on the master side.
	SI	SPI data output from the master MO/SI line. Paired with MO. Driven by MO on the master side.
	$\overline{\text{SSS}}$	SPI slave select output. Paired with $\overline{\text{MSS}}$. Driven by $\overline{\text{MSS}}$ on the master side.
	SGPO1	General purpose Output 1. Paired with MGPI1.
	SGPO2	General purpose Output 2. Paired with MGPI2.
	SGPI3	General purpose Input 3. Paired with MGPO3.
	SYNC	Frequency setting and synchronization input. Connect the SYNC pin to an external clock with a frequency between 350 kHz and 750 kHz. The switching frequency of the flyback regulator is half of the external clock frequency. If SYNC is not used, connect to SGND.
P5	SLEW	Flyback regulator slew rate control. The SLEW pin sets the slew rate for the SWP driver. For the fastest slew rate (best efficiency), leave the SLEW pin open. For the normal slew rate, connect the SLEW pin to VINP with Pin 1 and Pin 2 shorted. For the slowest slew rate (best electromagnetic interference (EMI) performance), connect the SLEW pin to GNDP with Pin 2 and Pin 3 shorted.
P6	EN	Precision enable control. The EN pin is compared to an internal precision reference to enable the flyback regulator output. Connect a jumper to Pin 2 and Pin 3 to turn on the flyback regulator. Connect a jumper to Pin 3 and Pin 4 to turn off the flyback regulator. Connect a jumper to Pin 1 and Pin 2 together with another jumper to Pin 3 and Pin 4 to use the input as a programmable undervoltage lockout (UVLO) through the R5 resistive divider and R6 resistive divider.

Jumper/Connector Designation	Jumper/Connector Mnemonic	Description
P8	SVDD Optional Supply	Option for VOUT2 to power SVDD. Connect a jumper to P8 to power the SVDD from VOUT2.
TP1	MGND	MGND test point.
TP2, TP6	SGND2	SGND2 test points. Connected to SGND1.
TP3	PGNDP	PGNDP test point.
TP4	SGND1	SGND1 test point. Connected to SGND2.
TP5	SWP	Flyback regulator switching node test point.
TP7	VOUT1	VOUT1 test point.
TP8	VOUT2	VOUT2 test point.
TP9	VOUT3	VOUT3 test point.

MEASUREMENT SETUP

REGULATOR OUTPUT MEASUREMENT

Figure 4 shows the recommended measurement setup to evaluate the ADP1031CP-EVALZ flyback regulator.

Figure 5 shows the recommended setup to evaluate the ADP1031CP-EVALZ buck regulator.

Figure 6 shows the recommended setup to evaluate the ADP1031CP-EVALZ inverting regulator.

POWER DOMAIN EFFICIENCY MEASUREMENT

Measure the actual input voltage and output voltage from the evaluation board for overall efficiency measurements. Figure 7 shows the recommended setup for the overall efficiency measurement for the ADP1031CP-EVALZ.

The overall efficiency is calculated using the following equation:

$$\eta_{OVERALL} = \left(\frac{\left((V_{OUT1} \times I_{OUT1}) + (V_{OUT2} \times I_{OUT2}) + (V_{OUT3} \times I_{OUT3}) \right)}{(V_{INP} \times I_{IN})} \right)$$

where:

$\eta_{OVERALL}$ = the overall efficiency of the ADP1031.
V_{OUT1} = the output voltage of the flyback regulator.
I_{OUT1} = the output current on the flyback regulator.
V_{OUT2} = the output voltage of the buck regulator.
I_{OUT2} = the output current on the buck regulator.
V_{OUT3} = the output voltage of the inverting regulator.
I_{OUT3} = the output current on the inverting regulator.
V_{INP} = the input supply voltage.
I_{IN} = the input supply current.

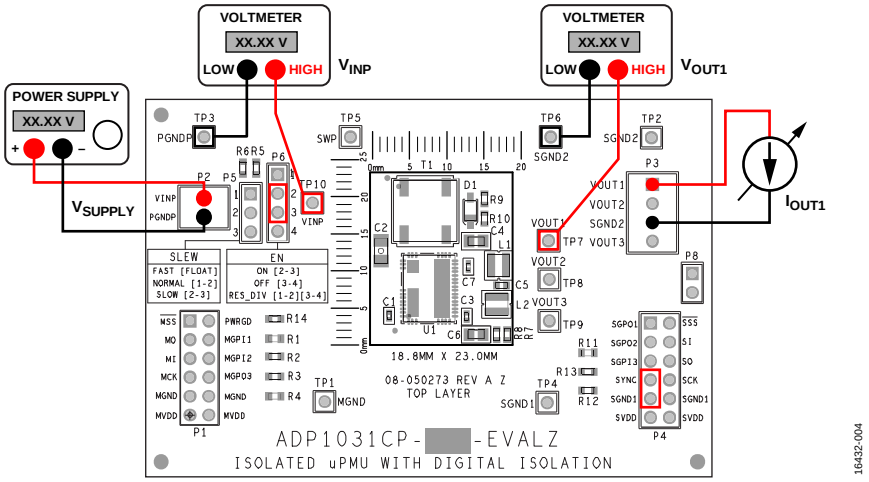

Figure 4. Flyback Regulator Measurement Setup

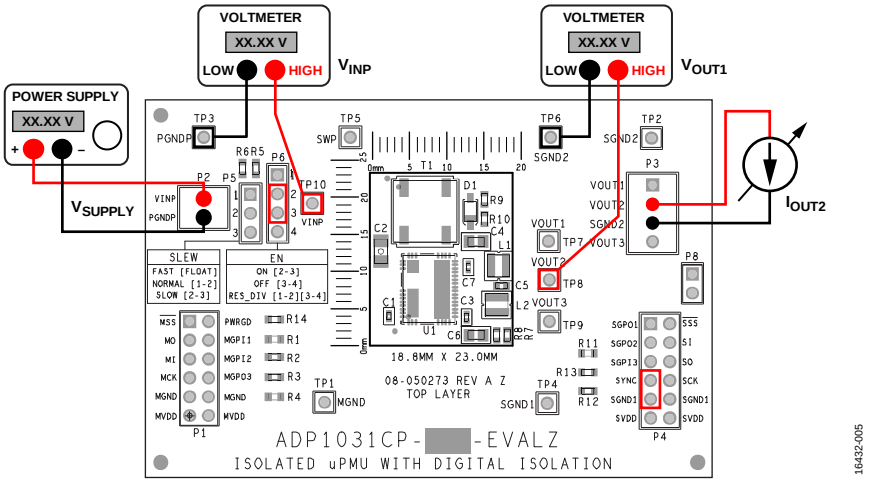

Figure 5. Buck Regulator Measurement Setup

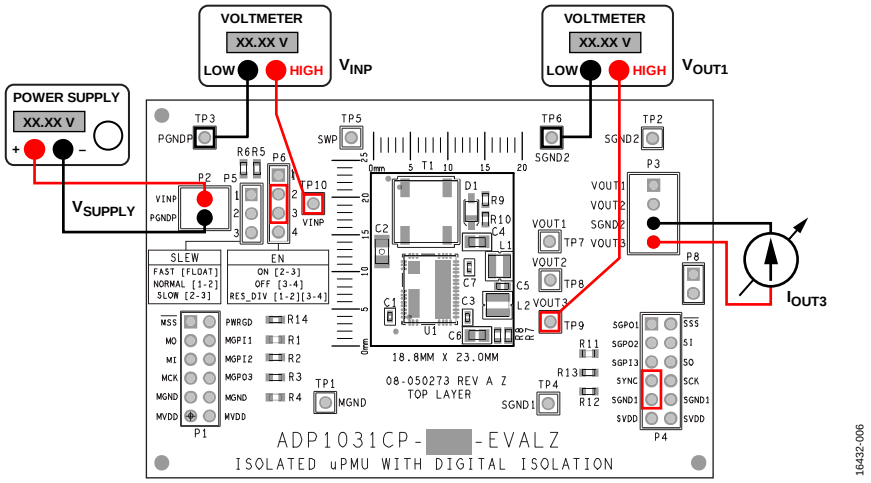

Figure 6. Inverting Measurement Setup

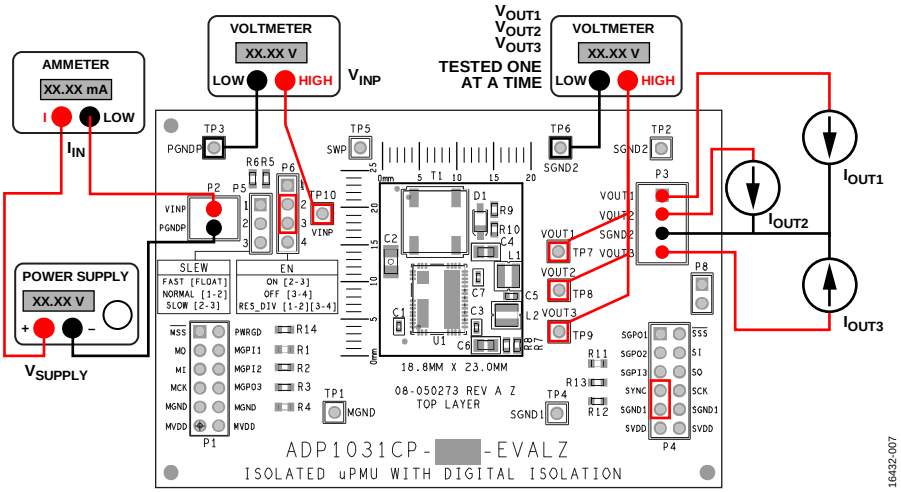

Figure 7. Overall Efficiency Measurement Setup

DATA INPUT/OUTPUT (I/O) MEASUREMENT

Each data channel, and the associated power supply input, is accessed through the P1 header connector and P4 header connector. Each side of the ADP1031CP-EVALZ isolator requires an off-board power source. The power sources must be independent from each other if users want to apply common-mode voltages across the isolation barrier. Sharing a single power supply for MVDD and SVDD does not harm the isolator. Sharing a power supply is also useful for testing the ADP1031 digital isolators when common-mode voltages are not present.

A 100 kΩ pull-down resistor to ground is installed on each digital input. A 100 kΩ pull-up resistor is installed across the PWRGD output and MVDD.

To properly operate the SPI channels and GPIO channels, refer the ADP1031 data sheet.

HIGH VOLTAGE CAPABILITY

Take appropriate care when using the evaluation board at high voltages. Do not rely on the printed circuit board (PCB) for safety functions because the PCB has not been high potential tested (also known as hipot tested or dielectric withstanding voltage tested) nor certified for safety.

OUTPUT VOLTAGE MEASUREMENTS

For accurate output voltage measurements from the evaluation board, connect the evaluation board to a voltage source and a voltmeter. Use a resistor or an electronic load (E-Load) as the load for the regulators.

Ensure that the resistor has an adequate power rating to handle the expected power dissipation. Taking into account the device efficiency, ensure that the power supply has enough current for the expected load levels.

Use the following steps to connect the power supply and voltmeter to the evaluation board (refer to Figure 4 through Figure 7 for setup diagrams):

1. Connect the negative terminal (−) of the power supply and voltmeter to the PGNDP power terminal in Connector P2 on the left side of the evaluation board.
2. Connect the positive terminal (+) of the power supply to the VINP terminal in Connector P2 on the left hand side of the evaluation board.
3. Connect a voltmeter across the VINP at TP10, and connect PGNDP at TP3 to monitor the actual input voltage supplied to the ADP1031.
4. Connect a load between the VOUT1, VOUT2, or VOUT3 terminal and the SGND2 terminal at the output connector (P3) on the right side of the evaluation board.
5. Connect the voltmeters to the output test points (TP7 for VOUT1, TP8 for VOUT2, and TP9 for VOUT3) in reference to SGND2 or SGND1.

Turn on the voltage source for VINP by pressing the power button. The regulators power up if Pin 2 and Pin 3 are connected to the EN jumper (P6).

If long power leads are used from the power supply, especially with higher loads, users are recommended to use a large capacitor (100 µF or more) connected across the VINP terminals and PGNDP to prevent losses from lead inductance. Likewise, adjust the input voltage to ensure that the supply voltage is within the user specified target range. A power supply with a 4-wire supply and sense arrangement can be used as an alternative to manually adjusting the supply voltage to be within the user specified range.

LINE REGULATION

For line regulation measurements, the voltmeter measures the regulator output while the input supply is varied. The line regulation measurement can be repeated under different load conditions. During line regulation tests, the leads to the power supply must be short, and any additional input capacitor must be removed. Figure 8 shows the typical line regulation performance of the ADP1031 flyback regulator output.

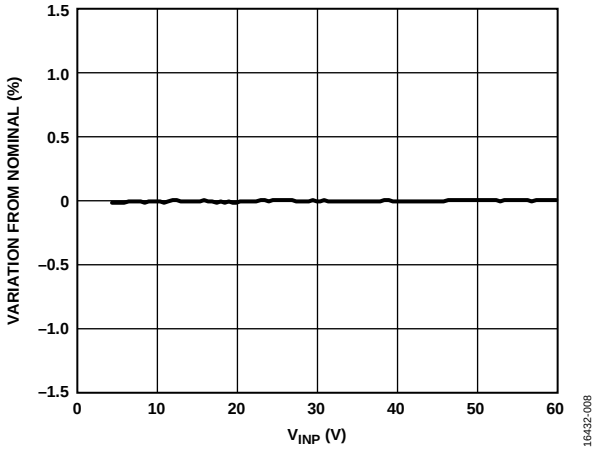

Figure 8. Flyback Regulator Output Line Regulation, Flyback Regulator Output Voltage (V_{OUT1}) = 24 V, Flyback Regulator Output Current (I_{OUT1}) = 20 mA, T_A = 25°C, Load Regulation, Nominal = V_{OUT1} at 24 V Input Supply

LOAD REGULATION

For load regulation measurements, monitor the regulator output while the load is varied. The input voltage must be held constant during the load regulation measurement. Figure 9, Figure 10, and Figure 11 show the typical ADP1031 load regulation performance at the flyback regulator output, buck regulator output and inverting regulator output, respectively. Keep power leads short during this test and ensure that the supply voltage is constant under all load conditions.

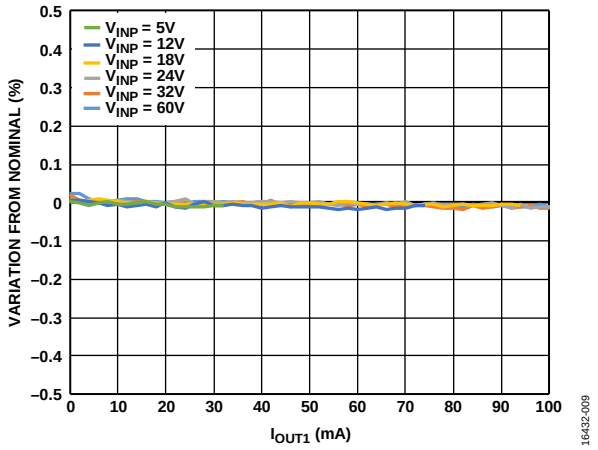

Figure 9. Flyback Regulator Output Load Regulation, V_{OUT1} = 24 V, T_A = 25°C, Nominal = V_{OUT1} at 20 mA Load

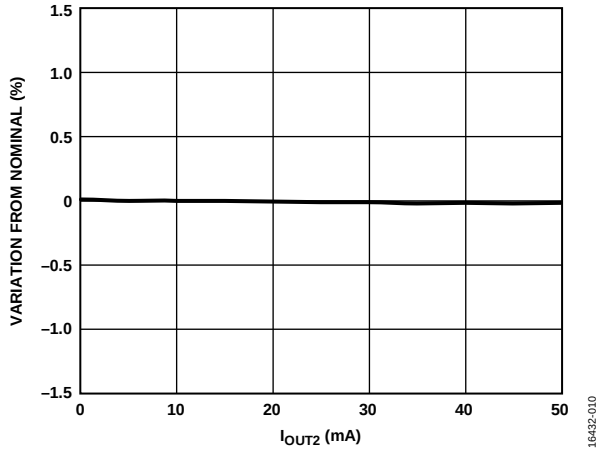

Figure 10. Buck Regulator Output Load Regulation, V_{OUT1} = 24 V, V_{OUT2} = 5.15 V, T_A = 25°C, Nominal = V_{OUT2} at 10 mA Load

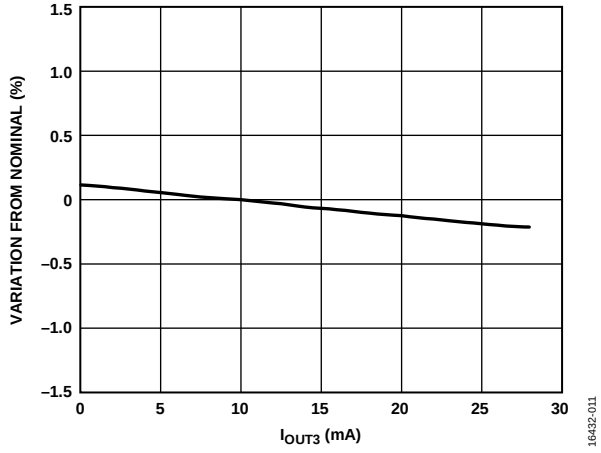

Figure 11. Inverting Regulator Output Load Regulation, V_{OUT1} = 24 V, V_{OUT3} = −15 V, T_A = 25°C, Nominal = V_{OUT3} at −7 mA Load

EFFICIENCY

For efficiency measurements, monitor the regulator input supply and output voltages while the load is varied. Keep power leads short during the efficiency measurement test and use a power supply with remote sense. Connect ammeters in series with the input supply and the loads. Connect voltmeters to the test points provided for the input and the outputs of the regulators. For the most accurate results, measure the voltage across the input and output capacitors. If possible, particularly at a low current, trigger the meters simultaneously and set the meters to perform average readings for a period of a few hundred milliseconds. Figure 12 shows the typical overall efficiency curve for the ADP1031 with a varying output load on the flyback regulator, and a constant load on the buck and the inverting regulators.

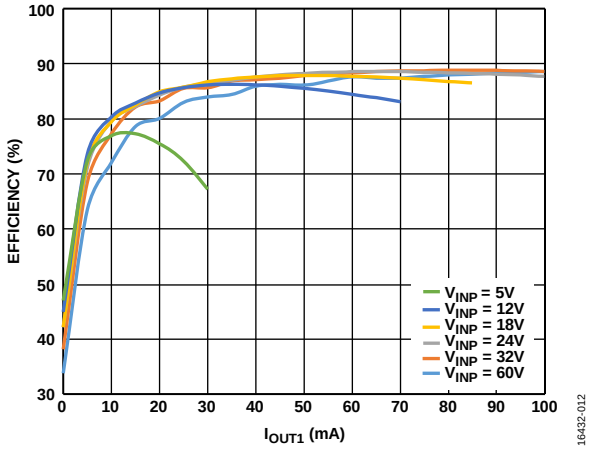

Figure 12. ADP1031 Overall Efficiency with Various Input Voltages, V_{OUT1} = 24 V, V_{OUT2} = 5.15 V, I_{OUT2} = 7 mA, V_{OUT3} = −15 V, I_{OUT3} = −0.3 mA, T_A = 25°C

EVALUATION BOARD SCHEMATICS AND ARTWORK

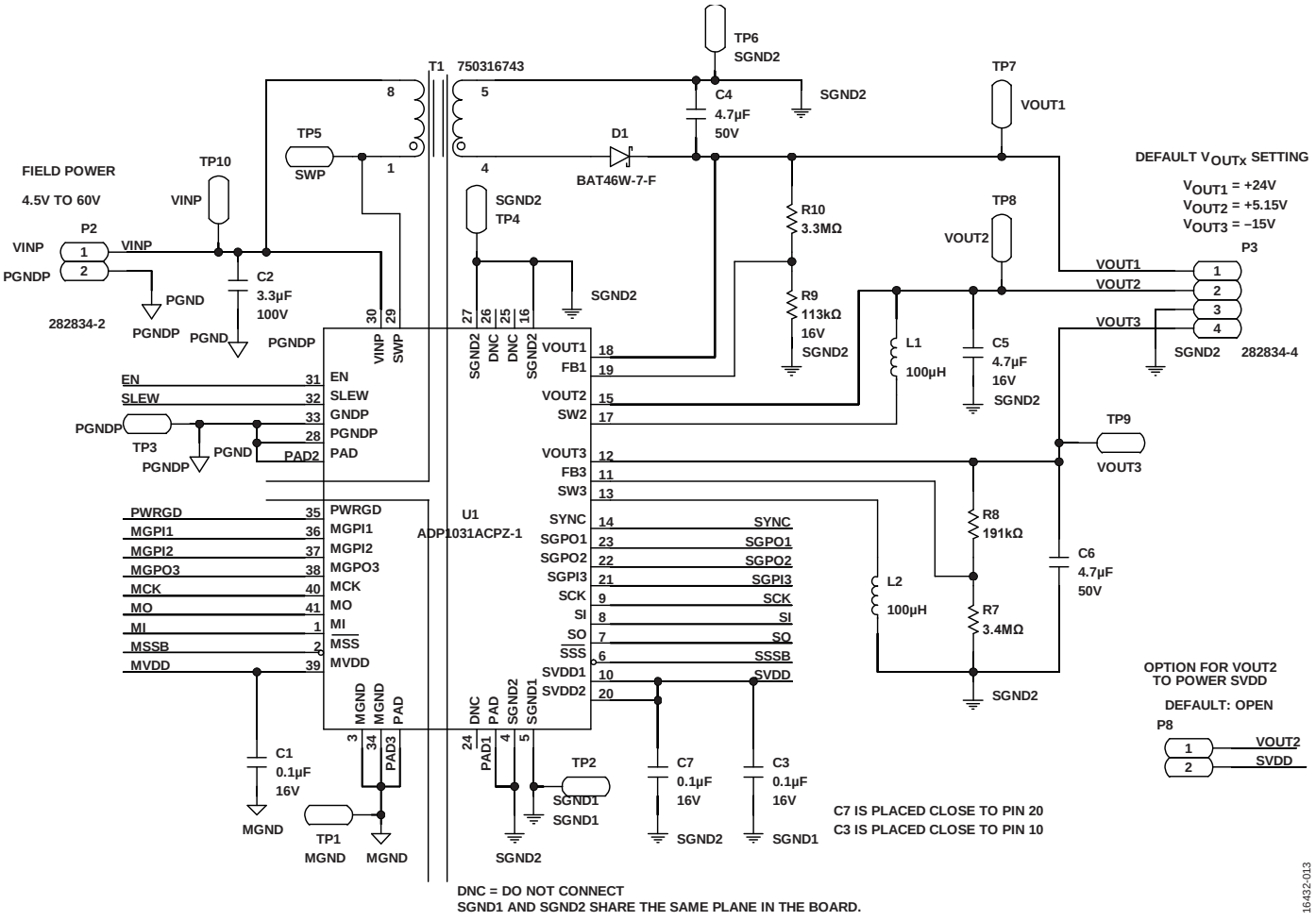

Figure 13. ADP1031CP-EVALZ Evaluation Board Schematic

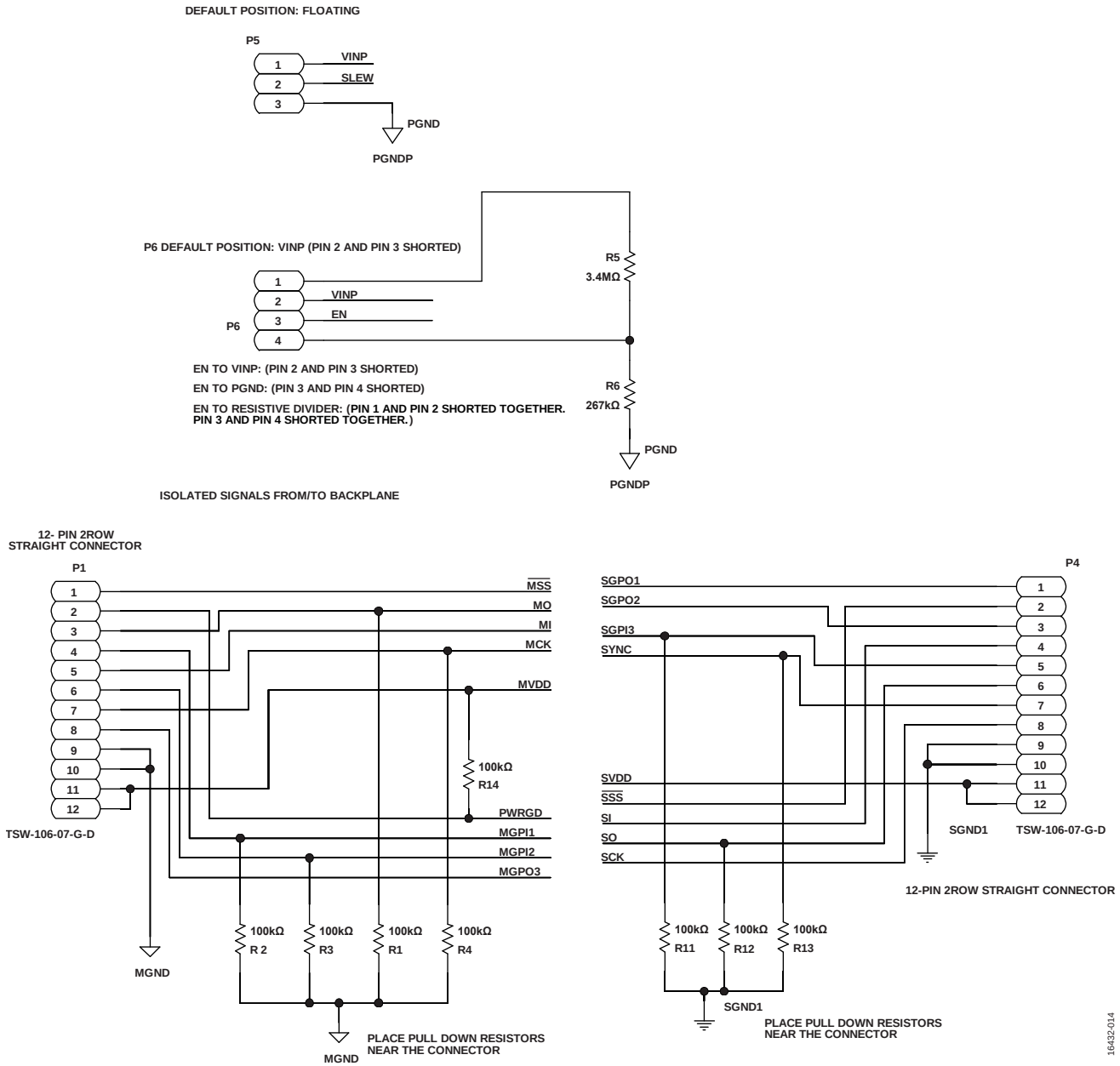

Figure 14. ADP1031CP-EVALZ Evaluation Board Schematic—Connectors and Peripherals

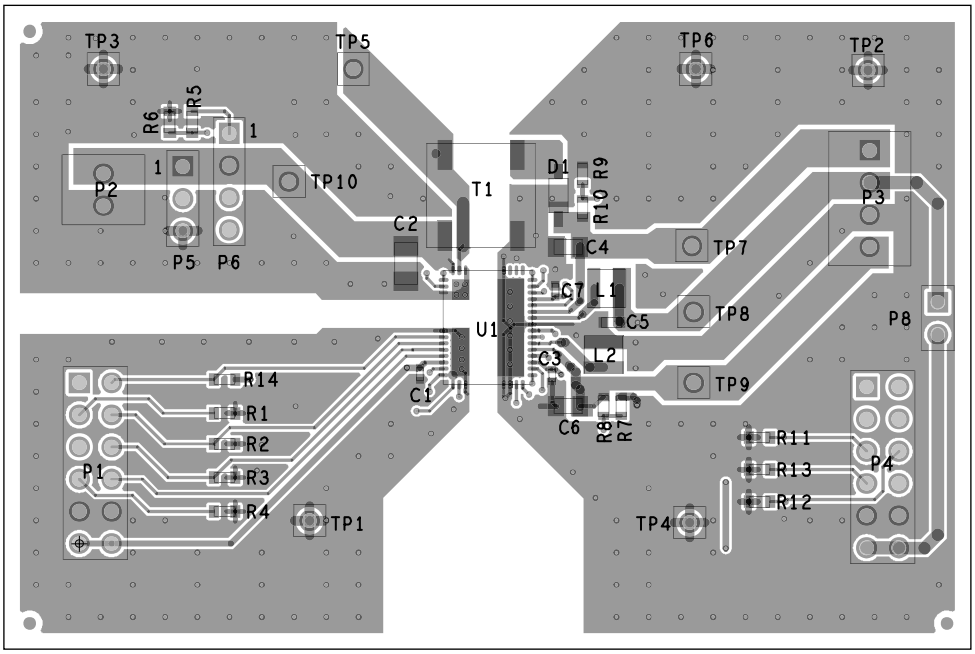

Figure 15. ADP1031CP-EVALZ Evaluation Board Top Layer

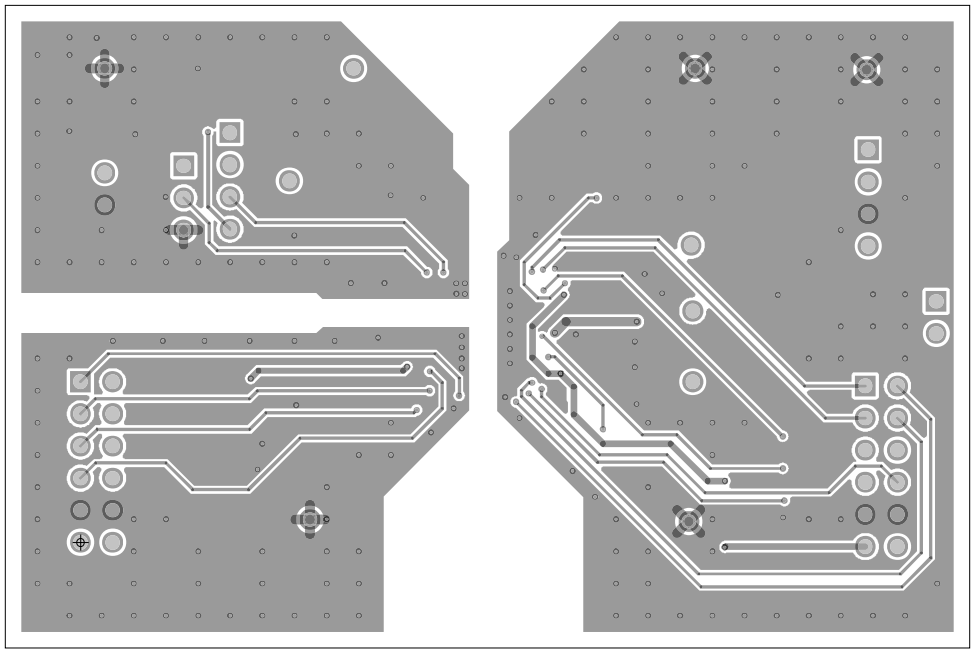

Figure 16. ADP1031CP-EVALZ Evaluation Board Bottom Layer

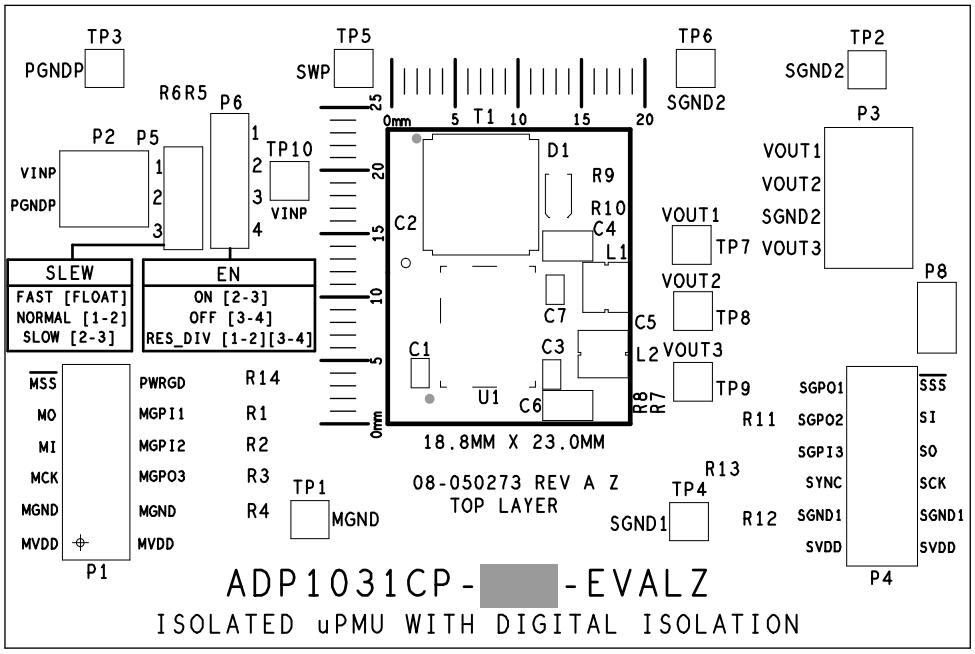

Figure 17. ADP1031CP-EVALZ Evaluation Board Silkscreen (Top)

ORDERING INFORMATION

BILL OF MATERIALS

Table 3. Bill of Materials

Quantity[1]	Reference Designator	Description	Manufacturer	Part Number
3	C1, C3, C7	Capacitors, MLCC, 0.1 µF, 16 V, 0402, X7R	Not applicable	Not applicable
1	C2	Capacitor, MLCC, 3.3 µF, 100 V, 1206, X7S	TDK Corporation	C3216X7S2A335K160AB
2	C4, C6	Capacitors, MLCC, 4.7 µF, 50 V, 0805, X7R	Murata	GRM21BZ71H475KE15L
1	C5	Capacitor, MLCC, 4.7 µF, 16 V, 0603, X7R	Murata	GRM188C81C475KE11D
1	D1	Diode, Schottky rectifier, surface-mount device (SMD)	Diodes Incorporated	BAT46W-7-F
2	L1, L2	Inductors, shielded,100 µH, 0.39 A	Coilcraft	XFL3012-104MEB
2	P1, P4	Headers, 12-pin	Samtec	TSW-106-07-G-D
1	P2	Terminal block, 2-pin	TE Connectivity	282834-2
1	P3	Terminal block, 4-pin	TE Connectivity	282834-4
1	P5	Header, 3-pin	Samtec	TSW-103-07-F-S
1	P6	Header, 4-pin	Samtec	TSW-104-07-G-S
10	TP1, TP2, TP3, TP4, TP5, TP6, TP7, TP8, TP9, TP10	Headers, 1-pin	Samtec	TSW-101-07-G-S
1	P8	Header, 2-pin	Samtec	TSW-101-07-G-D
8	R1, R2, R3, R4, R11, R12, R13, R14	Resistors, 100 kΩ, 1/10 W, 1%, 0603, SMD	Not applicable	Not applicable
2	R5, R7	Resistors, 3.4 MΩ, 1/10 W, 1%, 0603, SMD	Not applicable	Not applicable
1	R6	Resistor, 267 kΩ, 1/10 W, 1%, 0603, SMD	Not applicable	Not applicable
1	R8	Resistor, 191 kΩ, 1/10 W, 1%, 0603, SMD	Not applicable	Not applicable
1	R9	Resistor, 113 kΩ, 1/10 W, 1%, 0603, SMD	Not applicable	Not applicable
1	R10	Resistor, 3.3 MΩ, 1/10 W, 1%, 0603, SMD	Not applicable	Not applicable
1	T1	Transformer, 1:1 turn ratio, 300 µH, 350 mA	Wurth Elektronik	750316743
1	U1	3-channel isolated micropower management unit with 7-channel digital isolators	Analog Devices	ADP1031ACPZ-1, ADP1031ACPZ-2, ADP1031ACPZ-3, ADP1031ACPZ-4, ADP1031ACPZ-5

[1] R9 and R10 are not installed for the ADP1031CP-4 and ADP1031CP-5 board models.

NOTES

ESD Caution
ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

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