# FET Drive Simple Sequencers®

# ADM6819/ADM6820

## FEATURES

- **Single chip enables power supply sequencing of two supplies**
- **On-board charge pump fully enhances N-channel FET**
- **Adjustable primary supply monitor to 0.618 V**
- **Delay from primary supply to secondary supply enabled**
  - **Fixed 300 ms delay (ADM6819)**
  - **Capacitor adjustable delay (ADM6820)**
- **Logic/analog driven enable input (ADM6819)**
- **–40°C to +85°C operating range**
- **Packaged in small 6-lead SOT-23 package**
- **Pin-to-pin compatibility with MAX6819/MAX6820**

## APPLICATIONS

- **Multivoltage systems**
- **Dual voltage microprocessors/FPGAs/ASICs/DSPs**
- **Network processors**
- **Telecom and datacom systems**
- **PC/server applications**

## FUNCTIONAL BLOCK DIAGRAM

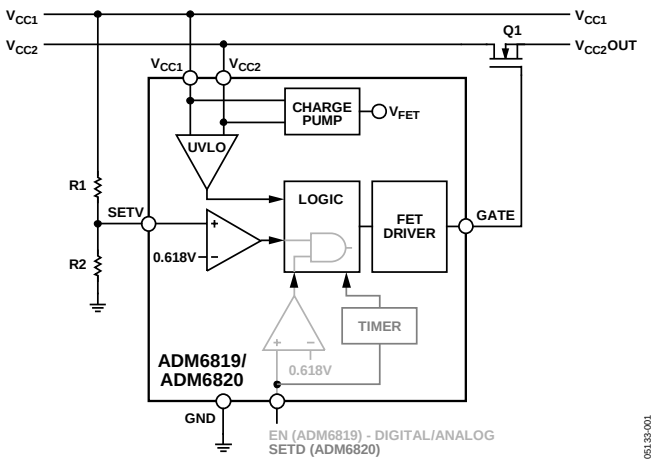



*Figure 1.*

## GENERAL DESCRIPTION

The ADM6819 and ADM6820 are simple power supply sequencers with FET drive capability for enhancing N-channel MOSFETs. These devices can monitor a primary supply voltage and enable/disable an external N-channel FET for a secondary supply. The ADM6819 has the ability to monitor two supplies. When more than two voltages require sequencing, multiple ADM6819/ADM6820 devices can be cascaded to achieve this. The devices operate over a supply range of 2.95 V to 5.5 V.

An internal comparator monitors the primary supply using the VSET pin. The input to this comparator is externally set via a resistor divider from the primary supply. When the voltage at the VSET pin rises above the comparator threshold, an internal charge pump on the GATE output enhances the secondary supply FET.

The ADM6819 features an enable (EN) pin that is fed to the input of an additional comparator and reference circuit. This pin can be used as a digital enable or a secondary power good comparator to monitor a second supply and enables the GATE only if both supplies are valid. When both inputs of the internal comparators are above the threshold, a fixed 300 ms timeout occurs before the GATE is driven high and the secondary supply is enabled.

The ADM6820 has only one comparator that is on the SETV pin. It also features a timeout period that is adjustable via a single external capacitor on the SETD pin.

The ADM6819/ADM6820 are packaged in small 6-lead SOT-23 packages.

**Rev. 0**


**One Technology Way, P.O. Box 9106, Norwood, MA 02062-9106, U.S.A.**
**Tel: 781.329.4700** **www.analog.com**
**Fax: 781.461.3113** 

# TABLE OF CONTENTS



## REVISION HISTORY

**7/06—Rev. 0: Initial Version**

# SPECIFICATIONS

$V_{CC1}$ or $V_{CC2}$ = 2.95 V to 5.5 V, $T_A$ = −40°C to +85°C, unless otherwise noted. Typical values are at $T_A$ = 25°C.[1]

**Table 1.**

| Parameter | Min | Typ | Max | Units | Conditions |
|---|---|---|---|---|---|
| $V_{CC1}$, $V_{CC2}$ PINS | | | | | $V_{CC1}$ or $V_{CC2}$ must be > 2.95 V |
| Operating Voltage Range, $V_{CC1}$ or $V_{CC2}$ | 0.9 | | 5.5 | V | $V_{CC1}$ or $V_{CC2}$ must be > 2.95 V |
| $V_{CC1}$ or $V_{CC2}$ Supply Current, $I_{CC}$ | | 350 | 500 | µA | $V_{CC1}$ = $V_{CC2}$ = 3.3 V |
| $V_{CC1}$ or $V_{CC2}$ Disable Mode Current | | 250 | | µA | $V_{CC1}$ = $V_{CC2}$ = 3.3 V, EN = GND |
| $V_{CC1}$ or $V_{CC2}$ Slew Rate[2] | 6 | | | V/s | ADM6819 |
| | $1.2/t_{DELAY}$ | | | V/s | ADM6820[3] |
| Undervoltage Lockout, $V_{UVLO}$ | 2.4 | 2.525 | 2.65 | V | $V_{CC}$ falling |
| SETV PIN | | | | | |
| SETV Threshold, $V_{TH}$ | 0.602 | 0.618 | 0.634 | V | $V_{SETV}$ rising, enables GATE |
| SETV Input Current[2] | | 10 | 100 | nA | |
| SETV Threshold Hysteresis | | −1 | | % | $V_{SETV}$ falling, disables GATE |
| SETV to GATE Delay, $t_{DELAY}$ | 240 | 300 | 350 | ms | $V_{SETV} > V_{TH}$; $V_{EN} > V_{TH}$ (ADM6819) |
| SETD PIN | | | | | ADM6820 |
| SETD Ramp Current, $I_{SETD}$ | 300 | 500 | 730 | nA | |
| | 400 | 500 | 600 | nA | $T_A$ = 25°C |
| SETD Voltage, $V_{SETD}$ | 1.295 | 1.326 | 1.357 | V | |
| GATE PIN | | | | | |
| GATE Turn-On Time, $t_{ON}$ | 0.5 | 1.5 | 10 | ms | $C_{GATE}$ = 1500 pF, $V_{CC2}$ = 3.3 V, $V_{GATE}$ = 7.8 V |
| GATE Turn-Off Time, $t_{OFF}$ | | 30 | | µs | $C_{GATE}$ = 1500 pF, $V_{CC2}$ = 3.3 V, $V_{GATE}$ = 0.5 V |
| GATE Voltage, $V_{GATE}$ | 4.5 | 5.5 | 6.0 | V | With respect to $V_{CCx}$, $R_{GATE}$ > 50 MΩ to $V_{CCx}$[4] |
| | 4.0 | 5.0 | 6 | V | With respect to $V_{CCx}$, $R_{GATE}$ > 5 MΩ to $V_{CCx}$[4] |
| | 8.9 | 9.4 | 9.9 | V | With respect to $V_{CCx}$, $R_{GATE}$ > 50 MΩ to $V_{CCx}$[5] |
| | 8.2 | 8.6 | 9.1 | V | With respect to $V_{CCx}$, $R_{GATE}$ > 5 MΩ to $V_{CCx}$[5] |
| ENABLE PIN | | | | | |
| EN Input Voltage Low, $V_{IL}$ | | | 0.4 | V | $V_{CC1}$ or $V_{CC2}$ must be > 2.95 V |
| EN Input Voltage High, $V_{IH}$ | 2.0 | | | V | $V_{CC1}$ or $V_{CC2}$ must be > 2.95 V |

[1] 100% production tested at $T_A$ = +25°C. Specifications over temperature limit are guaranteed by design.
[2] Guaranteed by design, not production tested.
[3] $t_{DELAY}$ (s) = $2.65 \times 10^6 \times C_{SET}$.
[4] Highest supply pin is represented by $V_{CCx}$ = 2.95 V.
[5] Highest supply pin is represented by $V_{CCx}$ = 5.5 V.

# TIMING DIAGRAMS

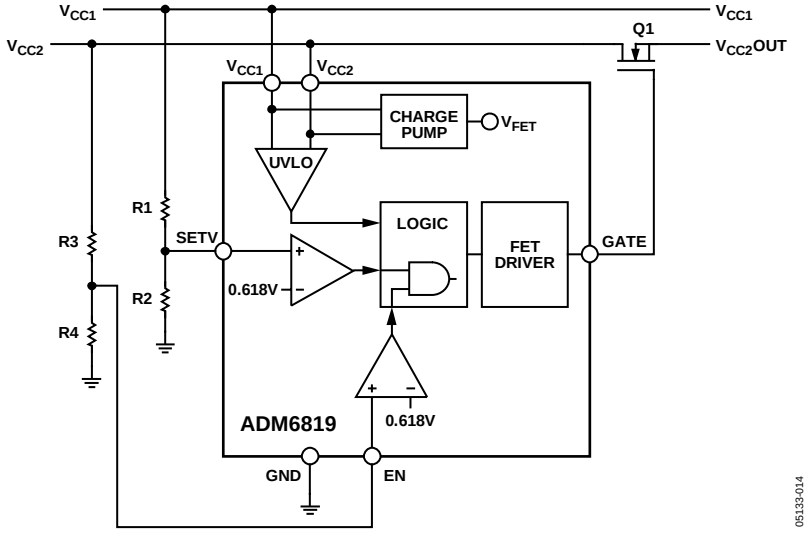



*Figure 2. ADM6819 Solution for Validating Two Supplies Before Sequencing*

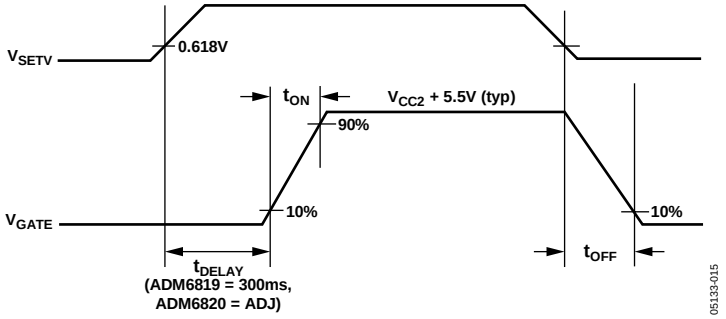



*Figure 3. ADM6819/ADM6820 Timing Diagram Using SETV for Sequencing*

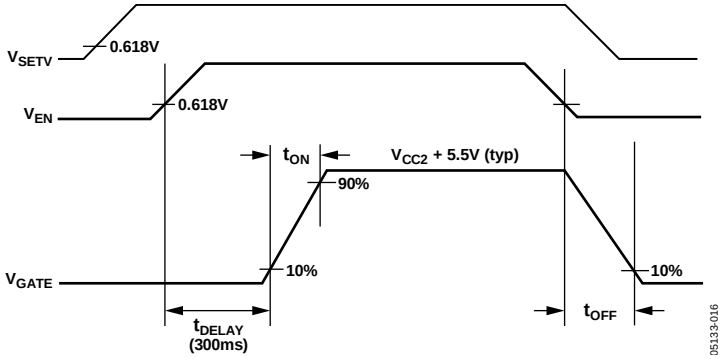



*Figure 4. ADM6819 Timing Diagram Using EN and SETV for Sequencing*

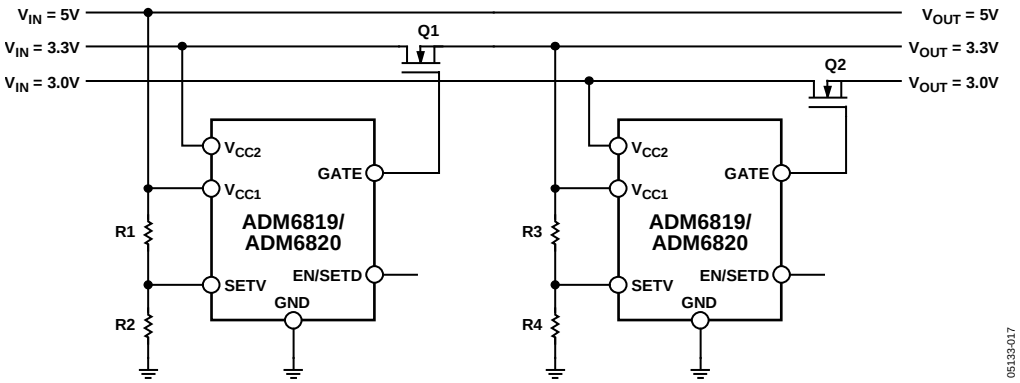



*Figure 5. ADM6819/ADM6820 Solution for Sequencing Three Supply Rails*

# ABSOLUTE MAXIMUM RATINGS

**Table 2.**

| Parameter | Rating |
|---|---|
| $V_{CC1}$, $V_{CC2}$ | −0.3 V to +6.0 V |
| SETV, SETD, EN | −0.3 V to +30 V |
| GATE | −0.3 V to ($V_{CCx}$ + 11 V) |
| Storage Temperature | −65°C to +150°C |
| Operating Temperature Range | −40°C to +85°C |
| Lead Temperature (Soldering 10 sec) | 300°C |
| Junction Temperature | 150°C |

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

## THERMAL CHARACTERISTICS

$\theta_{JA}$ is specified for the worst-case conditions, that is, a device soldered in a circuit board for surface-mount packages.

**Table 3. Thermal Resistance**

| Package Type | $\theta_{JA}$ | Unit |
|---|---|---|
| 6-Lead SOT-23 | 169.5 | °C/W |

## ESD CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although this product features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.

# PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

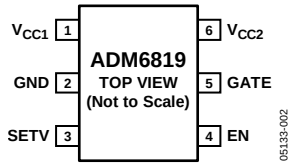



*Figure 6. ADM6819 Pin Configuration*

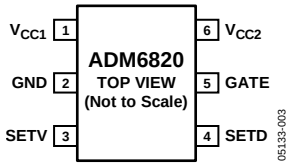



*Figure 7. ADM6820 Pin Configuration*

**Table 4. Pin Function Descriptions**

| Pin Number | | | |
|---|---|---|---|
| **ADM6819** | **ADM6820** | **Mnemonic** | **Description** |
| 1 | 1 | $V_{CC1}$ | Supply Voltage 1. Either $V_{CC1}$ or $V_{CC2}$ must be greater than the UVLO to enable external FET Drive. |
| 2 | 2 | GND | Chip Ground Pin. |
| 3 | 3 | SETV | Sequenced Threshold Set. Connect to an external resistor divider to set the $V_{CC1}$ threshold that enables GATE turn-on. The internal reference is 0.618 V. |
| 4 | – | EN | Active-High Enable. GATE drive is enabled $t_{DELAY}$ after EN is driven high. GATE drive is immediately disabled when EN is driven low. Connect this pin to the higher of $V_{CC1}$ or $V_{CC2}$ if not used. EN is internally identical to SETV (0.618 V threshold) and, therefore, can be used as a second supply monitor, enabling two supplies to be validated before sequencing begins. |
| – | 4 | SETD | GATE Delay Set Input. Connect an external capacitor from SETD to GND to adjust the delay from SETV > $V_{TH}$ to GATE turn-on. $t_{DELAY}(s) = 2.652 \times 10^6 \times C_{SET}(F)$. |
| 5 | 5 | GATE | GATE Drive Output. GATE drives an external N-channel FET to connect $V_{CC2}$ to the load. GATE drive enables $t_{DELAY}$ after SETV exceeds $V_{TH}$ and ENABLE is driven high. GATE drive is immediately disabled when SETV drops below $V_{TH}$ or ENABLE is driven low. When enabled, an internal charge pump drives GATE above $V_{CCX}$ to fully enhance the external N-channel FET. |
| 6 | 6 | $V_{CC2}$ | Supply Voltage 2. Either $V_{CC1}$ or $V_{CC2}$ must be greater than the UVLO to enable the external FET Drive. |

# TYPICAL PERFORMANCE CHARACTERISTICS

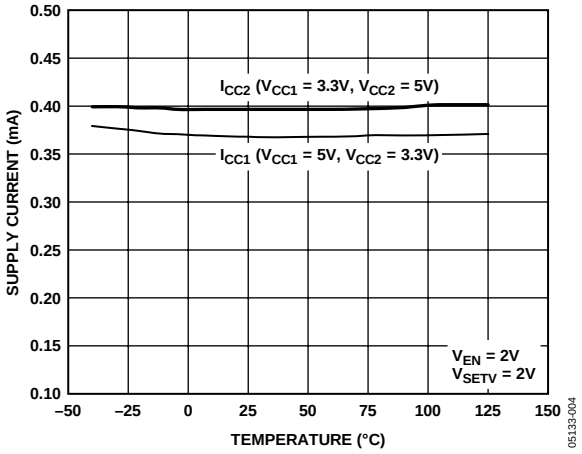



Figure 8. Supply Current vs. Temperature

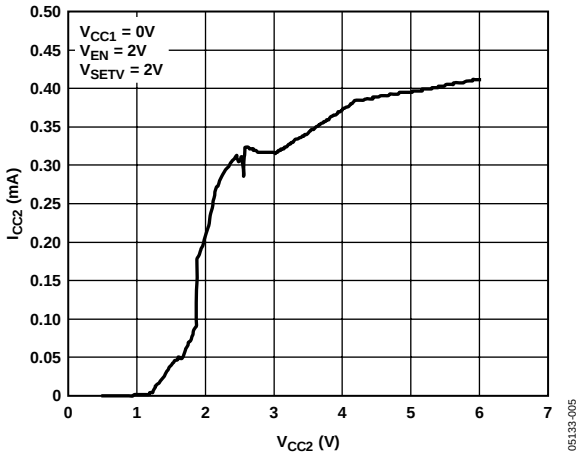



Figure 9. $I_{CC2}$ vs. $V_{CC2}$

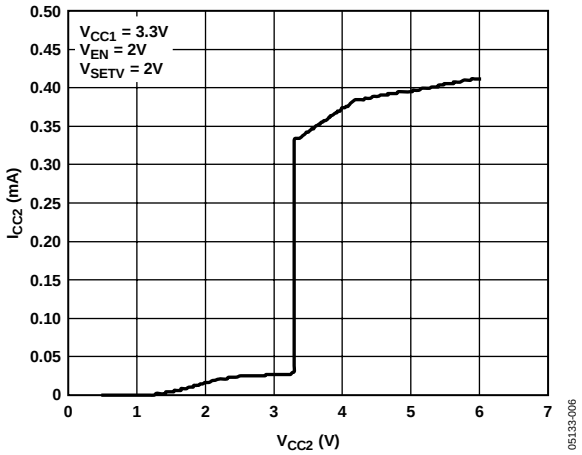



Figure 10. $I_{CC2}$ vs. $V_{CC2}$

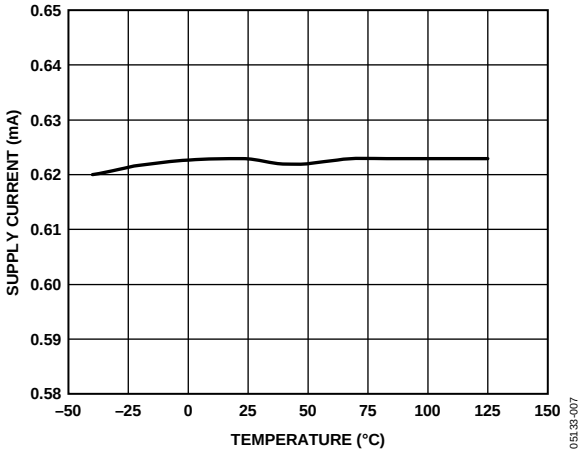



Figure 11. Supply Current vs. Temperature

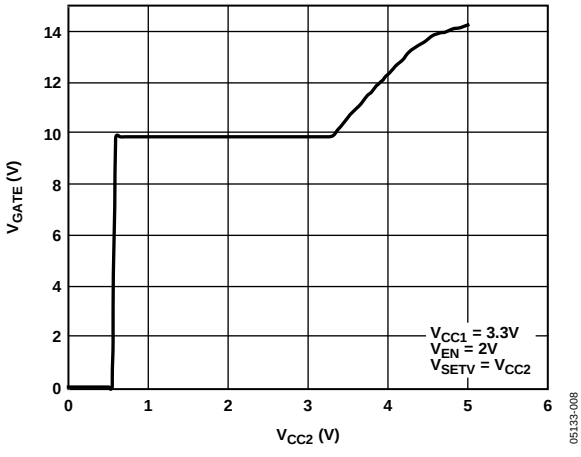



Figure 12. $V_{GATE}$ vs. $V_{CC2}$

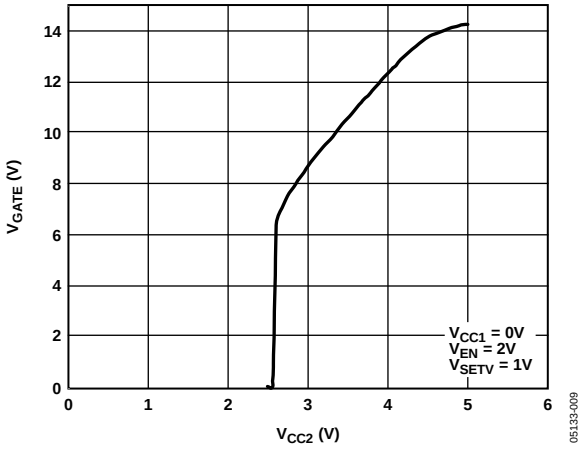



Figure 13. $V_{GATE}$ vs. $V_{CC2}$

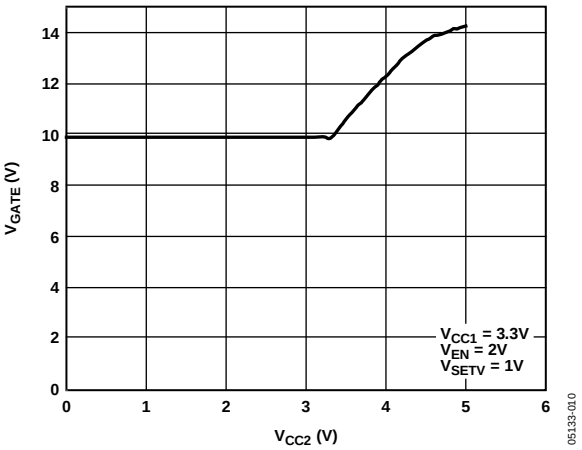



*Figure 14. $V_{GATE}$ vs. $V_{CC2}$*

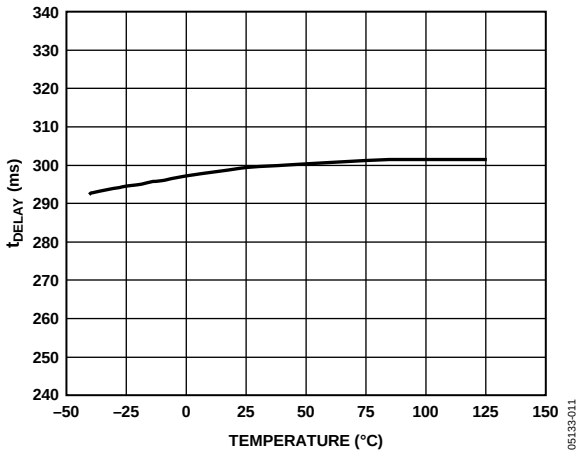



*Figure 15. $t_{DELAY}$ vs. Temperature*

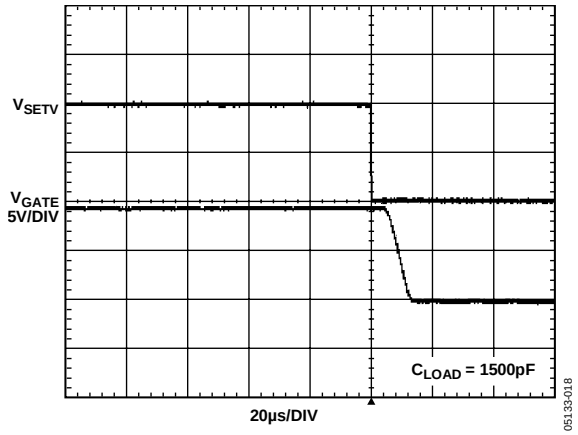



*Figure 16. Gate Turn-Off Time*

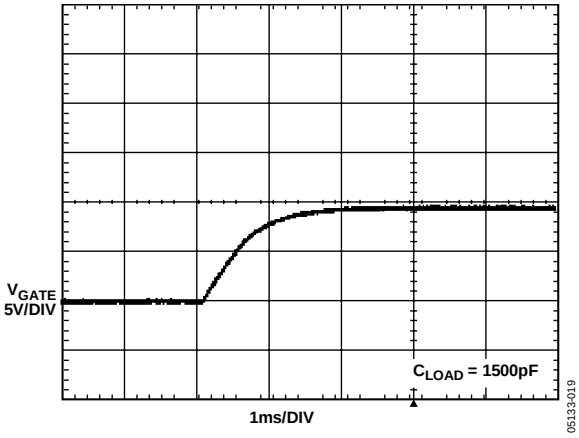



*Figure 17. Gate Turn-On Time*

# THEORY OF OPERATION

The ADM6819/ADM6820 provide local voltage sequencing in multisupply systems. Figure 18 and Figure 19 show typical application diagrams for these devices.

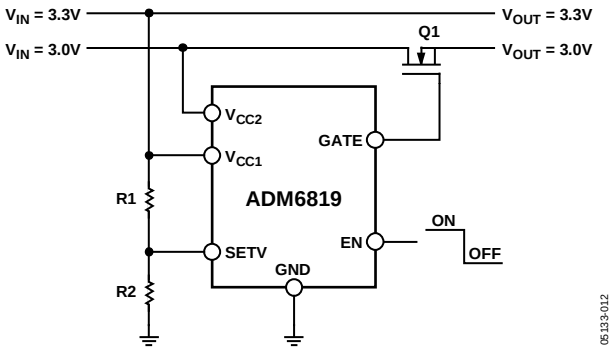



*Figure 18. ADM6819 Applications Diagram*

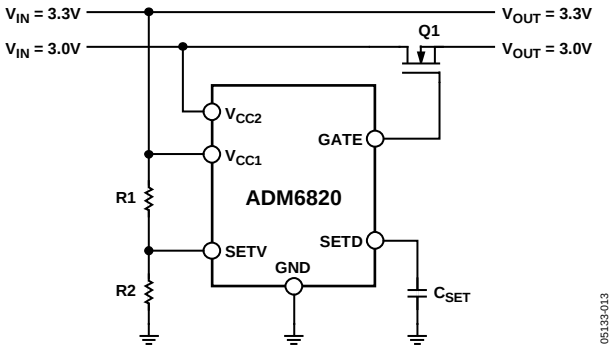



*Figure 19. ADM6820 Applications Diagram*

When the primary supply is above the desired threshold, the ADM6819/ADM6820 are designed to control the N-channel FET in the secondary power path to enable the secondary supply. The GATE pin is held low while both $V_{CC1}$ and $V_{CC2}$ are below the undervoltage threshold, ensuring that the FET is held off. When $V_{CC1}$ or $V_{CC2}$ is above UVLO and the primary supply is above the desired level dictated by the resistor divider to the VSET pin, the external FET is driven on after the delay has expired. An internal charge pump enhances the external FET. A FET with a low drain-source resistance and low $V_{TH}$ should be chosen to reduce voltage drop across the drain-source when the FET is fully enhanced. Either supply may act as the primary source if $V_{CC1}$ or $V_{CC2}$ is greater that 2.95 V. A decoupling capacitor of typically 100 nF should be used on whichever $V_{CC}$ is the main supply.

## SETV PIN

The ADM6819/ADM6820 enable a supply after a monitored supply voltage exceeds a programmed threshold. This threshold is programmed by a R1/R2 resistor divider on the SETV pin. Once the voltage on SETV exceeds the 0.618 V threshold, the FET switches on after the delay timer expires. On the ADM6820, this delay is programmable using a capacitor on the SETD pin. On the ADM6819, this delay is fixed at 300 ms and the EN pin must be valid high to begin the timer. The required turn-on voltage is calculated by the following equation:

$$R1 = R2\ ((VTRIP/V_{TH}) - 1)$$

where:
*VTRIP* is the minimum turn-on voltage at the supply being monitored.
$V_{TH}$ = 0.618 V.
High value resistors can be used because the SETV input current is typically 10 nA.

## EN PIN

The ADM6819 has an enable (EN) pin connected to the input of a second comparator, which is identical to that on the VSET pin. EN can be used as a digital input provided the signal $V_{OL}$ is below 0.6 V. Alternatively, the enable input can be used to validate a second supply. The fixed 300 ms timer does not begin counting until both SETV and EN are above the threshold. As a result, the output is not enabled until this timer has expired.

## GATE PIN

The internal charge pump is capable of driving the gate of an N-channel MOSFET with no external capacitors. This ensures that the MOSFET is enhanced to provide a minimum voltage drop across the MOSFET, thus reducing the voltage drop across the FET. This charge pump is designed to drive the high impedance capacitive load of a MOSFET gate input. The GATE pin should not be resistively loaded because it reduces the gate drive capability. During undervoltage lockout, GATE is held to GND.

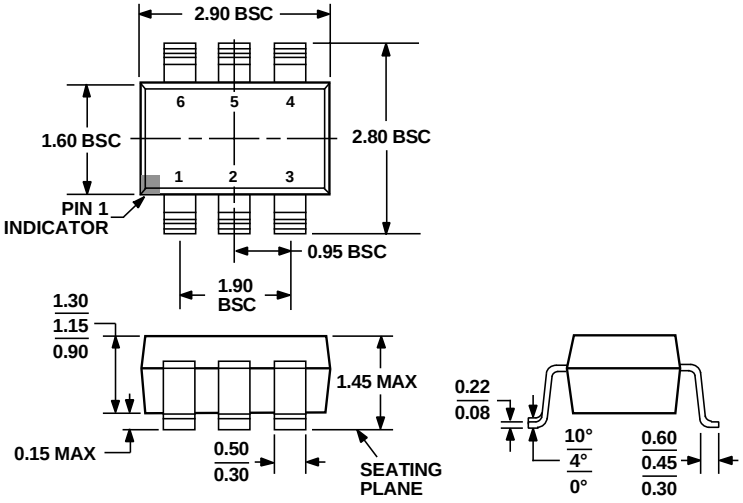
## SETD PIN

The ADM6820 features a capacitor adjustable sequencing delay. A capacitor connected to the SETD pin determines the length of the sequencing delay. The sequencing delay can be calculated by the following equation:

$$t_{DELAY}\ (\text{s}) = 2.652 \times 10^6 \times CSET$$

The ADM6819 has a fixed 300 ms delay.

# OUTLINE DIMENSIONS




**COMPLIANT TO JEDEC STANDARDS MO-178-AB**

*Figure 20. 6-Lead Small Outline Transistor Package [SOT-23]*
*(RJ-6)*
*Dimensions shown in millimeters*

## ORDERING GUIDE

| Model | Temperature Range | Package Description | Package Option | Branding |
|---|---|---|---|---|
| ADM6819ARJZ-REEL7[1] | −40°C to +85°C | 6-Lead Small Outline Transistor Package [SOT-23] | RJ-6 | M2R |
| ADM6820ARJZ-REEL7[1] | −40°C to +85°C | 6-Lead Small Outline Transistor Package [SOT-23] | RJ-6 | M2S |

[1] Z = Pb-free part.

## NOTES


D05113-0-7/06(0)

# Mouser Electronics

Authorized Distributor

Click to View Pricing, Inventory, Delivery & Lifecycle Information:

Analog Devices Inc.:

ADM6819ARJZ-REEL7 ADM6820ARJZ-REEL7