450 MHz to 6000 MHz TruPwr Detector

ADL5505

FEATURES

- True rms response detector
- Excellent temperature stability
- ±0.25 dB rms detection accuracy vs. temperature
- Over 35 dB input power dynamic range, inclusive of crest factor
- RF bandwidths from 450 MHz to 6000 MHz
- 500 Ω input impedance
- Single-supply operation: 2.5 V to 3.3 V
- Low power: 1.8 mA at 3.0 V supply
- RoHS-compliant part

APPLICATIONS

- Power measurement of W-CDMA, CDMA2000, QPSK-/QAM-based OFDM (LTE and WiMAX), and other complex modulation waveforms
- RF transmitter or receiver power measurement

FUNCTIONAL BLOCK DIAGRAM

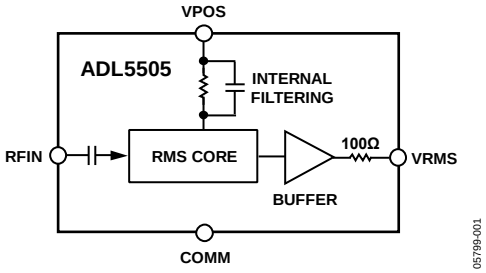

Figure 1.

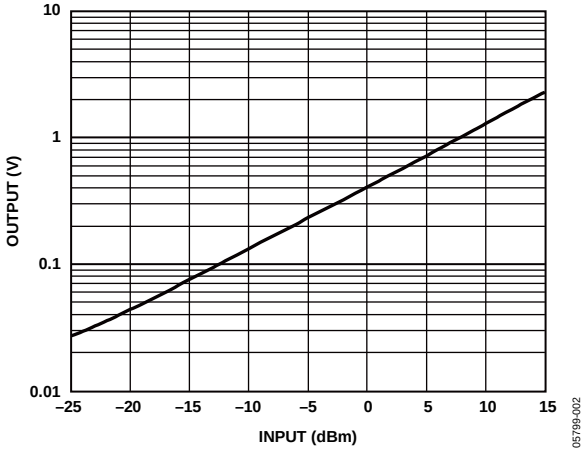

Figure 2. Output vs. Input Level, Supply = 3.0 V, Frequency = 1900 MHz

GENERAL DESCRIPTION

The ADL5505 is a TruPwr™ mean-responding (true rms) power detector for use in high frequency receiver and transmitter signal chains from 450 MHz to 6000 MHz. Requiring only a single supply between 2.5 V and 3.3 V, the detector draws less than 1.8 mA. The input is internally ac-coupled and has a nominal input impedance of 500 Ω. The rms output is a linear-responding dc voltage with a conversion gain of 1.86 V/V rms at 900 MHz.

The ADL5505 is a highly accurate, easy to use means of determining the rms of complex waveforms. It can be used for power measurements of both simple and complex waveforms but is particularly useful for measuring high crest factor (high peak-to-rms ratio) signals, such as W-CDMA, CDMA2000, WiMAX, WLAN, and LTE waveforms.

The on-chip modulation filter provides adequate averaging for most waveforms. An on-chip, 100 Ω series resistance at the output, combined with an external shunt capacitor, creates a low-pass filter response that reduces the residual ripple in the dc output voltage.

The ADL5505 offers excellent temperature stability across a 30 dB range and near 0 dB measurement error across temperature over the top portion of the dynamic range. In addition to its temperature stability, the ADL5505 offers low process variations that further reduce calibration complexity.

The power detector operates from −40°C to +85°C and is available in an 4-ball, 0.8 mm × 0.8 mm wafer-level chip scale package. It is fabricated on a high f_T silicon BiCMOS process.

Rev. A

One Technology Way, P.O. Box 9106, Norwood, MA 02062-9106, U.S.A.
Tel: 781.329.4700 **www.analog.com**
Fax: 781.461.3113

TABLE OF CONTENTS

REVISION HISTORY

1/11—Rev. 0 to Rev. A

Updated Outline Dimensions, Figure 46 ... 20
Change to Ordering Guide, Package Option ... 20

4/10—Revision 0: Initial Version

SPECIFICATIONS

T_A = 25°C, V_S = 3.0 V, C_{OUT} = open, light condition ≤ 600 lux, 75 Ω input termination resistor, unless otherwise noted.

Table 1.

Parameter	Test Conditions	Min	Typ	Max	Unit
FREQUENCY RANGE	Input RFIN	450		6000	MHz
RF INPUT (f = 450 MHz)	Input RFIN to output VRMS				
Input Impedance	No termination		510||1.01		Ω||pF
RMS Conversion					
Dynamic Range[1]	Continuous wave (CW) input, −40°C < T_A < +85°C				
±0.25 dB Error[2]	Delta from 25°C		25		dB
±0.25 dB Error[3]			16		dB
±1 dB Error[3]			36		dB
±2 dB Error[3]			40		dB
Maximum Input Level	±0.25 dB error[3]		15		dBm
Minimum Input Level	±1 dB error[3]		−22		dBm
Conversion Gain	VRMS = (gain × V_{IN}) + intercept		1.88		V/V rms
Output Intercept[4]			0.008		V
Output Voltage, High Input Power	P_{IN} = 5 dBm, 400 mV rms		0.755		V
Output Voltage, Low Input Power	P_{IN} = −15 dBm, 40 mV rms		0.082		V
Temperature Sensitivity	P_{IN} = 0 dBm				
	+25°C < T_A < +85°C		0.0027		dB/°C
	−40°C < T_A < +25°C		0.0024		dB/°C
RF INPUT (f = 900 MHz)	Input RFIN to output VRMS				
Input Impedance	No termination		370||0.80		Ω||pF
RMS Conversion					
Dynamic Range[1]	Continuous wave (CW) input, −40°C < T_A < +85°C				
±0.25 dB Error[2]	Delta from 25°C		26		dB
±0.25 dB Error[3]			17		dB
±1 dB Error[3]			36		dB
±2 dB Error[3]			40		dB
Maximum Input Level	±0.25 dB error[3]		15		dBm
Minimum Input Level	±1 dB error[3]		−23		dBm
Conversion Gain	VRMS = (gain × V_{IN}) + intercept	1.6	1.86	2.2	V/V rms
Output Intercept[4]		−0.1	+0.009	+0.1	V
Output Voltage, High Input Power	P_{IN} = 5 dBm, 400 mV rms		0.748		V
Output Voltage, Low Input Power	P_{IN} = −15 dBm, 40 mV rms		0.083		V
Temperature Sensitivity	P_{IN} = 0 dBm				
	+25°C < T_A < +85°C		0.0026		dB/°C
	−40°C < T_A < +25°C		0.0024		dB/°C

Parameter	Test Conditions	Min	Typ	Max	Unit
RF INPUT (f = 1900 MHz)	Input RFIN to output VRMS				
Input Impedance	No termination		270||0.67		Ω||pF
RMS Conversion					
Dynamic Range[1]	Continuous wave (CW) input, −40°C < T_A < +85°C				
±0.25 dB Error[2]	Delta from 25°C		21		dB
±0.25 dB Error[3]			16		dB
±1 dB Error[3]			36		dB
±2 dB Error[3]			40		dB
Maximum Input Level	±0.25 dB error[3]		15		dBm
Minimum Input Level	±1 dB error[3]		−22		dBm
Conversion Gain	VRMS = (gain × V_{IN}) + intercept		1.82		V/V rms
Output Intercept[4]			0.007		V
Output Voltage, High Input Power	P_{IN} = 5 dBm, 400 mV rms		0.727		V
Output Voltage, Low Input Power	P_{IN} = −15 dBm, 40 mV rms		0.079		V
Temperature Sensitivity	P_{IN} = 0 dBm				
	+25°C < T_A < +85°C		0.0017		dB/°C
	−40°C < T_A < +25°C		−0.0026		dB/°C
RF INPUT (f = 2600 MHz)	Input RFIN to output VRMS				
Input Impedance	No termination		240||0.58		Ω||pF
RMS Conversion					
Dynamic Range[1]	Continuous wave (CW) input, −40°C < T_A < +85°C				
±0.25 dB Error[2]	Delta from 25°C		14		dB
±0.25 dB Error[3]			11		dB
±1 dB Error[3]			35		dB
±2 dB Error[3]			40		dB
Maximum Input Level	±0.25 dB error[3]		15		dBm
Minimum Input Level	±1 dB error[3]		−22		dBm
Conversion Gain	VRMS = (gain × V_{IN}) + intercept		1.77		V/V rms
Output Intercept[4]			0.005		V
Output Voltage, High Input Power	P_{IN} = 5 dBm, 400 mV rms		0.700		V
Output Voltage, Low Input Power	P_{IN} = −15 dBm, 40 mV rms		0.075		V
Temperature Sensitivity	P_{IN} = 0 dBm				
	+25°C < T_A < +85°C		0.0016		dB/°C
	−40°C < T_A < +25°C		0.0042		dB/°C
RF INPUT (f = 3500 MHz)	Input RFIN to output VRMS				
Input Impedance	No termination		210||0.48		Ω||pF
RMS Conversion					
Dynamic Range[1]	Continuous wave (CW) input, −40°C < T_A < +85°C				
±0.25 dB Error[2]	Delta from 25°C		5		dB
±0.25 dB Error[3]			5		dB
±1 dB Error[3]			33		dB
±2 dB Error[3]			39		dB
Maximum Input Level	±0.25 dB error[3]		13		dBm
Minimum Input Level	±1 dB error[3]		−21		dBm
Conversion Gain	VRMS = (gain × V_{IN}) + intercept		1.61		V/V rms
Output Intercept[4]			0.001		V
Output Voltage, High Input Power	P_{IN} = 5 dBm, 400 mV rms		0.630		V
Output Voltage, Low Input Power	P_{IN} = −15 dBm, 40 mV rms		0.065		V
Temperature Sensitivity	P_{IN} = 0 dBm				
	+25°C < T_A < +85°C		0.0046		dB/°C
	−40°C < T_A < +25°C		0.0085		dB/°C

Parameter	Test Conditions	Min	Typ	Max	Unit
RF INPUT (f = 6000 MHz)	Input RFIN to output VRMS				
Input Impedance	No termination		80||0.42		Ω||pF
RMS Conversion					
Dynamic Range[1]	Continuous wave (CW) input, −40°C < T_A < +85°C				
±1 dB Error[3]			23		dB
±2 dB Error[3]			33		dB
Maximum Input Level	±0.25 dB error[3]		11		dBm
Minimum Input Level	±1 dB error[3]		−17		dBm
Conversion Gain	VRMS = (gain × V_{IN}) + intercept		0.77		V/V rms
Output Intercept[4]			0.002		V
Output Voltage, High Input Power	P_{IN} = 5 dBm, 400 mV rms		0.298		V
Output Voltage, Low Input Power	P_{IN} = −15 dBm, 40 mV rms		0.032		V
Temperature Sensitivity	P_{IN} = 0 dBm				
	+25°C < T_A < +85°C		0.0103		dB/°C
	−40°C < T_A < +25°C		0.0138		dB/°C
VRMS OUTPUT	Pin VRMS				
Output Offset	No signal at RFIN		10	100	mV
Maximum Output Voltage	V_S = 3.0 V, R_{LOAD} ≥ 10 kΩ		2.5		V
Available Output Current			3		mA
Pulse Response Time	C_{OUT} = open, 10 dB step, 10% to 90% of settling level		3		µs
Power-Up Response Time[5]	C_{OUT} = open, 0 dBm at RFIN		3		µs
POWER SUPPLIES					
Operating Range	−40°C < T_A < +85°C	2.5		3.3	V
Quiescent Current[6]	No signal at RFIN		1.8		mA

[1] The available output swing and, therefore, the dynamic range are altered by the supply voltage; see Figure 8.
[2] Error referred to delta from 25°C response; see Figure 13, Figure 14, Figure 15, Figure 19, Figure 20, and Figure 21.
[3] Error referred to best-fit line at 25°C; see Figure 10, Figure 11, Figure 12, Figure 16, Figure 17, and Figure 18.
[4] Calculated using linear regression.
[5] The response time is measured from 10% to 90% of settling level; see Figure 30 and Figure 31.
[6] Supply current is input level-dependent; see Figure 27.

ABSOLUTE MAXIMUM RATINGS

Table 2.

Parameter	Rating
Supply Voltage, V_S	3.5 V
VRMS	0 V to V_S
RFIN	1.25 V rms
Equivalent Power, Referred to 50 Ω	15 dBm
Internal Power Dissipation	150 mW
θ_{JA} (WLCSP)	260°C/W
Maximum Junction Temperature	125°C
Operating Temperature Range	−40°C to +85°C
Storage Temperature Range	−65°C to +150°C

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

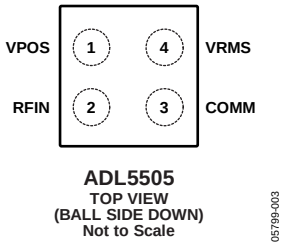

Figure 3. Pin Configuration

Table 3. Pin Function Descriptions

Pin No.	Mnemonic	Description
1	VPOS	Supply Voltage. The operational range is 2.5 V to 3.3 V.
2	RFIN	Signal Input. This pin is internally ac-coupled after internal termination resistance. The nominal input impedance is 500
3	COMM	Device Ground.
4	VRMS	RMS Output. This pin is a rail-to-rail voltage output with limited current drive capability. The output has an internal 100 Ω series resistance. High resistive loads and low capacitance loads are recommended to preserve output swing and allow fast response.

TYPICAL PERFORMANCE CHARACTERISTICS

T_A = 25°C; V_S = 3.0 V; C_{OUT} = open; light condition ≤ 600 lux; 75 Ω input termination resistor; colors: black = +25°C, blue = −40°C, red = +85°C; unless otherwise noted.

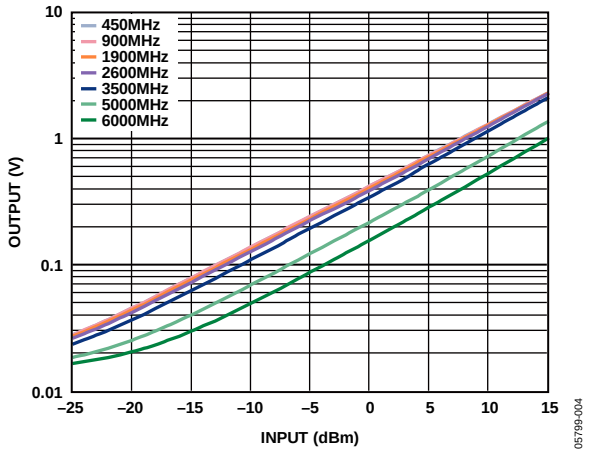

Figure 4. Output vs. Input Level; Frequencies = 450 MHz, 900 MHz, 1900 MHz, 2600 MHz, 3500 MHz, 5000 MHz, 6000 MHz; Supply = 3.0 V

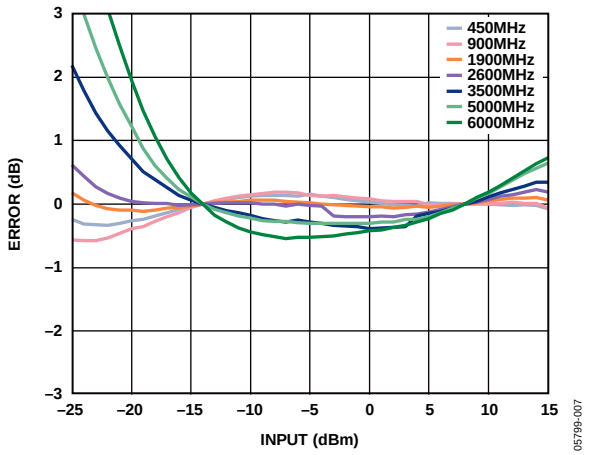

Figure 7. Linearity Error vs. Input Level; Frequencies = 450 MHz, 900 MHz, 1900 MHz, 2600 MHz, 3500 MHz, 5000 MHz, 6000 MHz; Supply = 3.0 V

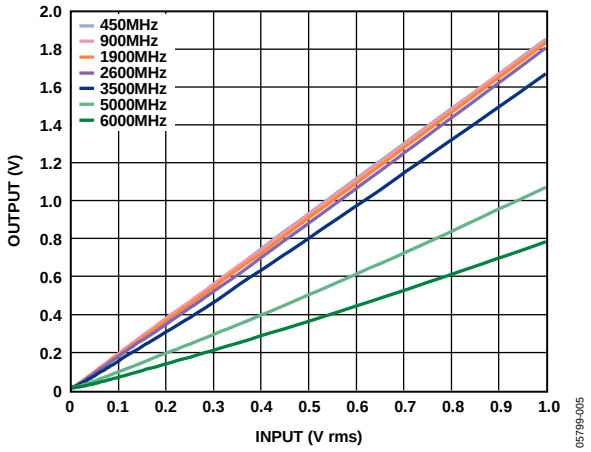

Figure 5. Output vs. Input Level (Linear Scale); Frequencies = 450 MHz, 900 MHz, 1900 MHz, 2600 MHz, 3500 MHz, 5000 MHz, 6000 MHz; Supply = 3.0 V

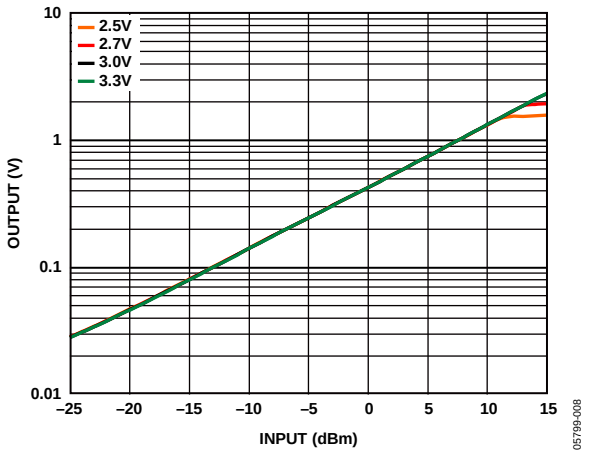

Figure 8. Output vs. Input Level; Supplies = 2.5 V, 2.7 V, 3.0 V, and 3.3 V; Frequency = 900 MHz

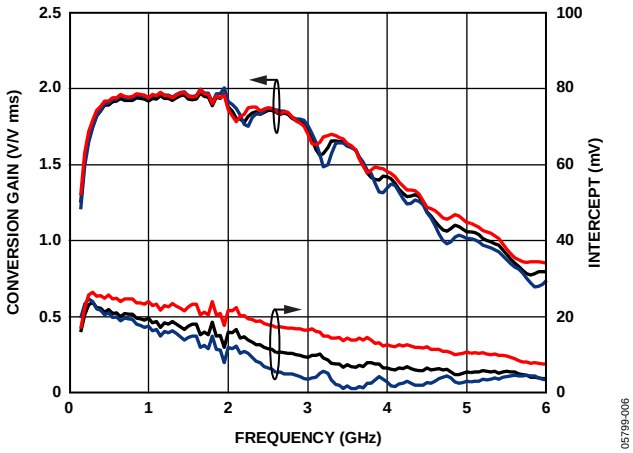

Figure 6. Conversion Gain and Intercept vs. Frequency; Supply = 3.0 V; Temperatures = −40°C, +25°C, and +85°C

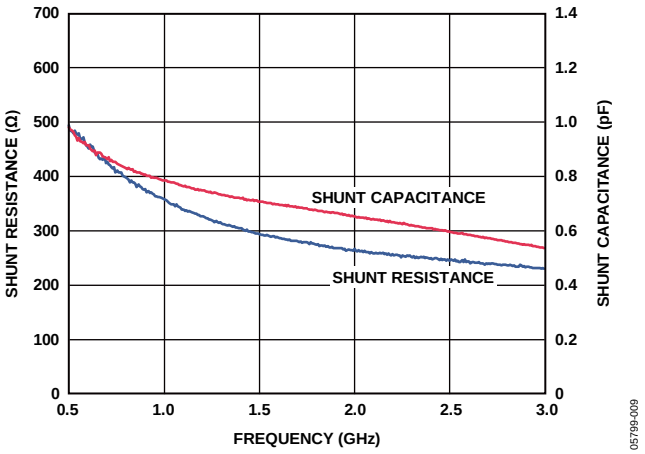

Figure 9. Input Impedance vs. Frequency; Supply = 3.0 V

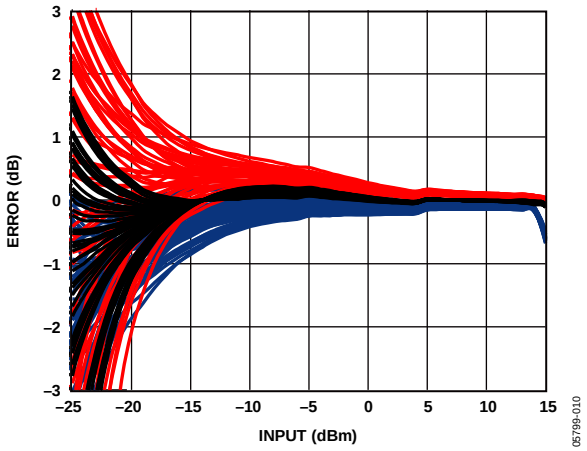

Figure 10. Output Temperature Drift from +25°C Linear Reference for 50 Devices at −40°C, +25°C, and +85°C; Frequency = 450 MHz

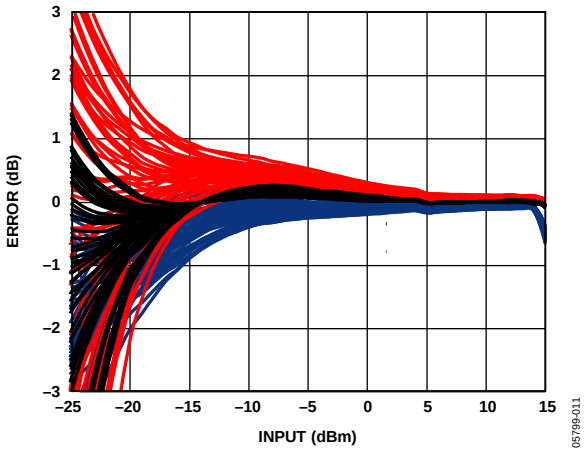

Figure 11. Output Temperature Drift from +25°C Linear Reference for 50 Devices at −40°C, +25°C, and +85°C; Frequency = 900 MHz

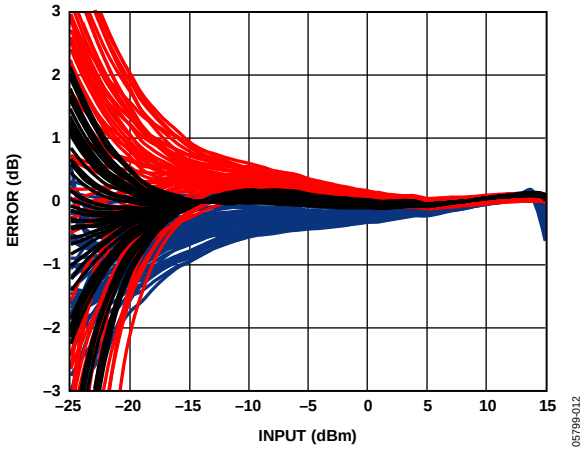

Figure 12. Output Temperature Drift from +25°C Linear Reference for 50 Devices at −40°C, +25°C, and +85°C; Frequency = 1900 MHz

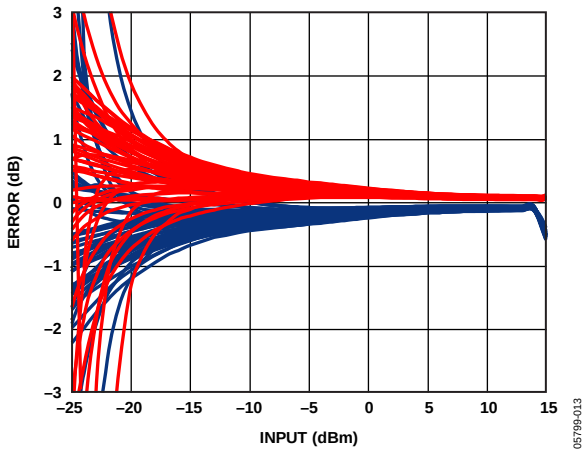

Figure 13. Output Delta from +25°C Output Voltage for 50 Devices at −40°C and +85°C; Frequency = 450 MHz

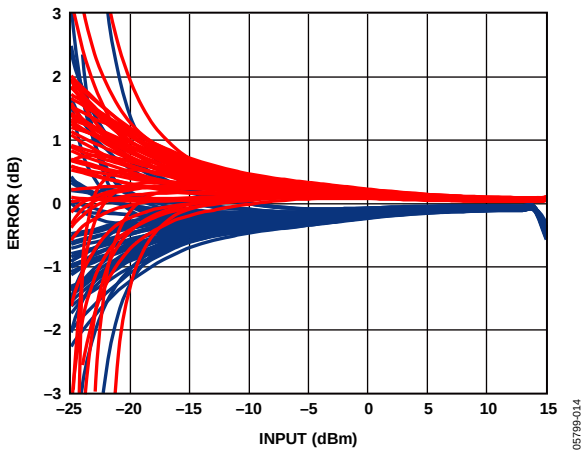

Figure 14. Output Delta from +25°C Output Voltage for 50 Devices at −40°C and +85°C; Frequency = 900 MHz

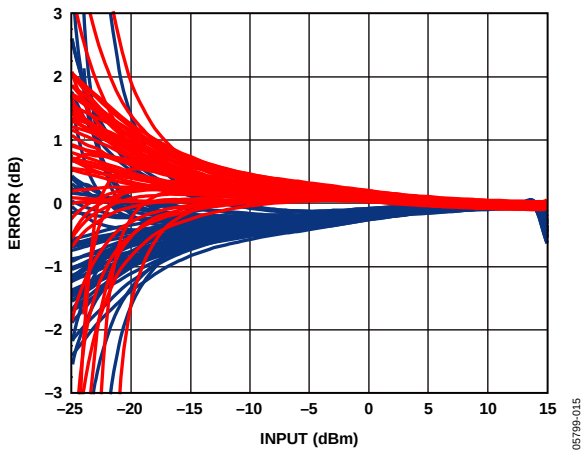

Figure 15. Output Delta from +25°C Output Voltage for 50 Devices at −40°C and +85°C; Frequency = 1900 MHz

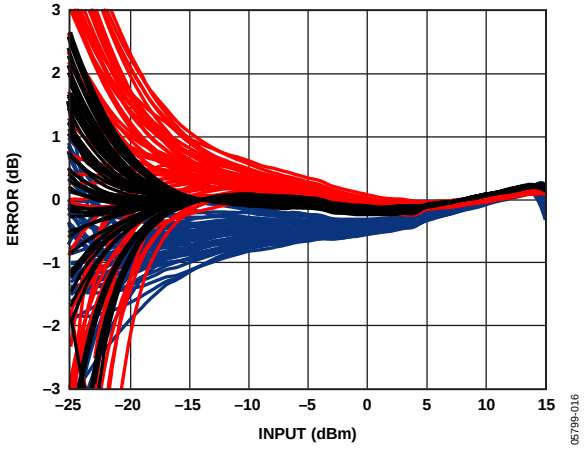

Figure 16. Output Temperature Drift from +25°C Linear Reference for 50 Devices at −40°C, +25°C, and +85°C; Frequency = 2600 MHz

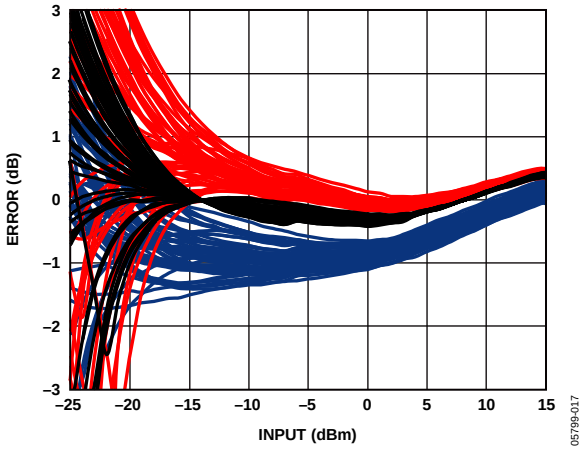

Figure 17. Output Temperature Drift from +25°C Linear Reference for 50 Devices at −40°C, +25°C, and +85°C; Frequency = 3500 MHz

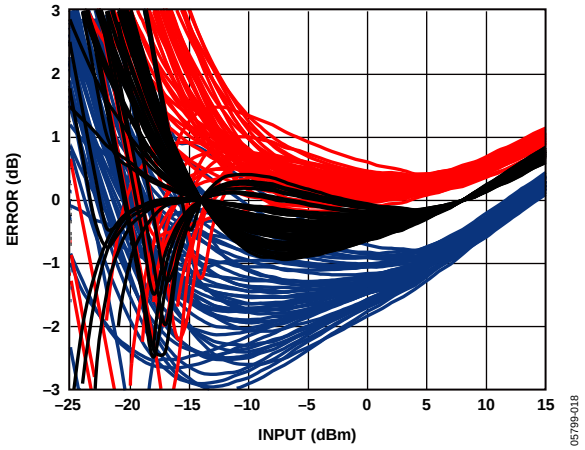

Figure 18. Output Temperature Drift from +25°C Linear Reference for 50 Devices at −40°C, +25°C, and +85°C; Frequency = 6000 MHz

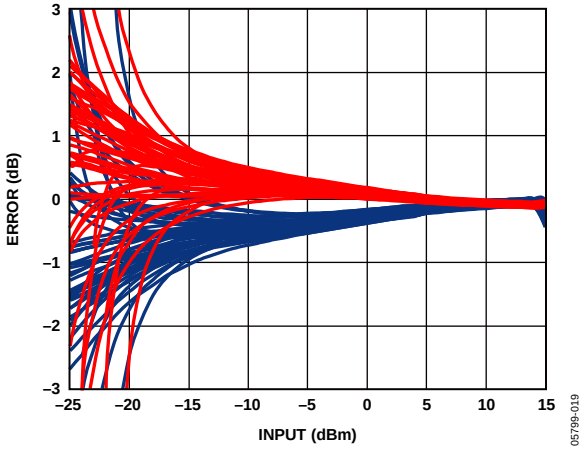

Figure 19. Output Delta from +25°C Output Voltage for 50 Devices at −40°C and +85°C; Frequency = 2600 MHz

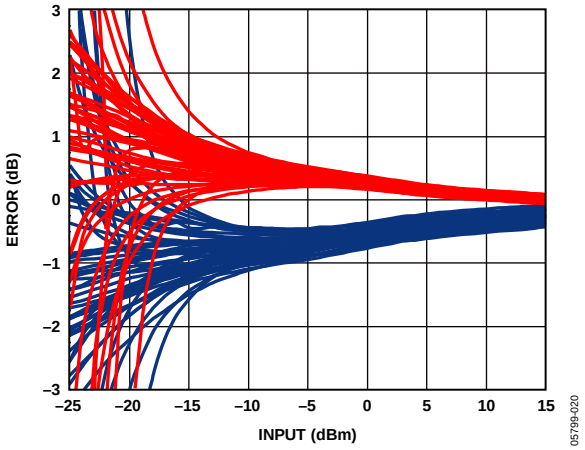

Figure 20. Output Delta from +25°C Output Voltage for 50 Devices at −40°C and +85°C; Frequency = 3500 MHz

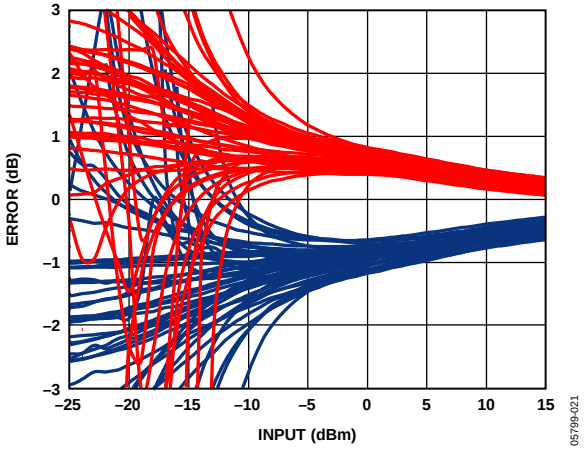

Figure 21. Output Delta from +25°C Output Voltage for 50 Devices at −40°C and +85°C; Frequency = 6000 MHz

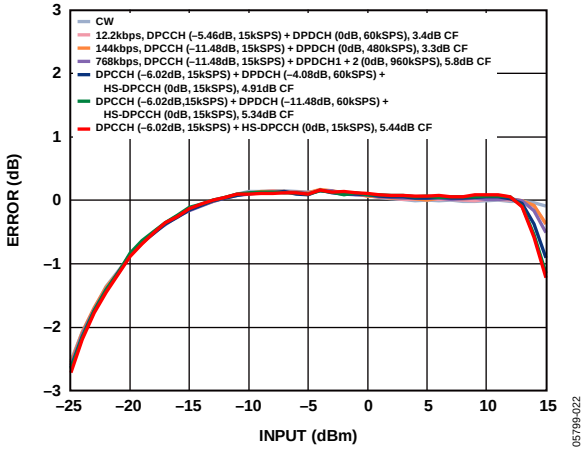

Figure 22. Error from CW Linear Reference vs. Input with Various W-CDMA Reverse Link Waveforms at 900 MHz, C_{OUT} = Open

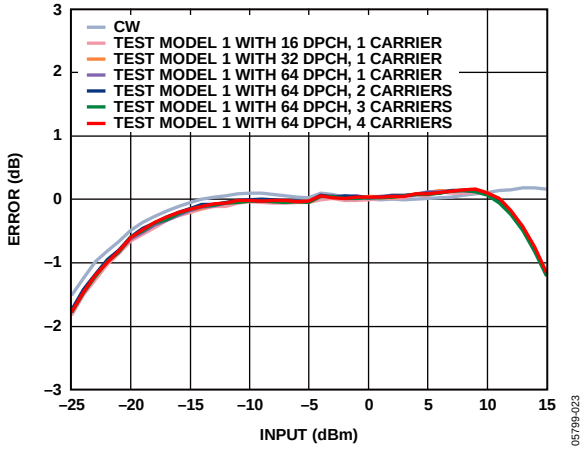

Figure 23. Error from CW Linear Reference vs. Input with Various W-CDMA Forward Link Waveforms at 2200 MHz, C_{OUT} = Open

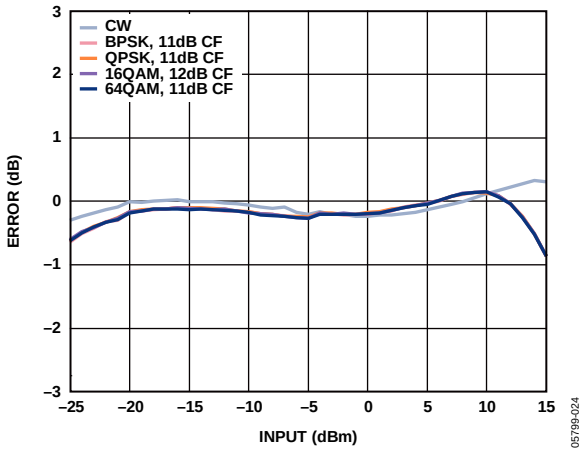

Figure 24. Error from CW Linear Reference vs. Input with Various 802.16 OFDM Waveforms at 3500 MHz, 10 MHz Signal BW, and 256 Subcarriers for All Modulated Signals, C_{OUT} = Open

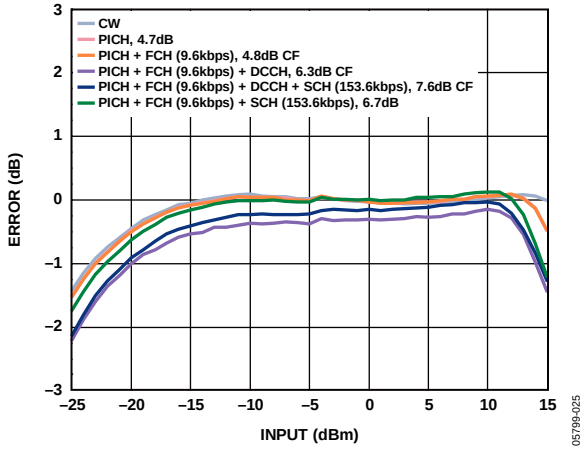

Figure 25. Error from CW Linear Reference vs. Input with Various CDMA2000 Reverse Link Waveforms at 1900 MHz, C_{OUT} = Open

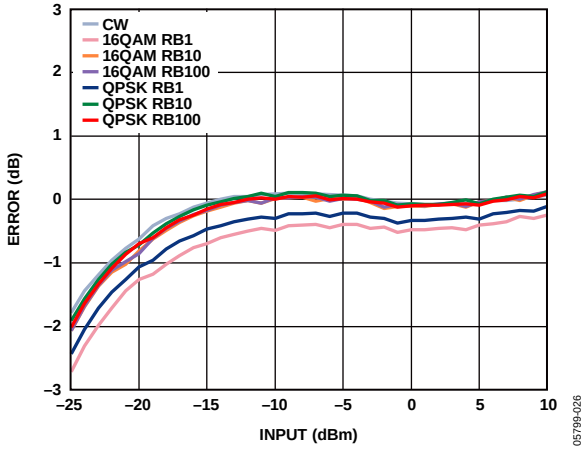

Figure 26. Error from CW Linear Reference vs. Input with Various LTE Reverse Link Waveforms at 2600 MHz, C_{OUT} = Open

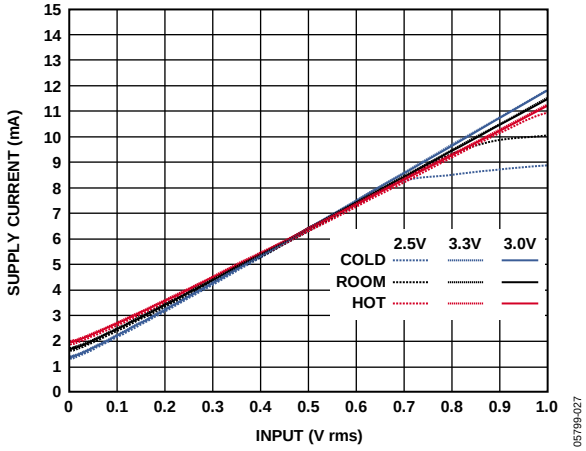

Figure 27. Supply Current vs. Input Level; Supplies = 2.5 V, 3.0 V, and 3.3 V; Frequency = 900 MHz; Temperatures = −40°C, +25°C, and +85°C

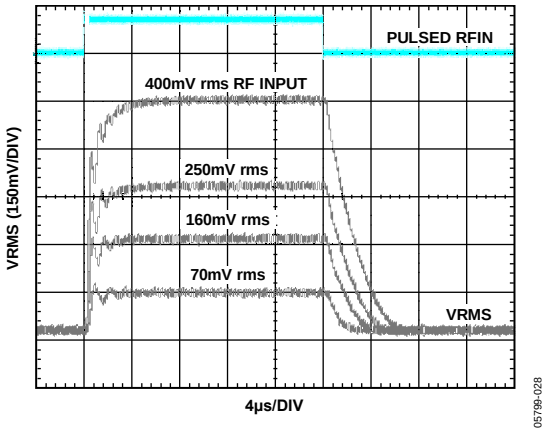

Figure 28. Output Response to Various RF Input Pulse Levels; Supply = 3.0 V; Frequency = 900 MHz; C_{OUT} = Open

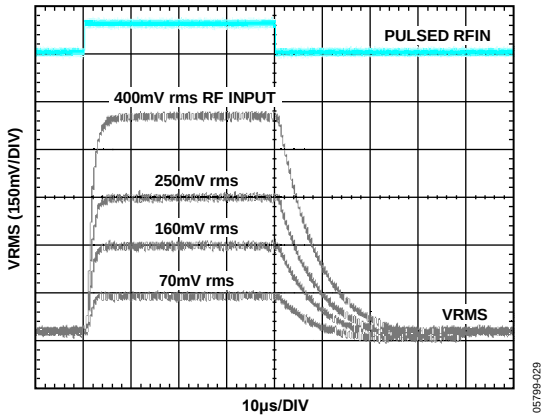

Figure 29. Output Response to Various RF Input Pulse Levels; Supply = 3.0 V; Frequency = 900 MHz; C_{OUT} = 100 nF

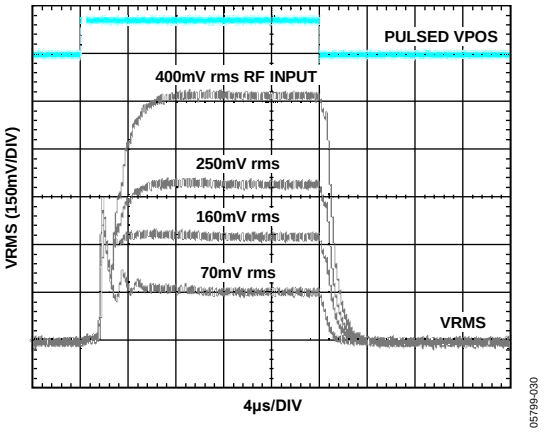

Figure 30. Output Response to Supply Gating at Various RF Input Levels; Supply = 3.0 V; Frequency = 900 MHz; C_{OUT} = Open

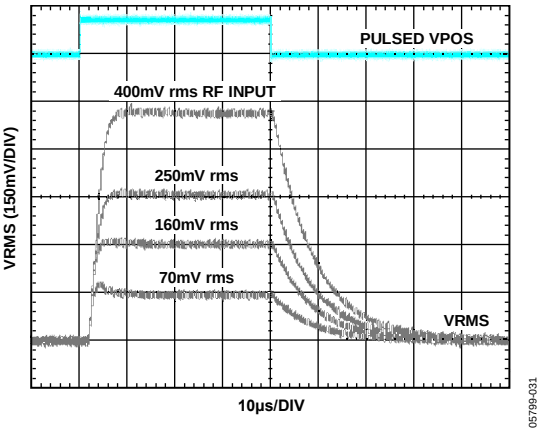

Figure 31. Output Response to Supply Gating at Various RF Input Levels; Supply = 3.0 V; Frequency = 900 MHz; C_{OUT} = 100 nF

CIRCUIT DESCRIPTION

The ADL5505 employs two-stage detection. The critical aspect of this technical approach is the concept of first stripping the carrier to reveal the envelope and then performing the required analog computation of rms.

RMS CIRCUIT DESCRIPTION AND FILTERING

The rms processing is executed using a proprietary translinear technique. This method is a mathematically accurate rms computing approach and allows for achieving unprecedented rms accuracies for complex modulation signals irrespective of the crest factor of the input signal. An integrating filter capacitor performs the square-domain averaging. The VRMS output can be expressed as

$$VRMS = A \times \sqrt{\frac{\int_{T1}^{T2} V_{IN}^2 \times dt}{T2 - T1}}$$

where A is a scaling parameter that is determined by the on-chip resistor ratio.

There are no other scaling parameters involved in this computation, which means that the rms output is inherently free from any sources of error due to temperature, supply, and process variations.

FILTERING

An important aspect of rms-dc conversion is the need for averaging (the function is root-mean-square). The on-chip averaging in the square domain has a corner frequency of approximately 180 kHz. and is sufficient for common modulation signals, such as CDMA-, CDMA2000-, W-CDMA-, and QPSK-/QAM-based OFDM (for example, LTE, WLAN, and WiMAX).

Adequate filtering ensures the accuracy of the rms measurement; however, some ripple or ac residual can still be present on the dc output. To reduce this ripple, an external shunt capacitor can be used at the output to form a low-pass filter with the on-chip, 100 Ω resistance (see the Selecting the Output Low-Pass Filter section).

OUTPUT BUFFER

A buffer takes the internal rms signal and amplifies it accordingly before it is output on the VRMS pin. The output stage of the rms buffer is a common source PMOS with a resistive load to provide a rail-to-rail output. The buffer has a 100 Ω on-chip series resistance on the output, allowing for easy low-pass filtering.

APPLICATIONS INFORMATION

BASIC CONNECTIONS

Figure 32 shows the basic connections for the ADL5505. The device is powered by a single supply between 2.5 V and 3.3 V, with a quiescent current of 1.8 mA. The VPOS pin is decoupled using 100 pF and 0.1 µF capacitors.

Placing a single 75 Ω resistor at the RF input provides a broadband match of 50 Ω. More precise resistive or reactive matches can be applied for narrow frequency band use (see the RF Input Interfacing section).

The ac residual can be reduced further by increasing the output capacitance, C_{OUT}. The combination of the internal 100 Ω output resistance and C_{OUT} produces a low-pass filter to reduce output ripple of the VRMS output (see the Selecting the Output Low-Pass Filter section for more details).

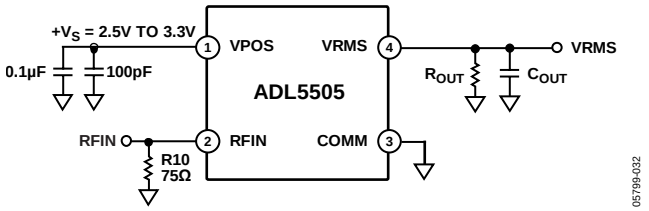

Figure 32. Basic Connections for ADL5505

RF INPUT INTERFACING

The input impedance of the ADL5505 decreases with increasing frequency in both its resistive and capacitive components (see Figure 9). The resistive component varies from 370 Ω at 900 MHz to about 245 Ω at 2600 MHz.

A number of options exist for input matching. For operation at multiple frequencies, a 75 Ω shunt to ground, as shown in Figure 33, provides the best overall match. For use at a single frequency, a resistive or a reactive match can be used. By plotting the input impedance on a Smith Chart, the best value for a resistive match can be calculated. (Both input impedance and input capacitance can vary by up to ±20% around their nominal values.) Where VSWR is critical, the match can be improved with a series inductor placed before the shunt component.

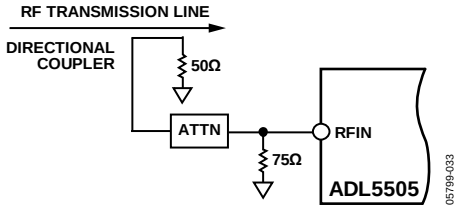

Figure 33. Input Interfacing to Directional Coupler

Resistive Tap RF Input

Figure 34 shows a technique for coupling the input signal into the ADL5505 that can be applicable when the input signal is much larger than the input range of the ADL5505. A series resistor combines with the input impedance of the ADL5505 to attenuate the input signal. Because this series resistor forms a divider with the frequency-dependent input impedance, the apparent gain changes greatly with frequency. However, this method has the advantage of very little power being tapped off in RF power transmission applications. If the resistor is large compared with the impedance of the transmission line, the VSWR of the system is relatively unaffected.

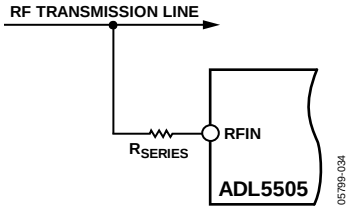

Figure 34. Attenuating the Input Signal

The resistive tap or series resistance, R_{SERIES}, can be expressed as

$$R_{SERIES} = R_{IN}\,(1 - 10^{ATTN/20})/(10^{ATTN/20}) \quad (1)$$

where:
R_{IN} is the input impedance of RFIN.
ATTN is the desired attenuation factor in decibels.

For example, if a power amplifier with a maximum output power of 28 dBm is matched to the ADL5505 input at 5 dBm, then a −23 dB attenuation factor is required. At 900 MHz, the input resistance, R_{IN}, is 370 Ω.

$$R_{SERIES} = (370\ \Omega)(1 - 10^{-23/20})/(10^{-23/20}) = 4856\ \Omega \quad (2)$$

Thus, for an attenuation of −23 dB, a series resistance of approximately 4.87 kΩ (the nearest available standard resistor value) is needed.

Multiple RF Inputs

Figure 35 shows a technique for combining multiple RF input signals to the ADL5505. Some applications can share a single detector for multiple bands. Three 16.5 Ω resistors in a T network combine the three 50 Ω terminations (including the ADL5505 with the shunt 75 Ω matching component). The broadband resistive combiner ensures that each port of the T network sees a 50 Ω termination. Because there are only 6 dB of isolation from one port of the combiner to the other ports, only one band should be active at a time.

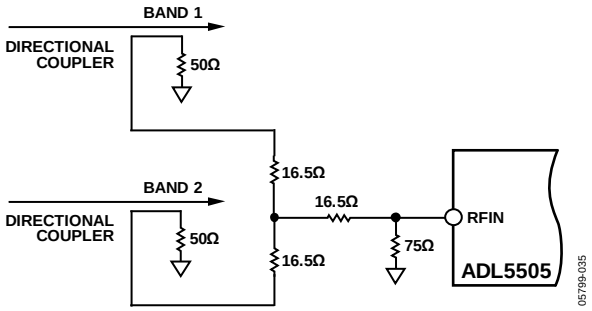

Figure 35. Combining Multiple RF Input Signals

LINEARITY

Because the ADL5505 is a linear responding device, plots of output voltage vs. input voltage result in a straight line (see Figure 4 and Figure 5) and the dynamic range in decibels (dB) is not clearly visible. It is more useful to plot the error on a logarithmic scale, as shown in Figure 7. The deviation of the plot from the ideal straight line characteristic is caused by input stage clipping at the high end and by signal offsets at the low end. However, offsets at the low end can be either positive or negative; therefore, the linearity error vs. input level plots (see Figure 7) can also trend upwards at the low end. Figure 10 to Figure 12 and Figure 16 to Figure 18 show error distributions for a large population of devices at specific frequencies over temperature.

It is also apparent in Figure 7 that the error at the lower portion of the dynamic range tends to shift up as frequency is increased. This is due to the calibration points chosen: −14 dBm and +8 dBm (see the Device Calibration and Error Calculation section).

The input impedance of the ADL5505 varies with frequency, decreasing the actual voltage across the input stage as the frequency increases and, thus, reducing the conversion gain. Similarly, conversion gain is less at frequencies near 450 MHz because of the small on-chip coupling capacitor. The dynamic range is near constant over frequency, but with a decrease in conversion gain as frequency is increased.

Output Swing

At 900 MHz, the VRMS output voltage is nominally 1.86 × the input rms voltage (a conversion gain of 1.86 V/V rms). The output voltage swings from near ground to 2.4 V on a 3.0 V supply.

Figure 8 shows the output swings of the ADL5505 to a CW input for various supply voltages. Only at the lowest supply voltages (2.5 V and 2.7 V) is there a reduction in the dynamic range as the input headroom decreases.

Output Offset

The ADL5505 has a ±1 dB error detection range of about 30 dB, as shown in Figure 10 to Figure 12 and Figure 16 to Figure 18. The error is referred to the best-fit line defined in the linear region of the output response (see the Device Calibration and Error Calculation section for more details). Below an input power of −16 dBm, the response is no longer linear and begins to lose accuracy. In addition, depending on the supply voltage, saturation may limit the detection accuracy above +14 dBm. Choose calibration points in the linear region, avoiding the nonlinear ranges at the high and low extremes.

Figure 36 shows a distribution of the output response vs. the input for multiple devices. The ADL5505 loses accuracy at low input powers as the output response begins to fan out. As the input power is reduced, the spread of the output response increases along with the error.

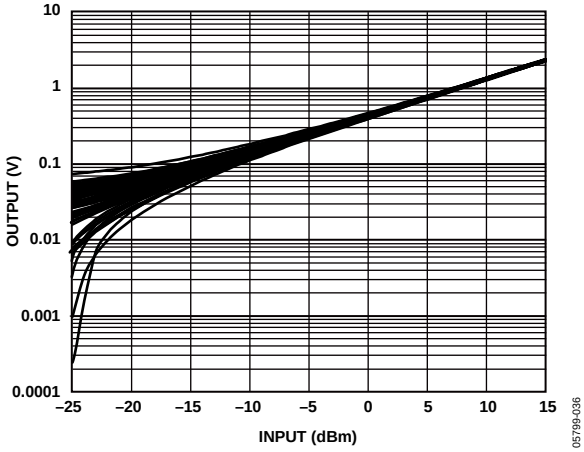

Figure 36. Output vs. Input Level Distribution of 50 Devices; Frequency = 900 MHz; Supply = 3.0 V

Although some devices follow the ideal linear response at very low input powers, not all devices continue the ideal linear regression to a near 0 V y-intercept. Some devices exhibit output responses that rapidly decrease, and some flatten out.

With no RF signal applied, the ADL5505 has a typical output offset of 10 mV (with a maximum of 100 mV) on VRMS.

OUTPUT DRIVE CAPABILITY AND BUFFERING

The ADL5505 is capable of sourcing a VRMS output current of approximately 3 mA. The output current is sourced through the on-chip, 100 Ω series resistor; therefore, any load resistor forms a voltage divider with this on-chip resistance. It is recommended that the ADL5505 VRMS output drive high resistance loads to preserve output swing. If an application requires driving a low resistance load (as well as in cases where increasing the nominal conversion gain is desired), a buffering circuit is necessary.

SELECTING THE OUTPUT LOW-PASS FILTER

The internal filter capacitor of the ADL5505 provides averaging in the square domain but leaves some residual ac on the output. Signals with high peak-to-average ratios, such as W-CDMA or CDMA2000, can produce ac residual levels on the ADL5505 VRMS dc output. To reduce the effects of these low frequency components in the waveforms, some additional filtering is required.

The output of the ADL5505 can be filtered directly by placing a capacitor between VRMS (Pin 4) and ground. The combination of the on-chip, 100 Ω output series resistance and the external shunt capacitor forms a low-pass filter to reduce the residual ac.

Figure 37 show the effects on the residual ripple vs. the output filter capacitor value at two communication standards with high peak-to-average ratios. Note that there is a trade-off between ac residual and response time. Large output filter capacitances increase the turn-on and pulse response times, as shown in Figure 38.

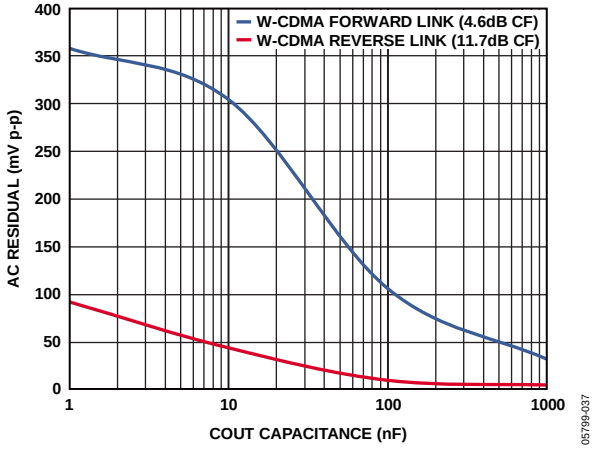

Figure 37. AC Residual vs. C_{OUT}, W-CDMA Reverse Link (11.7 dB CF) Waveform and W-CDMA Forward Link (4.6 dB CF) Waveform

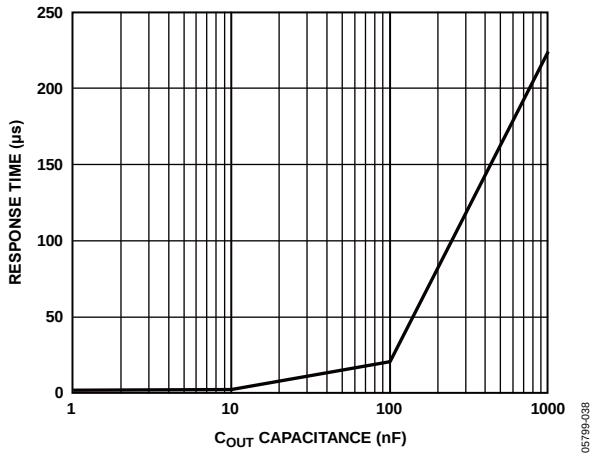

Figure 38. Effect of C_{OUT} on Response Time

The turn-on time and pulse response are strongly influenced by the sizes of the output shunt capacitor. Figure 39 shows a plot of the output response to an RF pulse on the RFIN pin, with a 0.1 µF output filter capacitor. The falling edge is particularly dependent on the output shunt capacitance, as shown in Figure 39.

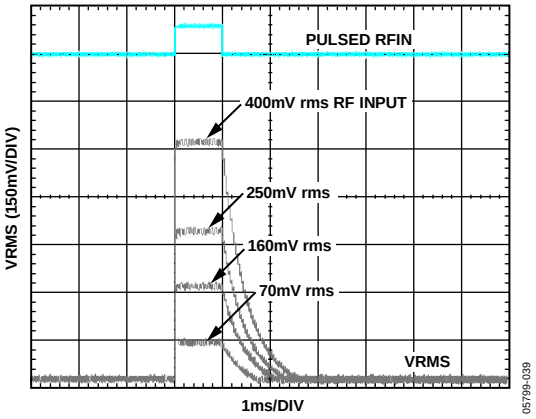

Figure 39. Output Response to Various RF Input Pulse Levels; Supply = 3 V; Frequency = 900 MHz; Square-Domain Filter Open; C_{OUT} = 0.1 µF

To improve the falling edge of the enable and pulse responses, a resistor can be placed in parallel with the output shunt capacitor. The added resistance helps to discharge the output filter capacitor. Although this method reduces the power-off time, the added load resistor also attenuates the output (see the Output Drive Capability and Buffering section).

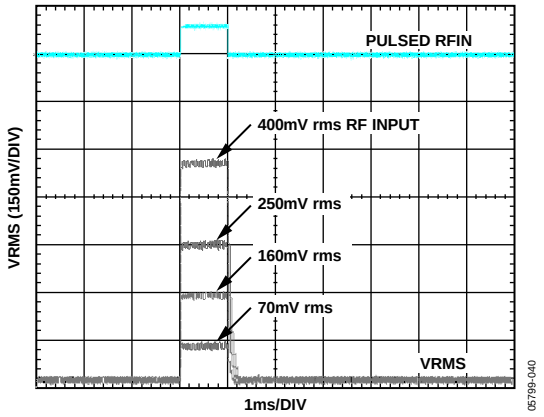

Figure 40. Output Response to Various RF Input Pulse Levels, Supply = 3 V, Frequency = 900 MHz; Square-Domain Filter Open; C_{OUT} = 0.1 µF with Parallel 1 kΩ

POWER CONSUMPTION

The quiescent current consumption of the ADL5505 varies linearly with the size of the input signal from approximately 1.8 mA for no signal up to 8.5 mA at an input level of 0.7 V rms (10 dBm, referred to 50 Ω) as shown in Figure 27. There is little variation in supply current across power supply voltage or temperature.

In applications requiring power saving, it is recommended that the ADL5505 be disabled while idle by removing the power supply to the device.

DEVICE CALIBRATION AND ERROR CALCULATION

Because slope and intercept vary from device to device, board-level calibration must be performed to achieve high accuracy. In general, calibration is performed by applying two input power levels to the ADL5505 and measuring the corresponding output voltages. The calibration points are generally chosen to be within the linear operating range of the device. The best-fit line is characterized by calculating the conversion gain (or slope) and intercept using the following equations:

$$Gain = (V_{VRMS2} - V_{VRMS1})/(V_{IN2} - V_{IN1}) \quad (3)$$

$$Intercept = V_{VRMS1} - (Gain \times V_{IN1}) \quad (4)$$

where:
V_{INx} is the rms input voltage to RFIN.
V_{VRMSx} is the voltage output at VRMS.

Once gain and intercept are calculated, an equation can be written that allows calculation of an (unknown) input power based on the measured output voltage.

$$V_{IN} = (V_{VRMS} - Intercept)/Gain \quad (5)$$

For an ideal (known) input power, the law conformance error of the measured data can be calculated as

$$ERROR\ (\text{dB}) = 20 \times \log\ [(V_{VRMS,\ MEASURED} - Intercept)/(Gain \times V_{IN,\ IDEAL})] \quad (6)$$

Figure 41 shows a plot of the error at 25°C, the temperature at which the ADL5505 is calibrated. Note that the error is not 0; this is because the ADL5505 does not perfectly follow the ideal linear equation, even within its operating region. The error at the calibration points is, however, equal to 0 by definition.

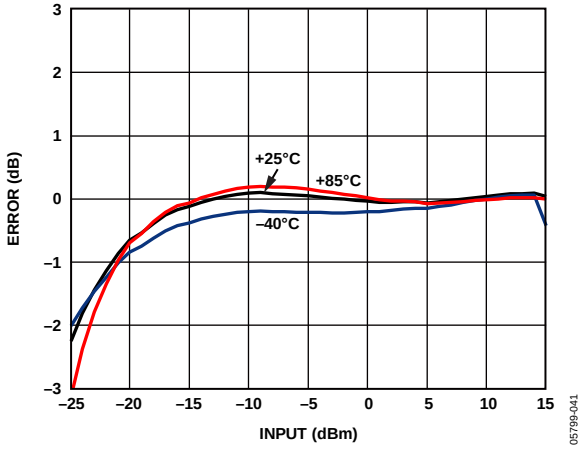

Figure 41. Error from Linear Reference vs. Input at −40°C, +25°C, and +85°C vs. +25°C Linear Reference, 1900 MHz Frequency, 3.0 V Supply

Figure 41 also shows error plots for the output voltage at −40°C and +85°C. These error plots are calculated using the gain and intercept at 25°C. This is consistent with calibration in a mass production environment where calibration at temperature is not practical.

CALIBRATION FOR IMPROVED ACCURACY

Another way of presenting the error function of the ADL5505 is shown in Figure 42. In this case, the decibel (dB) error at hot and cold temperatures is calculated with respect to the transfer function at ambient temperature. This is a key difference in comparison to Figure 41, in which the error was calculated with respect to the ideal linear transfer function at ambient temperature. When this alternative technique is used, the error at ambient temperature becomes equal to 0 by definition (see Figure 42).

This plot is a useful tool for estimating temperature drift at a particular power level with respect to the (nonideal) response at ambient temperature. The linearity and dynamic range tend to be improved artificially with this type of plot because the ADL5505 does not perfectly follow the ideal linear equation (especially outside of its linear operating range). Achieving this level of accuracy in an end application requires calibration at multiple points in the operating range of the device.

In some applications, very high accuracy is required at just one power level or over a reduced input range. For example, in a wireless transmitter, the accuracy of the high power amplifier (HPA) is most critical at or close to full power. The ADL5505 offers a tight error distribution in the high input power range, as shown in Figure 42. The high accuracy range, beginning around 6 dBm at 1900 MHz, offers 8 dB of ±0.15 dB detection error over temperature. Multiple point calibration at ambient temperature in the reduced range offers precise power measurement with near 0 dB error from −40°C to +85°C.

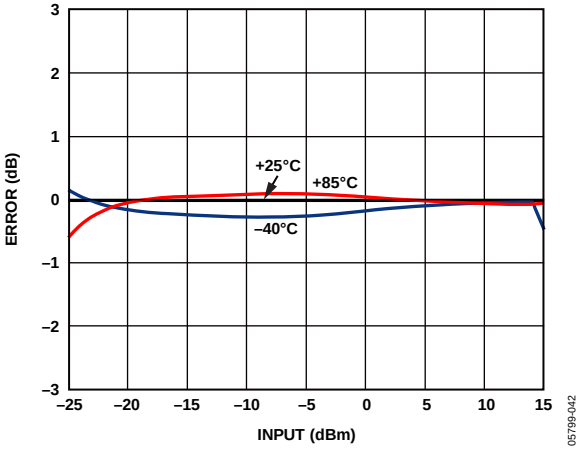

Figure 42. Error from +25°C Output Voltage at −40°C, +25°C, and +85°C After Ambient Normalization, 1900 MHz Frequency, 3.0 V Supply

Note that the high accuracy range center varies over frequency (see Figure 13 to Figure 15 and Figure 19 to Figure 21).

DRIFT OVER A REDUCED TEMPERATURE RANGE

Figure 43 shows the error over temperature for a 1.9 GHz input signal. The error due to drift over temperature consistently remains within ±0.15 dB and only begins to exceed this limit when the ambient temperature rises above +65°C and drops below −20°C. For all frequencies using a reduced temperature range, higher measurement accuracy is achievable.

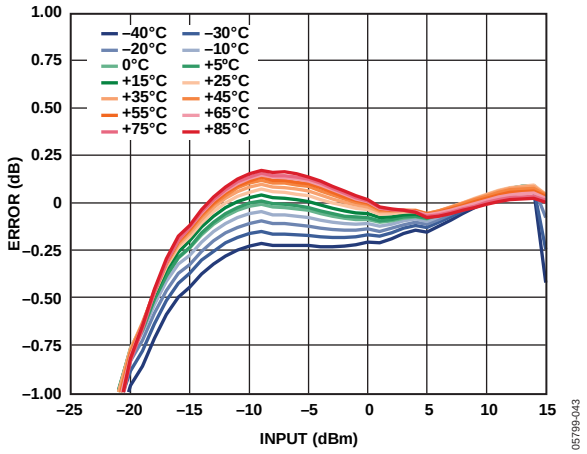

Figure 43. Typical Drift at 1.9 GHz for Various Temperatures

DEVICE HANDLING

The wafer level chip scale package consists of solder bumps connected to the active side of the die. The part is Pb-free and RoHS compliant with 95.5% tin, 4.0% silver, and 0.5% copper solder bump composition. The WLCSP can be mounted on printed circuit boards using standard surface-mount assembly techniques; however, caution should be taken to avoid damaging the die. See the AN-617 Application Note, *MicroCSP Wafer Level Chip Scale Package*, for additional information. WLCSP devices are bumped die; therefore, the exposed die may be sensitive to light, which can influence specified limits. Lighting in excess of 600 lux can degrade performance.

LAND PATTERN AND SOLDERING INFORMATION

Pad diameters of 0.20 mm are recommended with a solder paste mask opening of 0.30 mm. For the RF input trace, a trace width of 0.30 mm is used, which corresponds to a 50 Ω characteristic impedance for the dielectric material being used (FR4). All traces going to the pads are tapered down to 0.15 mm. For the RFIN line, the length of the tapered section is 0.20 mm.

EVALUATION BOARD

Figure 44 shows the schematic of the ADL5505 evaluation board. The board is powered by a single supply in the 2.5 V to 3.3 V range. The power supply is decoupled by 100 pF and 0.1 µF capacitors.

The RF input has a broadband match of 50 Ω using a single 75 Ω resistor at R7B. More precise matching at spot frequencies is possible (see the RF Input Interfacing section).

Table 4 details the various configuration options of the evaluation board. Figure 45 shows the layout of the evaluation board.

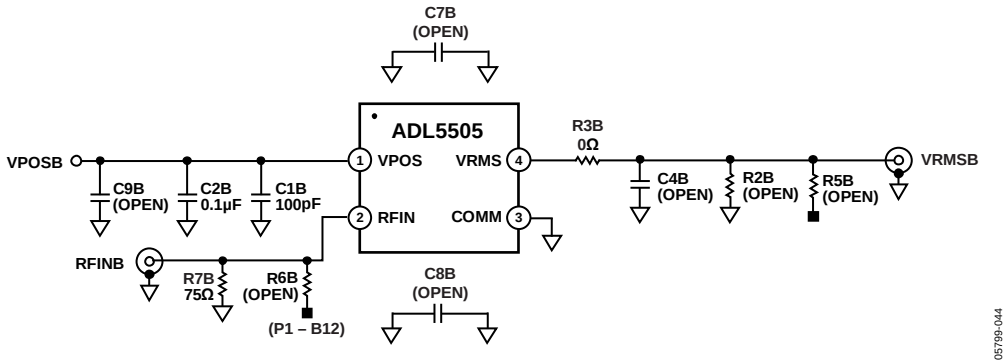

Figure 44. Evaluation Board Schematic

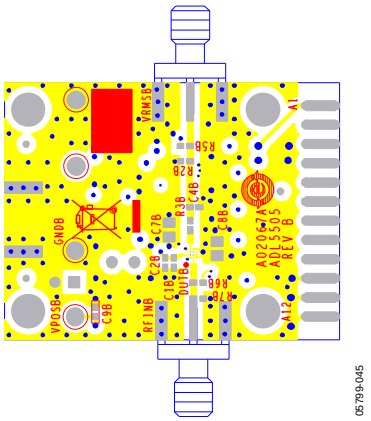

Figure 45. Layout of Evaluation Board, Component Side

Table 4. Evaluation Board Configuration Options

Component	Description	Default Condition
VPOSB, GNDB	Ground and supply vector pins.	Not applicable
C1B, C2B, C7B, C8B, C9B	Power supply decoupling. Nominal supply decoupling of 0.1 µF and 100 pF.	C1B = 100 pF (Size 0402) C2B = 0.1 µF (Size 0402) C7B = C8B = open (Size 0805) C9B = open (Size 0402)
R7B	RF input interface. The 75 Ω resistor at R7B combines with the ADL5505 internal input impedance to give a broadband input impedance of around 50 Ω.	R7B = 75 Ω (Size 0402)
C4B, R2B, R3B	Output filtering. The combination of the internal 100 Ω output resistance and C4B produce a low-pass filter to reduce output ripple of the VRMS output. The output can be scaled down using the resistor divider pads, R2B and R3B.	R3B = 0 Ω (Size 0402) R2B = open (Size 0402) C4B = open (Size 0402)
P1, R5B, R6B	Alternate interface. The end connector, P1, allows access to various ADL5505 signals. These signal paths are only used during factory test and characterization.	P1 = not installed R5B = R6B = open (Size 0402)

OUTLINE DIMENSIONS

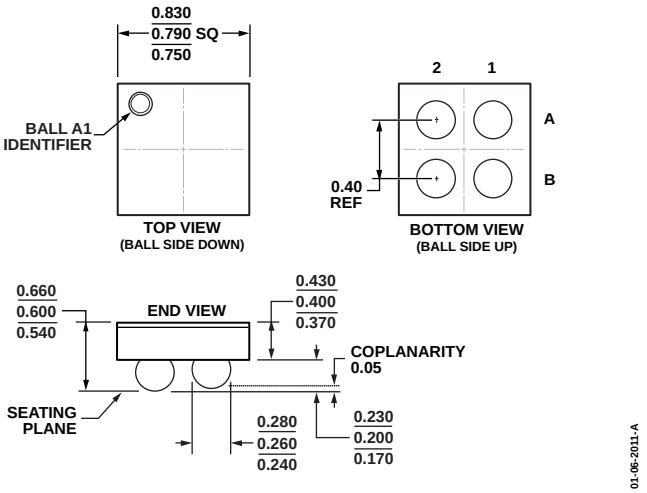

Figure 46. 4-Ball Wafer Level Chip Scale Package [WLCSP]
(CB-4-6)
Dimensions shown in millimeters

ORDERING GUIDE

Model[1]	Temperature Range	Package Description	Package Option	Branding	Ordering Quantity
ADL5505ACBZ-P7	–40°C to +85°C	4-Ball WLCSP, 7" Pocket Tape and Reel	CB-4-6	3R	3,000
ADL5505ACBZ-P2	–40°C to +85°C	4-Ball WLCSP, 7" Pocket Tape and Reel	CB-4-6	3R	250
ADL5505-EVALZ		Evaluation board			

[1] Z = RoHS Compliant Part.

Mouser Electronics

Authorized Distributor

Click to View Pricing, Inventory, Delivery & Lifecycle Information:

Analog Devices Inc.:

ADL5505ACBZ-P7 ADL5505-EVALZ