

## FEATURES

**0.5  $\Omega$  typical on resistance**  
**0.8  $\Omega$  maximum on resistance at 125°C**  
**1.65 V to 3.6 V operation**  
**Automotive temperature range: -40°C to +125°C**  
**High current carrying capability: 300 mA continuous**  
**Rail-to-rail switching operation**  
**Fast-switching times <20 ns**  
**Typical power consumption (<0.1  $\mu$ W)**

## APPLICATIONS

Cellular phones  
 PDAs  
 MP3 players  
 Power routing  
 Battery-powered systems  
 PCMCIA cards  
 Modems  
 Audio and video signal routing  
 Communication systems

## GENERAL DESCRIPTION

The **ADG836** is a low voltage complementary metal-oxide semiconductor (CMOS) device containing two independently selectable single-pole, double-throw (SPDT) switches. This device offers an ultralow on resistance of less than 0.8  $\Omega$  over the full temperature range. The **ADG836** is fully specified for 3.3 V, 2.5 V, and 1.8 V supply operation.

Each switch conducts equally well in both directions when on, and has an input signal range that extends to the supplies. The **ADG836** exhibits break-before-make switching action.

The **ADG836** is available in a 10-lead MSOP and in a 3 mm  $\times$  3 mm 12-lead LFCSP.

## FUNCTIONAL BLOCK DIAGRAM

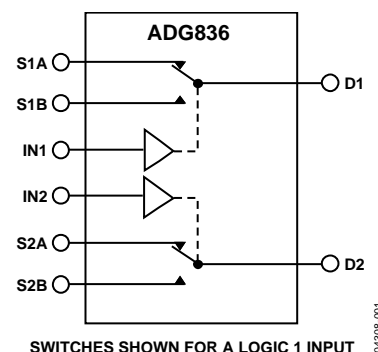


Figure 1.

## PRODUCT HIGHLIGHTS

1. <0.8  $\Omega$  over full temperature range of -40°C to +125°C.
2. Single 1.65 V to 3.6 V operation.
3. Compatible with 1.8 V CMOS logic.
4. High current handling capability (300 mA continuous current at 3.3 V).
5. Low total harmonic distortion plus noise (THD + N) (0.02% typical).
6. 3 mm  $\times$  3 mm LFCSP and 10-lead MSOP.

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REVISION HISTORY

<b>8/2020—Rev. B to Rev. C</b>		<b>4/2005—Rev. 0 to Rev. A</b>	
Changes to Table 1 .....	3	Updated Format .....	Universal
Changes to Table 2 .....	4	Changes to Table 1 .....	3
Changes to Table 3 .....	5	Changes to Table 2 .....	4
		Changes to Table 3 .....	5
		Changes to Ordering Guide.....	13
<b>6/2016—Rev. A to Rev. B</b>		<b>8/2003—Revision 0: Initial Version</b>	
Changed CP-12-1 to CP-12-4.....	Throughout		
Changes to Figure 3 and Table 6.....	7		
Added Terminology Section.....	13		
Updated Outline Dimensions.....	14		
Changes to Ordering Guide.....	14		

## SPECIFICATIONS

$V_{DD} = 2.7 \text{ V}$  to  $3.6 \text{ V}$ ,  $GND = 0 \text{ V}$ , unless otherwise noted. The temperature range for the Y version is  $-40^{\circ}\text{C}$  to  $+125^{\circ}\text{C}$ .

Table 1.

Parameter	+25°C	−40°C to +85°C	−40°C to +125°C	Unit	Test Conditions/Comments
ANALOG SWITCH					
Analog Signal Range			0 V to $V_{DD}$	V	
On Resistance ( $R_{ON}$ )	0.5			$\Omega$ typ	$V_{DD} = 2.7 \text{ V}$ , $V_S = 0 \text{ V}$ to $V_{DD}$ , $I_S = 100 \text{ mA}$ ; Figure 19
	0.75	0.85	0.9	$\Omega$ max	
On-Resistance Match Between Channels ( $\Delta R_{ON}$ )	0.04			$\Omega$ typ	$V_{DD} = 2.7 \text{ V}$ , $V_S = 0.65 \text{ V}$ , $I_S = 100 \text{ mA}$
	0.095	0.095	0.1	$\Omega$ max	
On-Resistance Flatness ( $R_{FLAT(ON)}$ )	0.1			$\Omega$ typ	$V_{DD} = 2.7 \text{ V}$ , $V_S = 0 \text{ V}$ to $V_{DD}$
	0.18	0.18	0.19	$\Omega$ max	$I_S = 100 \text{ mA}$
LEAKAGE CURRENTS					$V_{DD} = 3.6 \text{ V}$
Source Off Leakage $I_S$ (OFF)	$\pm 0.2$			nA typ	$V_S = 0.6 \text{ V}/3.3 \text{ V}$ , $V_D = 3.3 \text{ V}/0.6 \text{ V}$ ; Figure 20
Channel On Leakage $I_D$ , $I_S$ (ON)	$\pm 0.2$			nA typ	$V_S = V_D = 0.6 \text{ V}$ or $3.3 \text{ V}$ ; Figure 21
DIGITAL INPUTS					
Input High Voltage, $V_{INH}$			2	V min	
Input Low Voltage, $V_{INL}$			0.8	V max	
Input Current					
$I_{INL}$ or $I_{INH}$	0.005			$\mu\text{A}$ typ	$V_{IN} = V_{INL}$ or $V_{INH}$
			$\pm 0.1$	$\mu\text{A}$ max	
$C_{IN}$ , Digital Input Capacitance	4			pF typ	
DYNAMIC CHARACTERISTICS <sup>1</sup>					
$t_{ON}$	21			ns typ	$R_L = 50 \Omega$ , $C_L = 35 \text{ pF}$
	26	28	29	ns max	$V_S = 1.5 \text{ V}/0 \text{ V}$ ; Figure 22
$t_{OFF}$	4			ns typ	$R_L = 50 \Omega$ , $C_L = 35 \text{ pF}$
	7	8	9	ns max	$V_S = 1.5 \text{ V}$ ; Figure 22
Break-Before-Make Time Delay ( $t_{BBM}$ )	17			ns typ	$R_L = 50 \Omega$ , $C_L = 35 \text{ pF}$
			5	ns min	$V_{S1} = V_{S2} = 1.5 \text{ V}$ ; Figure 23
Charge Injection	40			pC typ	$V_S = 1.5 \text{ V}$ , $R_S = 0 \Omega$ , $C_L = 1 \text{ nF}$ ; Figure 24
Off Isolation	−67			dB typ	$R_L = 50 \Omega$ , $C_L = 5 \text{ pF}$ , $f = 100 \text{ kHz}$ ; Figure 25
Channel-to-Channel Crosstalk	−90			dB typ	S1A to S2A/S1B to S2B, $R_L = 50 \Omega$ , $C_L = 5 \text{ pF}$ , $f = 100 \text{ kHz}$ ; Figure 28
	−67			dB typ	S1A to S1B/S2A to S2B, $R_L = 50 \Omega$ , $C_L = 5 \text{ pF}$ , $f = 100 \text{ kHz}$ ; Figure 27
Total Harmonic Distortion Plus Noise (THD + N)	0.02			%	$R_L = 32 \Omega$ , $f = 20 \text{ Hz}$ to $20 \text{ kHz}$ , $V_S = 2 \text{ V p-p}$
Insertion Loss	−0.05			dB typ	$R_L = 50 \Omega$ , $C_L = 5 \text{ pF}$ ; Figure 26
−3 dB Bandwidth	57			MHz typ	$R_L = 50 \Omega$ , $C_L = 5 \text{ pF}$ ; Figure 26
$C_S$ (OFF)	25			pF typ	
$C_D$ , $C_S$ (ON)	75			pF typ	
POWER REQUIREMENTS					$V_{DD} = 3.6 \text{ V}$
$I_{DD}$	0.003			$\mu\text{A}$ typ	Digital inputs = 0 V or 3.6 V
		1	4	$\mu\text{A}$ max	

<sup>1</sup> Guaranteed by design, not subject to production test.

$V_{DD} = 2.5 \text{ V} \pm 0.2 \text{ V}$ ,  $GND = 0 \text{ V}$ , unless otherwise noted. The temperature range for the Y version is  $-40^{\circ}\text{C}$  to  $+125^{\circ}\text{C}$ .

Table 2.

Parameter	+25°C	−40°C to +85°C	−40°C to +125°C	Unit	Test Conditions/Comments
<b>ANALOG SWITCH</b>					
Analog Signal Range			0 V to $V_{DD}$	V	
On Resistance ( $R_{ON}$ )	0.65 0.84	0.92	1.0	$\Omega$ typ $\Omega$ max	$V_{DD} = 2.3 \text{ V}$ , $V_S = 0 \text{ V}$ to $V_{DD}$ , $I_S = 100 \text{ mA}$ ; Figure 19
On-Resistance Match Between Channels ( $\Delta R_{ON}$ )	0.04 0.1	0.1	0.105	$\Omega$ typ $\Omega$ max	$V_{DD} = 2.3 \text{ V}$ , $V_S = 0.7 \text{ V}$ , $I_S = 100 \text{ mA}$
On-Resistance Flatness ( $R_{FLAT(ON)}$ )	0.16 0.25	0.25	0.26	$\Omega$ typ $\Omega$ max	$V_{DD} = 2.3 \text{ V}$ , $V_S = 0 \text{ V}$ to $V_{DD}$ , $I_S = 100 \text{ mA}$
<b>LEAKAGE CURRENTS</b>					
Source Off Leakage $I_S$ (OFF)	$\pm 0.2$			nA typ	$V_{DD} = 2.7 \text{ V}$ $V_S = 0.6 \text{ V}/2.4 \text{ V}$ , $V_D = 2.4 \text{ V}/0.6 \text{ V}$ ; Figure 20
Channel On Leakage $I_D$ , $I_S$ (ON)	$\pm 0.2$			nA typ	$V_S = V_D = 0.6 \text{ V}$ or $2.4 \text{ V}$ ; Figure 21
<b>DIGITAL INPUTS</b>					
Input High Voltage, $V_{INH}$			1.7	V min	
Input Low Voltage, $V_{INL}$			0.7	V max	
Input Current $I_{INL}$ or $I_{INH}$	0.005		$\pm 0.1$	$\mu\text{A}$ typ $\mu\text{A}$ max	$V_{IN} = V_{INL}$ or $V_{INH}$
$C_{IN}$ , Digital Input Capacitance	4			pF typ	
<b>DYNAMIC CHARACTERISTICS<sup>1</sup></b>					
$t_{ON}$	23 29	30	31	ns typ ns max	$R_L = 50 \Omega$ , $C_L = 35 \text{ pF}$ $V_S = 1.5 \text{ V}/0 \text{ V}$ ; Figure 22
$t_{OFF}$	5 7	8	9	ns typ ns max	$R_L = 50 \Omega$ , $C_L = 35 \text{ pF}$ $V_S = 1.5 \text{ V}$ ; Figure 22
Break-before-Make Time Delay ( $t_{BBM}$ )	17		5	ns typ ns min	$R_L = 50 \Omega$ , $C_L = 35 \text{ pF}$ $V_{S1} = V_{S2} = 1.5 \text{ V}$ ; Figure 23
Charge Injection	30			pC typ	$V_S = 1.25 \text{ V}$ , $R_S = 0 \Omega$ , $C_L = 1 \text{ nF}$ ; Figure 24
Off Isolation	−67			dB typ	$R_L = 50 \Omega$ , $C_L = 5 \text{ pF}$ , $f = 100 \text{ kHz}$ ; Figure 25
Channel-to-Channel Crosstalk	−90 −67			dB typ dB typ	$S1A$ to $S2A/S1B$ to $S2B$ , $R_L = 50 \Omega$ , $C_L = 5 \text{ pF}$ , $f = 100 \text{ kHz}$ ; Figure 28 $S1A$ to $S1B/S2A$ to $S2B$ , $R_L = 50 \Omega$ , $C_L = 5 \text{ pF}$ , $f = 100 \text{ kHz}$ ; Figure 27
Total Harmonic Distortion Plus Noise (THD + N)	0.022			%	$R_L = 32 \Omega$ , $f = 20 \text{ Hz}$ to $20 \text{ kHz}$ , $V_S = 1.5 \text{ V}$ p-p
Insertion Loss	−0.06			dB typ	$R_L = 50 \Omega$ , $C_L = 5 \text{ pF}$ ; Figure 26
−3 dB Bandwidth	57			MHz typ	$R_L = 50 \Omega$ , $C_L = 5 \text{ pF}$ ; Figure 26
$C_S$ (OFF)	25			pF typ	
$C_D$ , $C_S$ (ON)	75			pF typ	
<b>POWER REQUIREMENTS</b>					
$I_{DD}$	0.003	1	4	$\mu\text{A}$ typ $\mu\text{A}$ max	$V_{DD} = 2.7 \text{ V}$ Digital inputs = 0 V or 2.7 V

<sup>1</sup> Guaranteed by design, not subject to production test.

$V_{DD} = 1.65 \text{ V} \pm 1.95 \text{ V}$ , GND = 0 V, unless otherwise noted. The temperature range for the Y version is  $-40^{\circ}\text{C}$  to  $+125^{\circ}\text{C}$ .

Table 3.

Parameter	+25°C	−40°C to +85°C	−40°C to +125°C	Unit	Test Conditions/Comments
ANALOG SWITCH					
Analog Signal Range			0 V to $V_{DD}$	V	$V_{DD} = 1.8 \text{ V}$ , $V_S = 0 \text{ V}$ to $V_{DD}$ , $I_S = 100 \text{ mA}$ ; Figure 19
On Resistance ( $R_{ON}$ )	1			$\Omega$ typ	
	1.6 2.7	2.4 4.2	2.4 4.2	$\Omega$ max $\Omega$ max	
On-Resistance Match Between Channels ( $\Delta R_{ON}$ )	0.1			$\Omega$ typ	$V_{DD} = 1.65 \text{ V}$ , $V_S = 0 \text{ V}$ to $V_{DD}$ , $I_S = 100 \text{ mA}$ ; Figure 19 $V_{DD} = 1.65 \text{ V}$ , $V_S = 0.7 \text{ V}$ , $I_S = 100 \text{ mA}$
LEAKAGE CURRENTS					$V_{DD} = 1.95 \text{ V}$
Source Off Leakage $I_S$ (OFF)	$\pm 0.2$			nA typ	$V_S = 0.6 \text{ V}/1.65 \text{ V}$ , $V_D = 1.65 \text{ V}/0.6 \text{ V}$ ; Figure 20
Channel On Leakage $I_D$ , $I_S$ (ON)	$\pm 0.2$			nA typ	$V_S = V_D = 0.6 \text{ V}$ or $1.65 \text{ V}$ ; Figure 21
DIGITAL INPUTS					
Input High Voltage, $V_{INH}$			$0.65 V_{DD}$	V min	$V_{IN} = V_{INL}$ or $V_{INH}$
Input Low Voltage, $V_{INL}$			$0.35 V_{DD}$	V max	
Input Current					
$I_{INL}$ or $I_{INH}$	0.005			$\mu\text{A}$ typ $\mu\text{A}$ max	
$C_{IN}$ , Digital Input Capacitance	4		$\pm 0.1$	pF typ	
DYNAMIC CHARACTERISTICS <sup>1</sup>					
$t_{ON}$	28 37	38	39	ns typ ns max	$R_L = 50 \Omega$ , $C_L = 35 \text{ pF}$ $V_S = 1.5 \text{ V}/0 \text{ V}$ ; Figure 22
$t_{OFF}$	7 9			ns typ ns max	
Break-Before-Make Time Delay ( $t_{BBM}$ )	21			ns typ ns min	
Charge Injection	20	10	11	pC typ	$V_{S1} = V_{S2} = 1 \text{ V}$ ; Figure 23 $V_S = 1 \text{ V}$ , $R_S = 0 \text{ V}$ , $C_L = 1 \text{ nF}$ ; Figure 24
Off Isolation	−67			dB typ	
Channel-to-Channel Crosstalk	−90			dB typ	
	−67			dB typ	
Total Harmonic Distortion (THD)	0.14			%	$R_L = 50 \Omega$ , $C_L = 5 \text{ pF}$ , $f = 100 \text{ kHz}$ ; Figure 25 S1A to S2A/S1B to S2B; $R_L = 50 \Omega$ , $C_L = 5 \text{ pF}$ , $f = 100 \text{ kHz}$ ; Figure 28 S1A to S1B/S2A to S2B; $R_L = 50 \Omega$ , $C_L = 5 \text{ pF}$ , $f = 100 \text{ kHz}$ ; Figure 27
Insertion Loss	−0.08			dB typ	$R_L = 32 \Omega$ , $f = 20 \text{ Hz}$ to $20 \text{ kHz}$ , $V_S = 1.2 \text{ V p-p}$
−3 dB Bandwidth	57			MHz typ	$R_L = 50 \Omega$ , $C_L = 5 \text{ pF}$ ; Figure 26
$C_S$ (OFF)	25			pF typ	$R_L = 50 \Omega$ , $C_L = 5 \text{ pF}$ ; Figure 26
$C_D$ , $C_S$ (ON)	75			pF typ	
POWER REQUIREMENTS					$V_{DD} = 1.95 \text{ V}$
$I_{DD}$	0.003			$\mu\text{A}$ typ $\mu\text{A}$ max	Digital inputs = 0 V or 1.95 V
		1.0	4		

<sup>1</sup> Guaranteed by design, not subject to production test.

## ABSOLUTE MAXIMUM RATINGS

$T_A = 25^\circ\text{C}$ , unless otherwise noted.

Table 4.

Parameter	Rating
$V_{DD}$ to GND	–0.3 V to +4.6 V
Analog Inputs <sup>1</sup>	–0.3 V to $V_{DD} + 0.3$ V
Digital Inputs <sup>1</sup>	–0.3 V to 4.6 V or 10 mA, whichever occurs first
Peak Current, S or D	
3.3 V Operation	500 mA
2.5 V Operation	460 mA
1.8 V Operation	420 mA (pulsed at 1ms, 10% duty cycle max)
Continuous Current, S or D	
3.3 V Operation	300 mA
2.5 V Operation	275 mA
1.8 V Operation	250 mA
Operating Temperature Range	
Automotive (Y Version)	–40°C to +125°C
Storage Temperature Range	–65°C to +150°C
Junction Temperature	150°C
Thermal Impedance	
MSOP	
$\theta_{JA}$	206°C/W
$\theta_{JC}$	44°C/W
LFCSP	
$\theta_{JA}$ (3-Layer Board)	61.1°C/W
IR Reflow, Peak Temperature <20 sec	235°C

<sup>1</sup> Overvoltages at IN, S, or D are clamped by internal diodes. Current should be limited to the maximum ratings given.

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

Only one absolute maximum rating may be applied at any one time.

Table 5. Truth Table

Logic	Switch A	Switch B
0	Off	On
1	On	Off

### ESD CAUTION



**ESD (electrostatic discharge) sensitive device.** Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

## PIN CONFIGURATIONS AND FUNCTION DESCRIPTIONS

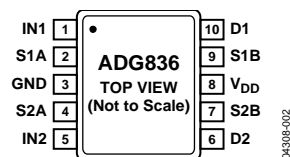
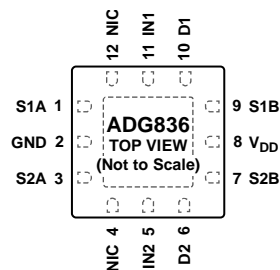


Figure 2. 10-Lead MSOP Pin Configuration (RM-10)



## NOTES

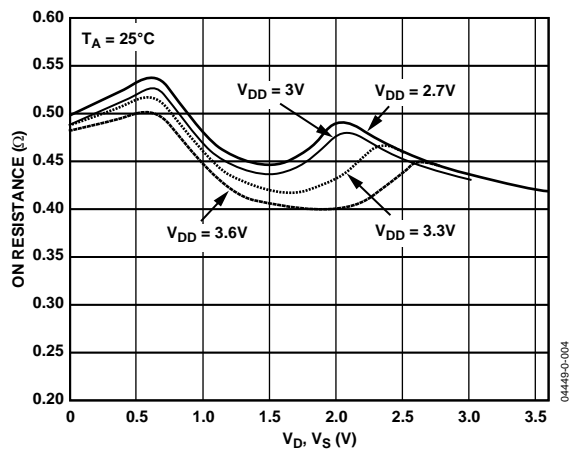
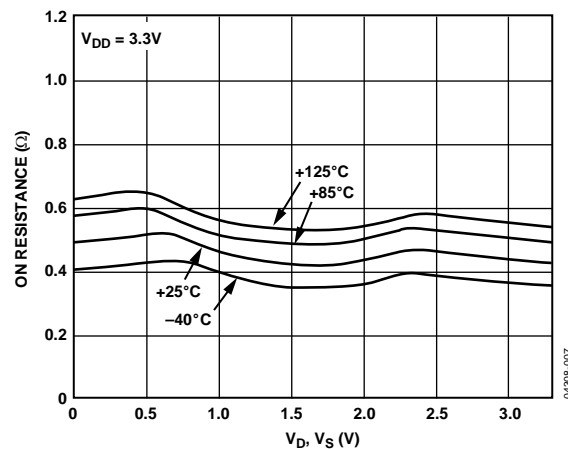
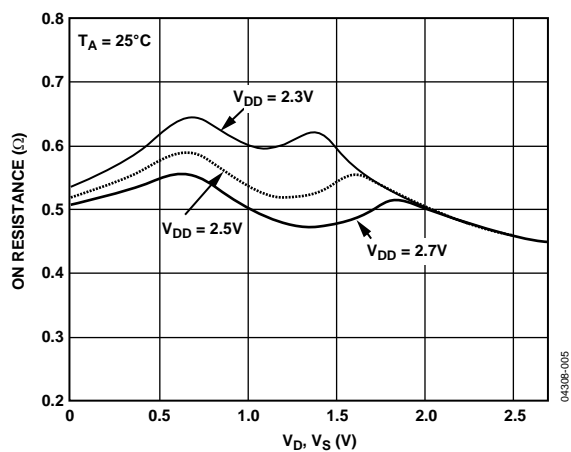
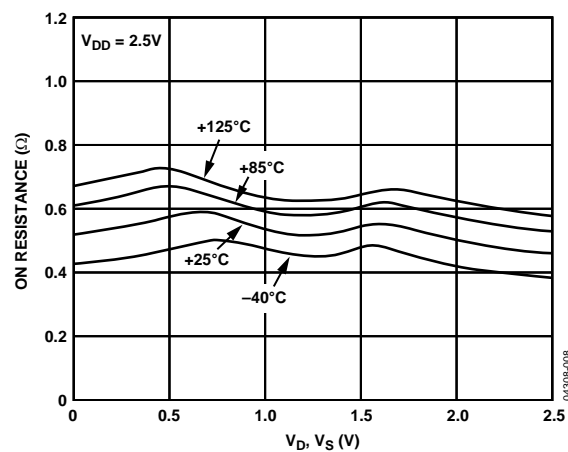
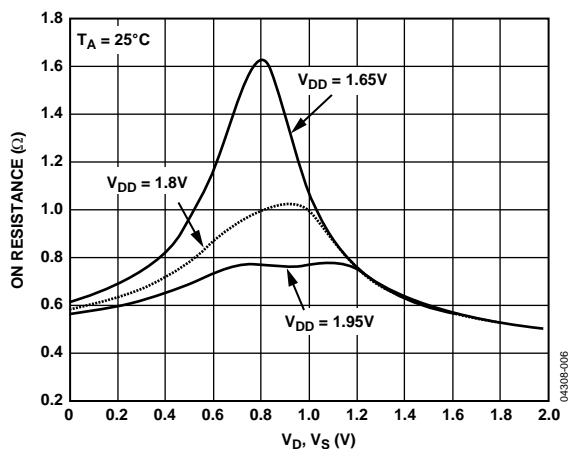
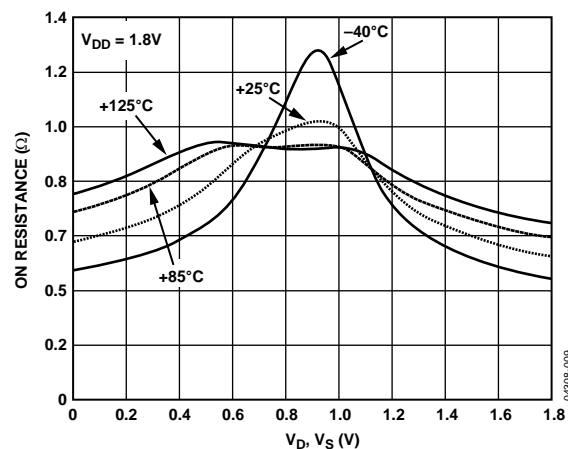
1. NIC = NO INTERNAL CONNECTION.
2. IT IS RECOMMENDED THAT THE EXPOSED PAD BE THERMALLY CONNECTED TO A COPPER PLANE FOR ENHANCED THERMAL PERFORMANCE. THE EXPOSED PAD SHOULD BE GROUNDED AS WELL.

Figure 3. 12-Lead LFCSP Pin Configuration (CP-12-4)

Table 6. Pin Function Descriptions

Pin No.		Mnemonic	Description
MSOP	LFCSP		
1, 5	11, 5	IN1, IN2	Logic Control Inputs.
2, 4, 7, 9	1, 3, 7, 9	S1A, S2A, S2B, S1B	Source Terminals. Can be inputs or outputs.
3	2	GND	Ground (0 V) Reference.
6, 10	6, 10	D2, D1	Drain Terminals. Can be inputs or outputs.
8	8	V <sub>DD</sub>	Most Positive Power Supply Potential.
Not applicable	4, 12	NIC	No Internal Connection.
Not applicable	0	EPAD	Exposed Pad. It is recommended that the exposed pad be thermally connected to a copper plane for enhanced thermal performance. The exposed pad should be grounded as well.

## TYPICAL PERFORMANCE CHARACTERISTICS

Figure 4. On Resistance vs.  $V_D$  ( $V_S$ ),  $V_{DD} = 2.7$  V to 3.6 VFigure 7. On Resistance vs.  $V_D$  ( $V_S$ ) for Different Temperatures, 3.3 VFigure 5. On Resistance vs.  $V_D$  ( $V_S$ ),  $V_{DD} = 2.5$  V to 0.2 VFigure 8. On Resistance vs.  $V_D$  ( $V_S$ ) for Different Temperatures, 2.5 VFigure 6. On Resistance vs.  $V_D$  ( $V_S$ ),  $V_{DD} = 1.8 \pm 3.6$ Figure 9. On Resistance vs.  $V_D$  ( $V_S$ ) for Different Temperatures, 1.8 V



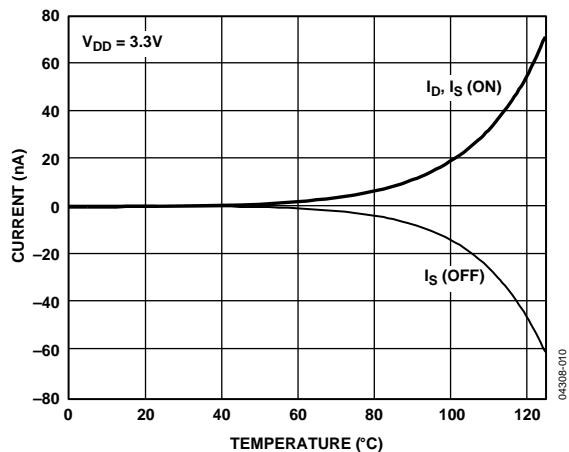


Figure 10. Leakage Current vs. Temperature, 3.3 V

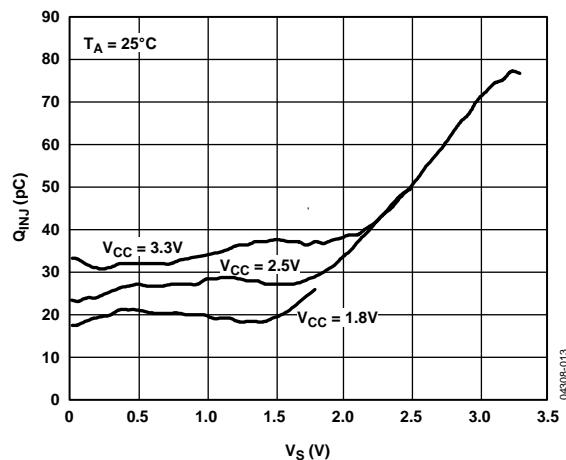


Figure 13. Charge Injection vs. Source Voltage

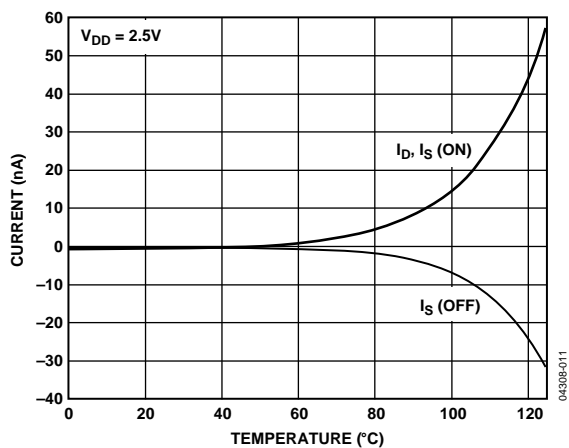


Figure 11. Leakage Current vs. Temperature, 2.5 V

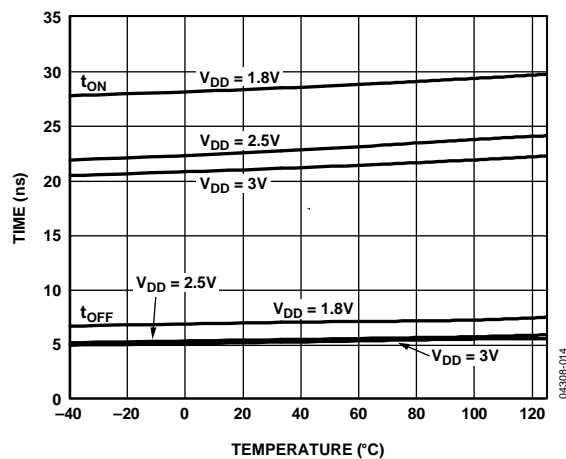
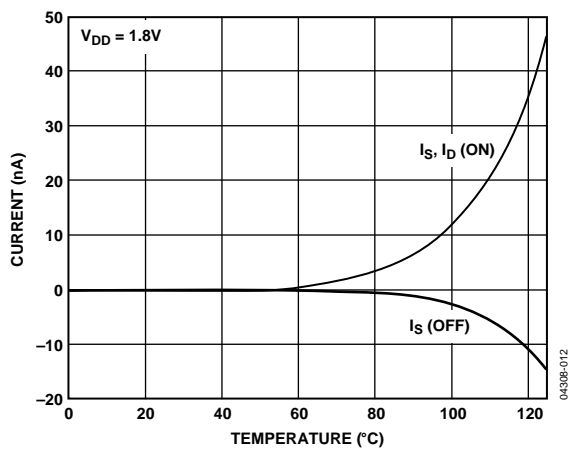
Figure 14.  $t_{ON}/t_{OFF}$  Times vs. Temperature

Figure 12. Leakage Current vs. Temperature, 1.8 V

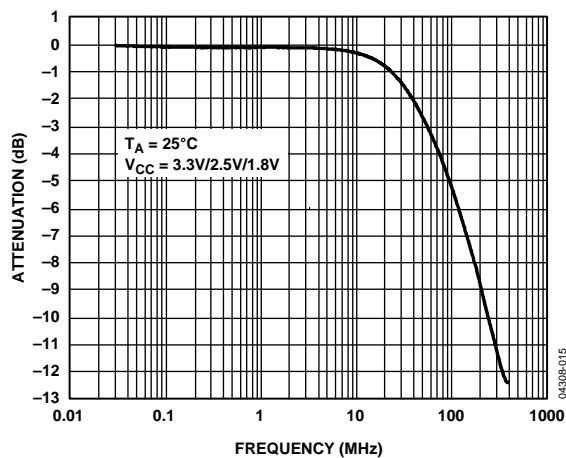


Figure 15. Bandwidth

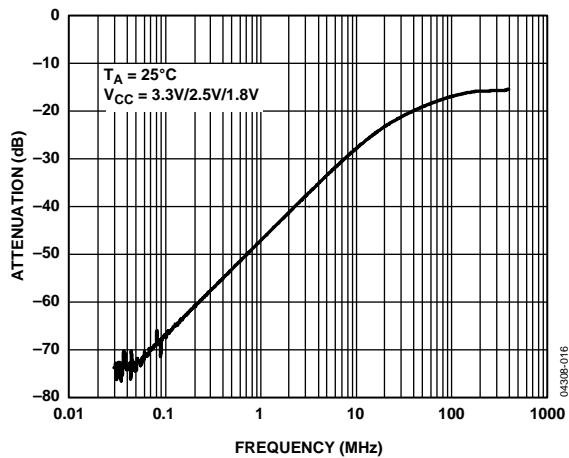


Figure 16. Off Isolation vs. Frequency

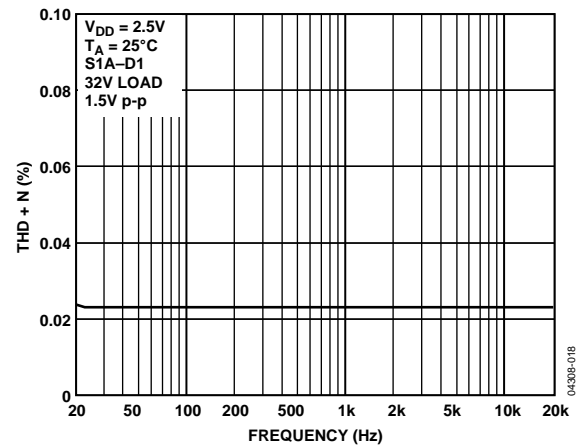


Figure 18. THD + N

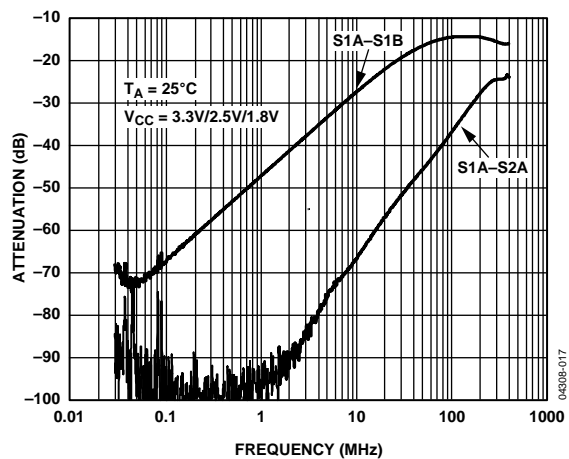


Figure 17. Crosstalk vs. Frequency

## TEST CIRCUITS

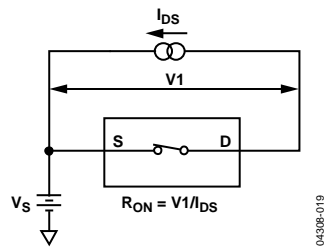


Figure 19. On Resistance

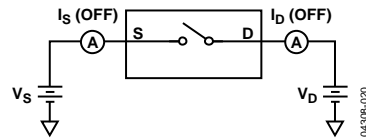


Figure 20. Off Leakage

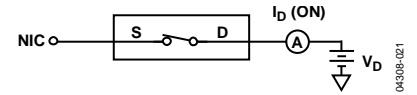


Figure 21. On Leakage

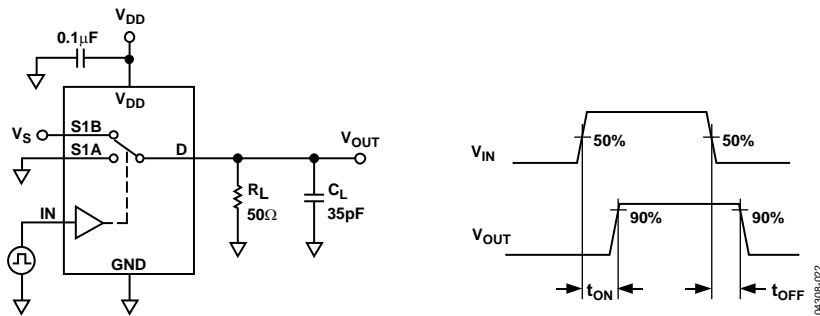
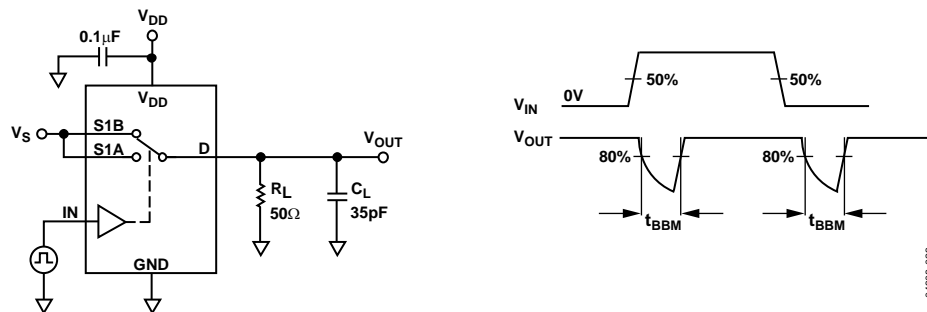
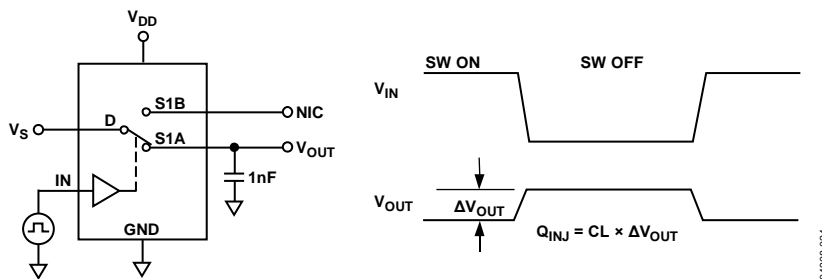
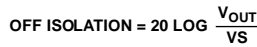
Figure 22. Switching Times,  $t_{ON}$ ,  $t_{OFF}$ Figure 23. Break-Before-Make Time Delay,  $t_{BBM}$ 

Figure 24. Charge Injection



04308-025



04308-027



04308-026



04308-028

## TERMINOLOGY

**I<sub>DD</sub>**

Positive supply current.

**V<sub>D</sub> (V<sub>S</sub>)**

Analog voltage on Terminal D and Terminal S.

**R<sub>ON</sub>**

Ohmic resistance between Terminal D and Terminal S.

**R<sub>FLAT</sub> (ON)**

Flatness is defined as the difference between the maximum and minimum value of on resistance as measured over the specified analog signal range.

**ΔR<sub>ON</sub>**

On-resistance match between any two channels.

**I<sub>S</sub> (OFF)**

Source leakage current with the switch off.

**I<sub>D</sub> (OFF)**

Drain leakage current with the switch off.

**I<sub>D</sub>, I<sub>S</sub> (ON)**

Channel leakage current with the switch on.

**V<sub>INL</sub>**

Maximum input voltage for Logic 0.

**V<sub>INH</sub>**

Minimum input voltage for Logic 1.

**I<sub>INL</sub> (I<sub>INH</sub>)**

Input current of the digital input.

**C<sub>S</sub> (OFF)**

Off switch source capacitance. Measured with reference to ground.

**C<sub>D</sub> (OFF)**

Off switch drain capacitance. Measured with reference to ground.

**C<sub>D</sub>, C<sub>S</sub> (ON)**

On switch capacitance. Measured with reference to ground.

**C<sub>IN</sub>**

Digital input capacitance.

**t<sub>ON</sub>**

Delay time between the 50% and the 90% points of the digital input and switch on condition.

**t<sub>OFF</sub>**

Delay time between the 50% and the 90% points of the digital input and switch off condition.

**t<sub>BBM</sub>**

On or off time measured between the 80% points of both switches when switching from one to another.

**Charge Injection**

A measure of the glitch impulse transferred from the digital input to the analog output during on-off switching.

**Off Isolation**

A measure of unwanted signal coupling through an off switch.

**Crosstalk**

A measure of unwanted signal, which is coupled through from one channel to another as a result of parasitic capacitance.

**–3 dB Bandwidth**

The frequency at which the output is attenuated by 3 dB.

**On Response**

The frequency response of the on switch.

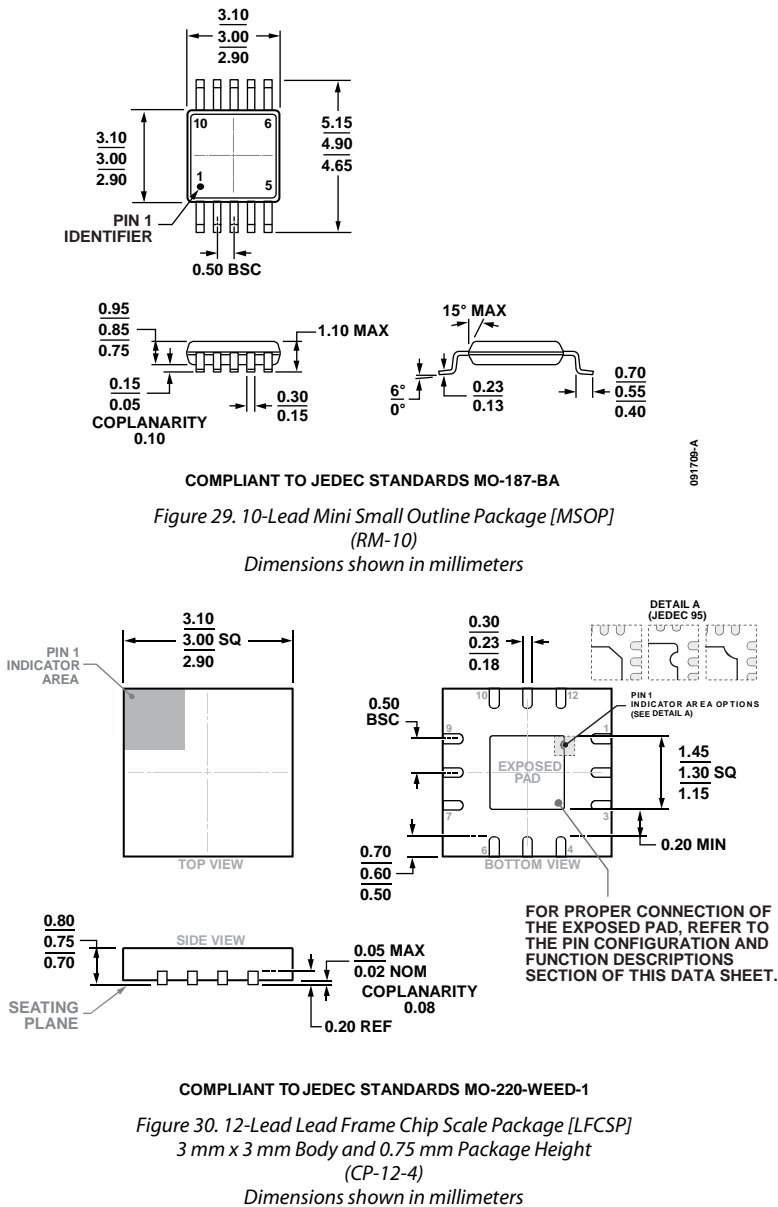
**Insertion Loss**

The loss due to the on resistance of the switch.

**Total Harmonic Distortion Plus Noise (THD + N)**

The ratio of the harmonics amplitude plus the noise of a signal to the fundamental.

## OUTLINE DIMENSIONS



## ORDERING GUIDE

Model <sup>1</sup>	Temperature Range	Package Description	Package Option	Branding <sup>2</sup>
ADG836YRM	−40°C to +125°C	10-Lead Mini Small Outline Package [MSOP]	RM-10	S9A
ADG836YRMZ	−40°C to +125°C	10-Lead Mini Small Outline Package [MSOP]	RM-10	S05
ADG836YRMZ-REEL	−40°C to +125°C	10-Lead Mini Small Outline Package [MSOP]	RM-10	S05
ADG836YRMZ-REEL7	−40°C to +125°C	10-Lead Mini Small Outline Package [MSOP]	RM-10	S05
ADG836YCPZ-REEL7	−40°C to +125°C	12-Lead Lead Frame Chip Scale Package [LFCSP]	CP-12-4	S05

<sup>1</sup> Z = RoHS Compliant Part.<sup>2</sup> Branding on this package is limited to three characters due to space constraints.

## NOTES

**NOTES**



# Mouser Electronics

Authorized Distributor

Click to View Pricing, Inventory, Delivery & Lifecycle Information:

[Analog Devices Inc.:](#)

[ADG836YRM](#)