

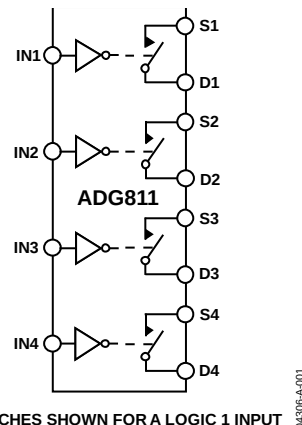
FEATURES

0.5 Ω typical on resistance
0.8 Ω maximum on resistance at 125°C
1.65 V to 3.6 V operation
Automotive temperature range: -40°C to +125°C
High current carrying capability: 300 mA continuous
Rail-to-rail switching operation
Fast switching times: <25 ns
Typical power consumption <0.1 μ W

APPLICATIONS

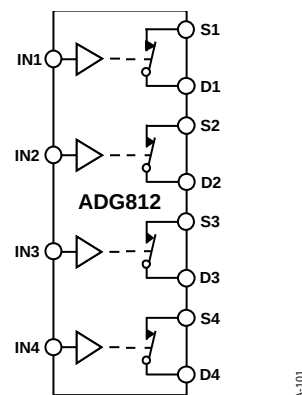
Cellular phones
MP3 players
Power routing
Battery-powered systems
PCMCIA cards
Modems
Audio and video signal routing
Communications systems

FUNCTIONAL BLOCK DIAGRAMS



SWITCHES SHOWN FOR A LOGIC 1 INPUT

Figure 1.



SWITCHES SHOWN FOR A LOGIC 1 INPUT

Figure 2.

GENERAL DESCRIPTION

The **ADG811/ADG812** are low voltage complementary metal-oxide semiconductor (CMOS) devices containing four independently selectable switches. These switches offer an ultralow on resistance of less than 0.8 Ω over the full temperature range. The digital inputs can handle 1.8 V logic with a 2.7 V to 3.6 V supply.

These devices contain four independent single-pole/single-throw (SPST) switches. The **ADG811** and **ADG812** differ only in that the digital control logic is inverted. The **ADG811** switches are turned on with a logic low on the appropriate control input, while a logic high is required to turn on the switches of the **ADG812**. Each switch conducts equally well in both directions when on and has an input signal range that extends to the supplies.

The **ADG811/ADG812** are fully specified for 3.3 V, 2.5 V, and 1.8 V supply operation. The **ADG811** is available in a 16-lead LFCSP, and the **ADG812** is available in a 16-lead TSSOP.

PRODUCT HIGHLIGHTS

1. <0.8 Ω on resistance over the full temperature range of -40°C to +125°C.
2. Single 1.65 V to 3.6 V operation.
3. Operational with 1.8 V CMOS logic.
4. High current handling capability (300 mA continuous current at 3.3 V).
5. Low total harmonic distortion plus noise (THD + N) (0.02% typical).
6. Small, 3 mm $\times$ 3 mm, 16-lead LFCSP and 16-lead TSSOP.

Rev. D

Document Feedback

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REVISION HISTORY

8/2020—Rev. C to Rev. D

Changes to Table 1	3
Changes to Table 2	4
Changes to Table 3	5

7/2016—Rev. B to Rev. C

Deleted ADG813	Universal
Changed CP-16-2 to CP-16-21.....	Throughout
Changes to Figure 1.....	1
Added Figure 2; Renumbered Sequentially	1
Deleted Table 6; Renumbered Sequentially	6
Changes to Figure 3 and Table 6.....	7
Changes to Figure 4 and Table 7.....	8
Change to Figure 16 Caption.....	10
Deleted Figure 23; Renumbered Sequentially	11
Updated Outline Dimensions.....	14
Changes to Ordering Guide.....	14

Pin Configurations and Function Descriptions.....	7
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Terminology.....	14
Outline Dimensions.....	15
Ordering Guide	15

11/2009—Rev. A to Rev. B

Added 16-Lead LFCSP	Universal
Changes to Table 4.....	6
Changes to Pin Configurations and Function Descriptions Section.....	7
Moved Terminology Section	13
Updated Outline Dimensions	14
Changes to Ordering Guide.....	15

5/2004—Rev. 0 to Rev. A

Updated Format	Universal
Updated Package Choices	Universal

11/2003—Revision 0: Initial Version

SPECIFICATIONS

$V_{DD} = 2.7\text{ V to }3.6\text{ V}$, $GND = 0\text{ V}$, unless otherwise noted. The temperature range for the Y version is $-40^{\circ}\text{C to }+125^{\circ}\text{C}$.

Table 1.

Parameter	+25°C	−40°C to +85°C	−40°C to +125°C	Unit	Test Conditions/Comments
ANALOG SWITCH					
Analog Signal Range			0 V to V_{DD}	V	
On Resistance, R_{ON}	0.5			Ω typ	$V_{DD} = 2.7\text{ V}$, $V_S = 0\text{ V to }V_{DD}$, $I_S = 10\text{ mA}$; see Figure 20
	0.75	0.85	0.9	Ω max	
On-Resistance Match Between Channels, ΔR_{ON}	0.04			Ω typ	$V_{DD} = 2.7\text{ V}$, $V_S = 0.5\text{ V}$, $I_S = 10\text{ mA}$
	0.095	0.095	0.1	Ω max	
On-Resistance Flatness, $R_{FLAT(ON)}$	0.1			Ω typ	$V_{DD} = 2.7\text{ V}$, $V_S = 0\text{ V to }V_{DD}$, $I_S = 10\text{ mA}$
	0.18	0.18	0.19	Ω max	
LEAKAGE CURRENTS					
Source Off Leakage, I_S (Off)	± 0.2			nA typ	$V_{DD} = 3.6\text{ V}$ $V_S = 0.6\text{ V}/3.3\text{ V}$, $V_D = 3.3\text{ V}/0.6\text{ V}$; see Figure 21
	± 1	± 8	± 80	nA max	
Drain Off Leakage, I_D (Off)	± 0.2			nA typ	$V_S = 0.6\text{ V}/3.3\text{ V}$, $V_D = 3.3\text{ V}/0.6\text{ V}$; see Figure 21
	± 1	± 8	± 80	nA max	
Channel On Leakage, I_D , I_S (On)	± 0.2			nA typ	$V_S = V_D = 0.6\text{ V or }3.3\text{ V}$; see Figure 22
	± 1	± 15	± 90	nA max	
DIGITAL INPUTS					
Input High Voltage, V_{INH}			2	V min	
Input Low Voltage, V_{INL}			0.8	V max	
Input Current, I_{INL} or I_{INH}	0.005		± 0.1	$\mu\text{A typ}$ $\mu\text{A max}$	$V_{IN} = V_{INL}$ or V_{INH}
Digital Input Capacitance, C_{IN}	6			pF typ	
DYNAMIC CHARACTERISTICS¹					
t_{ON}	21 25	26	28	ns typ ns max	$R_L = 50\ \Omega$, $C_L = 35\text{ pF}$ $V_S = 1.5\text{ V}/0\text{ V}$; see Figure 23
t_{OFF}	4 5	6	7	ns typ ns max	$R_L = 50\ \Omega$, $C_L = 35\text{ pF}$ $V_S = 1.5\text{ V}$; see Figure 23
Charge Injection	30			pC typ	$V_S = 1.5\text{ V}$, $R_S = 0\ \Omega$, $C_L = 1\text{ nF}$; see Figure 24
Off Isolation	−67			dB typ	$R_L = 50\ \Omega$, $C_L = 5\text{ pF}$, $f = 100\text{ kHz}$; see Figure 25
Channel-to-Channel Crosstalk	−90			dB typ	$R_L = 50\ \Omega$, $C_L = 5\text{ pF}$, $f = 100\text{ kHz}$; see Figure 27
Total Harmonic Distortion Plus Noise (THD + N)	0.02			%	$R_L = 32\ \Omega$, $f = 20\text{ Hz to }20\text{ kHz}$, $V_S = 2\text{ V p-p}$
Insertion Loss	−0.05			dB typ	$R_L = 50\ \Omega$, $C_L = 5\text{ pF}$, $f = 100\text{ kHz}$
−3 dB Bandwidth	90			MHz typ	$R_L = 50\ \Omega$, $C_L = 5\text{ pF}$; see Figure 26
C_S (Off)	30			pF typ	
C_D (Off)	35			pF typ	
C_D , C_S (On)	60			pF typ	
POWER REQUIREMENTS					
I_{DD}	0.003	1.0	4	$\mu\text{A typ}$ $\mu\text{A max}$	$V_{DD} = 3.6\text{ V}$ Digital inputs = 0 V or 3.6 V

¹ Guaranteed by design, but not subject to production test.

$V_{DD} = 2.5 \text{ V} \pm 0.2 \text{ V}$, $GND = 0 \text{ V}$, unless otherwise noted. The temperature range for the Y version is -40°C to $+125^{\circ}\text{C}$.

Table 2.

Parameter	+25°C	−40°C to +85°C	−40°C to +125°C	Unit	Test Conditions/Comments
ANALOG SWITCH					
Analogue Signal Range			0 V to V_{DD}	V	
On Resistance, R_{ON}	0.65			Ω typ	$V_{DD} = 2.3 \text{ V}$, $V_S = 0 \text{ V}$ to V_{DD} , $I_S = 10 \text{ mA}$; see Figure 20
On-Resistance Match Between Channels, ΔR_{ON}	0.84 0.04	0.92	1.0	Ω max Ω typ	$V_{DD} = 2.3 \text{ V}$, $V_S = 0.55 \text{ V}$, $I_S = 10 \text{ mA}$
On-Resistance Flatness, $R_{FLAT(ON)}$	0.1 0.16 0.25	0.1 0.25	0.105 0.26	Ω max Ω typ Ω max	$V_{DD} = 2.3 \text{ V}$, $V_S = 0 \text{ V}$ to V_{DD} , $I_S = 10 \text{ mA}$
LEAKAGE CURRENTS					
Source Off Leakage, I_S (Off)	± 0.2			nA typ	$V_{DD} = 2.7 \text{ V}$ $V_S = 0.6 \text{ V}/2.4 \text{ V}$, $V_D = 2.4 \text{ V}/0.6 \text{ V}$; see Figure 21
Drain Off Leakage, I_D (Off)	± 1 ± 0.2	± 6	± 35	nA max nA typ	$V_S = 0.6 \text{ V}/2.4 \text{ V}$, $V_D = 2.4 \text{ V}/0.6 \text{ V}$; see Figure 21
Channel On Leakage, I_D , I_S (On)	± 1 ± 0.2 ± 1	± 6 ± 11	± 35 ± 70	nA max nA typ nA max	$V_S = V_D = 0.6 \text{ V}$ or 2.4 V ; see Figure 22
DIGITAL INPUTS					
Input High Voltage, V_{INH}			1.7	V min	
Input Low Voltage, V_{INL}			0.7	V max	
Input Current, I_{INL} or I_{INH}	0.005		± 0.1	μA typ μA max	$V_{IN} = V_{INL}$ or V_{INH}
Digital Input Capacitance, C_{IN}	6			pF typ	
DYNAMIC CHARACTERISTICS¹					
t_{ON}	22 27	29	30	ns typ ns max	$R_L = 50 \Omega$, $C_L = 35 \text{ pF}$ $V_S = 1.5 \text{ V}/0 \text{ V}$; see Figure 23
t_{OFF}	4 6	7	8	ns typ ns max	$R_L = 50 \Omega$, $C_L = 35 \text{ pF}$ $V_S = 1.5 \text{ V}$; see Figure 23
Charge Injection	25			pC typ	$V_S = 1.25 \text{ V}$, $R_S = 0 \Omega$, $C_L = 1 \text{ nF}$; see Figure 24
Off Isolation	−67			dB typ	$R_L = 50 \Omega$, $C_L = 5 \text{ pF}$, $f = 100 \text{ kHz}$; see Figure 25
Channel-to-Channel Crosstalk	−90			dB typ	$R_L = 50 \Omega$, $C_L = 5 \text{ pF}$, $f = 100 \text{ kHz}$; see Figure 27
Total Harmonic Distortion Plus Noise (THD + N)	0.022			%	$R_L = 32 \Omega$, $f = 20 \text{ Hz}$ to 20 kHz , $V_S = 1.5 \text{ V}$ p-p
Insertion Loss	−0.06			dB typ	$R_L = 50 \Omega$, $C_L = 5 \text{ pF}$, $f = 100 \text{ kHz}$
−3 dB Bandwidth	90			MHz typ	$R_L = 50 \Omega$, $C_L = 5 \text{ pF}$; see Figure 26
C_S (Off)	32			pF typ	
C_D (Off)	37			pF typ	
C_D , C_S (On)	60			pF typ	
POWER REQUIREMENTS					
I_{DD}	0.003	1.0	4	μA typ μA max	$V_{DD} = 2.7 \text{ V}$ Digital inputs = 0 V or 2.7 V

¹ Guaranteed by design, but not subject to production test.

$V_{DD} = 1.65\text{ V}$ to 1.95 V , $GND = 0\text{ V}$, unless otherwise noted. The temperature range for the Y version is -40°C to $+125^{\circ}\text{C}$.

Table 3.

Parameter	+25°C	−40°C to +85°C	−40°C to +125°C	Unit	Test Conditions/Comments
ANALOG SWITCH					
Analog Signal Range			0 V to V_{DD}	V	
On Resistance, R_{ON}	1			Ω typ	$V_{DD} = 1.8\text{ V}$, $V_S = 0\text{ V}$ to V_{DD} , $I_S = 10\text{ mA}$; see Figure 20
	1.6	2.4	2.4	Ω max	
	2.7	4.2	4.2	Ω max	$V_{DD} = 1.65\text{ V}$, $V_S = 0\text{ V}$ to V_{DD} , $I_S = 10\text{ mA}$
On-Resistance Match Between Channels, ΔR_{ON}	0.1			Ω typ	$V_{DD} = 1.65\text{ V}$, $V_S = 0.7\text{ V}$, $I_S = 10\text{ mA}$
LEAKAGE CURRENTS					
Source Off Leakage I_S (Off)	± 0.2			nA typ	$V_{DD} = 1.95\text{ V}$ $V_S = 0.6\text{ V}/1.65\text{ V}$, $V_D = 1.65\text{ V}/0.6\text{ V}$; see Figure 21
Drain Off Leakage I_D (Off)	± 1 ± 0.2	± 5	± 30	nA max nA typ	$V_S = 0.6\text{ V}/1.65\text{ V}$, $V_D = 1.65\text{ V}/0.6\text{ V}$; see Figure 21
Channel On Leakage I_D , I_S (On)	± 1 ± 0.2 ± 1	± 5 ± 9	± 30 ± 60	nA max nA typ nA max	$V_S = V_D = 0.6\text{ V}$ or 1.65 V ; see Figure 22
DIGITAL INPUTS					
Input High Voltage, V_{INH}			$0.65V_{DD}$	V min	
Input Low Voltage, V_{INL}			$0.35V_{DD}$	V max	
Input Current, I_{INL} or I_{INH}	0.005		± 0.1	μA typ μA max	$V_{IN} = V_{INL}$ or V_{INH}
Digital Input Capacitance, C_{IN}	6			pF typ	
DYNAMIC CHARACTERISTICS ¹					
t_{ON}	27 35	36	37	ns typ ns max	$R_L = 50\ \Omega$, $C_L = 35\text{ pF}$ $V_S = 1.5\text{ V}/0\text{ V}$; see Figure 23
t_{OFF}	6 8	9	10	ns typ ns max	$R_L = 50\ \Omega$, $C_L = 35\text{ pF}$ $V_S = 1.5\text{ V}$; see Figure 23
Charge Injection	15			pC typ	$V_S = 1\text{ V}$, $R_S = 0\ \Omega$, $C_L = 1\text{ nF}$; see Figure 24
Off Isolation	−67			dB typ	$R_L = 50\ \Omega$, $C_L = 5\text{ pF}$, $f = 100\text{ kHz}$; Figure 25
Channel-to-Channel Crosstalk	−90			dB typ	$R_L = 50\ \Omega$, $C_L = 5\text{ pF}$, $f = 100\text{ kHz}$; see Figure 27
Total Harmonic Distortion Plus Noise (THD + N)	0.14			%	$R_L = 32\ \Omega$, $f = 20\text{ Hz}$ to 20 kHz , $V_S = 1.2\text{ V p-p}$
Insertion Loss	−0.08			dB typ	$R_L = 50\ \Omega$, $C_L = 5\text{ pF}$, $f = 100\text{ kHz}$
−3 dB Bandwidth	90			MHz typ	$R_L = 50\ \Omega$, $C_L = 5\text{ pF}$; see Figure 26
C_S (Off)	32			pF typ	
C_D (Off)	38			pF typ	
C_D , C_S (On)	60			pF typ	
POWER REQUIREMENTS					
I_{DD}	0.003	1.0	4	μA typ μA max	$V_{DD} = 1.95\text{ V}$ Digital inputs = 0 V or 1.95 V

¹ Guaranteed by design, but not subject to production test.

ABSOLUTE MAXIMUM RATINGS

$T_A = 25^\circ\text{C}$, unless otherwise noted.

Table 4.

Parameter	Rating
V_{DD} to GND	–0.3 V to +4.6 V
Analog Inputs ¹	–0.3 V to $V_{DD} + 0.3$ V
Digital Inputs ¹	GND – 0.3 V to 4.6 V or 10 mA, whichever occurs first
Peak Current, S or D	(Pulsed at 1 ms, 10% duty-cycle maximum)
3.3 V Operation	500 mA
2.5 V Operation	460 mA
1.8 V Operation	420 mA
Continuous Current, S or D	
3.3 V Operation	300 mA
2.5 V Operation	275 mA
1.8 V Operation	250 mA
Operating Temperature Range, Automotive (Y Version)	–40°C to +125°C
Storage Temperature Range	–65°C to +150°C
Junction Temperature	150°C
Thermal Impedance	
TSSOP	
θ_{JA}	150°C/W
θ_{JC}	27°C/W
LFCSP	
θ_{JA}	70°C/W
IR Reflow, Peak Temperature <20 sec	235°C

¹ Overvoltages at IN, S, or D are clamped by internal diodes. Current should be limited to the maximum ratings given.

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

Only one absolute maximum rating may be applied at any one time.

Table 5. ADG811/ADG812 Truth Table

ADG811 IN	ADG812 IN	Switch Condition
0	1	On
1	0	Off

ESD CAUTION



ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATIONS AND FUNCTION DESCRIPTIONS

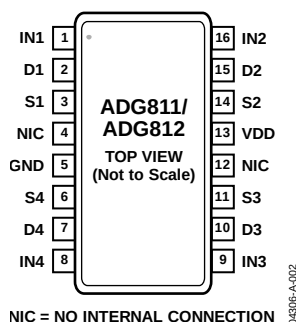
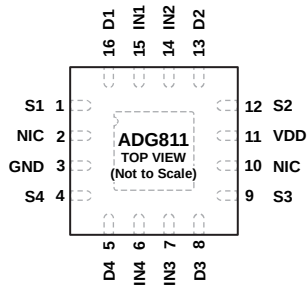


Figure 3. ADG811/ADG812 Pin Configuration (16-Lead TSSOP)

Table 6. ADG811/ADG812 Pin Function Descriptions (16-Lead TSSOP)

Pin No.		Mnemonic	Description
TSSOP	LFCSP		
1	15	IN1	Logic control input.
2	16	D1	Drain Terminal. This pin may be an input or output.
3	1	S1	Source Terminal. This pin may be an input or output.
4, 12	2, 10	NIC	No Internal Connection.
5	3	GND	Ground (0 V) reference.
6	4	S4	Source Terminal. This pin may be an input or output.
7	5	D4	Drain Terminal. This pin may be an input or output.
8	6	IN4	Logic Control Input.
9	7	IN3	Logic Control Input.
10	8	D3	Drain Terminal. This pin may be an input or output.
11	9	S3	Source Terminal. This pin may be an input or output.
13	11	VDD	Most Positive Power Supply Potential.
14	12	S2	Source Terminal. This pin may be an input or output.
15	13	D2	Drain Terminal. This pin may be an input or output.
16	14	IN2	Logic Control Input.
Not applicable	17	EPAD	Exposed Pad. Connect exposed pad to GND.



NOTES
1. NIC = NO INTERNAL CONNECTION.
2. CONNECT EXPOSED PAD TO GND.

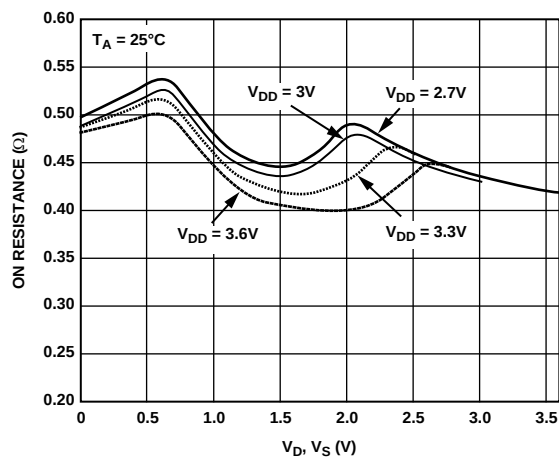
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Figure 4. ADG811 Pin Configuration (16-Lead LFCSP)

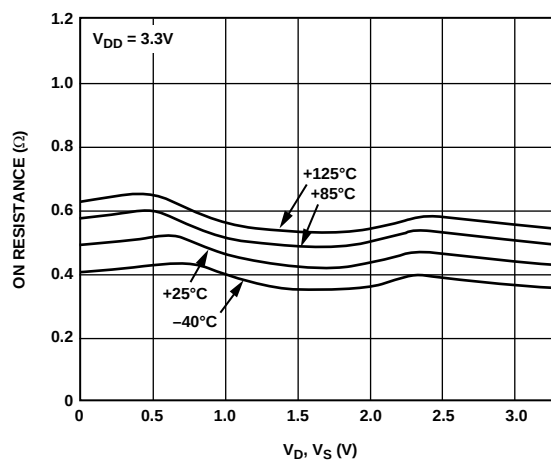
Table 7. ADG811 Pin Function Descriptions (16-Lead LFCSP)

Pin No.	Mnemonic	Description
1	S1	Source Terminal. This pin may be an input or output.
2, 10	NIC	No Internal Connection.
3	GND	Ground (0 V) reference.
4	S4	Source Terminal. This pin may be an input or output.
5	D4	Drain Terminal. This pin may be an input or output.
6	IN4	Logic Control Input.
7	IN3	Logic Control Input.
8	D3	Drain Terminal. This pin may be an input or output.
9	S3	Source Terminal. This pin may be an input or output.
11	VDD	Most Positive Power Supply Potential.
12	S2	Source Terminal. This pin may be an input or output.
13	D2	Drain Terminal. This pin may be an input or output.
14	IN2	Logic Control Input.
15	IN1	Logic control input.
16	D1	Drain Terminal. This pin may be an input or output.
17	EPAD	Exposed Pad. Connect exposed pad to GND.

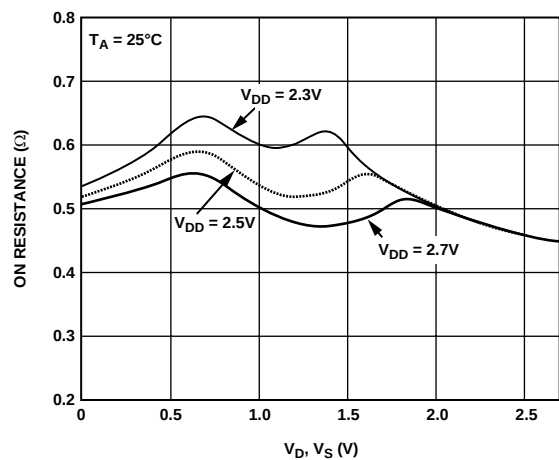
TYPICAL PERFORMANCE CHARACTERISTICS

Figure 5. On Resistance vs. V_D (V_S), $V_{DD} = 2.7$ V to 3.6 V

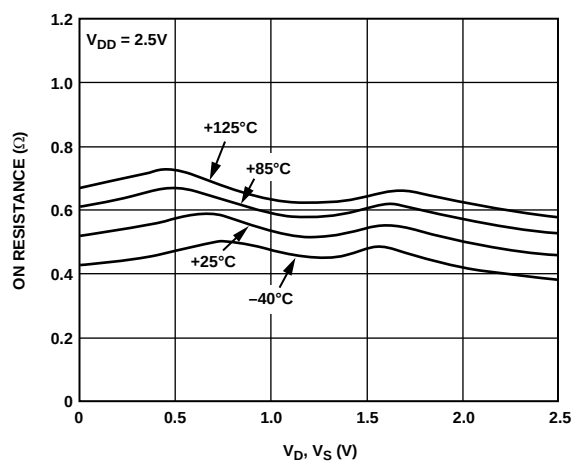
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Figure 8. On Resistance vs. V_D (V_S) for Different Temperatures, $V_{DD} = 3.3$ V

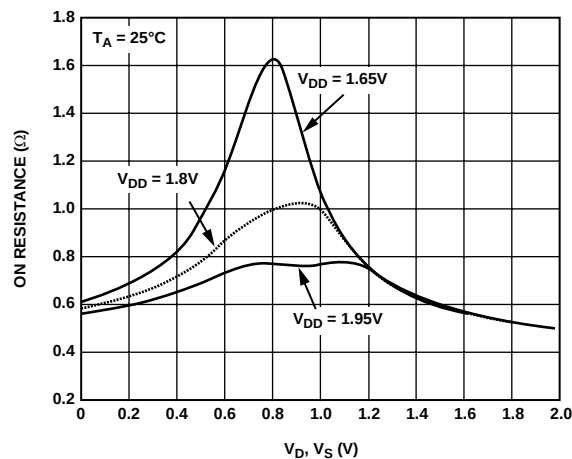
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Figure 6. On Resistance vs. V_D (V_S), $V_{DD} = 2.5$ V $\pm$ 0.2 V

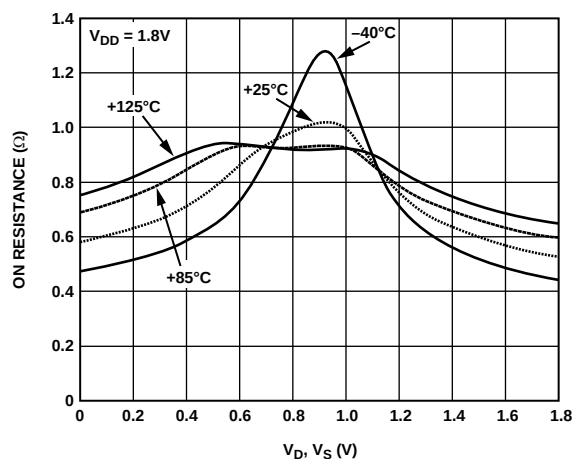
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Figure 9. On Resistance vs. V_D (V_S) for Different Temperatures, $V_{DD} = 2.5$ V

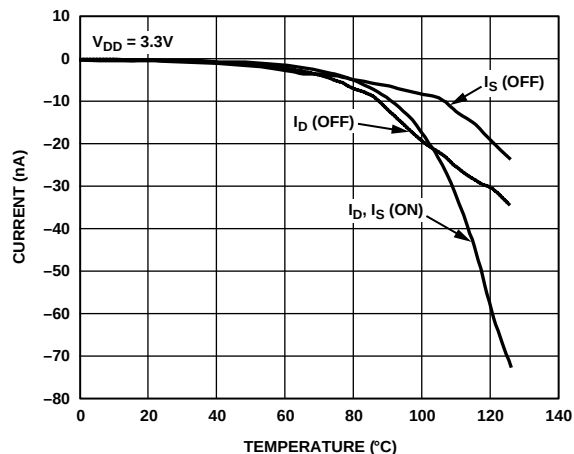
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Figure 7. On Resistance vs. V_D (V_S), $V_{DD} = 1.8$ V $\pm$ 0.15 V

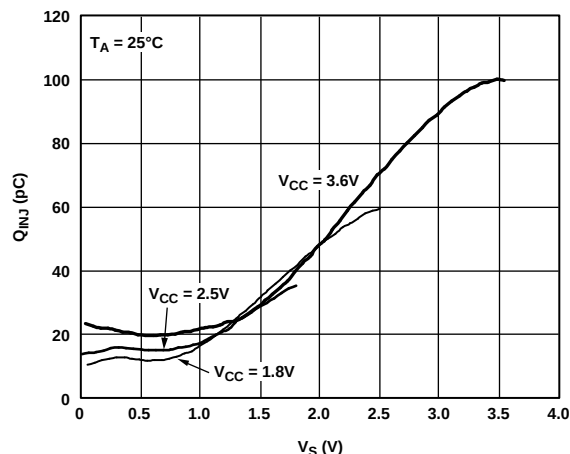
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Figure 10. On Resistance vs. V_D (V_S) for Different Temperatures, $V_{DD} = 1.8$ V

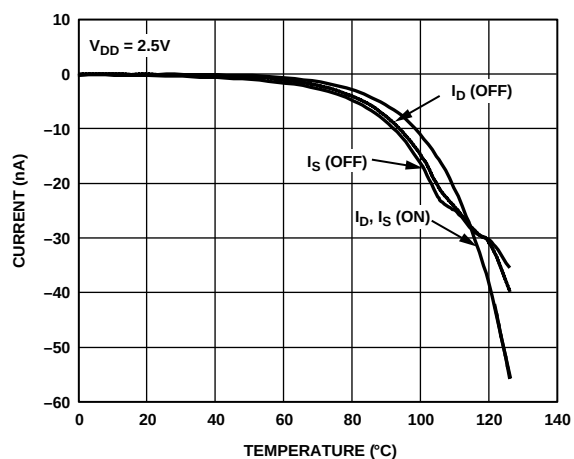
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Figure 11. Leakage Current vs. Temperature, $V_{DD} = 3.3V$

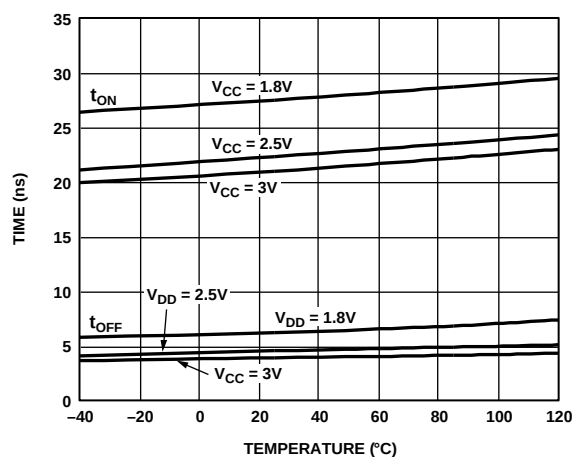
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Figure 14. Charge Injection (Q_{INJ}) vs. Source Voltage (V_S)

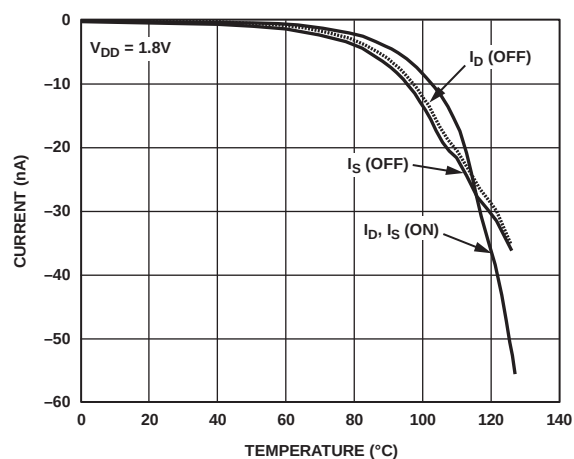
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Figure 12. Leakage Current vs. Temperature, $V_{DD} = 2.5V$

04306-A-010

Figure 15. t_{ON}/t_{OFF} Times vs. Temperature

04306-A-013

Figure 13. Leakage Current vs. Temperature, $V_{DD} = 1.8V$

04306-A-011

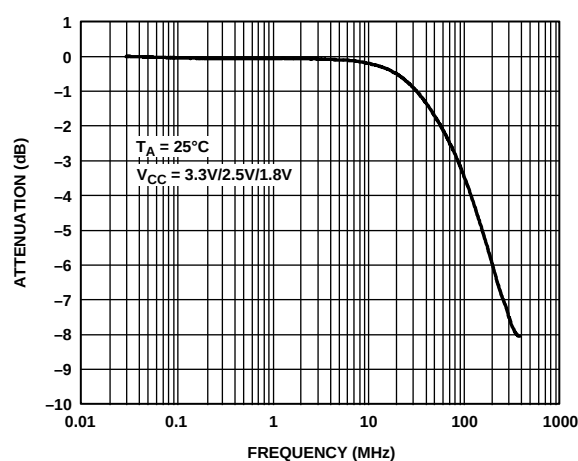


Figure 16. Bandwidth vs. Frequency

04306-A-014

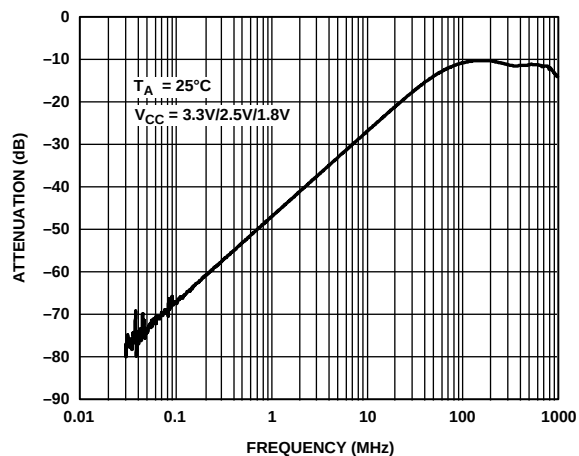


Figure 17. Crosstalk vs. Frequency

04306-A-015

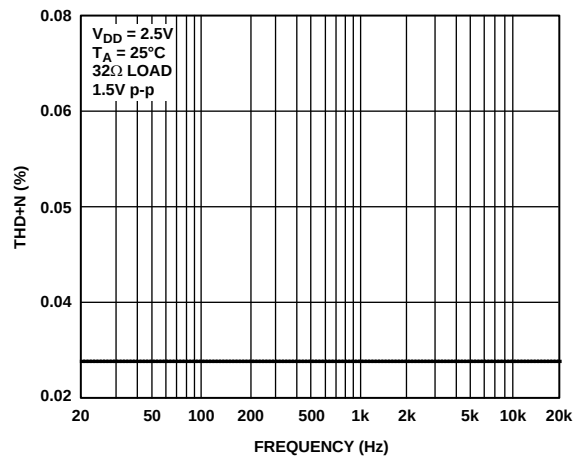


Figure 19. Total Harmonic Distortion Plus Noise (THD + N) vs. Frequency

04306-A-017

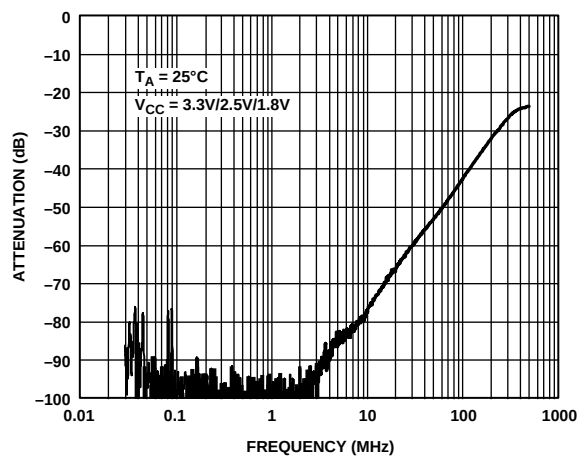


Figure 18. Off Isolation vs. Frequency

04306-A-016

TEST CIRCUITS

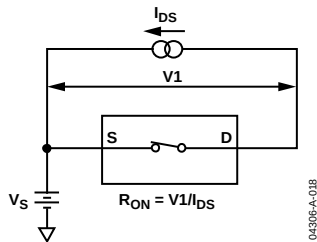


Figure 20. On Resistance

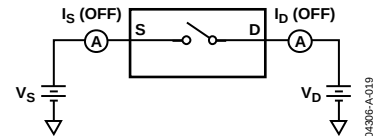


Figure 21. Off Leakage

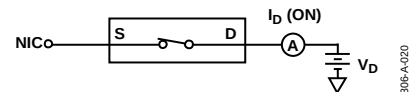


Figure 22. On Leakage

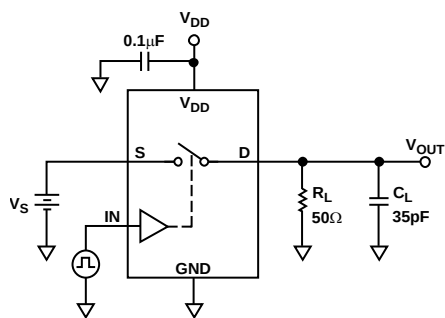


Figure 23. Switching Times

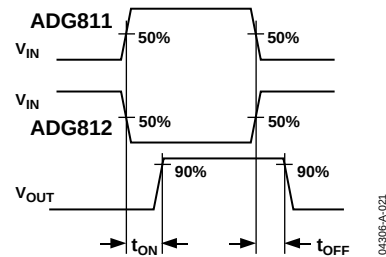


Figure 24. Charge Injection

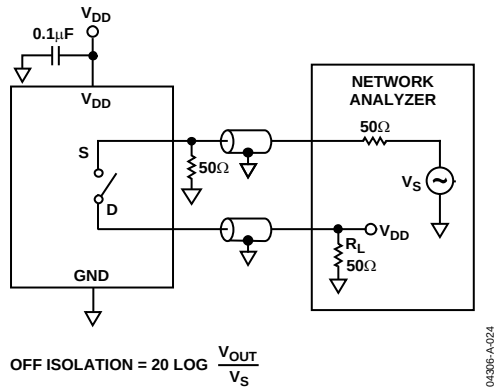


Figure 25. Off Isolation

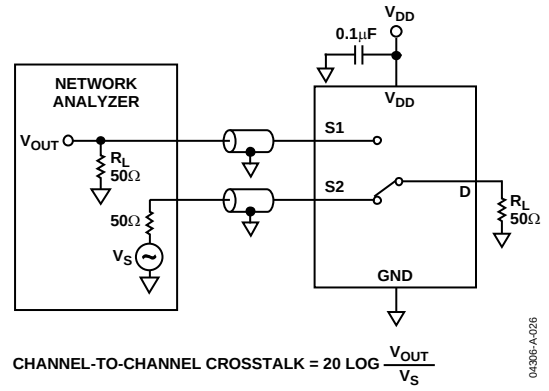


Figure 27. Channel-to-Channel Crosstalk

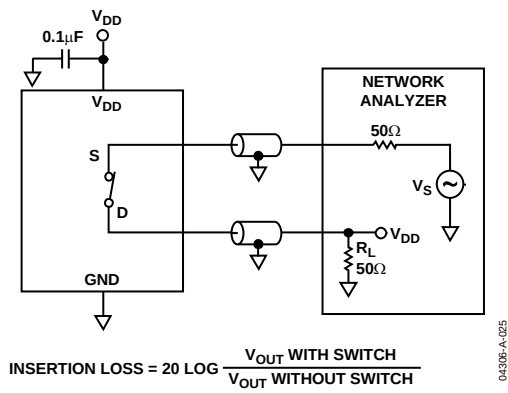


Figure 26. Bandwidth

TERMINOLOGY

I_{DD}

Positive supply current.

V_D, V_S

Analog voltage on Terminal D and Terminal S.

R_{ON}

Ohmic resistance between Terminal D and Terminal S.

R_{FLAT} (ON)

Flatness is defined as the difference between the maximum and minimum value of on resistance as measured over the specified analog signal range.

ΔR_{ON}

On-resistance match between any two channels, that is, R_{ON} maximum – R_{ON} minimum.

I_S (Off)

Source leakage current with the switch off.

I_D (Off)

Drain leakage current with the switch off.

I_D, I_S (On)

Channel leakage current with the switch on.

V_{INL}

Maximum input voltage for Logic 0.

V_{INH}

Minimum input voltage for Logic 1.

I_{INL} (I_{INH})

Input current of the digital input.

C_S (Off)

Off switch source capacitance. Measured with reference to ground.

C_D (Off)

Off switch drain capacitance. Measured with reference to ground.

C_D, C_S (On)

On switch capacitance. Measured with reference to ground.

C_{IN}

Digital input capacitance.

t_{ON}

Delay time between the 50% and the 90% points of the digital input and switch on condition.

t_{OFF}

Delay time between the 50% and the 90% points of the digital input and switch off condition.

t_{BEM}

On or off time measured between the 80% points of both switches, when switching from one to another.

Charge Injection

A measure of the glitch impulse transferred from the digital input to the analog output during on-to-off switching.

Off Isolation

A measure of unwanted signal coupling through an off switch.

Crosstalk

A measure of unwanted signal that is coupled through from one channel to another because of parasitic capacitance.

–3 dB Bandwidth

The frequency at which the output is attenuated by 3 dB.

On Response

The frequency response of the on switch.

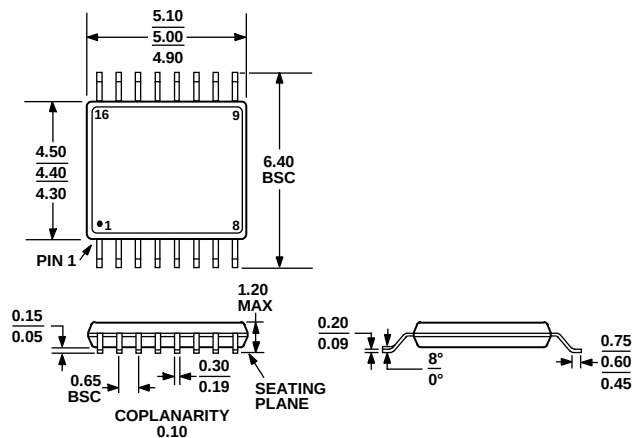
Insertion Loss

The loss due to the on resistance of the switch.

Total Harmonic Distortion Plus Noise (THD + N)

The ratio of the harmonic amplitudes plus the noise of a signal to the fundamental.

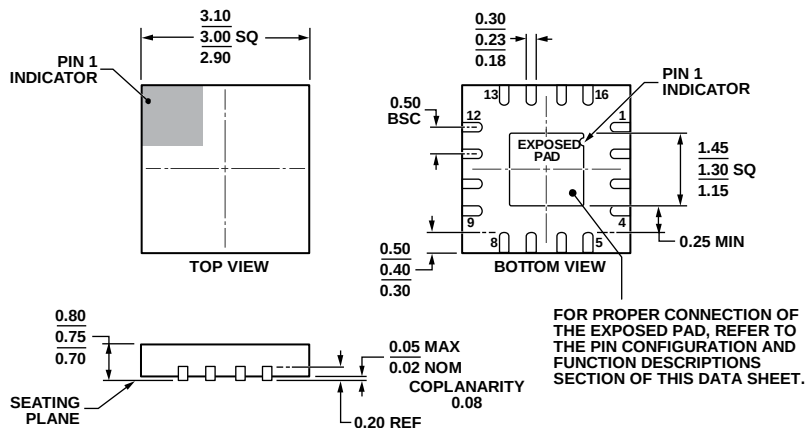
OUTLINE DIMENSIONS



COMPLIANT TO JEDEC STANDARDS MO-153-AB

Figure 28. 16-Lead Thin Shrink Small Outline Package [TSSOP]
(RU-16)

Dimensions shown in millimeters



COMPLIANT TO JEDEC STANDARDS MO-220-WEED.

Figure 29. 16-Lead Lead Frame Chip Scale Package [LFCSP]
3 mm × 3 mm Body and 0.75 mm Package Height
(CP-16-21)

Dimensions shown in millimeters

ORDERING GUIDE

Model ¹	Temperature Range	Package Description	Package Option
ADG811YRUZ	−40°C to +125°C	16-Lead Thin Shrink Small Outline [TSSOP]	RU-16
ADG811YCPZ-REEL7	−40°C to +125°C	16-Lead Lead Frame Chip Scale Package [LFCSP]	CP-16-21
ADG812YRUZ	−40°C to +125°C	16-Lead Thin Shrink Small Outline [TSSOP]	RU-16
ADG812YRUZ-REEL7	−40°C to +125°C	16-Lead Thin Shrink Small Outline [TSSOP]	RU-16

¹ Z = RoHS Compliant Part.

Mouser Electronics

Authorized Distributor

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