CMOS, ±5 V/+5 V, 4 Ω Dual SPST Switches

Data Sheet **ADG621**

FEATURES

- 5.5 Ω (maximum) on resistance
- 0.9 Ω (typical) on resistance flatness
- 2.7 V to 5.5 V single supply
- ±2.7 V to ±5.5 V dual supply
- Rail-to-rail operation
- 10-lead MSOP package
- Typical power consumption: <0.01 µW
- TTL-/CMOS-compatible inputs

APPLICATIONS

- Automatic test equipment
- Power routing
- Communication systems
- Data acquisition systems
- Sample-and-hold systems
- Avionics
- Relay replacements
- Battery-powered systems

GENERAL DESCRIPTION

The ADG621 is a monolithic, CMOS, single-pole, single-throw (SPST) switch. The ADG621 conducts equally well in both directions when on. The ADG621 contains two independent switches. The ADG621 is a normally open switch.

The ADG621 offers low on resistance of 4 Ω, which is matched to within 0.25 Ω between channels. The ADG621 also provides low power dissipation yet offers high switching speeds.

All digital inputs have 0.8 V to 2.4 V logic thresholds, ensuring TTL/CMOS compatibility when using single +5 V or dual ±5 V supplies. The ADG621 is available in a 10-lead MSOP package.

FUNCTIONAL BLOCK DIAGRAM

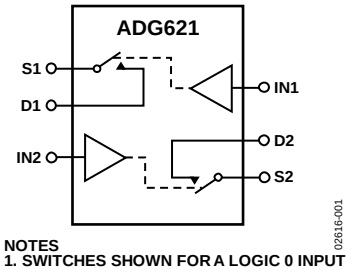

Figure 1.

PRODUCT HIGHLIGHTS

1. Low on resistance, R_{ON} (4 Ω typical).
2. Dual ±2.7 V to ±5.5 V or single +2.7 V to +5.5 V.
3. Low power dissipation; CMOS construction ensures low power dissipation.
4. Tiny 10-lead MSOP package.

Rev. C

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5/2017—Rev. B to Rev. C

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11/2001—Revision 0: Initial Version

SPECIFICATIONS

DUAL SUPPLY

V_{DD} = 5 V ± 10%, V_{SS} = −5 V ± 10%, GND = 0 V, unless otherwise noted.

Table 1.

Parameter	+25°C	−40°C to +85°C	Unit	Test Conditions/Comments
ANALOG SWITCH				
Analog Signal Range		V_{SS} to V_{DD}	V	V_{DD} = +4.5 V, V_{SS} = −4.5 V
On Resistance, R_{ON}	4		Ω typ	V_S = ±4.5 V, I_S = −10 mA, see Figure 14
	5.5	7	Ω max	
On Resistance Match Between Channels, ΔR_{ON}	0.25		Ω typ	V_S = ±4.5 V, I_S = −10 mA
	0.35	0.4	Ω max	
On Resistance Flatness, $R_{FLAT(ON)}$	0.9	0.9	Ω typ	V_S = ±3.3 V, I_S = −10 mA
		1.5	Ω max	
LEAKAGE CURRENTS				V_{DD} = +5.5 V, V_{SS} = −5.5 V
Source Off Leakage, I_S (Off)	±0.01		nA typ	V_S = ±4.5 V, V_D = ∓ 4.5 V, see Figure 15
	±0.25	±1	nA max	
Drain Off Leakage, I_D (Off)	±0.01		nA typ	V_S = ±4.5 V, V_D = ∓ 4.5 V, see Figure 15
	±0.25	±1	nA max	
Channel On Leakage, I_D, I_S (On)	±0.01		nA typ	V_S = V_D = ±4.5 V, see Figure 16
	±0.25	±1	nA max	
DIGITAL INPUTS				
Input High Voltage, V_{INH}		2.4	V min	
Input Low Voltage, V_{INL}		0.8	V max	
Input Current, I_{INL} or I_{INH}	0.005		μA typ	V_{IN} = V_{INL} or V_{INH}
		±0.1	μA max	
Digital Input Capacitance, C_{IN}	2		pF typ	
DYNAMIC CHARACTERISTICS[1]				
t_{ON}	75		ns typ	R_L = 300 Ω, C_L = 35 pF; V_S = 3.3 V, see Figure 17
	120	155	ns max	
t_{OFF}	45		ns typ	R_L = 300 Ω, C_L = 35 pF; V_S = 3.3 V, see Figure 17
	70	85	ns max	
Charge Injection, Q_{INJ}	110		pC typ	V_S = 0 V, R_S = 0 Ω, C_L = 1 nF, see Figure 18
Off Isolation	−65		dB typ	R_L = 50 Ω, C_L = 5 pF, f = 1 MHz, see Figure 19
Channel to Channel Crosstalk	−90		dB typ	R_L = 50 Ω, C_L = 5 pF, f = 1 MHz, see Figure 20
−3 dB Bandwidth	230		MHz typ	R_L = 50 Ω, C_L = 5 pF, see Figure 21
C_S (Off)	20		pF typ	f = 1 MHz
C_D (Off)	20		pF typ	f = 1 MHz
C_D, C_S (On)	70		pF typ	f = 1 MHz
POWER REQUIREMENTS[2]				V_{DD} = 5.5 V, V_{SS} = −5.5 V
I_{DD}	0.001		μA typ	Digital inputs = 0 V or 5.5 V
		1.0	μA max	
I_{SS}	0.001		μA typ	Digital inputs = 0 V or 5.5 V
		1.0	μA max	

[1] Guaranteed by design; not subject to production test.

[2] The device is fully specified at ±5 V dual supply and at +5 V single supply only. It is possible to operate the ADG621 with unbalanced supplies or at other voltage supplies (±2.7 V to ±5.5 V dual supply, and +2.7 V to +5.5 V single supply); however, the switch characteristics change. These changes include, but are not limited to, analog signal range, on resistance, leakage, V_{INL}, V_{INH}, and switching times. The optimal power-up sequence for the device is ground, V_{DD}, V_{SS}, and then the digital inputs, before applying the analog input signal.

SINGLE SUPPLY

V_{DD} = 5 V ± 10%, V_{SS} = 0 V, GND = 0 V, unless otherwise noted.

Table 2.

Parameter	+25°C	−40°C to +85°C	Unit	Test Conditions/Comments
ANALOG SWITCH				
Analog Signal Range		0 to V_{DD}	V	V_{DD} = 4.5 V, V_{SS} = 0 V
On Resistance, R_{ON}	7		Ω typ	V_S = 0 V to 4.5 V, I_S = −10 mA, see Figure 14
	10	12.5	Ω max	
On Resistance Match Between Channels, ΔR_{ON}	0.5		Ω typ	V_S = 0 V to 4.5 V, I_S = −10 mA
	0.75	1	Ω max	
On Resistance Flatness, $R_{FLAT(ON)}$	0.5	0.5	Ω typ	V_S = 1.5 V to 3.3 V, I_S = −10 mA
		1.2	Ω max	
LEAKAGE CURRENTS				V_{DD} = 5.5 V
Source Off Leakage I_S (Off)	±0.01		nA typ	V_S = 1 V/4.5 V, V_D = 4.5 V/1 V, see Figure 15
	±0.25	±1	nA max	
Drain Off Leakage I_D (Off)	±0.01		nA typ	V_S = 1 V/4.5 V, V_D = 4.5 V/1 V, see Figure 15
	±0.25	±1	nA max	
Channel On Leakage, I_D, I_S (On)	±0.01		nA typ	V_S = V_D = 1 V/4.5 V, see Figure 16
	±0.25	±1	nA max	
DIGITAL INPUTS				
Input High Voltage, V_{INH}		2.4	V min	
Input Low Voltage, V_{INL}		0.8	V max	
Input Current, I_{INL} or I_{INH}	0.005		μA typ	V_{IN} = V_{INL} or V_{INH}
		±0.1	μA max	
Digital Input Capacitance, C_{IN}	2		pF typ	
DYNAMIC CHARACTERISTICS[1]				
t_{ON}	120		ns typ	R_L = 300 Ω, C_L = 35 pF; V_S = 3.3 V, see Figure 17
	210	260	ns max	
t_{OFF}	50		ns typ	R_L = 300 Ω, C_L = 35 pF; V_S = 3.3 V, see Figure 17
	75	100	ns max	
Charge Injection, Q_{INJ}	6		pC typ	V_S = 0 V; R_S = 0 Ω, C_L = 1 nF, see Figure 18
Off Isolation	−65		dB typ	R_L = 50 Ω, C_L = 5 pF, f = 1 MHz, see Figure 19
Channel-to-Channel Crosstalk	−90		dB typ	R_L = 50 Ω, C_L = 5 pF, f = 1 MHz, see Figure 20
−3 dB Bandwidth	230		MHz typ	R_L = 50 Ω, C_L = 5 pF, see Figure 21
C_S (Off)	20		pF typ	f = 1 MHz
C_D (Off)	20		pF typ	f = 1 MHz
C_D, C_S (On)	70		pF typ	f = 1 MHz
POWER REQUIREMENTS[2]				V_{DD} = 5.5 V
I_{DD}	0.001		μA typ	Digital Inputs = 0 V or 5.5 V
		1.0	μA max	

[1] Guaranteed by design; not subject to production test.

[2] The device is fully specified at ±5 V dual supply and at +5 V single supply only. It is possible to operate the ADG621 with unbalanced supplies or at other voltage supplies (±2.7 V to ±5.5 V dual supply, and +2.7 V to +5.5 V single supply); however, the switch characteristics change. These changes include, but are not limited to, analog signal range, on resistance, leakage, V_{INL}, V_{INH}, and switching times. The optimal power-up sequence for the device is ground, V_{DD}, V_{SS}, and then the digital inputs, before applying the analog input signal.

ABSOLUTE MAXIMUM RATINGS

T_A = 25°C, unless otherwise noted.

Table 3.

Parameter	Rating
V_{DD} to V_{SS}[1]	13 V
V_{DD} to GND	−0.3 V to +6.5 V
V_{SS} to GND	+0.3 V to −6.5 V
Analog Inputs[2]	V_{SS} − 0.3 V to V_{DD} + 0.3 V
Digital Inputs[2]	−0.3 V to V_{DD} + 0.3 V or 30 mA, whichever occurs first
Peak Current, Sx or Dx	100 mA (pulsed at 1 ms, 10% duty cycle maximum)
Continuous Current, S or D	50 mA
Operating Temperature Range	
Industrial	−40°C to +85°C
Storage Temperature Range	−65°C to +150°C
Junction Temperature	150°C
MSOP Package	
θ_{JA} Thermal Impedance	206°C/W
θ_{JC} Thermal Impedance	44°C/W
Lead Soldering	
Lead Temperature, Soldering (10 sec)	300°C
Infrared (IR) Reflow, Peak Temperature	220°C
Pb-Free Soldering	
Reflow, Peak Temperature	260 (+0/−5)°C
Time at Peak Temperature	20 sec to 40 sec

[1] The device is fully specified at ±5 V dual supply and at +5 V single supply only. It is possible to operate the ADG621 with unbalanced supplies or at other voltage supplies (±2.7 V to ±5.5 V, and 2.7 V to 5.5 V); however, the switch characteristics change. These changes include, but are not limited to, analog signal range, on resistance, leakage, V_{INL}, V_{INH}, and switching times. The optimal power-up sequence for the device is ground, V_{DD}, V_{SS}, and then the digital inputs, before applying the analog input signal.

[2] Overvoltages at INx, S, or D must be clamped by internal diodes. Limit currents to the maximum ratings given.

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

Only one absolute maximum rating can be applied at any one time.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

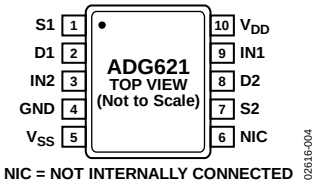

Figure 2. Pin Configuration

Table 4. Pin Function Descriptions

Pin No.	Mnemonic	Description
1, 7	S1, S2	Source Terminals. S1 and S2 can be inputs or outputs.
2, 8	D1, D2	Drain Terminals. D1 and D2 can be inputs or outputs.
3, 9	IN2, IN1	Control Inputs.
4	GND	Ground (0 V) Reference.
5	V_{SS}	Most Negative Power Supply in a Dual-Supply Application. In single-supply applications, tie this pin to ground at the device.
6	NIC	Not Internally Connected.
10	V_{DD}	Most Positive Power Supply Potential.

Table 5. Truth Table

INx	Switch Sx Condition
0	Off
1	On

TYPICAL PERFORMANCE CHARACTERISTICS

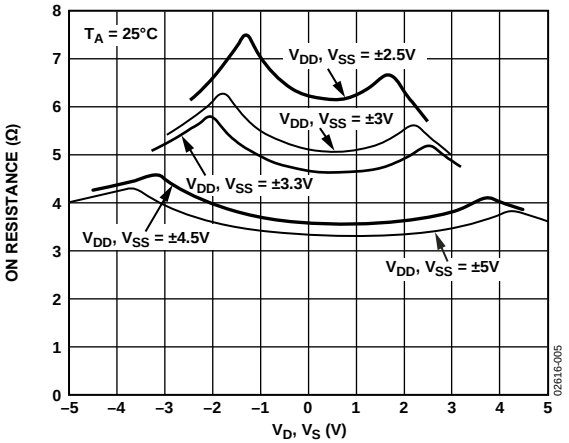

Figure 3. On Resistance vs. V_D, V_S (Dual Supply)

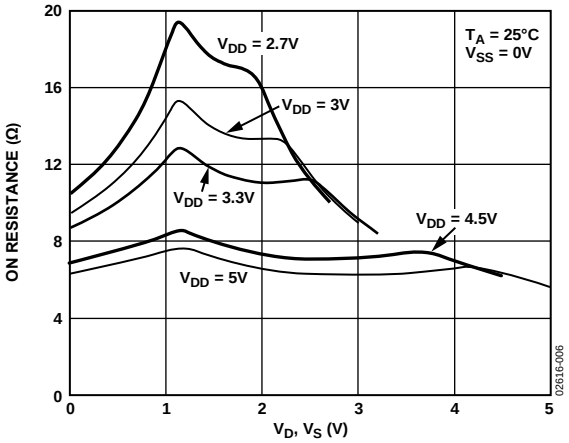

Figure 4. On Resistance vs. V_D, V_S (Single Supply)

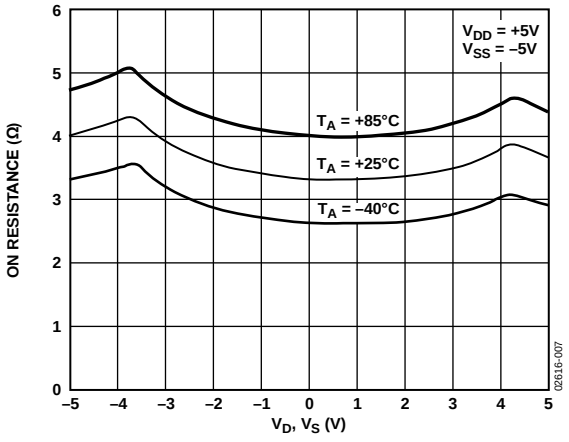

Figure 5. On Resistance vs. V_D, V_S for Different Temperatures (Dual Supply)

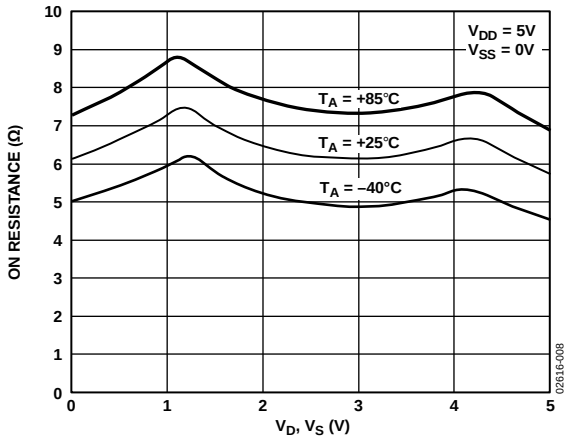

Figure 6. On Resistance vs. V_D, V_S for Different Temperature (Single Supply)

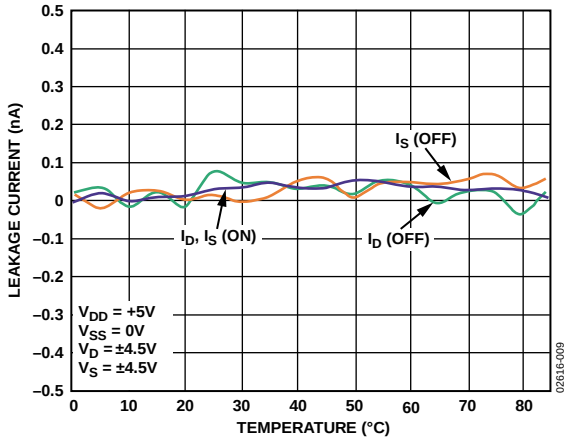

Figure 7. Leakage Current vs. Temperature (Dual Supply)

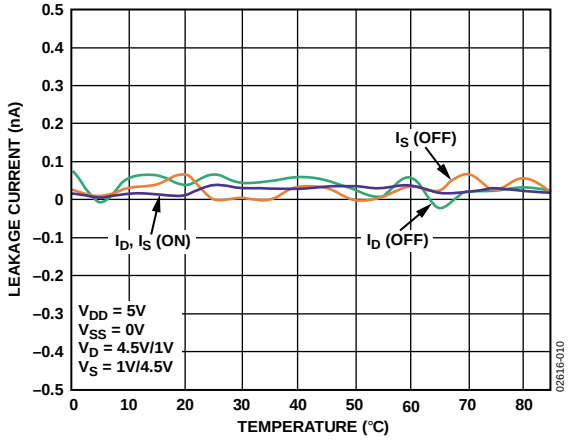

Figure 8. Leakage Current vs. Temperature (Single Supply)

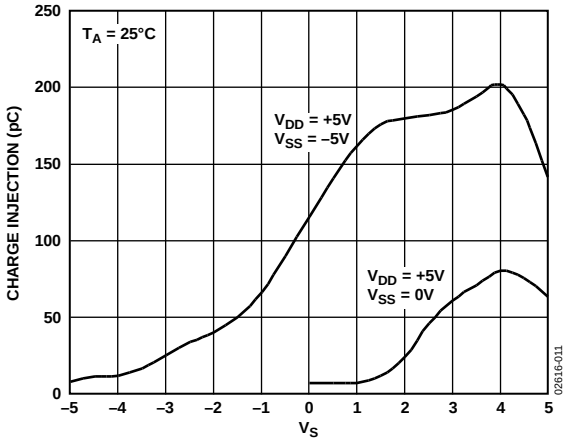

Figure 9. Charge Injection vs. Source Voltage (V_S)

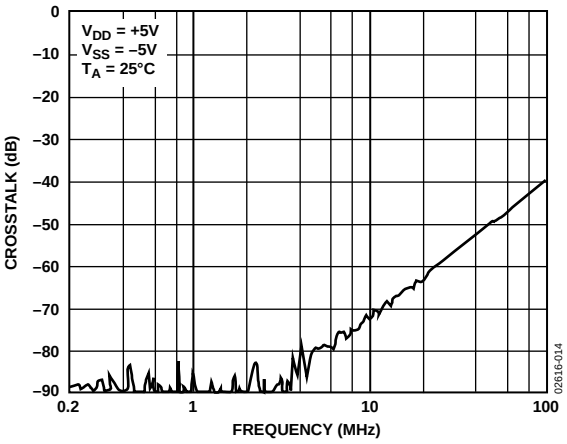

Figure 12. Crosstalk vs. Frequency

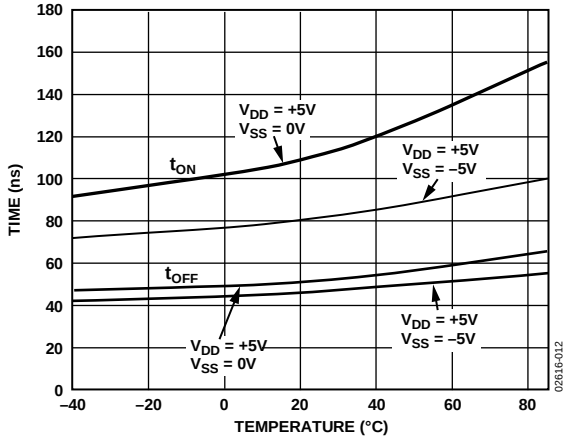

Figure 10. t_{ON}/t_{OFF} Times vs. Temperature

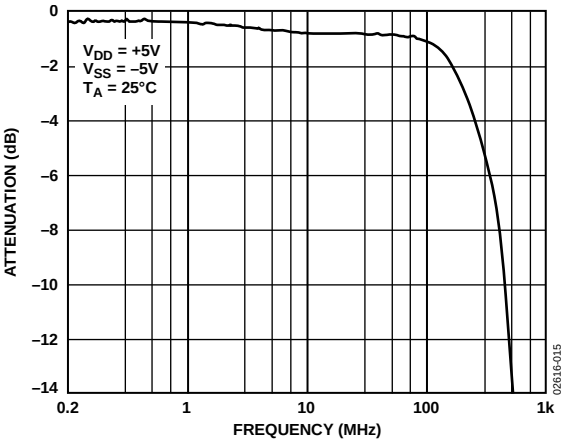

Figure 13. Bandwidth vs. Frequency

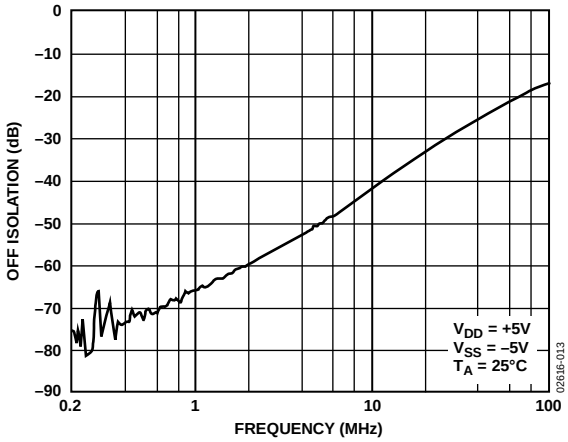

Figure 11. Off Isolation vs. Frequency

TEST CIRCUITS

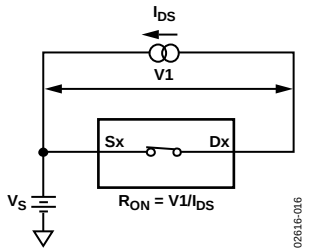

Figure 14. On Resistance

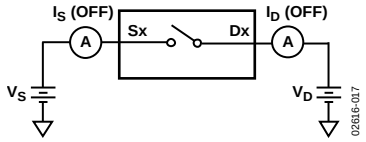

Figure 15. Off Leakage

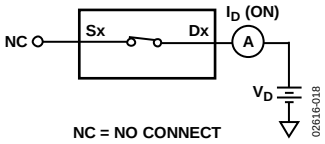

Figure 16. On Leakage

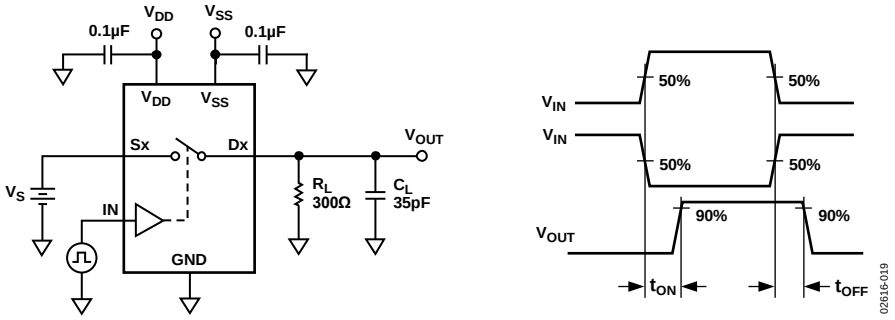

Figure 17. Switching Times (t_{ON}, t_{OFF})

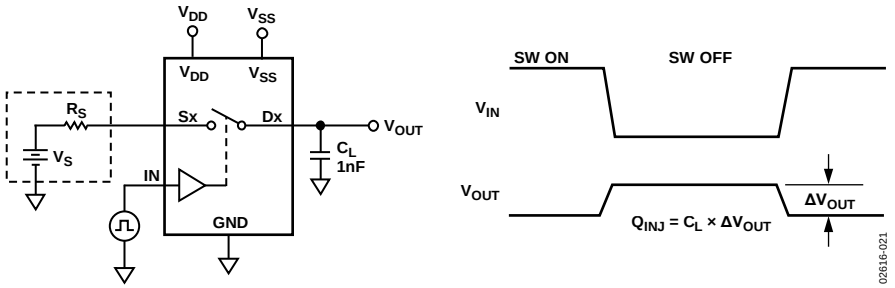

Figure 18. Charge Injection

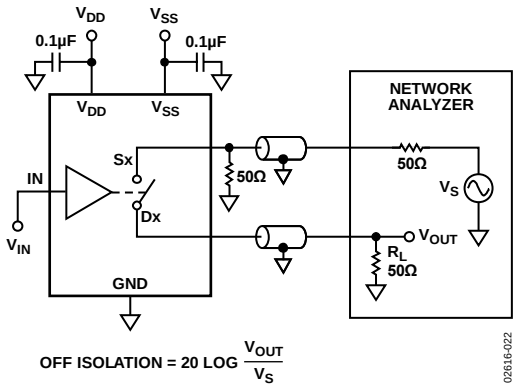

Figure 19. Off Isolation

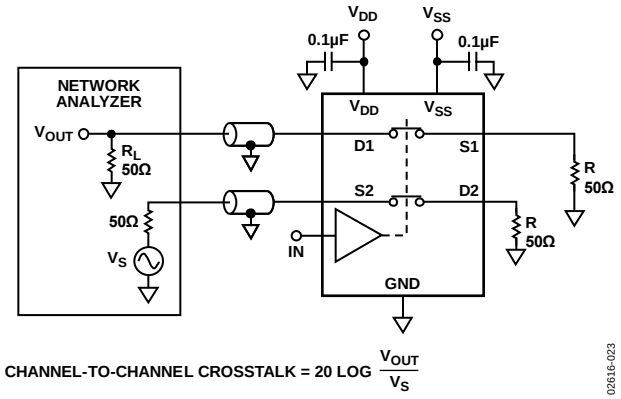

Figure 20. Channel to Channel Crosstalk

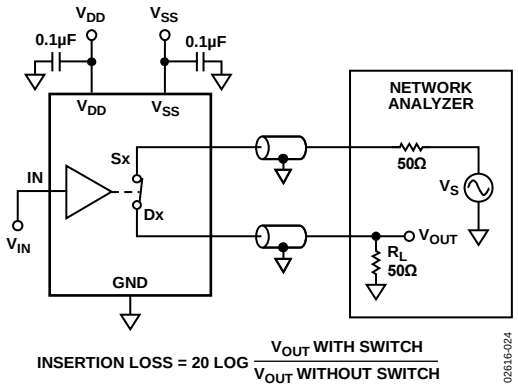

Figure 21. Bandwidth

TERMINOLOGY

I_{DD}
I_{DD} is the positive supply current.

I_{SS}
I_{SS} is the negative supply current.

V_D (V_S)
V_D and V_S are the analog voltages on Terminal D and Terminal S, respectively.

R_{ON}
R_{ON} is the ohmic resistance between Terminal D and Terminal S.

$R_{FLAT (ON)}$
On resistance flatness is defined as the difference between the maximum and minimum value of on resistance as measured over the specified analog signal range.

ΔR_{ON}
ΔR_{ON} is the on resistance match between any two channels.

I_S (Off)
I_S (Off) is the source leakage current with the switch off.

I_D (Off)
I_D (Off) is the drain leakage current with the switch off.

I_D, I_S (On)
I_D (On) and I_S (On) are the channel leakage currents with the switch on.

V_{INL}
V_{INL} is the maximum input voltage for Logic 0.

V_{INH}
V_{INH} is the minimum input voltage for Logic 1.

I_{INL} (I_{INH})
I_{INL} and I_{INH} are the input currents of the digital input.

C_S (Off)
C_S (Off) is the off switch source capacitance, measured with reference to ground.

C_D (Off)
C_D (Off) is the off switch drain capacitance, measured with reference to ground.

C_D, C_S (On)
C_D (On) and C_S (On) are the on switch capacitances, measured with reference to ground.

C_{IN}
C_{IN} is the digital input capacitance.

t_{ON}
t_{ON} is the delay time between the 50% and the 90% points of the digital input and switch on condition.

t_{OFF}
t_{OFF} is the delay time between the 50% and the 90% points of the digital input and switch off condition.

Charge Injection
Charge injection, Q_{INJ}, is a measure of the glitch impulse transferred from the digital input to the analog output during on and off switching.

Off Isolation
Off isolation is a measure of an unwanted signal coupling through an off switch.

Crosstalk
Crosstalk is a measure of an unwanted signal that is coupled through from one channel to another as a result of parasitic capacitance.

−3 dB Bandwidth
−3 dB bandwidth is the frequency at which the output is attenuated by −3 dB.

On Response
On response is the frequency response of the on switch.

Insertion Loss
Insertion loss is the attenuation between the input and output ports of the switch when the switch is in the on condition and is due to the on resistance of the switch.

OUTLINE DIMENSIONS

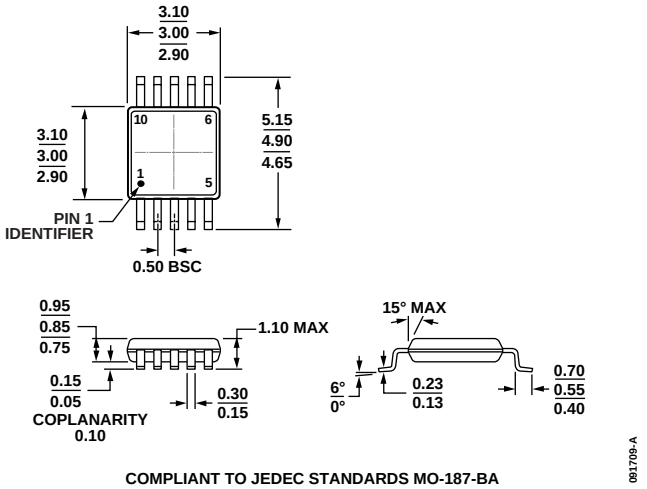

Figure 22. 10-Lead Mini Small Outline Package [MSOP]
(RM-10)
Dimensions shown in millimeters

ORDERING GUIDE

Model[1]	Temperature Range	Package Description	Package Option	Branding[2]
ADG621BRMZ	−40°C to +85°C	10-Lead Mini Small Outline Package [MSOP]	RM-10	SXB#
ADG621BRMZ-REEL	−40°C to +85°C	10-Lead Mini Small Outline Package [MSOP]	RM-10	SXB#

[1] Z = RoHS Compliant Part.
[2] # denotes RoHS compliant product; may be top or bottom marked.

Mouser Electronics

Authorized Distributor

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Analog Devices Inc.:

ADG621BRMZ-REEL ADG621BRMZ