2.5 V/3.3 V, 10-Bit, 2-Port Level Translating, Bus Switch

FEATURES

- 225 ps Propagation Delay through the Switch
- 4.5 Ω Switch Connection between Ports
- Data Rate 1.244 Gbps
- 2.5 V/3.3 V Supply Operation
- Selectable Level Shifting/Translation
- Small Signal Bandwidth 610 MHz
- Level Translation
  - 3.3 V to 2.5 V
  - 3.3 V to 1.8 V
  - 2.5 V to 1.8 V
- 24-Lead LFCSP Package

APPLICATIONS

- 3.3 V to 1.8 V Voltage Translation
- 3.3 V to 2.5 V Voltage Translation
- 2.5 V to 1.8 V Voltage Translation
- Bus Switching
- Bus Isolation
- Hot Swap
- Hot Plug
- Analog Signal Switching

GENERAL DESCRIPTION

The ADG3246 is a 2.5 V or 3.3 V, 10-bit, 2-port digital switch. It is designed on Analog Devices' low voltage CMOS process, which provides low power dissipation yet gives high switching speed and very low on resistance, allowing inputs to be connected to outputs without additional propagation delay or generating additional ground bounce noise.

The switches are enabled by means of the bus enable ($\overline{BE}$) input signal. These digital switches allow bidirectional signals to be switched when ON. In the OFF condition, signal levels up to the supplies are blocked.

This device is ideal for applications requiring level translation. When operated from a 3.3 V supply, level translation from 3.3 V inputs to 2.5 V outputs occurs. Similarly, if the device is operated from a 2.5 V supply and 2.5 V inputs are applied, the device will translate the outputs to 1.8 V. In addition to this, the ADG3246 has a level translating select pin ($\overline{SEL}$). When $\overline{SEL}$ is low, V_{CC} is reduced internally, allowing for level translation between 3.3 V inputs and 1.8 V outputs. This makes the device suited to applications requiring level translation between different supplies, such as converter to DSP/microcontroller interfacing.

FUNCTIONAL BLOCK DIAGRAM

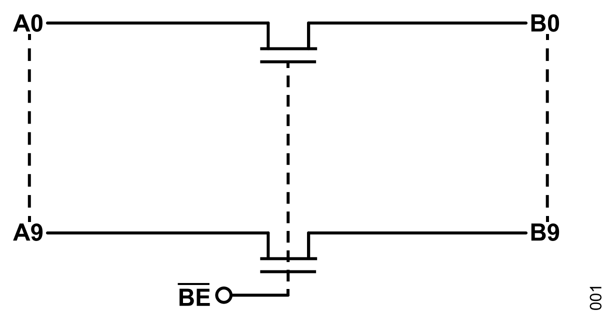

Figure 1.

PRODUCT HIGHLIGHTS

1. 3.3 V or 2.5 V supply operation.
2. Extremely low propagation delay through switch.
3. 4.5 Ω switches connect inputs to outputs.
4. Level/voltage translation.
5. 24-lead 4 mm × 4 mm LFCSP package.

Rev. B

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REVISION HISTORY

8/2022—Rev. A to Rev. B

SPECIFICATIONS

V_{CC} = 2.3 V to 3.6 V, GND = 0 V, all specifications T_{MIN} to T_{MAX}, unless otherwise noted.

Table 1.

Parameter	+25°C	−40°C to +85°C	−40°C to +105°C	Unit	Test Conditions/Comments
DC ELECTRICAL CHARACTERISTICS					
Input High Voltage (V_{INH})		2.0	2.0	V min	V_{CC} = 2.7 V to 3.6 V
		1.7	1.7	V min	V_{CC} = 2.3 V to 2.7 V
Input Low Voltage (V_{INL})		0.8	0.8	V max	V_{CC} = 2.7 V to 3.6 V
		0.7	0.7	V max	V_{CC} = 2.3 V to 2.7 V
Input Leakage Current (I_I)	±0.01			μA typ	
		±1	±1	μA max	
OFF State Leakage Current (I_{OZ} OFF)	±0.01			μA typ	0 ≤ A, B ≤ V_{CC}
		±1	±1	μA max	0 ≤ A, B ≤ V_{CC}
ON State Leakage Current (I_{OZ} ON)	±0.01			μA typ	0 ≤ A, B ≤ V_{CC}
		±1	±1	μA max	0 ≤ A, B ≤ V_{CC}
Maximum Pass Voltage (V_P)	2.5			V typ	$V_A/V_B = V_{CC} = \overline{SEL}$ = 3.3 V, I_O = −5 μA
		2.0	2.0	V min	
		2.9	2.9	Vmax	
	1.8			V typ	$V_A/V_B = V_{CC} = \overline{SEL}$ = 2.5 V, I_O = −5 μA
		1.5	1.5	V min	
		2.1	2.1	V max	
	1.8			V typ	$V_A/V_B = V_{CC}$ = 3.3 V, $\overline{SEL}$ = 0 V, I_O = −5 μA
		1.5	1.5	V min	
		2.1	2.1	V max	
CAPACITANCE					
A Port Off Capacitance (C_A OFF)	5			pF	f = 1 MHz
B Port Off Capacitance (C_B OFF)	5			pF	f = 1 MHz
A, B Port On Capacitance (C_A, C_B ON)	10			pF	f = 1 MHz
Control Input Capacitance (C_{IN})	6			pF	f = 1 MHz
SWITCHING CHARACTERISTICS					
Propagation Delay A to B or B to A[1] (t_{PD})	0.225			ns typ	C_L = 50 pF, V_{CC} = 3 V, $\overline{SEL}$ = 3 V
			3.5	ns max	
	0.275			ns typ	C_L = 50 pF, V_{CC} = 3.3 V, $\overline{SEL}$ = 0 V
			2	ns max	
Propagation Delay Matching[2] (Δt_{PD})	22.5			ps typ	C_L = 50 pF, V_{CC} = 3 V, $\overline{SEL}$ = 3 V
			200	ps max	
	37.5			ps typ	C_L = 50 pF, V_{CC} = 3.3 V, $\overline{SEL}$ = 0 V
			200	ps max	
Bus Enable Time $\overline{BE}$ to A or B[3] (t_{PZH}, t_{PZL})	3.2			ns typ	V_{CC} = 3.0 V to 3.6 V, $\overline{SEL}$ = V_{CC}
		1		ns min	
		4.8		ns max	
	2.2			ns typ	V_{CC} = 3.0 V to 3.6 V, $\overline{SEL}$ = 0 V
		0.5		ns min	
		3.3		ns max	
	2.2			ns typ	V_{CC} = 2.3 V to 2.7 V, $\overline{SEL}$ = V_{CC}
		0.5		ns min	
		3		ns max	
Bus Disable Time $\overline{BE}$ to A or B[3] (t_{PHZ}, t_{PLZ})	3.2			ns typ	V_{CC} = 3.0 V to 3.6 V, $\overline{SEL}$ = V_{CC}
		1		ns min	
		4.8		ns max	

SPECIFICATIONS

Table 1.

Parameter	+25°C	−40°C to +85°C	−40°C to +105°C	Unit	Test Conditions/Comments
	1.7			ns typ	V_{CC} = 3.0 V to 3.6 V, $\overline{SEL}$ = 0 V
		0.5		ns min	
		2.9		ns max	
	1.75			ns typ	V_{CC} = 2.3 V to 2.7 V, $\overline{SEL}$ = V_{CC}
		0.5		ns min	
		2.6		ns max	
Maximum Data Rate	1.244			Gbps typ	V_{CC} = 3.3 V, $\overline{SEL}$ = 3.3 V; V_A/V_B = 2 V
			0.2	Gbps max	
Channel Jitter	50			ps p-p	V_{CC} = 3.3 V, $\overline{SEL}$ = 3.3 V; V_A/V_B = 2 V
Operating Frequency—Bus Enable ($f_{\overline{BE}}$)		10		MHz max	
DIGITAL SWITCH					
On Resistance (R_{ON})	4.5			Ω typ	V_{CC} = 3 V, $\overline{SEL}$ = 3 V, V_A = 0 V, I_{BA} = 8 mA
		8		Ω max	
	15			Ω typ	V_{CC} = 3 V, $\overline{SEL}$ = 3 V, V_A = 1.7 V, I_{BA} = 8 mA
		28		Ω max	
	5			Ω typ	V_{CC} = 2.3 V, $\overline{SEL}$ = 2.3 V, V_A = 0 V, I_{BA} = 8 mA
		9		Ω max	
	11			Ω typ	V_{CC} = 2.3 V, $\overline{SEL}$ = 2.3 V, V_A = 1 V, I_{BA} = 8 mA
		18		Ω max	
	5			Ω typ	V_{CC} = 3 V, $\overline{SEL}$ = 0 V, V_A = 0 V, I_{BA} = 8 mA
		8	40	Ω max	
	5.5			Ω typ	V_{CC} = 3.3 V, $\overline{SEL}$ = 0 V, V_A = 0 V, I_{BA} = 8 mA
			40	Ω max	
	14			Ω typ	V_{CC} = 3 V, $\overline{SEL}$= 0 V, V_A = 1 V, I_{BA} = 8 mA
			240	Ω max	
	11			Ω typ	V_{CC} = 3.3 V, $\overline{SEL}$= 0 V, V_A = 1 V, I_{BA} = 8 mA
			40	Ω max	
On Resistance Matching (ΔR_{ON})	0.45			Ω typ	V_{CC} = 3 V, $\overline{SEL}$ = 3 V, V_A = 0 V, I_{BA} = 8 mA
			4	Ω max	
	0.75			Ω typ	V_{CC} = 3.3 V, $\overline{SEL}$= 0 V, V_A = 0 V, I_{BA} = 8 mA
			4	Ω max	
	0.65			Ω typ	V_{CC} = 3 V, $\overline{SEL}$ = 3 V, V_A = 1 V, I_{BA} = 8 mA
			4	Ω max	
	0.85			Ω typ	V_{CC} = 3.3 V, $\overline{SEL}$= 0 V, V_A = 1 V, I_{BA} = 8 mA
			4	Ω max	
POWER REQUIREMENTS					
Positive Power Supply Voltage (V_{CC})		2.3	2.3	V min	
		3.6	3.6	V max	
Quiescent Power Supply Current (I_{CC})	0.001			µA typ	Digital Inputs = 0 V or V_{CC}, $\overline{SEL}$ = V_{CC}
		1	2	µA max	
	0.65			mA typ	Digital Inputs = 0 V or V_{CC}, $\overline{SEL}$ = 0 V
		1.2	1.3	mA max	

SPECIFICATIONS

Table 1.

Parameter	+25°C	−40°C to +85°C	−40°C to +105°C	Unit	Test Conditions/Comments
Increase in I_{CC} per Input[4] (ΔI_{CC})		130		μA max	V_{CC} = 3.6 V, $\overline{SEL}$ = 3.6 V, $\overline{BE}$ = 3.0 V

1 The digital switch contributes no propagation delay other than the RC delay of the typical R_{ON} of the switch and the load capacitance when driven by an ideal voltage source. Since the time constant is much smaller than the rise/fall times of typical driving signals, it adds very little propagation delay to the system. Propagation delay of the digital switch when used in a system is determined by the driving circuit on the driving side of the switch and its interaction with the load on the driven side. This specification is calculated by using the following equation: $t_{PD} = R_{ON} \times C_L$, where R_{ON} is 4.5 Ω and C_L is 50 pF.

2 Propagation delay matching between channels is calculated from the on resistance matching and load capacitance of 50 pF. This specification is calculated by using the following equation: $\Delta t_{PD} = \Delta R_{ON} \times C_L$, where R_{ON} is 0.45 Ω and C_L is 50 pF.

3 See the Test Circuits section.

4 This current applies to the control pin ($\overline{BE}$) only. The A and B ports contribute no significant AC or DC currents as they transition.

ABSOLUTE MAXIMUM RATINGS

T_A = 25 °C, unless otherwise noted.

Table 2.

Parameter	Rating
V_{CC} to GND	–0.5 V to +4.6 V
Digital Inputs to GND	–0.5 V to +4.6 V
DC Input Voltage	–0.5 V to +4.6 V
DC Output Current	25 mA per channel
Operating Temperature Range	–40°C to +105°C
Storage Temperature Range	–65°C to +150°C
Junction Temperature	150°C
Reflow Soldering Peak Temperature, Pb-Free	As per JEDEC J-STD-020

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

THERMAL RESISTANCE

Thermal performance is directly linked to printed circuit board (PCB) design and operating environment. Careful attention to PCB thermal design is required.

θ_{JA} is the natural convection junction-to-ambient thermal resistance measured in a one cubic foot sealed enclosure.

Table 3. Thermal Resistance

Package Type[1]	θ_{JA}	Unit
CP-24-10	35	°C/W

[1] Test Condition 1: Thermal impedance simulated values are based on JEDEC 2S2P thermal test board with four thermal vias. See the JEDEC JESD-51.

ELECTROSTATIC DISCHARGE (ESD) RATINGS

The following ESD information is provided for handling of ESD-sensitive devices in an ESD protected area only.

Human body model (HBM) per ANSI/ESDA/JEDEC JS-001.

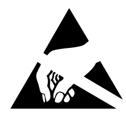
ESD RATINGS FOR ADG3246

Table 4. ADG3246, 24-Lead LFCSP

ESD Model	Withstand Threshold (kV)	Class
HBM[1]	1	Class 1

[1] This is the HBM for the input/output port to supplies, the input/output port to input/output port, and for all other pins.

ESD CAUTION



ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

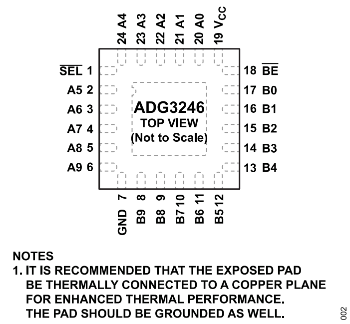


Figure 2. Pin Configuration

Table 5. Pin Function Descriptions

Pin No.	Mnemonic	Description
1	$\overline{\text{SEL}}$	Level Translation Select (Active Low).
2	A5	Port A5. This pin can be an input or output.
3	A6	Port A6. This pin can be an input or output.
4	A7	Port A7. This pin can be an input or output.
5	A8	Port A8. This pin can be an input or output.
6	A9	Port A9. This pin can be an input or output.
7	GND	Ground (0 V) Reference.
8	B9	Port B9. This pin can be an input or output.
9	B8	Port B8. This pin can be an input or output.
10	B7	Port B7. This pin can be an input or output.
11	B6	Port B6. This pin can be an input or output.
12	B5	Port B5. This pin can be an input or output.
13	B4	Port B4. This pin can be an input or output.
14	B3	Port B3. This pin can be an input or output.
15	B2	Port B2. This pin can be an input or output.
16	B1	Port B1. This pin can be an input or output.
17	B0	Port B0. This pin can be an input or output.
18	$\overline{\text{BE}}$	Bus Enable (Active Low).
19	V_{CC}	Positive Power Supply Potential.
20	A0	Port A0. This pin can be an input or output.
21	A1	Port A1. This pin can be an input or output.
22	A2	Port A2. This pin can be an input or output.
23	A3	Port A3. This pin can be an input or output.
24	A4	Port A4. This pin can be an input or output.
EP	EPAD	Exposed Pad. It is recommended that the exposed pad be thermally connected to a copper plane enhanced thermal performance. The pad should be grounded as well.

Table 6. Truth Table

$\overline{\text{BE}}$	$\overline{\text{SEL}}$[1]	Function
L	L	A = B, 3.3 V to 1.8 V level shifting.
L	H	A = B, 3.3 V to 2.5 V/2.5 V to 1.8 V level shifting.
H	X	Disconnect.

[1] $\overline{\text{SEL}}$ = 0 only when V_{CC} = 3.3 V ± 10%.

TYPICAL PERFORMANCE CHARACTERISTICS

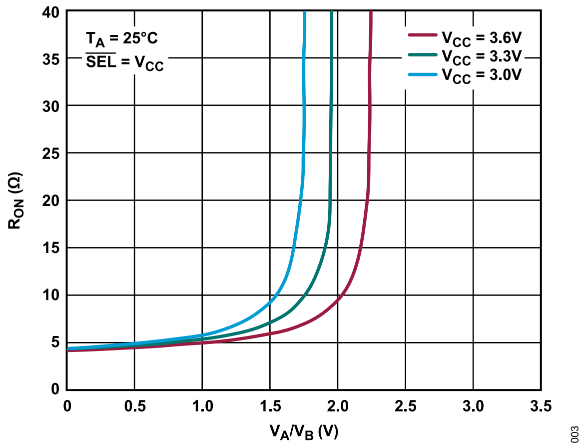


Figure 3. On Resistance vs. Input Voltage, V_{CC} = 3 V, 3.3 V, and 3.6 V

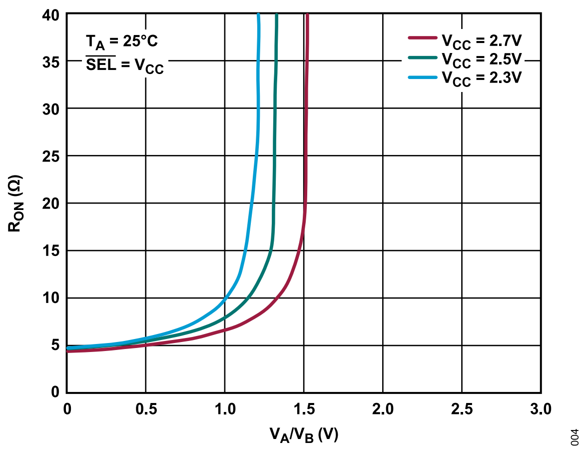


Figure 4. On Resistance vs. Input Voltage, V_{CC} = 2.3 V, 2.5 V, and 2.7 V

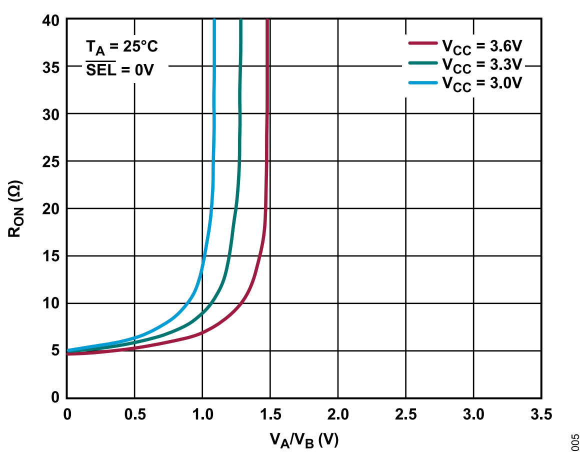


Figure 5. On Resistance vs. Input Voltage, $\overline{SEL}$ = 0 V

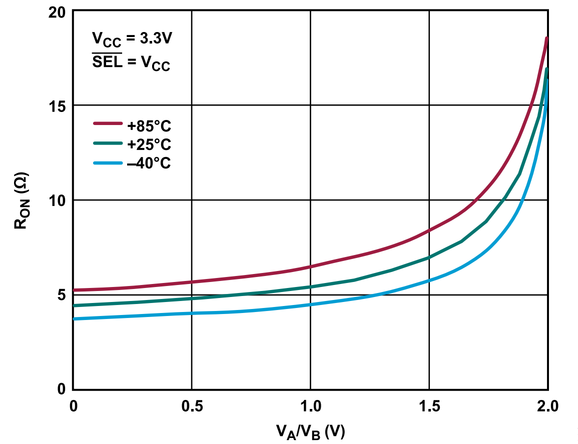


Figure 6. On Resistance vs. Input Voltage for Different Temperatures, V_{CC} = 3.3 V

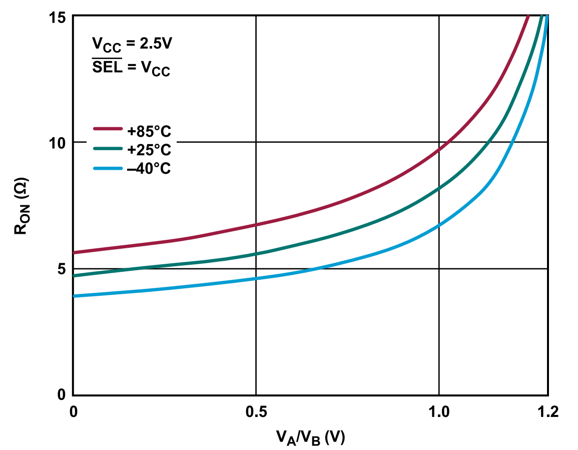


Figure 7. On Resistance vs. Input Voltage for Different Temperatures, V_{CC} = 2.5 V

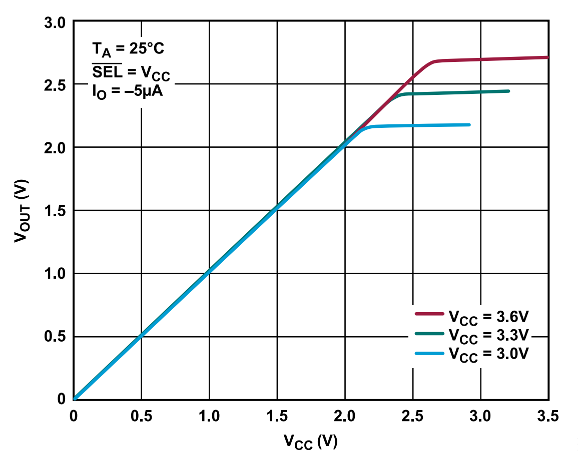


Figure 8. Pass Voltage vs. V_{CC}, V_{CC} = 3 V, 3.3 V, and 3.6 V

TYPICAL PERFORMANCE CHARACTERISTICS

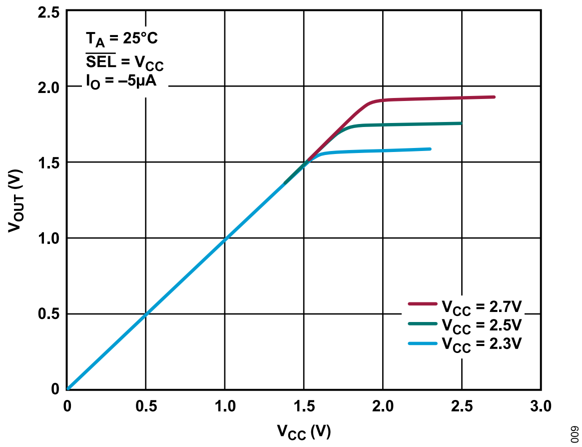


Figure 9. Pass Voltage vs. V_{CC}, V_{CC} = 2.3 V, 2.5 V, and 2.7 V

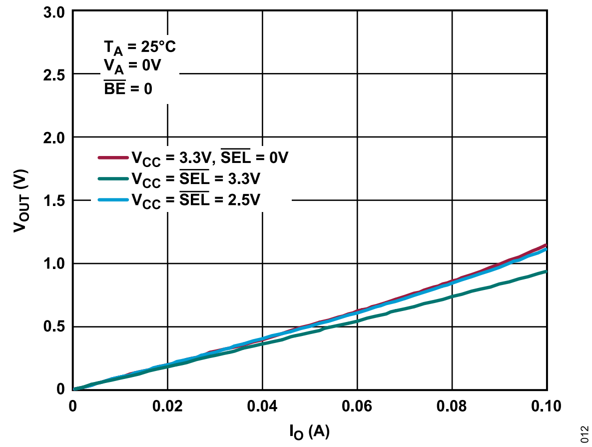


Figure 12. Output Low Characteristic

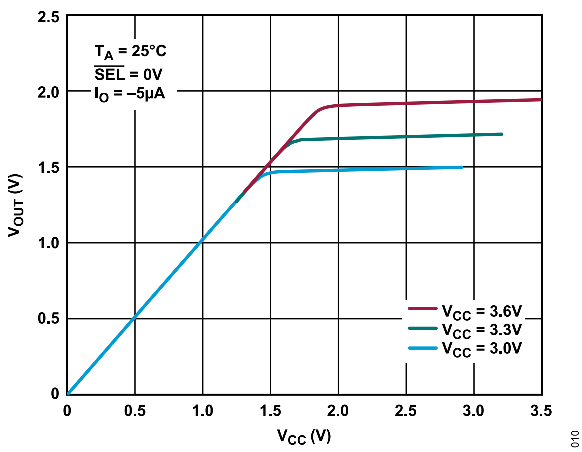


Figure 10. Pass Voltage vs. V_{CC}, $\overline{SEL}$ = 0 V

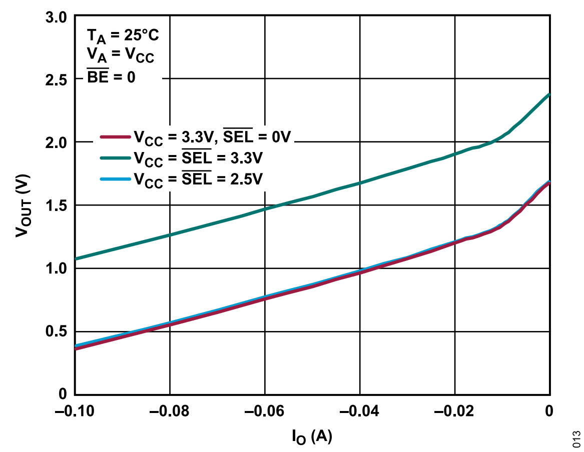


Figure 13. Output High Characteristic

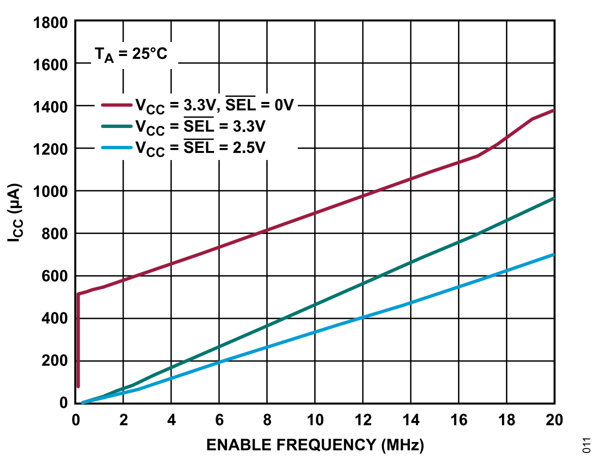


Figure 11. I_{CC} vs. Enable Frequency

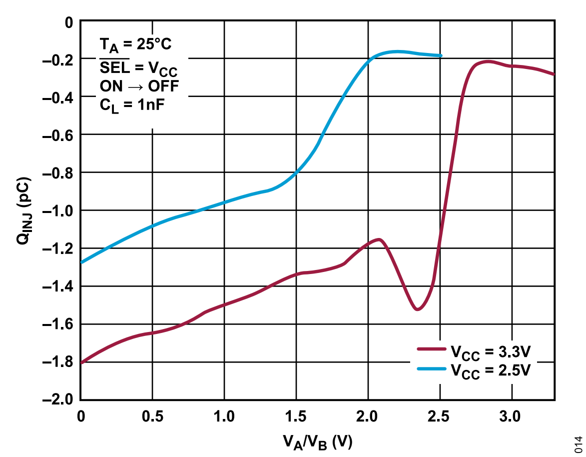


Figure 14. Charge Injection vs. Source Voltage

TYPICAL PERFORMANCE CHARACTERISTICS

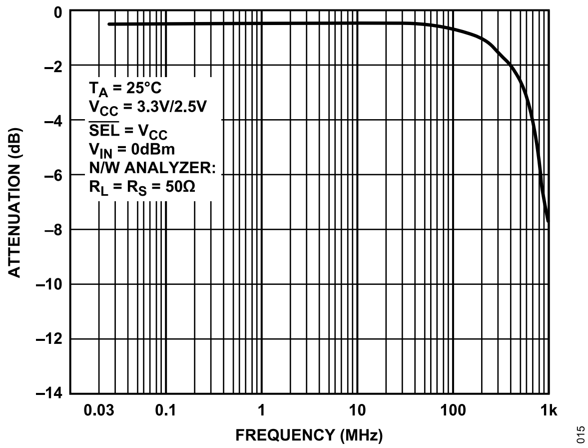


Figure 15. Bandwidth vs. Frequency

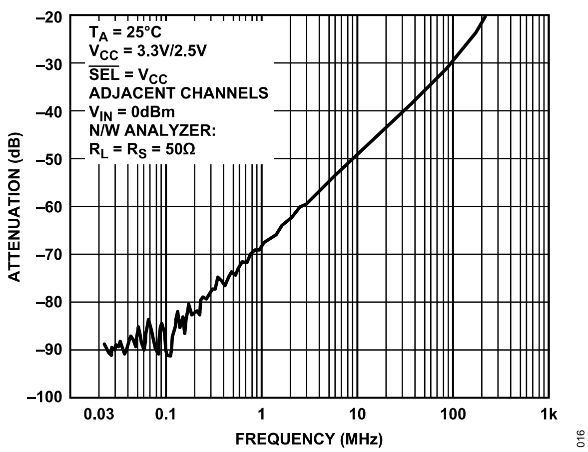


Figure 16. Crosstalk vs. Frequency

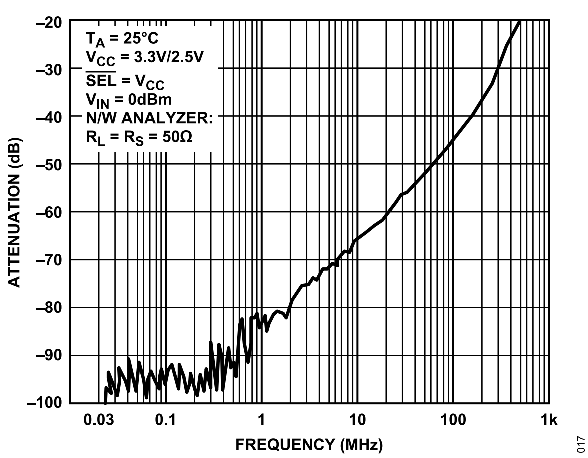


Figure 17. Off Isolation vs. Frequency

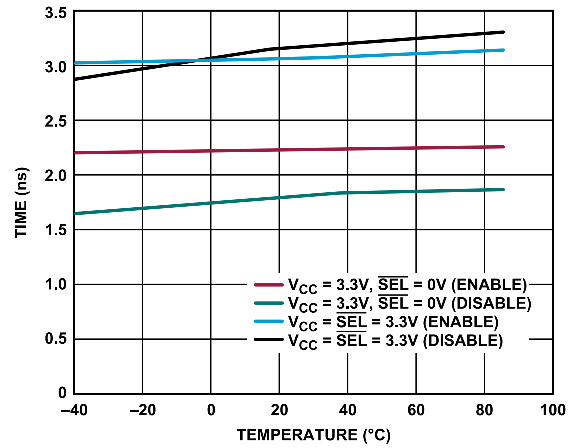


Figure 18. Enable/Disable Time vs. Temperature, V_{CC} = 3.3 V

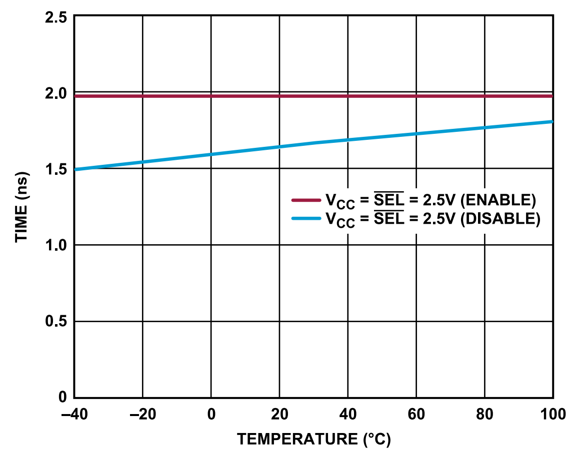


Figure 19. Enable/Disable Time vs. Temperature, V_{CC} = 2.5 V

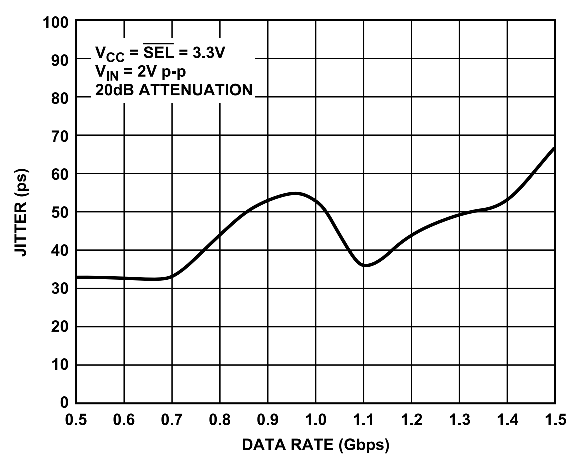


Figure 20. Jitter vs. Data Rate; PRBS 31

TYPICAL PERFORMANCE CHARACTERISTICS

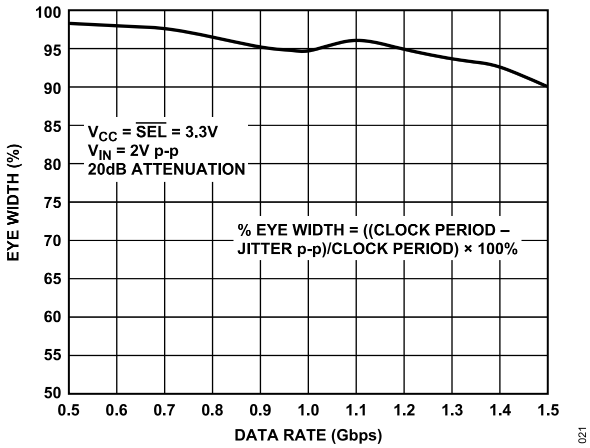


Figure 21. Eye Width vs. Data Rate; PRBS 31

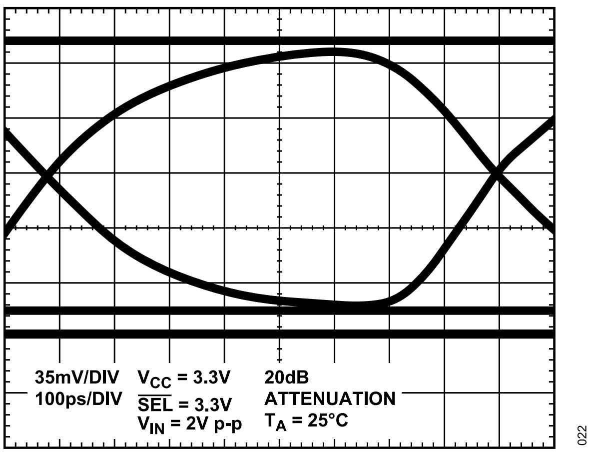


Figure 22. Eye Pattern; 1.244 Gbps, V_{CC} = 3.3 V, PRBS 31

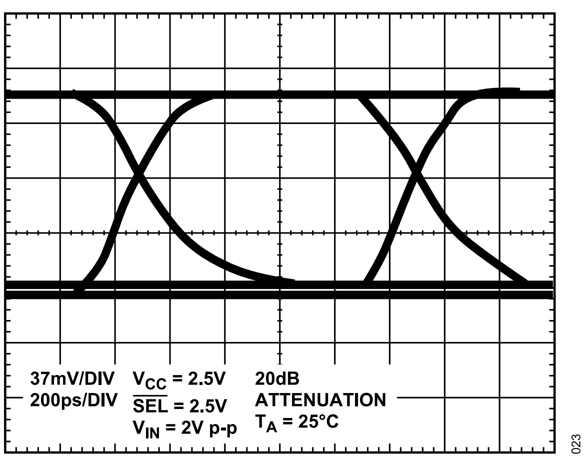


Figure 23. Eye Pattern; 1 Gbps, V_{CC} = 2.5 V, PRBS 31

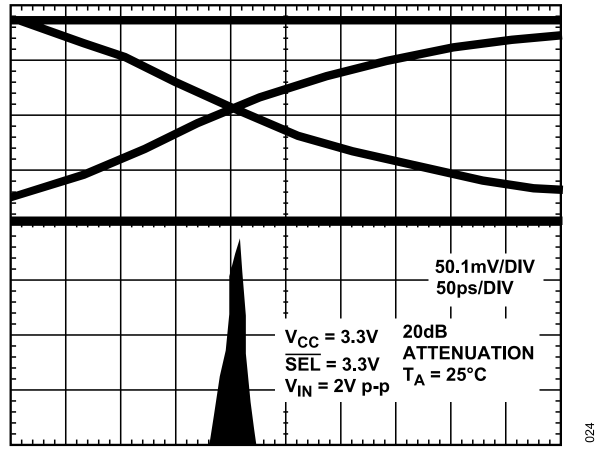


Figure 24. Jitter at 1.244 Gbps, PRBS 31

TEST CIRCUITS

For the following load circuit and waveforms, the notation that is used is V_{IN} and V_{OUT}, where $V_{IN} = V_A$ and $V_{OUT} = V_B$ or $V_{IN} = V_B$ and $V_{OUT} = V_A$.

For V_{CC} = 3.3 V ± 0.3 V ($\overline{SEL} = V_{CC}$), R_L = 500 Ω, V_A = 300 mV, C_L = 50 pF, and V_T = 1.5 V.

For V_{CC} = 2.5 V ± 0.2 V ($\overline{SEL} = V_{CC}$), R_L = 500 Ω, V_A = 150 mV, C_L = 30 pF, and V_T = 0.9 V.

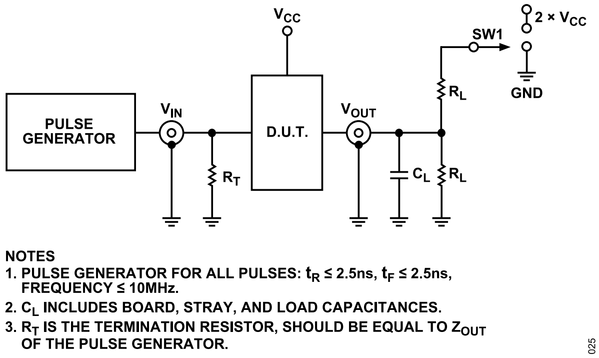


Figure 25. Load Circuit

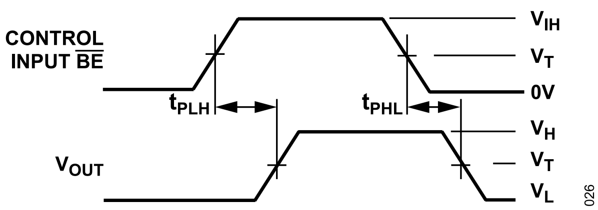


Figure 26. Propagation Delay

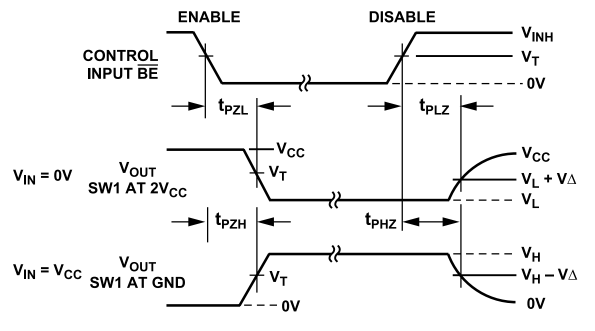


Figure 27. Enable and Disable Time

Table 7. Switch Position

Test	S1
t_{PLZ}, t_{PZL}	2 × V_{CC}
t_{PHZ}, t_{PZH}	GND

TERMINOLOGY

V_{CC}

Positive Power Supply Voltage.

GND

Ground (0 V) Reference.

V_{INH}

Minimum Input Voltage for Logic 1.

V_{INL}

Minimum Input Voltage for Logic 0.

I_I

Input Leakage Current at the Control Inputs.

I_{OZ}

OFF State Leakage Current. It is the maximum leakage current at the switch pin in the OFF state.

I_{OL}

ON State Leakage Current. It is the maximum leakage current at the switch pin in the ON state.

V_P

Maximum Pass Voltage. The maximum pass voltage relates to the clipped output voltage of an NMOS device when the switch input voltage is equal to the supply voltage.

R_{ON}

Ohmic Resistance Offered by a Switch in the ON State. It is measured at a given voltage by forcing a specified amount of current through the switch.

ΔR_{ON}

On Resistance Match between Any Two Channels, that is, R_{ON} Max – R_{ON} Min.

C_X OFF

OFF Switch Capacitance.

C_X ON

ON Switch Capacitance.

C_{IN}

Control Input Capacitance. This consists of $\overline{BE}$ and $\overline{SEL}$.

I_{CC}

Quiescent Power Supply Current. It is measured when all control inputs are at a logic HIGH or LOW level and the switches are OFF.

ΔI_{CC}

Extra power supply current component for the $\overline{BE}$ control input when the input is not driven at the supplies.

t_{PLH}, t_{PHL}

Data Propagation Delay through the Switch in the ON State. Propagation delay is related to the RC time constant $R_{ON} \times C_L$, where CL_L is the load capacitance.

t_{PZH}, t_{PZL}

Bus Enable Times. These are times taken to cross the V_T voltage at the switch output when the switch turns on in response to the control signal, $\overline{BE}$.

t_{PHZ}, t_{PLZ}

Bus Disable Times. This is the time taken to place the switch in the high impedance OFF state in response to the control signal. It is measured as the time taken for the output voltage to change by V_Δ from the original quiescent level, with reference to the logic level transition at the control input. (Refer to Figure 27 for enable and disable times.)

Max Data Rate

Maximum Rate at which Data Can be Passed through the Switch.

Channel Jitter

Peak-to-Peak Value of the Sum of the Deterministic and Random Jitter of the Switch Channel.

$f_{\overline{BE}}$

Operating Frequency of Bus Enable. This is the maximum frequency at which bus enable ($\overline{BE}$) can be toggled.

APPLICATIONS INFORMATION

BUS SWITCH APPLICATIONS

Bus switches can used to provide an ideal solution for interfacing between mixed voltage systems. The ADG3246 is suitable for applications where voltage translation from 3.3 V technology to a lower voltage technology is needed. This device can translate from 3.3 V to 1.8 V, from 2.5 V to 1.8 V, or from 3.3 V directly to 2.5 V.

Figure 28 shows a block diagram of a typical application in which a user needs to interface between a 3.3 V ADC and a 2.5 V microprocessor. The microprocessor may not have 3.3 V tolerant inputs, therefore placing the ADG3246 between the two devices allows the devices to communicate easily. The bus switch directly connects the two blocks, thus introducing minimal propagation delay, timing skew, or noise.

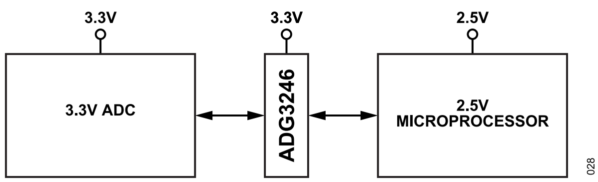


Figure 28. Level Translation Between a 3.3 V ADC and a 2.5 V Microprocessor

Mixed Voltage Operation, Level Translation

3.3 V to 2.5 V Translation

When V_{CC} is 3.3 V ($\overline{SEL}$ = V_{CC}) and the input signal range is 0 V to V_{CC}, the maximum output signal will be clamped to within a voltage threshold below the V_{CC} supply.

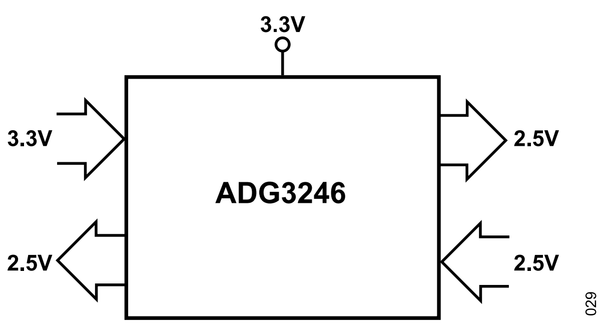


Figure 29. 3.3 V to 2.5 V Voltage Translation, $\overline{SEL}$ = V_{CC}

In this case, the output will be limited to 2.5 V, as shown in Figure 30.

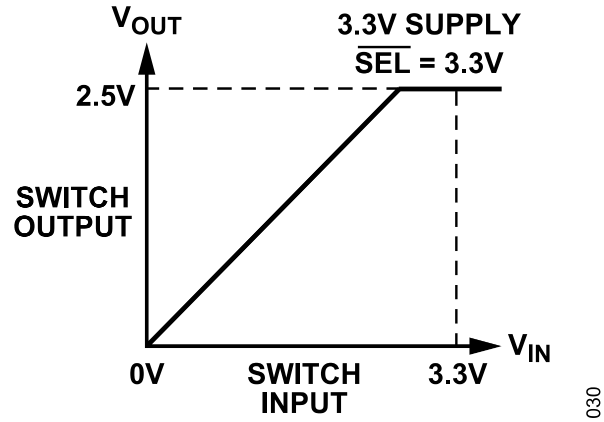


Figure 30. 3.3 V to 2.5 V Voltage Translation, $\overline{SEL}$ = V_{CC}

This device can be used for translation from 2.5 V to 3.3 V devices and also between two 3.3 V devices.

2.5 V to 1.8 V Translation

When V_{CC} is 2.5 V ($\overline{SEL}$ = V_{CC}) and the input signal range is 0 V to V_{CC}, the maximum output signal will, as before, be clamped to within a voltage threshold below the V_{CC} supply.

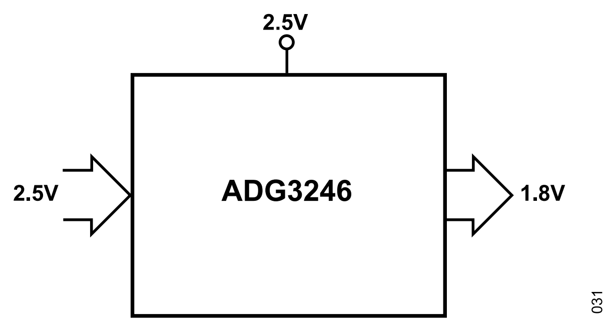


Figure 31. 2.5 V to 1.8 V Voltage Translation, $\overline{SEL}$ = V_{CC}

In this case, the output is limited to approximately 1.8 V, as shown in Figure 32.

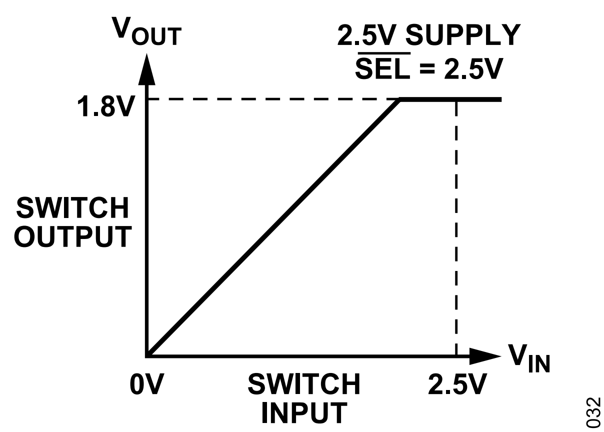


Figure 32. 2.5 V to 1.8 V Voltage Translation, $\overline{SEL}$ = V_{CC}

APPLICATIONS INFORMATION

3.3 V to 1.8 V Translation

The ADG3246 offers the option of interfacing between a 3.3 V device and a 1.8 V device. This is possible through use of the $\overline{\text{SEL}}$ pin.

$\overline{\text{SEL}}$ pin: An active low control pin. $\overline{\text{SEL}}$ activates internal circuitry in the ADG3246 that allows voltage translation between 3.3 V devices and 1.8 V devices.

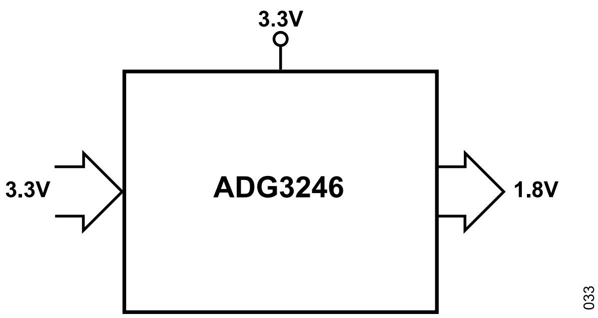


Figure 33. 3.3 V to 1.8 V Voltage Translation, $\overline{\text{SEL}}$ = 0 V

When V_{CC} is 3.3 V and the input signal range is 0 V to V_{CC}, the maximum output signal will be clamped to 1.8 V, as shown in Figure 34. To do this, the $\overline{\text{SEL}}$ pin must be tied to Logic 0. If $\overline{\text{SEL}}$ is unused, it should be tied directly to V_{CC}.

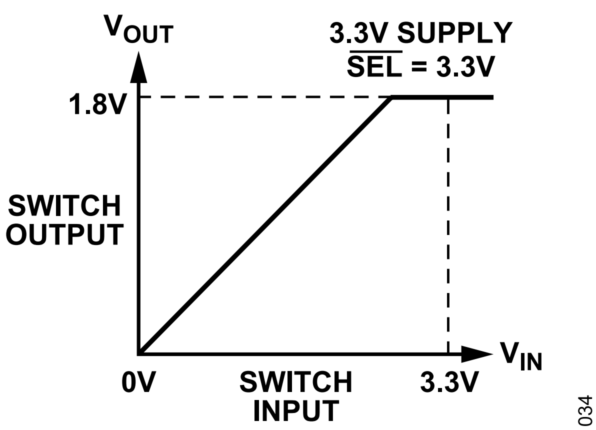


Figure 34. 3.3 V to 1.8 V Voltage Translation, $\overline{\text{SEL}}$ = 0 V

Bus Isolation

A common requirement of bus architectures is low capacitance loading of the bus. Such systems require bus bridge devices that extend the number of loads on the bus without exceeding the specifications. Because the ADG3246 is designed specifically for applications that do not need drive yet require simple logic functions, it solves this requirement. The device isolates access to the bus, thus minimizing capacitance loading.

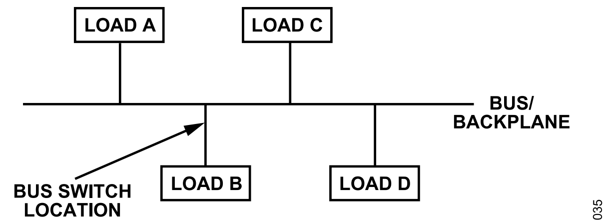


Figure 35. Location of Bus Switch in a Bus Isolation Application

Hot Plug and Hot Swap Isolation

The ADG3246 is suitable for hot swap and hot plug applications. The output signal of the ADG3246 is limited to a voltage that is below the VCC supply, as shown in Figure 30, Figure 32, and Figure 34. Therefore the switch acts like a buffer to take the impact from hot insertion, protecting vital and expensive chipsets from damage.

In hot-plug applications, the system cannot be shut down when new hardware is being added. To overcome this, a bus switch can be positioned on the backplane between the bus devices and the hot plug connectors. The bus switch is turned off during hot plug. Figure 36 shows a typical example of this type of application.

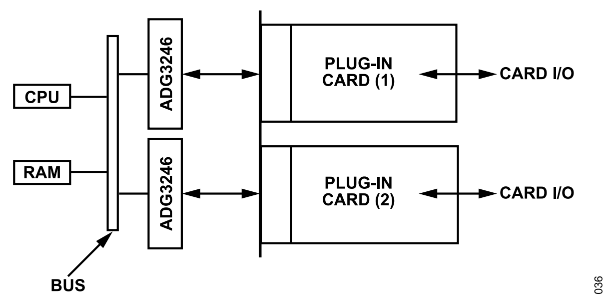


Figure 36. ADG3246 in a Hot Plug Application

There are many systems that require the ability to handle hot swapping, such as docking stations, PCI boards for servers, and line cards for telecommunications switches. If the bus can be isolated prior to insertion or removal, then there is more control over the hot swap event. This isolation can be achieved using a bus switch. The bus switches are positioned on the hot swap card between the connector and the devices. During hot swap, the ground pin of the hot swap card must connect to the ground pin of the back plane before any other signal or power pins.

Analog Switching

Bus switches can be used in many analog switching applications, for example, video graphics. Bus switches can have lower on resistance, smaller ON and OFF channel capacitance and thus improved frequency performance than their analog counterparts. The bus switch channel itself consisting solely of an NMOS switch limits the operating voltage (see Figure 3 for a typical plot), but in many cases, this does not present an issue.

APPLICATIONS INFORMATION

High Impedance During Power-Up and Power-Down

To ensure the high impedance state during power-up or power-down, $\overline{BE}$ should be tied to V_{CC} through a pull-up resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

PACKAGE AND PINOUT

The ADG3246 is packaged in a tiny 24-lead LFCSP package. The area of the LFCSP option is 16 mm^2. This makes the LFCSP option an excellent choice for space-constrained applications.

OUTLINE DIMENSIONS

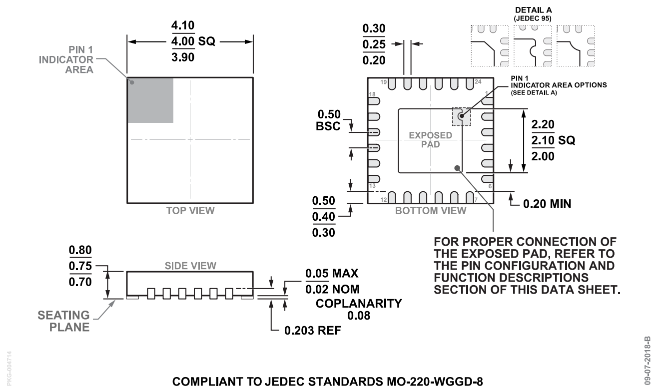


Figure 37. 24-Lead Lead Frame Chip Scale Package (LFCSP)
4 mm × 4 mm Body and 0.75 mm Package Height
(CP-24-10)
Dimension shown in millimeters

Updated: April 30, 2022

ORDERING GUIDE

Model[1]	Temperature Range	Package Description	Packing Quantity	Package Option
ADG3246BCPZ	-40°C to +105°C	24-Lead LFCSP (4mm x 4mm x 0.75mm w/ EP)		CP-24-10
ADG3246BCPZ-REEL7	-40°C to +105°C	24-Lead LFCSP (4mm x 4mm x 0.75mm w/ EP)	Reel, 1500	CP-24-10

1 Z = RoHS Compliant Part.