Data Sheet

ADAQ4003

18-Bit, 2 MSPS, µModule Data Acquisition Solution

FEATURES

- Improved design journey
  - Fully differential ADC driver with selectable input range
    - Input ranges with 5 V V_{REF}: ±10 V, ±5 V, or ±2.5 V
  - Essential passive components included
    - ±0.005% *i*Passives matched resistor array
  - Wide input common-mode voltage range
  - High common-mode rejection ratio
  - Single-ended to differential conversion
- Increased signal chain density
  - Small, 7 mm × 7 mm, 0.80 mm pitch, 49-ball CSP_BGA
    - 4× footprint reduction vs. discrete solution
  - On-board reference buffer with V_{CM} generation
- High performance
  - Throughput: 2 MSPS, no pipeline delay
  - Guaranteed 18-bit no missing codes
  - INL: ±3 ppm typical, ±8 ppm guaranteed
  - SINAD: 99 dB typical (G = 0.454)
  - Offset error drift: 0.7 ppm/°C typical (G = 0.454)
  - Gain error drift: ±0.5 ppm/°C typical
- Low total power consumption: 51.6 mW typical at 2 MSPS
- SPI-/QSPI-/MICROWIRE-/DSP-compatible serial interface
  - Versatile logic interface supply with 1.8 V, 2.5 V, 3 V, or 5 V

APPLICATIONS

- Automatic test equipment
- Machine automation
- Process controls
- Medical instrumentation
- Digital control loops

FUNCTIONAL BLOCK DIAGRAM

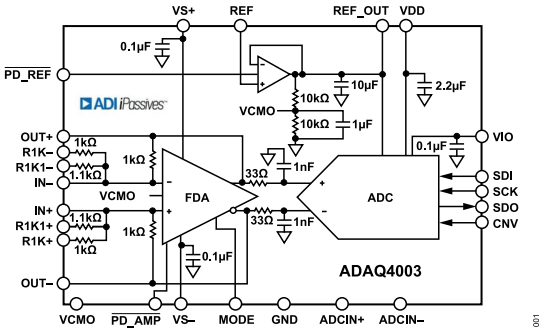

Figure 1.

GENERAL DESCRIPTION

The ADAQ4003 is a µModule® precision data acquisition (DAQ), signal chain solution that reduces the development cycle of a precision measurement system by transferring the signal chain design challenge of component selection, optimization, and layout from the designer to the device.

Using system-in-package (SIP) technology, the ADAQ4003 reduces end system component count by combining multiple common signal processing and conditioning blocks into a single device. These blocks include a high resolution 18-bit, 2 MSPS successive approximation register (SAR), analog-to-digital converter (ADC), a low noise, fully differential ADC driver amplifier (FDA), and a stable reference buffer.

Using Analog Devices, Inc., *i*Passives® technology, the ADAQ4003 also incorporates crucial passive components with superior matching and drift characteristics to minimize temperature dependent error sources and to offer optimized performance (see Figure 1). Housing this signal chain solution in a small, 7 mm × 7 mm, 0.80 mm pitch, 49-ball CSP_BGA enables compact form factor designs without sacrificing performance and simplifies end system bill of materials management. This level of system integration makes the ADAQ4003 much less sensitive to printed circuit board (PCB) layout while still providing flexibility to adapt to a wide range of signal levels.

The serial peripheral interface (SPI)-compatible, serial user interface is compatible with 1.8 V, 2.5 V, 3 V, or 5 V logic, using a separate VIO supply. Specified operation of ADAQ4003 is from −40°C to +125°C.

Table 1. µModule Data Acquisition Solutions

Type	500 kSPS	≥1000 kSPS
16-Bit	ADAQ7988	ADAQ7980
18-Bit		ADAQ4003

Rev. A

DOCUMENT FEEDBACK

TECHNICAL SUPPORT

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2/2022—Rev. 0 to Rev. A

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9/2020—Revision 0: Initial Version

SPECIFICATIONS

VDD = 1.8 V ± 5%, VS+ = 5.5 V ± 5%, VS− = 0 V, VIO = 1.7 V to 5.5 V, reference voltage (V_{REF}) = 5 V, sampling frequency (f_S) = 2 MSPS, all specifications T_{MIN} to T_{MAX}, high-Z mode disabled, span compression disabled, and turbo mode enabled, unless otherwise noted. ADC driver configured in single-ended to differential configuration and fast mode, unless otherwise noted.

Table 2.

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
RESOLUTION		18			Bit
ANALOG INPUTS	IN+, IN−, R1K1+, R1K1−, R1K+, and R1K−				
Input Impedance (Z_{IN})	Single-ended to differential configuration				
	G = 0.454, input voltage (V_{IN}) = 22 V p-p		1.3		kΩ
	G = 0.909, V_{IN} = 11 V p-p		1.44		kΩ
	G = 1, V_{IN} = 10 V p-p		1.33		kΩ
	G = 1.9, V_{IN} = 5.2 V p-p		778		Ω
	Fully differential configuration				
	G = 0.454 and G = 0.909, V_{IN} = 22 V p-p and 11 V p-p		1.1		kΩ
	G = 1, V_{IN} = 10 V p-p		1		kΩ
	G = 1.9, V_{IN} = 5.2 V p-p		523		Ω
Differential Input Voltage Ranges[1]	G = 0.454, V_{IN} = 22 V p-p	−2.2 × V_{REF}		+2.2 × V_{REF}	V
	G = 0.909, V_{IN} = 11 V p-p	−1.1 × V_{REF}		+1.1 × V_{REF}	V
	G = 1, V_{IN} = 10 V p-p	−V_{REF}		+V_{REF}	V
	G = 1.9, V_{IN} = 5.2 V p-p	−0.526 × V_{REF}		+0.526 × V_{REF}	V
Input Capacitance	IN+ and IN−		15		pF
THROUGHPUT					
Complete Cycle		500			ns
Conversion Time			290	320	ns
Acquisition Phase[2]		290			ns
Throughput Rate[3]		0		2	MSPS
Transient Response[4]			40		µs
DC ACCURACY	Single-ended to differential configuration				
No Missing Codes		18			Bits
Integral Linearity Error (INL)	All gains, VS− = −1 V	−8	±3	+8	ppm
		−2.1	±0.8	+2.1	LSB[5]
Differential Linearity Error (DNL)	All gains, VS− = −1 V	−1	±0.4	+1	LSB[5]
		−3.8	±2.66	+3.8	ppm
Transition Noise	G = 0.454		0.93		LSB
	G = 0.909 and G = 1		1.24		LSB
	G = 1.9		1.10		LSB
Gain Error	All gains	−0.05	±0.005	+0.05	%FS
Gain Error Drift	All gains	−3	±0.5	+3	ppm/°C
Offset Error	G = 0.454	−1	±0.1	+1	mV
	G = 0.909, G = 1	−0.9	±0.06	+0.9	mV
	G = 1.9	−1.5	±0.01	+1.5	mV
Offset Error Drift	G = 0.454	−8	+0.7	+8	ppm/°C
	G = 0.909 and G = 1	−10	+1.6	+10	ppm/°C
	G = 1.9	−15	+2.6	+15	ppm/°C
Common-Mode Rejection Ratio (CMRR)	Fully differential configuration, all gains		90		dB
Power Supply Rejection Ratio (PSRR)					
Positive	VDD = 1.71 V to 1.89 V		72		dB
	VS+ = 5.225 V to 5.775 V, VS− = 0 V		110		dB
Negative	VS+ = +5.5 V, VS− = 0 V to −0.5 V		107		dB

SPECIFICATIONS

Table 2.

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
1/f Noise[6]	Referred to input, bandwidth = 0.1 Hz to 10 Hz, normalized to 0 V, all gains		2		µV p-p
Input Current Noise	Input frequency (f_{IN}) = 100 kHz		1		pA/√Hz
AC ACCURACY	Single-ended to differential and fully differential configuration				
Dynamic Range	All gains, −60 dBFS	94.5			dB
	G = 0.454		100		dB
	G = 0.909 and G = 1		97.5		dB
	G = 1.9		98.5		dB
Oversampled Dynamic Range	Oversampling ratio (OSR) = 2, all gains		103		dB
	OSR = 256, all gains		122		dB
Total RMS Noise (Referred to Output (RTO))	G = 0.454		35.4		µV rms
	G = 0.909 and G = 1		47.1		µV rms
	G = 1.9		42		µV rms
Noise Spectral Density[7]	G = 0.454		13.4		nV/√Hz
	G = 0.909 and G = 1		17.9		nV/√Hz
	G = 1.9		16		nV/√Hz
Signal-to-Noise Ratio (SNR)	f_{IN} = 1 kHz, −0.5 dBFS	94.2			dB
	G = 0.454		99.5		dB
	G = 0.909 and G =1		97		dB
	G = 1.9		98		dB
	f_{IN} = 100 kHz, G = 0.909		95.3		dB
	f_{IN} = 400 kHz, G = 0.909		88.3		dB
	Low power mode enabled, G = 0.909		96		dB
	VS+ = 3.3 V, VS− = 0 V, V_{REF} = 2.5 V, G = 0.909		92		dB
Signal-to-Noise + Distortion (SINAD)	f_{IN} = 1 kHz, −0.5 dBFS	94			dB
	G = 0.454		99		dB
	G = 0.909 and G =1		96.5		dB
	G = 1.9		97.5		dB
	f_{IN} = 100 kHz, G = 0.909		94.9		dB
	f_{IN} = 400 kHz, G = 0.909		85.7		dB
	Low power mode enabled, G = 0.909		95.5		dB
	VS+ = 3.3 V, VS− = 0 V, V_{REF} = 2.5 V, G = 0.909		91.5		dB
Total Harmonic Distortion (THD)	f_{IN} = 1 kHz, −0.5 dBFS, all gains		−120		dB
	f_{IN} = 100 kHz, G = 0.909		−100		dB
	f_{IN} = 400 kHz, G = 0.909		−95		dB
	Low power mode enabled, G = 0.909		−110		dB
	VS+ = 3.3 V, VS− = 0 V, V_{REF} = 2.5 V, G = 0.909		−118		dB
Spurious-Free Dynamic Range (SFDR)	f_{IN} = 1 kHz, −0.5 dBFS, all gains		122		dB
	f_{IN} = 100 kHz, G = 0.909		101		dB
	f_{IN} = 400 kHz, G = 0.909		95		dB
	Low power mode enabled, G = 0.909		110		dB
	VS+ = 3.3 V, VS− = 0 V, V_{REF} = 2.5 V, G = 0.909		118		dB
−3 dB Input Bandwidth			4.4		MHz
Aperture Delay			1		ns
Aperture Jitter			1		ps rms
REFERENCE					
V_{REF} Range	Buffer enabled	2.4		5.1 or VS+ − 0.08	V
Input Current (I_{REF})	Buffer enabled		60		µA

SPECIFICATIONS

Table 2.

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
REF_OUT Current (I_{REF_OUT})	Buffer disabled, 2 MSPS, V_{REF} = 5 V		1.27		mA
VCMO					
VCMO Voltage (V_{VCMO})[8]		$V_{REF}/2 - 0.003$	$V_{REF}/2$	$V_{REF}/2 + 0.003$	V
Output Impedance			5		kΩ
DIGITAL INPUTS	SDI, SCK, and CNV				
Logic Levels					
Input Low Voltage (V_{IL})	VIO > 2.7 V	−0.3		+0.3 × VIO	V
	VIO ≤ 2.7 V	−0.3		+0.2 × VIO	V
Input High Voltage (V_{IH})	VIO > 2.7 V	0.7 × VIO		VIO + 0.3	V
	VIO ≤ 2.7 V	0.8 × VIO		VIO + 0.3	V
Input Low Current (I_{IL})		−1		+1	µA
Input High Current (I_{IH})		−1		+1	µA
Input Pin Capacitance			6		pF
DIGITAL OUTPUTS[9]					
Data Format			Twos complement		
Output Low Voltage (V_{OL})	Sink current (I_{SINK}) = +500 µA			0.4	V
Output High Voltage (V_{OH})	Source current (I_{SOURCE}) = −500 µA	VIO − 0.3			V
POWER-DOWN AND MODE SIGNALING					
FDA and Reference Buffer					
$\overline{PD\_AMP}$, $\overline{PD\_REF}$, and MODE Voltage					
Low	Powered down, low power mode		<1		V
High	Enabled, normal mode		>1.7		V
Turn-On Time	All devices enabled				
	Low to high[10]		120		µs
	High[11]		1		µs
POWER REQUIREMENTS					
VDD		1.71	1.8	1.89	V
VS+		3	5.5	VS− + 10	V
VS−		VS+ − 10	0	0.1	V
VIO		1.7		5.5	V
Total Standby Current[12, 13]	Static, all devices enabled		11	14	mA
Power-Down Current	ADC driver, reference buffer disabled		100	250	nA
Power Dissipation	VDD = VIO = 1.8 V, VS+ = 5.5 V, VS− = 0 V				
VS+			41.5	51.5	mW
VDD			9.5	12	mW
VIO			0.6	0.7	mW
Total			51.6	64.2	mW
	VDD = VIO = 1.8 V, VS+ = 5 V, VS− = 0 V, high-Z mode enabled				
VS+			44	53	mW
VDD			12.8	16.5	mW
VIO			0.6	0.7	mW
Total			57.4	70.2	mW
TEMPERATURE RANGE					
Specified Performance	T_{MIN} to T_{MAX}	−40		+125	°C

[1] V_{IN} must be within the allowed input common-mode range as per Figure 35, Figure 36, and Figure 37 and is dependent on the VS+ and VS− supply rails used.

[2] The acquisition phase is the time available for the input sampling capacitors to acquire a new input with the ADC running at a throughput rate of 2 MSPS.

SPECIFICATIONS

Table 2.

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit

[3] A throughput rate of 2 MSPS can only be achieved with turbo mode enabled and a minimum SCK rate of 75 MHz. Refer to Table 5 for the maximum achievable throughput for different modes of operation.

[4] Transient response is the time required for the ADAQ4003 to acquire a full-scale input step to ±1 LSB accuracy.

[5] The weight of the LSB, referred to input, changes depending on the input voltage range. See Table 10 for the LSB size.

[6] See the 1/f noise plot in Figure 28.

[7] Noise Spectral Density for each gain can be calculated using the equation: Total RMS Noise (RTO)/√(π/2 × bandwidth), where bandwidth is the −3 dB Input Bandwidth equal to 4.4 MHz.

[8] The VCMO voltage can be used for other circuitry, but it should be driven with a buffer to ensure the VCMO voltage remains stable as per the specified range.

[9] There is no pipeline delay. Conversion results are available immediately after a conversion is completed.

[10] The time it takes for a reference buffer to charge a 10 µF reference capacitor to 90% of the reference voltage.

[11] The time it takes for the FDA to charge the 1 nF filter capacitor to 90% of the final value.

[12] With all digital inputs forced to VIO or GND as required.

[13] The total standby current during the acquisition phase.

TIMING SPECIFICATIONS

VDD = 1.8 V ± 5%, VS+ = 5.5 V ± 5%, VS− = 0 V, VIO = 1.71 V to 5.5V, V_{REF} = 5 V, f_S = 2 MSPS, all specifications T_{MIN} to T_{MAX}, high-Z mode disabled, span compression disabled, and turbo mode enabled, unless otherwise noted.

Table 3. Digital Interface Timing

Parameter	Symbol	Min	Typ	Max	Unit
Conversion Time—CNV Rising Edge to Data Available	t_{CONV}		290	320	ns
Acquisition Phase[1]	t_{ACQ}	290			ns
Time Between Conversions	t_{CYC}	500			ns
CNV Pulse Width ($\overline{CS}$ Mode)[2]	t_{CNVH}	10			ns
SCK Period ($\overline{CS}$ Mode)[3]	t_{SCK}				
VIO > 2.7 V		9.8			ns
VIO > 1.7 V		12.3			ns
SCK Period (Daisy-Chain Mode)[4]	t_{SCK}				
VIO > 2.7 V		20			ns
VIO > 1.7 V		25			ns
SCK Low Time	t_{SCKL}	3			ns
SCK High Time	t_{SCKH}	3			ns
SCK Falling Edge to Data Remains Valid Delay	t_{HSDO}	1.5			ns
SCK Falling Edge to Data Valid Delay	t_{DSDO}				
VIO > 2.7 V				7.5	ns
VIO > 1.7 V				10.5	ns
CNV or SDI Low to SDO D17 MSB Valid Delay ($\overline{CS}$ Mode)	t_{EN}				
VIO > 2.7 V				10	ns
VIO > 1.7 V				13	ns
CNV Rising Edge to First SCK Rising Edge Delay	t_{QUIET1}	190			ns
Last SCK Falling Edge to CNV Rising Edge Delay	t_{QUIET2}	60			ns
CNV or SDI High or Last SCK Falling Edge to SDO High Impedance ($\overline{CS}$ Mode)	t_{DIS}			20	ns
SDI Valid Setup Time from CNV Rising Edge	$t_{SSDICNV}$	2			ns
SDI Valid Hold Time from CNV Rising Edge ($\overline{CS}$ Mode)	$t_{HSDICNV}$	2			ns
SCK Valid Hold Time from CNV Rising Edge (Daisy-Chain Mode)	$t_{HSCKCNV}$	12			ns
SDI Valid Setup Time from SCK Rising Edge (Daisy-Chain Mode)	$t_{SSDISCK}$	2			ns

SPECIFICATIONS

Table 3. Digital Interface Timing

Parameter	Symbol	Min	Typ	Max	Unit
SDI Valid Hold Time from SCK Rising Edge (Daisy-Chain Mode)	$t_{HSDISCK}$	2			ns

[1] The acquisition phase is the time available for the input sampling capacitors to acquire a new input with the ADC running at a throughput rate of 2 MSPS.

[2] For turbo mode, t_{CNVH} must match the t_{QUIET1} minimum.

[3] A throughput rate of 2 MSPS can only be achieved with turbo mode enabled and a minimum SCK rate of 75 MHz.

[4] A 50% duty cycle is assumed for SCK.

Table 4. Register Read and Write Timing

Parameter	Symbol	Min	Typ	Max	Unit
READ AND WRITE OPERATION					
CNV Pulse Width[1]	t_{CNVH}	10			ns
SCK Period	t_{SCK}				
VIO > 2.7 V		9.8			ns
VIO > 1.7 V		12.3			ns
SCK Low Time	t_{SCKL}	3			ns
SCK High Time	t_{SCKH}	3			ns
READ OPERATION					
CNV Low to SDO D17 MSB Valid Delay	t_{EN}				
VIO > 2.7 V				10	ns
VIO > 1.7 V				13	ns
SCK Falling Edge to Data Remains Valid	t_{HSDO}	1.5			ns
SCK Falling Edge to Data Valid Delay	t_{DSDO}				
VIO > 2.7 V				7.5	ns
VIO > 1.7 V				10.5	ns
CNV Rising Edge to SDO High Impedance	t_{DIS}			20	ns
WRITE OPERATION					
SDI Valid Setup Time from SCK Rising Edge	$t_{SSDISCK}$	2			ns
SDI Valid Hold Time from SCK Rising Edge	$t_{HSDISCK}$	2			ns
CNV Rising Edge to SCK Edge Hold Time	$t_{HCNVSCK}$	0			ns
CNV Falling Edge to SCK Active Edge Setup Time	$t_{SCNVSCK}$	6			ns

[1] For turbo mode, t_{CNVH} must match the t_{QUIET1} minimum.

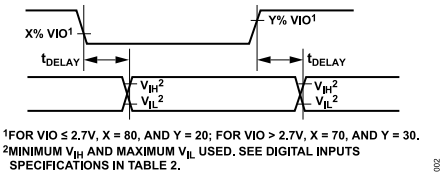

Figure 2. Voltage Levels for Timing

Table 5. Achievable Throughput for Different Modes of Operation

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
THROUGHPUT, $\overline{CS}$ MODE					
3-Wire and 4-Wire Turbo Mode	f_{SCK} = 100 MHz, VIO ≥ 2.7 V			2	MSPS
	f_{SCK} = 80 MHz, VIO < 2.7 V			2	MSPS
3-Wire and 4-Wire Turbo Mode and Six Status Bits	f_{SCK} = 100 MHz, VIO ≥ 2.7 V			2	MSPS
	f_{SCK} = 80 MHz, VIO < 2.7 V			1.78	MSPS
3-Wire and 4-Wire Mode	f_{SCK} = 100 MHz, VIO ≥ 2.7 V			1.75	MSPS

SPECIFICATIONS

Table 5. Achievable Throughput for Different Modes of Operation

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
3-Wire and 4-Wire Mode and Six Status Bits	f_{SCK} = 80 MHz, VIO < 2.7 V			1.62	MSPS
	f_{SCK} = 100 MHz, VIO ≥ 2.7 V			1.59	MSPS
	f_{SCK} = 80 MHz, VIO < 2.7 V			1.44	MSPS

ABSOLUTE MAXIMUM RATINGS

Table 6.

Parameter	Rating
Analog Inputs	
R1K+, R1K−, R1K1+, R1K1− to GND	−16 V to +16 V or ±18 mA
Supply Voltage	
REF_OUT and VIO to GND	−0.3 V to +6.0 V
VDD to GND	−0.3 V to +2.1 V
VDD to VIO	−6 V to +2.4 V
VS+ to VS−	11 V
VS+ to GND	−0.3 V to +11 V
VS− to GND	−11 V to +0.3 V
Digital Inputs to GND	−0.3 V to VIO + 0.3 V
Digital Outputs to GND	−0.3 V to VIO + 0.3 V
Temperature	
Storage Range	−65°C to +150°C
Junction	150°C
Lead Soldering	260°C reflow as per JEDEC J-STD-020

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

THERMAL RESISTANCE

Thermal performance is directly linked to PCB design and operating environment. Careful attention to PCB thermal design is required.

Table 7. Thermal Resistance

Package Type[1]	θ_{JA}	θ_{JC_TOP}	θ_{JC_BOTTOM}	θ_{JB}	Ψ_{JT}	Ψ_{JB}	Unit
BC-49-5	53.5	54.9	58.7	28.8	15.6	28.6	°C/W

[1] Test Condition 1: thermal impedance simulated values are based upon use of a 2S2P JEDEC standard PCB configuration per JEDEC Standard JESD51-7.

ELECTROSTATIC DISCHARGE (ESD) RATINGS

The following ESD information is provided for handling of ESD-sensitive devices in an ESD protected area only.

Human body model (HBM) per ANSI/ESDA/JEDDEC JS-001.

Field induced charged device model (FICDM) per ANSI/ ESDA/JEDEC JS-002.

ESD Ratings for ADAQ4003

Table 8. ADAQ4003, 49-Ball CSP_BGA

ESD Model	Withstand Threshold (V)	Class
HBM	4000	2
FICDM	1000	C4

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

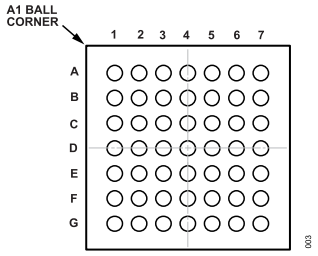

Figure 3. Ball Configuration, Top View

	1	2	3	4	5	6	7
A	GND	VDD	OUT+	VS−	REF_OUT	REF	GND
B	R1K−	R1K−	OUT+	VS−	GND	VIO	VIO
C	R1K1−	R1K1−	VS−	VS−	DNC	$\overline{\text{PD\_AMP}}$	SDI
D	IN−	IN+	DNC	DNC	DNC	$\overline{\text{PD\_REF}}$	SCK
E	R1K1+	R1K1+	MODE	VS+	ADCIN+	GND	SDO
F	R1K+	R1K+	OUT−	VS+	DNC	DNC	CNV
G	GND	VCMO	OUT−	VS+	VS+	ADCIN−	GND

004

Figure 4. Ball Configuration

Table 9. Ball Function Descriptions

Ball No.	Mnemonic	Type[1]	Description
A1, A7, B5, E6, G1, G7	GND	P	Power Supply Ground.
A2	VDD	P	1.8 V Power Supply. The VDD range is 1.71 V to 1.89 V.
A3, B3	OUT+	AO	Positive Output of the Fully Differential ADC Driver.
A4, B4, C3, C4	VS−	P	Negative Supply of the Fully Differential ADC Driver.
A5	REF_OUT	AO	Reference Buffer Output Voltage.
A6	REF	AI	Reference Buffer Input Voltage.
B1, B2	R1K−	AI	1 kΩ Resistor Input to Negative Input of the Fully Differential ADC Driver.
B6, B7	VIO	P	Input and Output Interface Digital Power. Nominally, the VIO pins are at the same supply as the host interface (1.8 V, 2.5 V, 3 V, or 5 V).
C1, C2	R1K1−	AI	1.1 kΩ Resistor Input to Negative Input of the Fully Differential ADC Driver.
C5, D3 to D5, F5, F6	DNC	N/A	Do Not Connect. Do not connect to this pin.
C6	$\overline{\text{PD\_AMP}}$	DI	Power-Down Amplifier. Active low. Connect the $\overline{\text{PD\_AMP}}$ pin to GND to power down the fully differential ADC driver. Otherwise, connect the $\overline{\text{PD\_AMP}}$ pin to logic high.
C7	SDI	DI	Serial Data Input. This input provides multiple features. SDI selects the interface mode of the ADC as follows: Daisy-chain mode is selected if SDI is low during the CNV rising edge. In this mode, SDI is used as a data input to daisy-chain the conversion results of two or more ADCs onto a single SDO line. The digital data level on SDI is output on SDO with a delay of 18 SCK cycles. $\overline{\text{CS}}$ mode is selected if SDI is high during the CNV rising edge. In this mode, either SDI or CNV can enable the serial output signals when low. If SDI or CNV is low when the conversion is complete, the busy indicator feature is enabled. With CNV low, the device can be programmed by clocking in a 16-bit word on SDI on the rising edge of SCK.
D1	IN−	AI	Negative Input of the Fully Differential ADC Driver.
D2	IN+	AI	Positive Input of the Fully Differential ADC Driver.
D6	$\overline{\text{PD\_REF}}$	DI	Power-Down Reference Buffer. Active low. Connect the $\overline{\text{PD\_REF}}$ pin to GND to power down the reference buffer. Otherwise, connect the $\overline{\text{PD\_REF}}$ pin to logic high.
D7	SCK	DI	Serial Data Clock Input. When the device is selected, the conversion result is shifted out by this clock.
E1, E2	R1K1+	AI	1.1 kΩ Resistor Input to Positive Input of the Fully Differential ADC Driver.
E3	MODE	DI	Power Mode for the Fully Differential ADC Driver. Full performance when the MODE pin is high, and low power mode when the MODE pin is low.
E4, F4, G4, G5	VS+	P	Fully Differential ADC Driver and Reference Buffer Positive Supply.
E5	ADCIN+	AO	Positive Input to the ADC. Extra capacitance can be added on the ADCIN+ pin to reduce the RC filter bandwidth.
E7	SDO	DO	Serial Data Output. The conversion result is output on the SDO pin. SDO synchronizes to SCK.
F1, F2	R1K+	AI	1 kΩ Resistor Input to Positive Input of the Fully Differential ADC Driver.
F3, G3	OUT−	AO	Negative Output of the Fully Differential ADC Driver.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

Table 9. Ball Function Descriptions

Ball No.	Mnemonic	Type[1]	Description
F7	CNV	DI	Convert Input. This input has multiple functions. On its leading edge, CNV initiates the conversions and selects the interface mode of the device: daisy-chain mode or $\overline{CS}$ mode. In $\overline{CS}$ mode, the SDO pin is enabled when CNV is low. In daisy-chain mode, the data is read when CNV is high.
G2	VCMO	AO	Fully Differential ADC Driver Output Common-Mode Voltage. Nominally, $V_{REF}/2$.
G6	ADCIN−	AO	Negative Input to the ADC. Extra capacitance can be added on the ADCIN− pin to reduce the RC filter bandwidth.

[1] P is power, AO is analog output, AI is analog input, N/A is not applicable, DI is digital input, and DO is digital output.

TYPICAL PERFORMANCE CHARACTERISTICS

VS+ = 5.5 V, VS− = 0 V, VDD = 1.8 V, VIO = 3.3 V, V_{REF} = 5 V, T_A = 25°C, high-Z mode disabled, span compression disabled, turbo mode enabled, and f_S = 2 MSPS, unless otherwise noted.

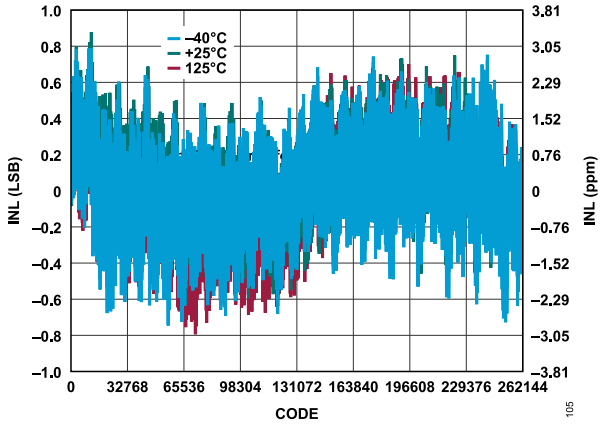

Figure 5. INL vs. Code for Various Temperatures, V_{REF} = 5 V, G = 0.454

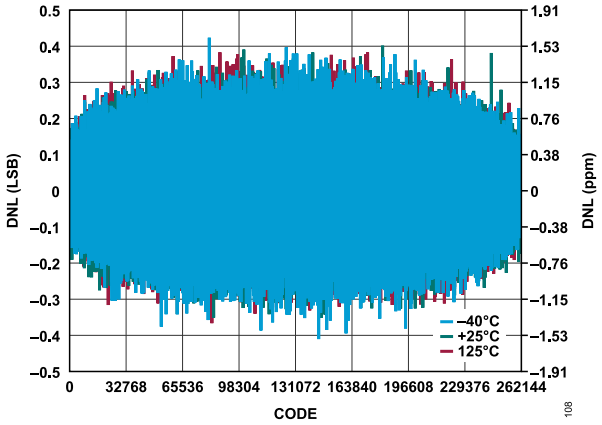

Figure 8. DNL vs. Code for Various Temperatures, V_{REF} = 5 V, G = 0.454

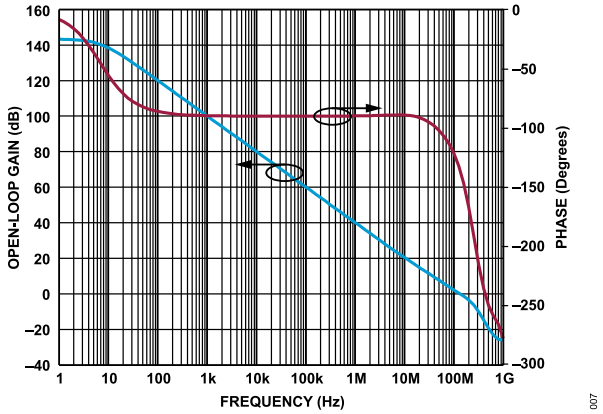

Figure 6. ADC Driver Open-Loop Gain and Phase vs. Frequency

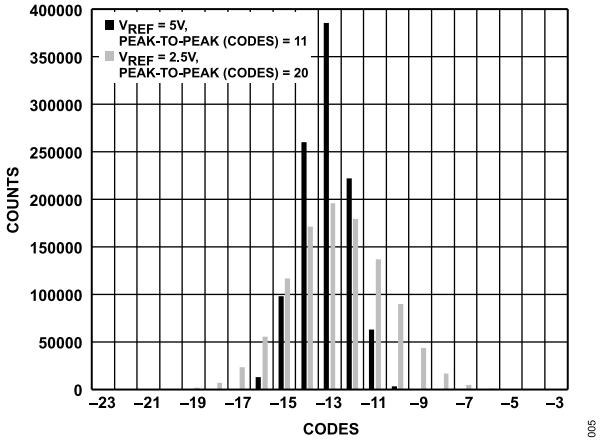

Figure 9. Histogram of a DC Input at the Code Center, V_{REF} = 2.5 V and V_{REF} = 5 V

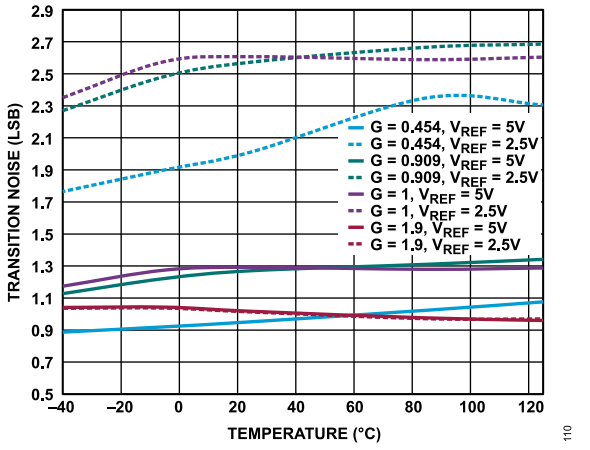

Figure 7. Transition Noise vs. Temperature for G = 0.454, G = 0.909, G = 1, and G = 1.9 and V_{REF} = 5 V and V_{REF} = 2.5 V

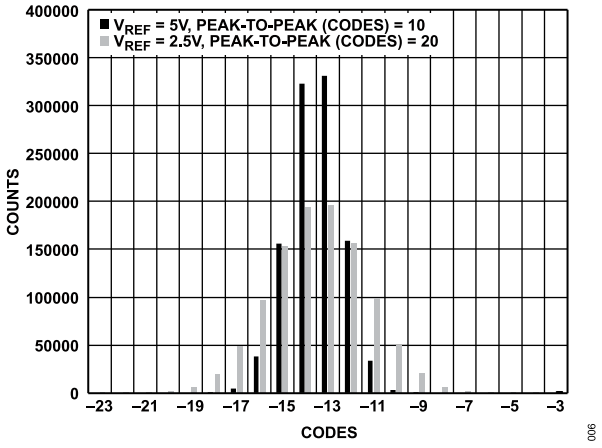

Figure 10. Histogram of a DC Input at the Code Transition, V_{REF} = 2.5 V and V_{REF} = 5 V

TYPICAL PERFORMANCE CHARACTERISTICS

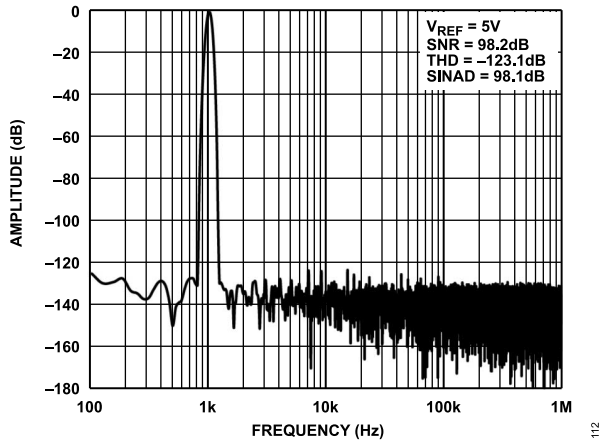

Figure 11. 1 kHz, −0.5 dBFS Input Tone Fast Fourier Transform (FFT), Wide View, G = 1, V_{REF} = 5 V, Differential

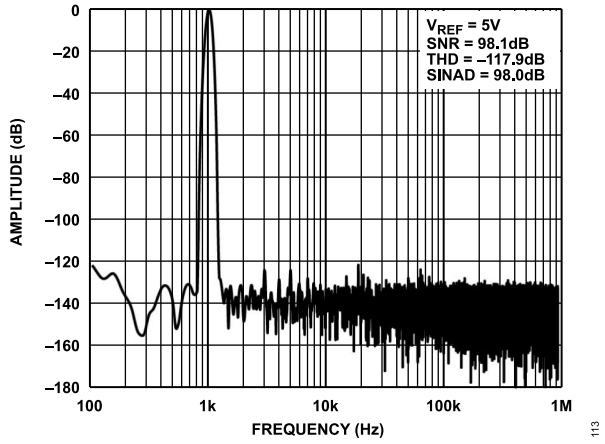

Figure 12. 1 kHz, −0.5 dBFS Input Tone FFT, Wide View, G = 1, V_{REF} = 5 V, Single-Ended

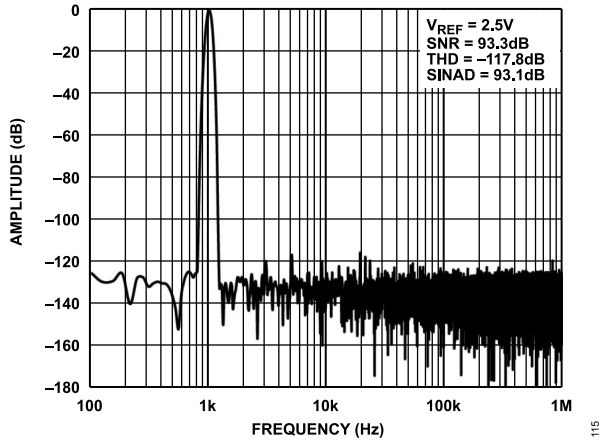

Figure 13. 1 kHz, −0.5 dBFS Input Tone FFT, Wide View, G = 1, V_{REF} = 2.5 V, Differential

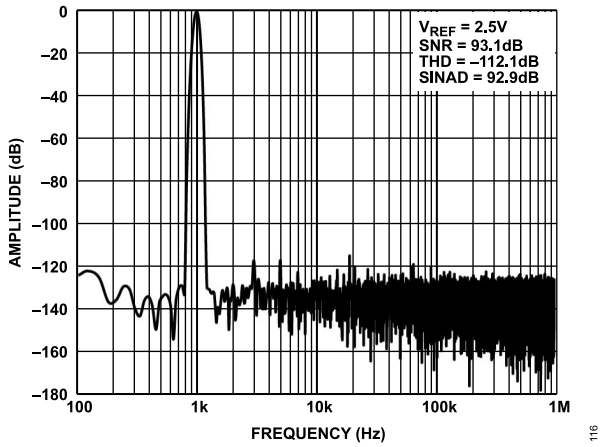

Figure 14. 1 kHz, −0.5 dBFS Input Tone FFT, Wide View, G = 1, V_{REF} = 2.5 V, Single-Ended

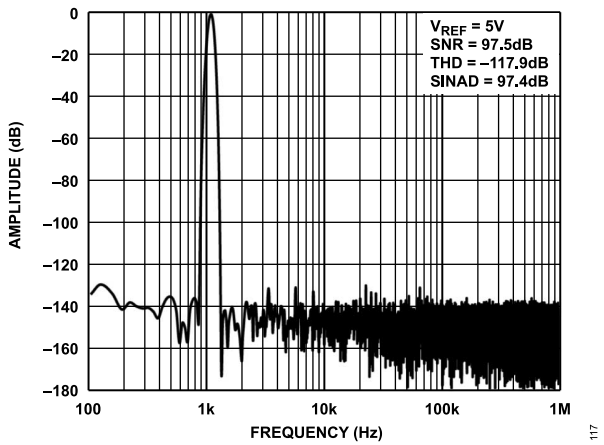

Figure 15. 1 kHz, −0.5 dBFS Input Tone FFT, Wide View, Differential, G = 0.909, V_{REF} = 5 V, Low Power Mode

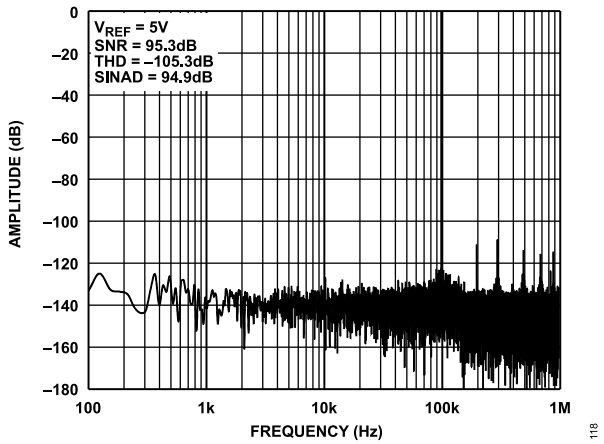

Figure 16. 100 kHz, −0.5 dBFS Input Tone FFT, Wide View, G = 1, V_{REF} = 5 V

TYPICAL PERFORMANCE CHARACTERISTICS

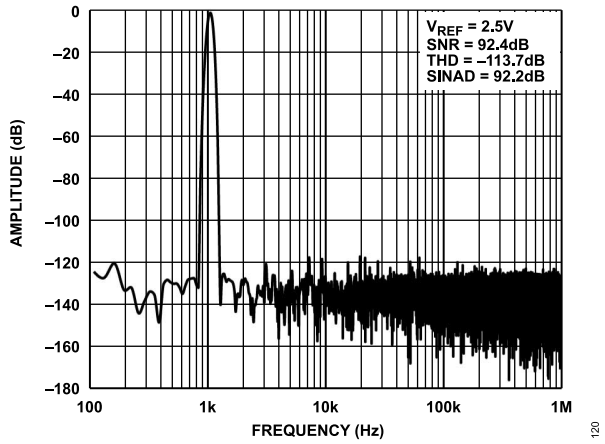

Figure 17. 1 kHz, −0.5 dBFS Input Tone FFT, Wide View, Differential, G = 0.909, V_{REF} = 2.5 V, Low Power Mode

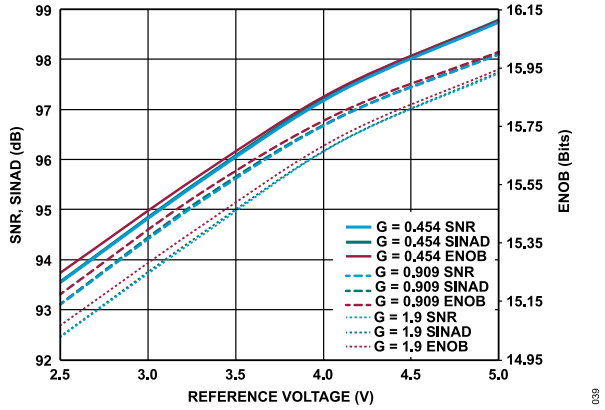

Figure 18. SNR, SINAD, and Effective Number of Bits (ENOB) vs. Reference Voltage for G = 0.454, G = 0.909, and G = 1.9, f_{IN} = 1 kHz

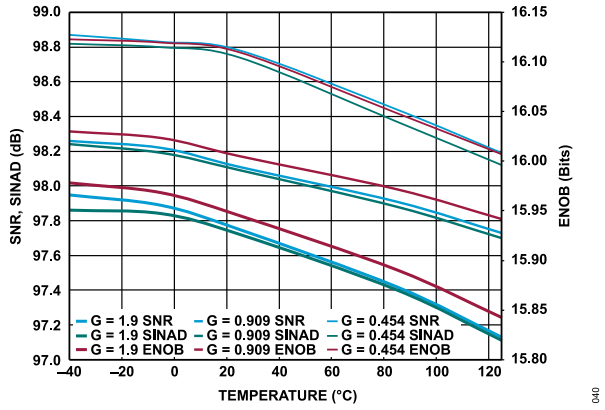

Figure 19. SNR, SINAD, and ENOB vs. Temperature, G =1.9, G = 0.909, and G = 0.454, f_{IN} = 1 kHz

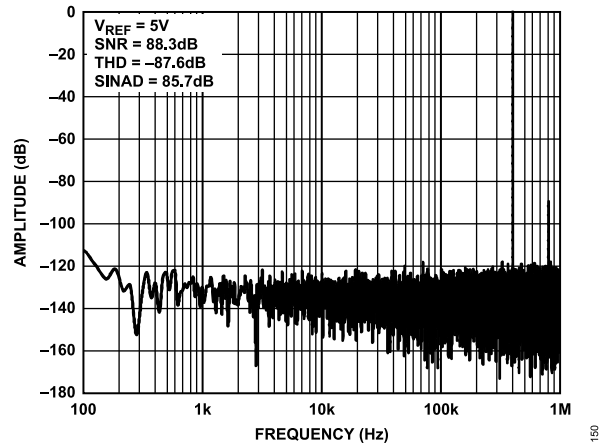

Figure 20. 400 kHz, −0.5 dBFS Input Tone FFT, G = 1, Wide View, V_{REF} = 5 V

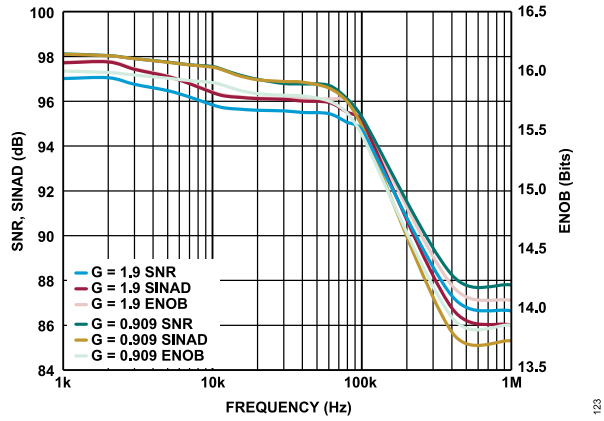

Figure 21. SNR, SINAD, and ENOB vs. Frequency for G = 1.9 and G = 0.909, V_{REF} = 5 V

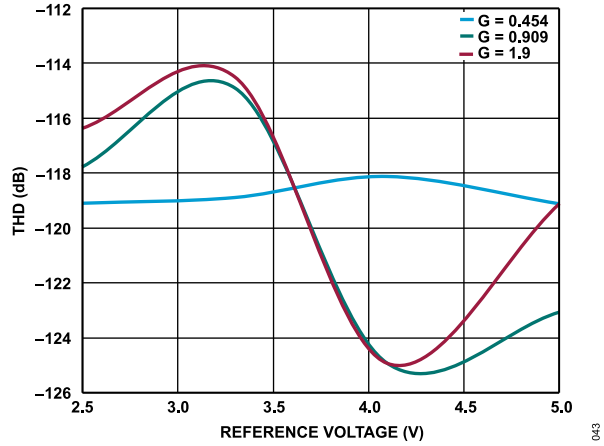

Figure 22. THD vs. Reference Voltage, G = 0.454, G = 0.909, and G = 1.9, f_{IN} = 1 kHz

TYPICAL PERFORMANCE CHARACTERISTICS

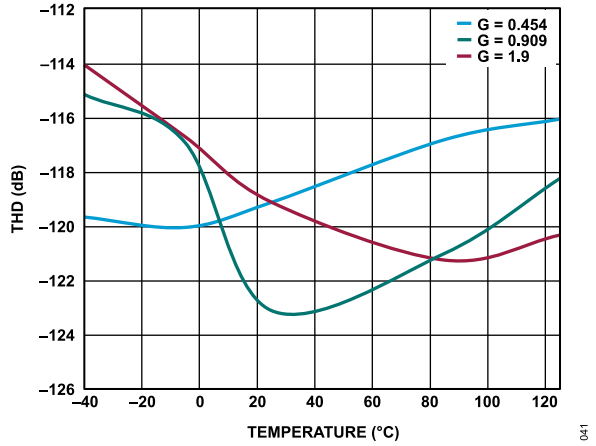

Figure 23. THD vs. Temperature for G = 0.454, G = 0.909, and G = 1.9, f_{IN} = 1 kHz

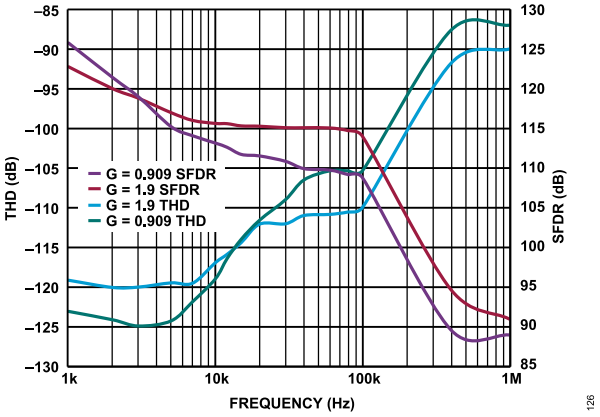

Figure 24. THD and SFDR vs. Frequency for G = 0.909 and G = 1.9, V_{REF} = 5 V

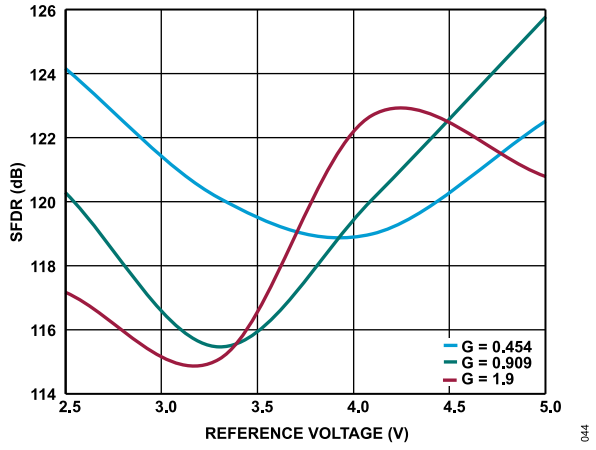

Figure 25. SFDR vs. Reference Voltage for G = 0.454, G = 0.909, and G = 1.9, f_{IN} = 1 kHz

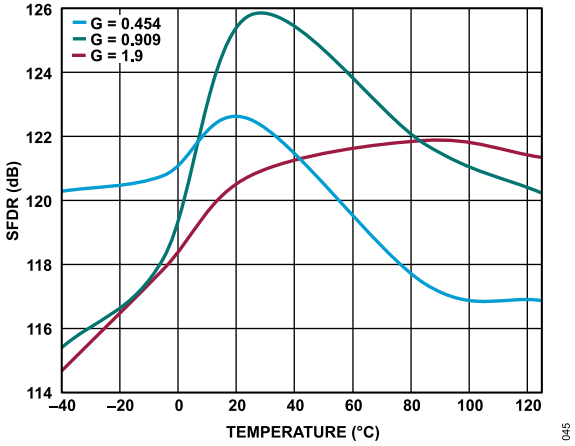

Figure 26. SFDR vs. Temperature for G = 0.454, G = 0.909, and G = 1.9, f_{IN} = 1kHz

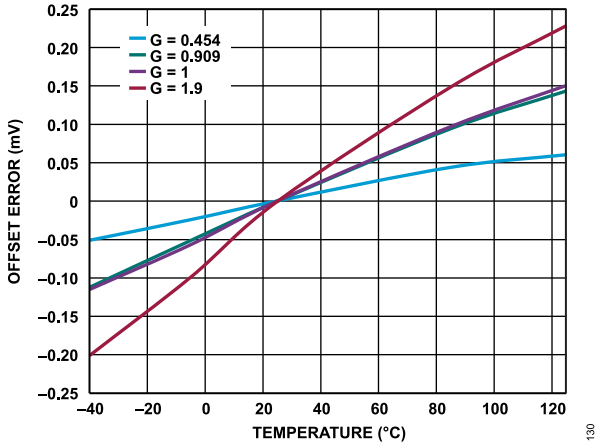

Figure 27. Offset Error vs. Temperature for G = 0.454, G = 0.909, G = 1, and G = 1.9

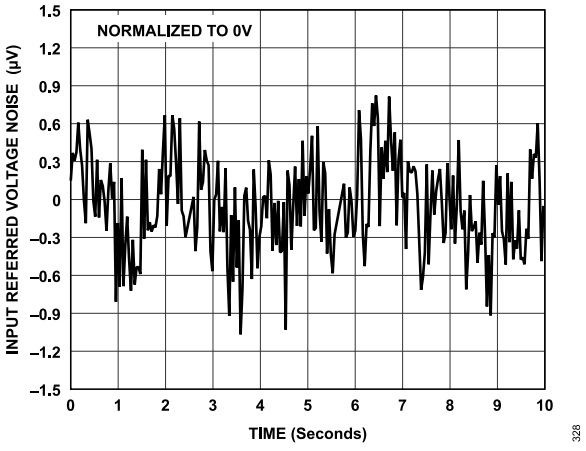

Figure 28. Voltage Noise for 0.1 Hz to 10 Hz Bandwidth, 100 kSPS, 250 Samples Averaged per Reading

TYPICAL PERFORMANCE CHARACTERISTICS

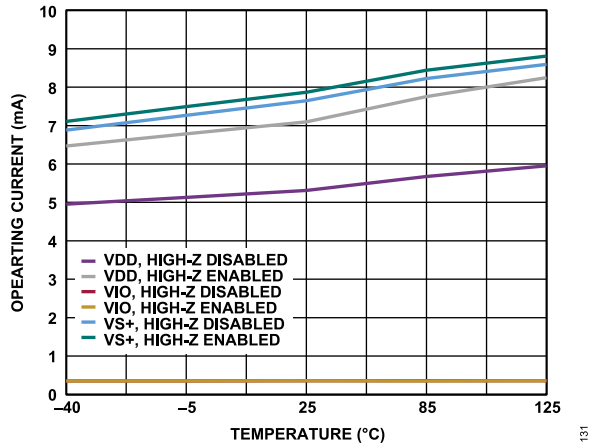

Figure 29. Operating Current vs. Temperature, 2 MSPS

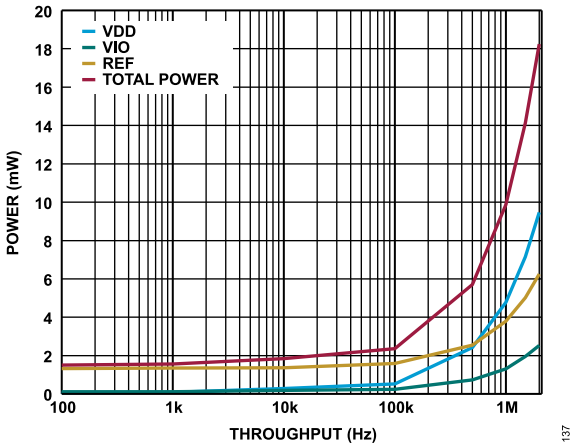

Figure 32. Power vs. Throughput

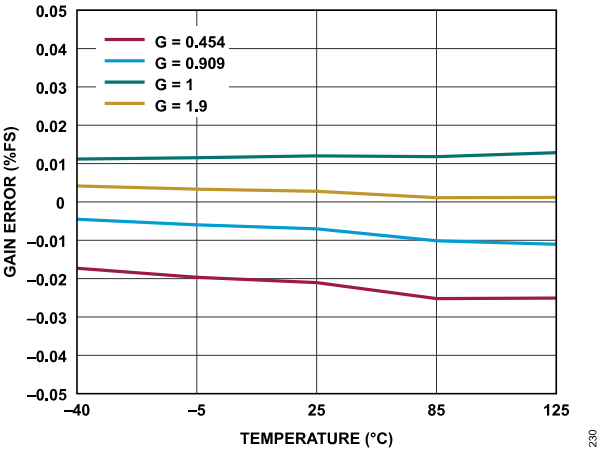

Figure 30. Gain Error vs. Temperature, V_{REF} = 5.0 V, Normal Mode

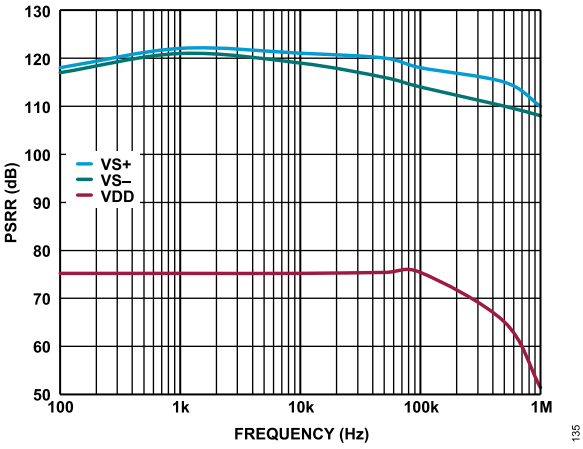

Figure 33. PSRR vs. Frequency

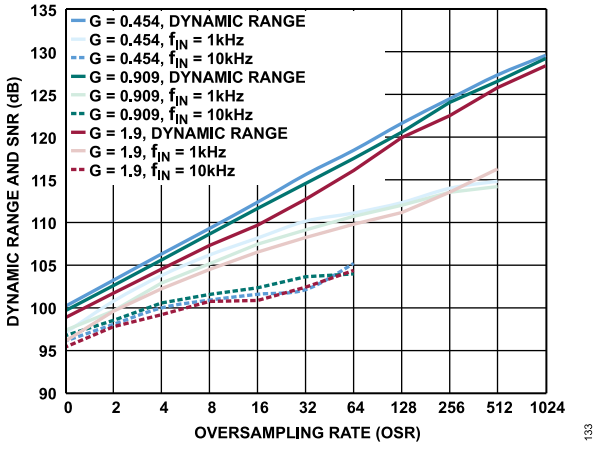

Figure 31. Dynamic Range and SNR vs. Oversampling Rate for G = 0.454, G = 0.909, and G = 1.9, and for Input Frequencies, 2 MSPS

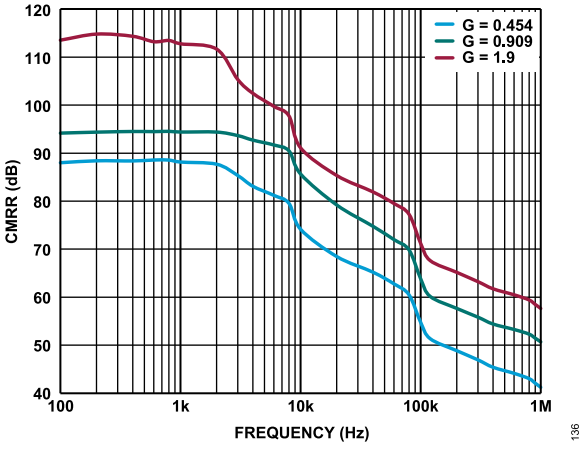

Figure 34. CMRR vs. Frequency for G = 0.454, G = 0.909, and G = 1.9

TYPICAL PERFORMANCE CHARACTERISTICS

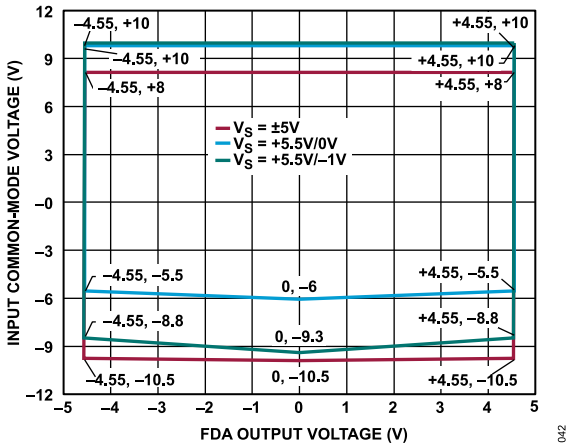

Figure 35. Input Common-Mode Voltage vs. FDA Output Voltage, G = 0.454, Differential Input

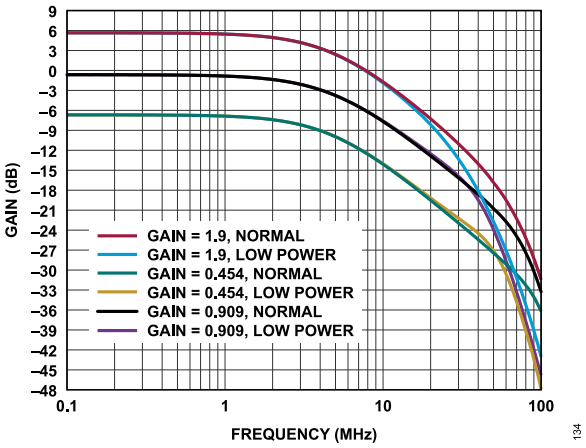

Figure 38. Small Signal Frequency Response for G = 1.9, G = 0.454, and G = 0.909 at Full Power and Low Power

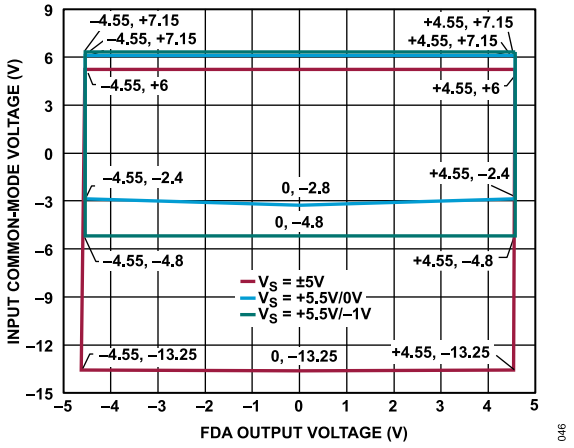

Figure 36. Input Common-Mode Voltage vs. FDA Output Voltage, G = 0.909, Differential Input

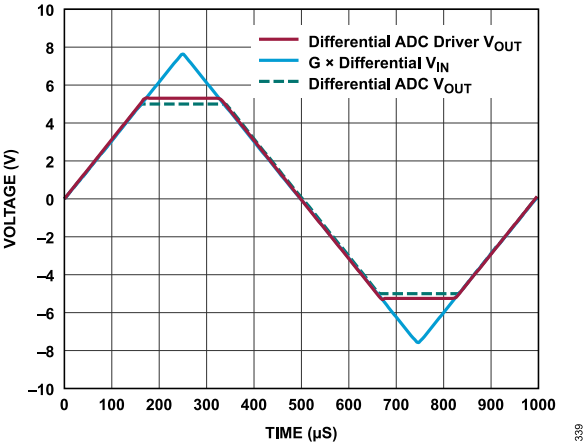

Figure 39. Output Drive Recovery, f_{IN} = 1 kHz

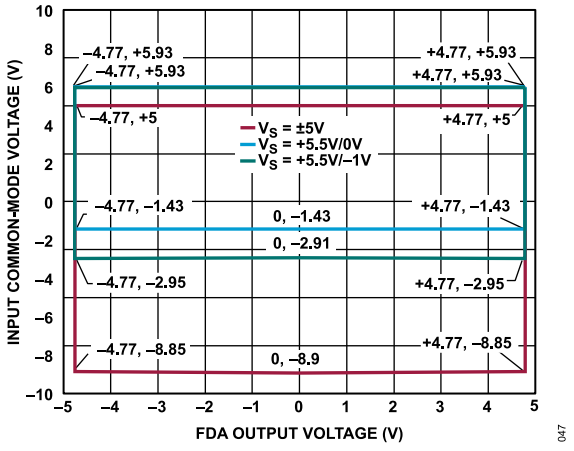

Figure 37. Input Common-Mode Voltage vs. FDA Output Voltage, G = 1.9, Differential Input

TERMINOLOGY

Integral Nonlinearity INL Error

INL error is the deviation of each individual code from a line drawn from negative full scale through positive full scale. The point used as negative full scale occurs ½ LSB before the first code transition. Positive full scale is defined as a level 1½ LSB beyond the last code transition. The deviation is measured from the middle of each code to the true straight line (see Figure 40).

Differential Nonlinearity DNL Error

In an ideal ADC, code transitions are 1 LSB apart. DNL is the maximum deviation from this ideal value. DNL error is often specified in terms of resolution for which no missing codes are guaranteed.

Offset Error

The first transition occurs at a level ½ LSB above analog ground. Offset error is the difference between the ideal midscale input voltage (0 V) and the actual voltage producing the midscale output code.

Offset Error Drift

Offset error drift is the ratio of the offset error change due to a temperature change of 1°C and the full-scale code range. Offset error drift is expressed in parts per million per degree Celsius as follows:

$$\text{Offset Error Drift (ppm/°C)} = 10^6 \times (\text{Offset Error\_}T_{MAX} - \text{Offset Error\_}T_{MIN}) / (T_{MAX} - T_{MIN}) \quad (1)$$

where:

T_{MAX} = 125 ºC.
T_{MIN} = −40 ºC .

Gain Error

The first transition occurs at a level ½ LSB above nominal negative full scale. The last transition occurs for an analog voltage 1½ LSB below the nominal full scale. The gain error is the deviation of the difference between the actual level of the last transition and the actual level of the first transition from the difference between the ideal levels after the offset error is removed. Gain error is expressed as a percentage as follows:

$$\text{Gain Error}(\%) = 100 \times ((PFS - NFS)_{\text{ACTUAL\_CODE}} - (PFS - NFS)_{\text{IDEAL\_CODE}}) / (PFS - NFS)_{\text{IDEAL\_CODE}} \quad (2)$$

where:

PFS is the positive full scale.
NFS is the negative full scale.

Gain Error Drift

Gain error drift is the ratio of the gain error change due to a temperature change of 1°C and the full-scale range. Gain error drift is expressed in parts per million per degree Celsius as follows:

$$\text{Gain Error Drift (ppm/°C)} = 10^6 \times (\text{Gain Error\_}T_{MAX} - \text{Gain Error\_}T_{MIN}) / (T_{MAX} - T_{MIN}) \quad (3)$$

where:

T_{MAX} = 125ºC.
T_{MIN} = −40ºC.

Spurious-Free Dynamic Range (SFDR)

SFDR is the difference, in decibels (dB), between the rms amplitude of the input signal and the peak spurious signal, including harmonics.

Effective Number of Bits (ENOB)

ENOB is a measurement of the resolution with a sine wave input. ENOB is related to SINAD as follows:

$$ENOB = (SINAD_{dB} - 1.76)/6.02$$

ENOB is expressed in bits.

Total Harmonic Distortion THD

THD is the ratio of the rms sum of the first five harmonic components to the rms value of a full-scale input signal and is expressed in decibels.

Dynamic Range

Dynamic range is the ratio of the rms value of the full scale to the total rms noise measured. The value for dynamic range is expressed in decibels. Dynamic range is measured with a signal at −60 dBFS so that the range includes all noise sources and DNL artifacts.

Signal-to-Noise Ratio (SNR)

SNR is the ratio of the rms value of the actual input signal to the rms sum of all other spectral components below the Nyquist frequency, excluding harmonics and dc. The value for SNR is expressed in decibels.

Signal-to-Noise-and-Distortion Ratio SINAD

SINAD is the ratio of the rms value of the actual input signal to the rms sum of all other spectral components that are less than the Nyquist frequency, including harmonics but excluding dc. The value of SINAD is expressed in decibels.

Aperture Delay

Aperture delay is the measure of the acquisition performance and is the time between the rising edge of the CNV input and when the input signal is held for a conversion.

Transient Response

Transient response is the time required for the ADC to acquire a full-scale input step to ±1 LSB accuracy.

TERMINOLOGY

Common-Mode Rejection Ratio (CMRR)

CMRR is the ratio of the power in the µModule output at the frequency, f, to the power of a 1.3 V p-p sine wave applied to the input common-mode voltage of f.

$$CMRR(\text{dB})=10\log(P_{\mu Module\_IN}/P_{\mu Module\_OUT}) \quad (4)$$

where:

$P_{\mu Module\_IN}$ is the common-mode power at f applied to the inputs.

$P_{\mu Module\_OUT}$ is the power at f in the µModule output.

Power Supply Rejection Ratio (PSRR)

PSRR is the ratio of the power in the µModule output at f to the power of a 500 mV p-p sine wave applied to the VDD and VS+ supply voltage centered at 5 V and 100 mV p-p for a VS− supply voltage centered at − 1 V of f.

$$PSRR\ (\text{dB}) = 10\log(P_{\mu Module\_IN}/P_{\mu Module\_OUT})$$

where:

$P_{\mu Module\_IN}$ is the power at f at each of the VDD, VS+, and VS− supply pins.
$P_{\mu Module\_OUT}$ is the power at f in the µModule output.

THEORY OF OPERATION

CIRCUIT INFORMATION

The ADAQ4003 SiP is a fast, precision DAQ signal chain that uses a SAR architecture. As shown in Figure 1, the ADAQ4003 µModule DAQ solution contains a high bandwidth, fully differential, ADC driver, a low noise reference buffer, and an 18-bit SAR ADC, along with the critical precision passive components required to achieve optimized performance with pin-selectable gain options of 0.454, 0.909, 1, or 1.9. All active components including *i*Passives thin film resistors with ±0.005% matching in the circuit are designed by Analog Devices, which are factory calibrated to achieve a high degree of specified accuracy and minimize temperature dependent error sources.

The ADAQ4003 is capable of converting 2,000,000 samples per second (2 MSPS). The ADAQ4003 has a valid first conversion after being powered down for long periods that can reduce power consumed in applications where the ADC does not convert constantly.

The ADAQ4003 offers a significant reduction in form factor and total cost of ownership compared to traditional discrete signal chains from a selection of individual components, size of PCB, and manufacturing perspective, while still providing flexibility to adapt to a wide array of applications.

The ADAQ4003 incorporates a fully differential, high speed ADC driver with integrated precision resistors. The precision resistors can be pin strapped to achieve different gains for the fully differential ADC driver, which allows the user to match the input signal range. The fully ADC driver can be used in a differential manner or to perform a single-ended to differential conversion for a single-ended input.

The fast conversion time of the ADAQ4003, along with turbo mode, allows low clock rates to read back conversions, even when running at its maximum throughput rate. Note that for the ADAQ4003, the full throughput rate of 2 MSPS can be achieved only with turbo mode enabled. Because the ADAQ4003 has on-board conversion clocks, the serial clock (SCK) is not required for the conversion process.

The ADAQ4003 interfaces to any 1.8 V to 5 V digital logic family. The device is housed in a 7 mm × 7 mm, 0.80 mm pitch 49-ball CSP_BGA that provides significant space savings and allows flexible configurations.

TRANSFER FUNCTIONS

The ideal transfer characteristics for the ADAQ4003 are shown in Figure 40 and Table 10.

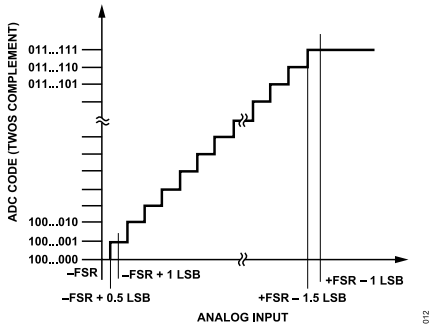

Figure 40. ADC Ideal Transfer Function (FSR Is Full-Scale Range)

Table 10. Output Codes and Ideal Input Voltages

Description	Analog Inputs		Digital Output Code[1] (Twos Complement, Hex)
	Span Compression Disabled	Span Compression Enabled	
FSR − 1 LSB	(131,071 × V_{REF})/(131,072 × G)	(131,071 × 0.8 × V_{REF})/(131,072 × G)	0x1FFFF[2]
Midscale + 1 LSB	V_{REF}/(131,072 × G)	0.8 × V_{REF}/(131,072 × G)	0x00001
Midscale	0 V	0 V	0x00000
Midscale − 1 LSB	−V_{REF}/(131,072 × G)	−0.8 × V_{REF}/(131,072 × G)	0x3FFFF
−FSR + 1 LSB	−(131,071 × V_{REF})/(131,072 × G)	−(131,071 × 0.8 × V_{REF})/(131,072 × G)	0x20001
−FSR	−V_{REF} × G	−0.8 × V_{REF} × G	0x20000[3]

[1] This output code assumes that the negative input, IN−, of the ADC driver is being driven.

[2] This output code is also the code for an overranged analog input (IN+ − IN− above V_{REF} with the span compression disabled and above 0.8 × V_{REF} with the span compression enabled).

[3] This output code is also the code for an underranged analog input (IN+ − IN− below −V_{REF} with the span compression disabled and above 0.8 × V_{REF} with the span compression enabled).

APPLICATIONS INFORMATION

TYPICAL APPLICATION DIAGRAMS

Figure 41 through Figure 48 show the recommended connection diagrams for the ADAQ4003 when applying a single-ended and differential input signal for four different gain options with respect to ground reference. Table 11 shows how the input signal is applied for a given gain or input range option.

Table 11. Gain Configuration and Input Range

Gain	Input Range	Input Signal on Pins	Test Conditions
0.454	±11 V	R1K1−, R1K1+	Leave the IN− and IN+ pins floating. Connect the OUT+ to R1K− pins and OUT− to R1K+ pins together. See Figure 41 and Figure 45.
0.909	±5.5 V	R1K1−, R1K1+	Leave the IN−, IN+, R1K−, and R1K+ pins floating. See Figure 42 and Figure 46.
1	±5 V	R1K−, R1K+	Leave the IN−, IN+, R1K1−, and R1K1+ pins floating. See Figure 43 and Figure 47.
1.9	±2.6 V	R1K−/R1K1−, R1K+/R1K1+	Leave the IN− and IN+ pins floating. Connect the R1K− to R1K1− pins and R1K+ to R1K1+ pins together. See Figure 44 and Figure 48.

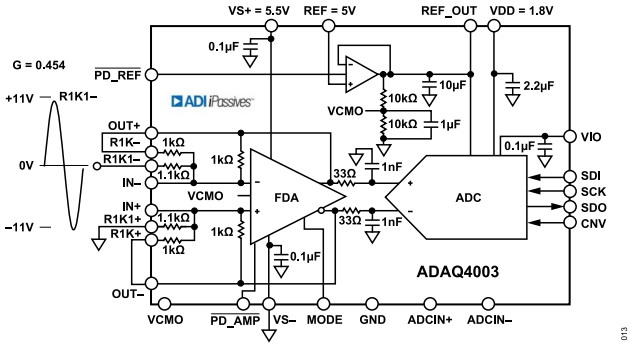

Figure 41. Single-Ended to Differential Configuration with G = 0.454

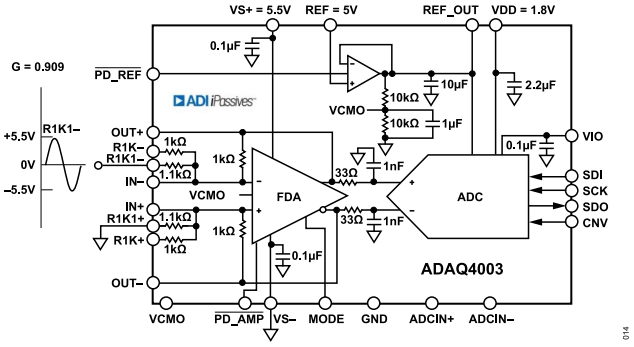

Figure 42. Single-Ended to Differential Configuration with G = 0.909

APPLICATIONS INFORMATION

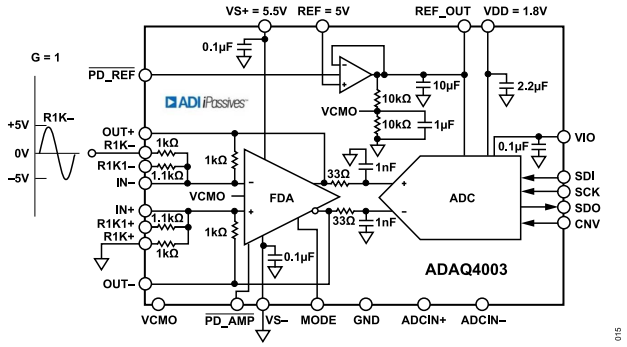

Figure 43. Single-Ended to Differential Configuration with G = 1

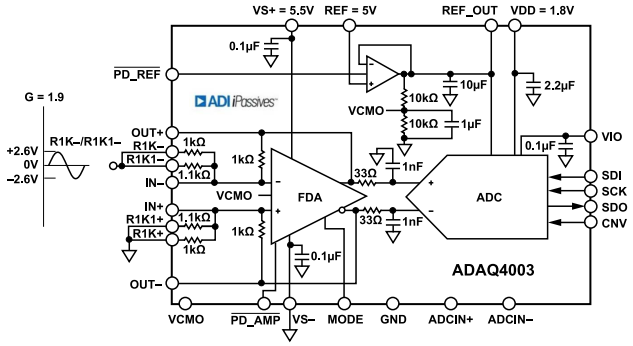

Figure 44. Single-Ended to Differential Configuration with G = 1.9

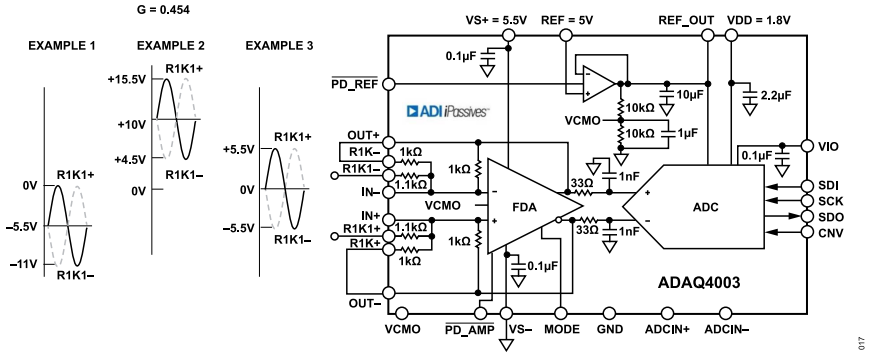

Figure 45. Differential Configuration with G = 0.454

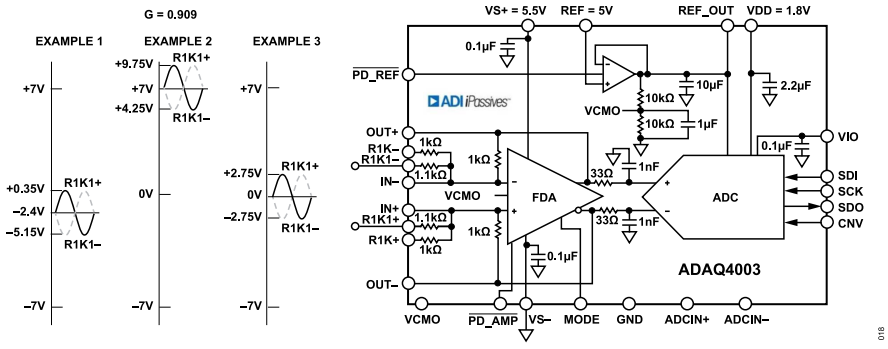

Figure 46. Differential Configuration with G = 0.909

APPLICATIONS INFORMATION

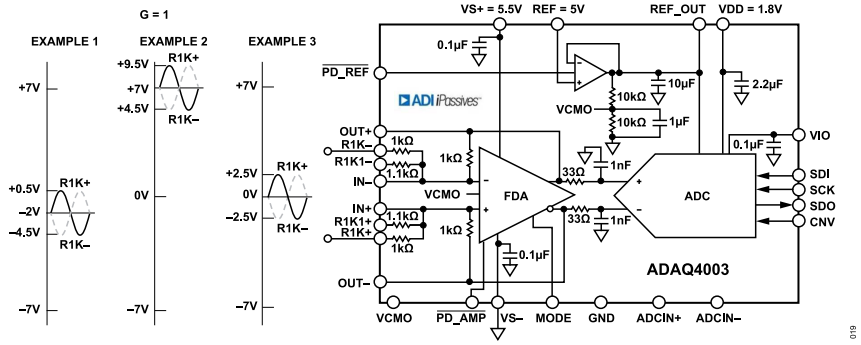

Figure 47. Differential Configuration with G = 1

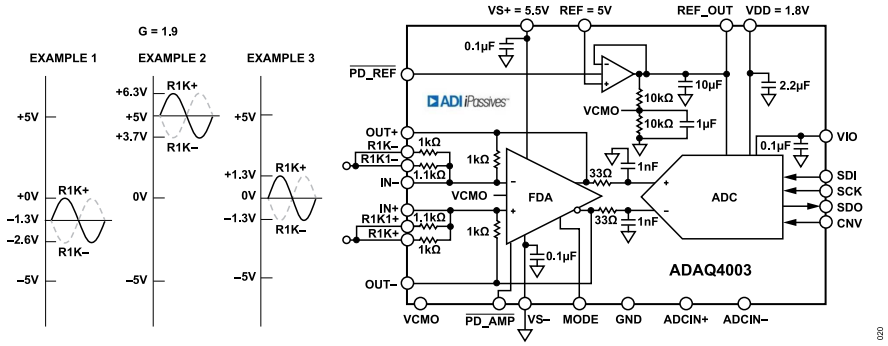

Figure 48. Differential Configuration with G = 1.9

APPLICATIONS INFORMATION

ANALOG INPUTS

High Frequency Input Signals

The ADAQ4003 ac performance over a wide input frequency range using a 5 V reference voltage is shown in Figure 21 and Figure 24. The ADAQ4003 maintains exceptional ac performance for input frequencies up to the Nyquist frequency with minimal performance degradation.

EASE OF DRIVE FEATURES

Input Span Compression

The ADAQ4003 includes a span compression feature that increases the headroom and footroom available to the ADC driver by reducing the input range by 10% from the top and bottom of the range while still accessing all available ADC codes. The SNR decreases by approximately 1.9 dB (20 × log(8/10)) for the reduced input range when span compression is enabled. Span compression is disabled by default but can be enabled by writing to the relevant register bit (see the Digital Interface section).

ADC High-Z Mode

The ADAQ4003 incorporates ADC high-Z mode, which reduces the nonlinear charge kickback when the capacitor DAC switches back to the input at the start of the acquisition. The ADC high-Z mode is disabled by default but can be enabled by writing to the register (see Table 15). Disable high-Z mode for input frequencies above 100 kHz or when multiplexing.

Driving the ADAQ4003 Using a High Impedance PGIA

The majority of instrumentation and programmable gain instrumentation amplifiers (PGIAs) are single-ended output, which cannot directly drive the fully differential data acquisition signal chain. However, the LTC6373 PGIA offers fully differential outputs, low noise, low distortion, and high bandwidth. The LTC6373 is dc-coupled on the input and the output with programmable gain settings (using the A2, A1, and A0 pins). These features enable the LTC6373 to drive the ADAQ4003 directly in many signal chain applications without sacrificing precision performance.

In Figure 51, the LTC6373 is used in a differential input to differential output configuration with dual supplies of ±15V. The LTC6373 can also be used in a single-ended input to differential output configuration, if required. The LTC6373 is directly driving the ADAQ4003 with its gain set as 0.454. The V_{OCM} pin of LTC6373 is connected to ground and its outputs swing between −5.5 V and +5.5 V (opposite in phase). The FDA of ADAQ4003 level shifts the outputs of the LTC6373 to match the desired input common mode of the ADAQ4003 and provides the signal amplitude necessary to utilize the maximum 2 × V_{REF} peak-to-peak differential signal range of the ADC inside the ADAQ4003 µModule. Figure 49 and Figure 50 show the SNR and THD performance using various gain settings of the LTC6373 for the circuit configuration shown in Figure 51.

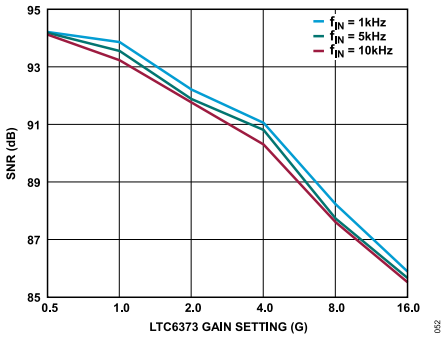

Figure 49. SNR vs. LTC6373 Gain Setting, LTC6373 Driving the ADAQ4003 (Gain = 0.454)

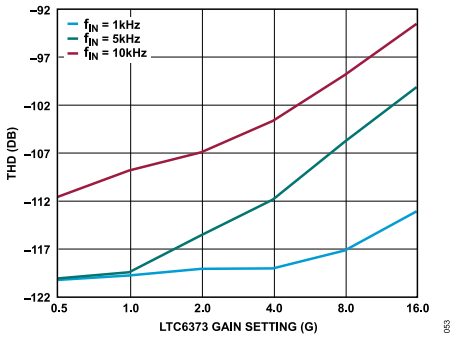

Figure 50. THD vs. LTC6373 Gain Setting, LTC6373 Driving the ADAQ4003 (Gain = 0.454)

APPLICATIONS INFORMATION

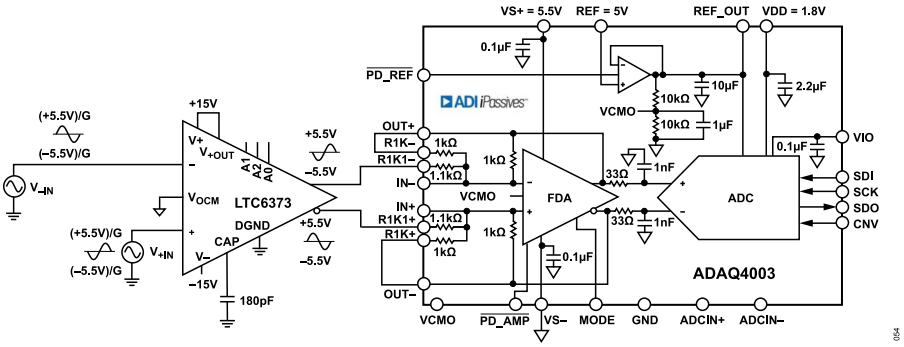

Figure 51. LTC6373 Driving ADAQ4003 (G = 0.454)

VOLTAGE REFERENCE INPUT

The ADAQ4003 voltage reference input (REF) is the noninverting node of the on board, low noise reference buffer. The reference buffer is included to optimally drive the dynamic input impedance of the SAR ADC reference node.

Also housed in the ADAQ4003 is a 10 µF decoupling capacitor that is ideally laid out within the device. This decoupling capacitor is a required piece of the SAR architecture. The REF_OUT capacitor is not just a bypass capacitor. This capacitor is part of the SAR ADC that cannot fit on the silicon simply. During the bit decision process, because the bits are settled in a few tens of nanoseconds or faster, the storage capacitor replenishes the charge of the internal capacitive DAC. As the binary bit weighted conversion is processed, small chunks of charge are taken from the 10 µF capacitor. The internal capacitor array is a fraction of the size of the decoupling capacitor, but this large value storage capacitor is required to meet the SAR bit decision settling time. There is no need for an additional lower value ceramic decoupling capacitor (for example, 100 nF) between the REF_OUT and GND pins.

The reference value sets the maximum ADC input voltage that the SAR capacitor array can quantize. The reference buffer is set in the unity-gain configuration. Therefore, the user sets the reference voltage value with the REF pin and observes this value at the REF_OUT pin. The user is responsible for selecting a reference voltage value that is appropriate for the system under design. Allowable reference values range from 2.4 V to 5.1 V. However, do not violate the input common-mode voltage range specification of the reference buffer. With the inclusion of the reference buffer, the user can implement a much lower power reference source than many traditional SAR ADC signal chains because the reference source drives a high impedance node instead of the dynamic load of the SAR capacitor array. Root sum square the reference buffer noise with the reference source noise to arrive at a total noise estimate. Generally, the reference buffer has a noise density much less than that of the reference source.

For highest performance and lower drift, use a reference such as the ADR4550, or use a low power reference such as the ADR3450 at the expense of a decrease in the noise performance.

POWER SUPPLY (POWER TREE)

The ADAQ4003 uses four power supply pins: an ADC driver positive (VS+) and negative supply (VS−), a core ADC supply (VDD), a digital input and output interface supply (VIO). VIO allows direct interface with any logic among 1.8 V, 2.5 V, 3 V, or 5 V. To reduce the number of supplies needed, VIO and VDD can be tied together for 1.8 V operation. A combination of the ADP5070 (dual, high performance dc-to-dc switching regulator), the LT3032 (dual, low noise, positive and negative, low dropout voltage linear regulator), and the LT3023 (dual, micropower, low noise, low dropout regulator) can generate independently regulated positive and negative rails for all four power supply pins, including ±15 V rails for any additional signal conditioning. Refer to the EVAL-ADAQ4003FMCZ user guide for details. The ADAQ4003 is insensitive to power supply variations (PSRR) over a wide frequency range, as shown in Figure 33.

The ADAQ4003 ADC powers down automatically at the end of each conversion phase. Therefore, the power scales linearly with the sampling rate. This feature makes the device ideal for low sampling rates (even a few samples per second) and battery-powered applications. Figure 32 shows the ADAQ4003 total power dissipation and individual power dissipation for each rail.

POWER-DOWN MODE

The power-down mode of the FDA is asserted by applying a low logic level (GND) to the $\overline{\text{PD\_AMP}}$ pin to minimize the quiescent current consumed when the ADAQ4003 is not used. When the $\overline{\text{PD\_AMP}}$ pin is connected to GND, the FDA output is high impedance. When the $\overline{\text{PD\_AMP}}$ pin is connected to a high logic level, the ADAQ4003 operates normally. The logic levels for the $\overline{\text{PD\_AMP}}$ pin are determined by VS+. It is not recommended to leave the MODE pin floating.

DIGITAL INTERFACE

Although the ADAQ4003 has a reduced number of pins, the device offers flexibility in its serial interface modes. The ADAQ4003 can also be programmed via 16-bit SPI writes to the configuration registers.

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When in $\overline{CS}$ mode, the ADAQ4003 is compatible with SPI, QSPI™, MICROWIRE®, digital hosts, and digital signal processors (DSPs). In this mode, the ADAQ4003 can use either a 3-wire or 4-wire interface. A 3-wire interface using the CNV, SCK, and SDO signals minimizes wiring connections, which is useful in isolated applications. A 4-wire interface using the SDI, CNV, SCK, and SDO signals allows CNV, which initiates the conversions, to be independent of the readback timing (SDI). This interface is useful in low jitter sampling or simultaneous sampling applications.

The ADAQ4003 provides a daisy-chain feature using the SDI for cascading multiple ADCs on a single data line, similar to a shift register.

The mode in which the ADAQ4003 operates depends on the SDI level when the CNV rising edge occurs. $\overline{CS}$ mode is selected if SDI is high, and daisy-chain mode is selected if SDI is low. The SDI hold time is such that when SDI and CNV are connected together, daisy-chain mode is automatically selected.

In either 3-wire or 4-wire mode, the ADAQ4003 offers the option of forcing a start bit in front of the data bits. This start bit can be used as a busy signal indicator to interrupt the digital host and trigger the data reading. Otherwise, without a busy indicator, the user must time out the maximum conversion time prior to readback.

The busy indicator feature is enabled in $\overline{CS}$ mode if CNV or SDI is low when the ADC conversion ends.

The state of SDO on power-up is either low or high-Z depending on the states of CNV and SDI (see Table 12).

Table 12. State of SDO on Power-Up

CNV	SDI	SDO
0	0	Low
0	1	Low
1	0	Low
1	1	High-Z

The ADAQ4003 has a turbo mode capability in both 3-wire and 4-wire mode. Turbo mode is enabled by writing to the configuration register and replaces the busy indicator feature when enabled. Turbo mode allows a slower SPI clock rate, making interfacing simpler. The maximum throughput of 2 MSPS for the ADAQ4003 can be achieved only with turbo mode enabled and a minimum SCK rate of 75 MHz. The SCK rate must be sufficiently fast to ensure the conversion result is clocked out before another conversion initiates. The minimum required SCK rate for an application can be derived based on the sample period (t_{CYC}), the number of bits that must be read (including the data and optional status bits), and the digital interface mode used. Timing diagrams and explanations for each digital interface mode are given in the digital modes of operation sections (see the $\overline{CS}$ Mode, 3-Wire Turbo Mode section and the $\overline{CS}$ Mode, 4-Wire with Busy Indicator section).

Status bits can also be clocked out at the end of the conversion data if the status bits are enabled in the configuration register. The six status bits are described in Table 13.

The ADAQ4003 is configured by 16-bit SPI writes to the desired configuration register. The 16-bit word can be written via the SDI line while CNV is held low. The 16-bit word consists of an 8-bit header and 8-bit register data. For isolated systems, the ADuM141D is recommended, which can support the 75 MHz SCK rate required to run the ADAQ4003 at its full throughput of 2 MSPS.

REGISTER READ AND WRITE FUNCTIONALITY

The ADAQ4003 register bits are programmable, and the bits default statuses are listed in Table 13. The register map is shown in Table 15. The $\overline{OV}$ clamp flag is a read only sticky bit, and this bit is cleared only if the register is read and the overvoltage condition is no longer present. The $\overline{OV}$ clamp flag gives an indication of the overvoltage condition when this bit is set to 0.

Table 13. Register Bits

Register Bits	Default Status
$\overline{OV}$ Clamp Flag	1 bit, 1 = inactive (default)
Span Compression	1 bit, 0 = disabled (default)
High-Z Mode	1 bit, 0 = disabled (default)
Turbo Mode	1 bit, 0 = disabled (default)
Enable Six Status Bits	1 bit, 0 = disabled (default)

All access to the register map must start with a write to the 8-bit command register in the SPI interface block. The ADAQ4003 ignores all 1s until the first 0 is clocked in (represented by $\overline{WEN}$ in Figure 52, Figure 53, and Table 14). The value loaded into the command register is always 0 followed by seven command bits. This command determines whether that operation is a write or a read. The ADAQ4003 command register is listed in Table 14.

Table 14. Command Register

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
$\overline{WEN}$	R/$\overline{W}$	0	1	0	1	0	0

All register read and writes must occur while CNV is low. Data on SDI is clocked in on the rising edge of SCK. Data on SDO is clocked out on the falling edge of SCK. At the end of the data transfer, SDO is put in a high impedance state on the rising edge of CNV if daisy-chain mode is not enabled. If daisy-chain mode is enabled, SDO goes low on the rising edge of CNV. Register reads are not allowed in daisy-chain mode.

A register write requires three signal lines: SCK, CNV, and SDI. During a register write to read the current conversion results on SDO, the CNV pin must be brought low after the conversion completes. Otherwise, the conversion results may be incorrect on SDO. However, the register write occurs regardless.

The LSB of each configuration register is reserved because a user reading 16-bit conversion data may be limited to a 16-bit SPI frame. The state of SDI on the last bit in the SDI frame may be the

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state that then persists when CNV rises. Because interface mode is partly set based on the SDI state when CNV rises, in this scenario, the user may need to set the final SDI state.

The timing diagrams in Figure 52 through Figure 54 show how data is read and written when the ADAQ4003 is configured in register read, write, and daisy-chain mode.

Table 15. Register Map

ADDR[1:0]	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Reset
0x0	Reserved	Reserved	Reserved	Enable six status bits	Span compression	High-Z mode	Turbo mode	$\overline{OV}$ clamp flag (read only sticky bit)	0xE1

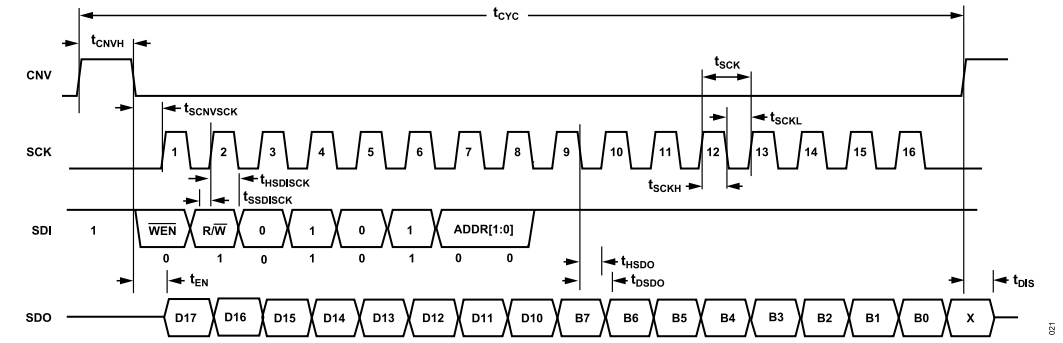

Figure 52. Register Read Timing Diagram

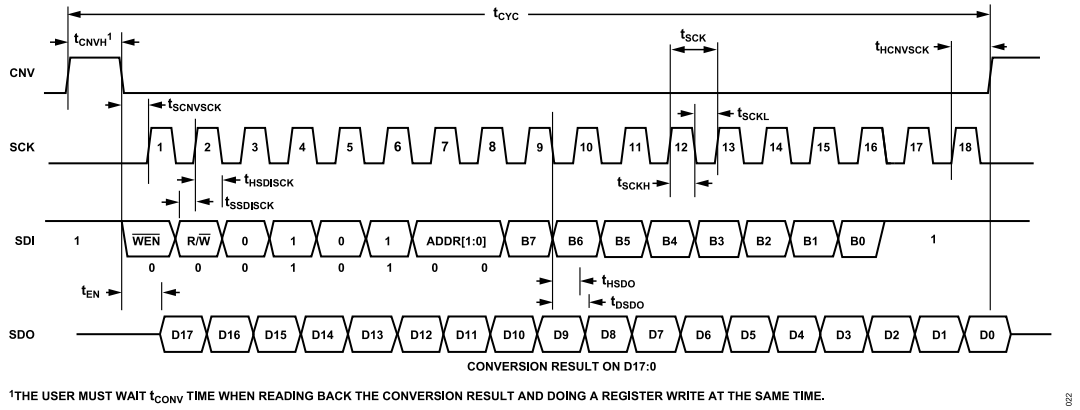

Figure 53. Register Write Timing Diagram

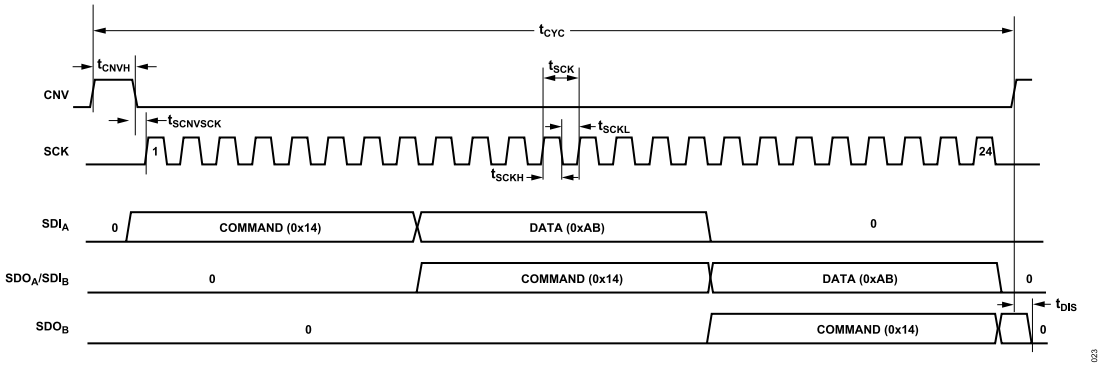

Figure 54. Register Write Timing Diagram, Daisy-Chain Mode

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STATUS WORD

The 6-bit status word can be appended to the end of a conversion result, and the default conditions of these bits are shown in Table 16. The status bits must be enabled in the register setting. When the $\overline{OV}$ clamp flag is 0, this bit indicates an overvoltage condition. The $\overline{OV}$ clamp flag status bit updates on a per conversion basis.

The SDO line returns to high impedance after the sixth status bit is clocked out (except in daisy-chain mode). The user is not required to clock out all status bits to start the next conversion. The serial interface timing for $\overline{CS}$ mode, 3-wire without busy indicator, including status bits, is shown in Figure 55.

Table 16. Table 15. Status Bits (Default Conditions)

Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
$\overline{OV}$ clamp flag	Span compression	High-Z mode	Turbo mode	Reserved	Reserved

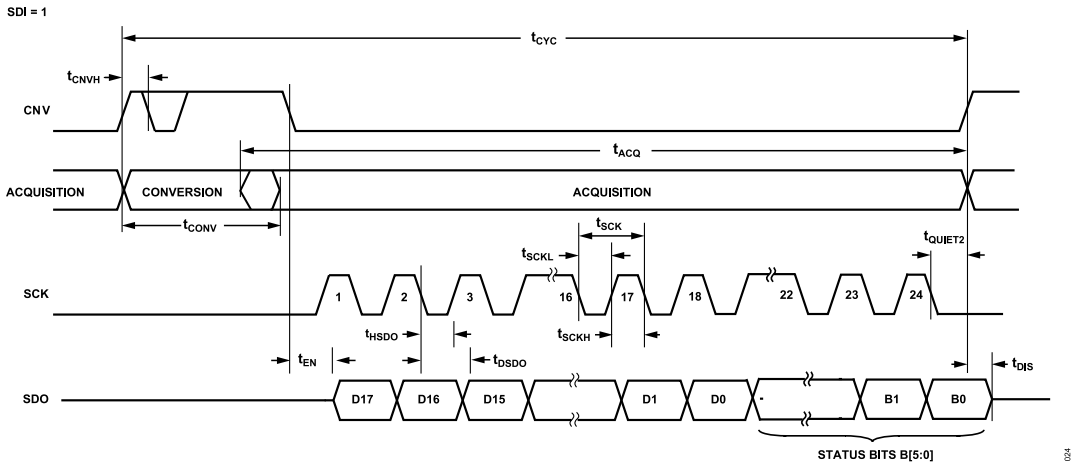

Figure 55. $\overline{CS}$ Mode, 3-Wire Without Busy Indicator Serial Interface Timing Diagram Including Status Bits (SDI High)

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$\overline{CS}$ MODE, 3-WIRE TURBO MODE

This mode is typically used when a single ADAQ4003 device is connected to an SPI-compatible digital host. This mode provides additional time during the end of the ADC conversion process to clock out the previous conversion result, providing a lower SCK rate. The ADAQ4003 can achieve a throughput rate of 2 MSPS only when turbo mode is enabled and using a minimum SCK rate of 75 MHz. The connection diagram is shown in Figure 56, and the corresponding timing diagram is shown in Figure 57.

To enable turbo mode, set the turbo mode enable bit in the configuration register to 1 (see Table 13). This mode replaces the 3-wire with busy indicator mode by programming the turbo mode bit, Bit 1 (see Table 15). Writing to the user configuration register requires SDI to be connected to the digital host (see the Register Read and Write Functionality section). When turbo mode is enabled, the conversion result read on SDO corresponds to the result of the previous conversion.

When performing conversions in this mode, SDI must be held high, and a CNV rising edge initiates a conversion and forces SDO to high impedance. The user must wait the t_{QUIET1} time after CNV is brought high before bringing CNV low to clock out the previous conversion result. When the conversion is complete (after t_{CONV}), the ADAQ4003 enters the acquisition phase and powers down. The user must also wait the t_{QUIET2} time after the last falling edge of SCK to when CNV is brought high.

When CNV goes low, the MSB is output to SDO. The remaining data bits are clocked by subsequent SCK falling edges. The data is valid on both SCK edges. Although the rising edge can capture the data, a digital host using the SCK falling edge allows a faster reading rate, provided it has an acceptable hold time, as dictated by t_{HSDO} (see Table 3). If the status bits are not enabled, SDO returns to high impedance after the 18th SCK falling edge. If the status bits are enabled, the bits are shifted out on SDO on the 19th through the 24th SCK falling edges (see the Status Word section). SDO returns to high impedance after the 18th SCK falling edge, or when CNV goes high (whichever occurs first). The user must also provide a delay of t_{QUIET2} between the final SCK falling edge and the next CNV rising edge to ensure specified performance.

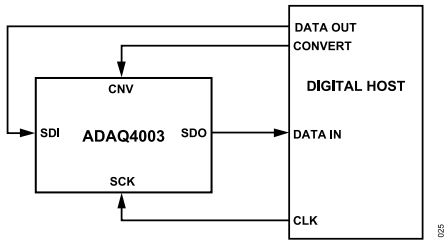

Figure 56. $\overline{CS}$ Mode, 3-Wire Turbo Mode Connection Diagram (SDI High)

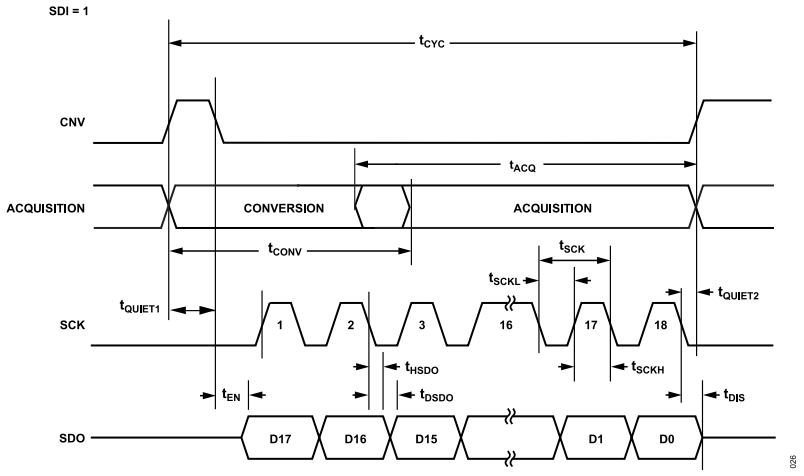

Figure 57. $\overline{CS}$ Mode, 3-Wire Turbo Mode Serial Interface Timing Diagram (SDI High)

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$\overline{CS}$ MODE, 3-WIRE WITHOUT BUSY INDICATOR

This mode is typically used when a single ADAQ4003 device is connected to an SPI-compatible digital host. The connection diagram is shown in Figure 58, and the corresponding timing diagram is shown in Figure 59.

When SDI is connected to VIO, a rising edge on CNV initiates a conversion, selects the $\overline{CS}$ mode, and forces SDO to high impedance. After a conversion initiates, it continues until completion irrespective of the state of CNV. This feature can be useful, for instance, to bring CNV low to select other SPI devices, such as analog multiplexers. However, CNV must be returned high before the minimum conversion time elapses and then held high for the maximum possible conversion time to avoid the generation of the busy signal indicator.

When the conversion completes, the ADAQ4003 enters the acquisition phase and powers down. When CNV goes low, the MSB is output onto SDO. The remaining data bits are clocked by subsequent SCK falling edges. The data is valid on both SCK edges. Although the rising edge can capture the data, a digital host using the SCK falling edge allows a faster reading rate, provided that the digital host has an acceptable hold time. After the 18th SCK falling edge or when CNV goes high (whichever occurs first), SDO returns to high impedance.

There must not be any digital activity on SCK during the conversion.

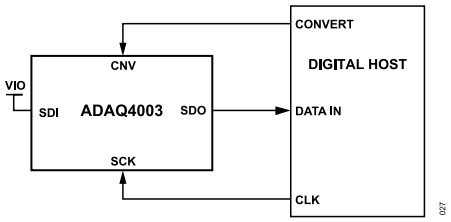

Figure 58. $\overline{CS}$ Mode, 3-Wire Without Busy Indicator Connection Diagram (SDI High)

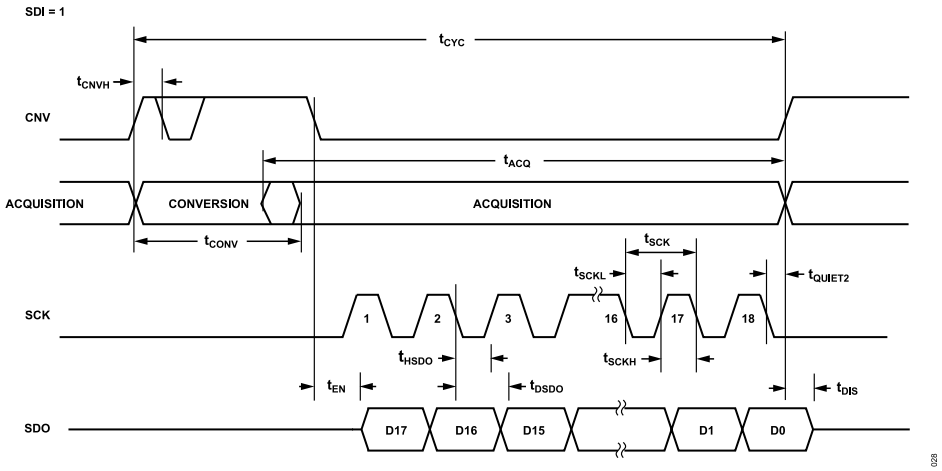

Figure 59. $\overline{CS}$ Mode, 3-Wire Without Busy Indicator Serial Interface Timing Diagram (SDI High)

APPLICATIONS INFORMATION

$\overline{CS}$ MODE, 3-WIRE WITH BUSY INDICATOR

This mode is typically used when a single ADAQ4003 device is connected to an SPI-compatible digital host with an interrupt input ($\overline{IRQ}$).

The connection diagram is shown in Figure 60, and the corresponding timing diagram is shown in Figure 61.

When SDI is connected to VIO, a rising edge on CNV initiates a conversion, selects the $\overline{CS}$ mode, and forces SDO to high impedance. SDO is maintained in high impedance until the completion of the conversion irrespective of the state of CNV. Prior to the minimum conversion time, CNV can select other SPI devices, such as analog multiplexers. However, CNV must be returned low before the minimum conversion time elapses and then held low for the maximum possible conversion time to guarantee the generation of the busy signal indicator.

When the conversion completes, SDO goes from high impedance to low impedance. With a pull-up resistor of 1 kΩ on the SDO line, this transition can be used as an interrupt signal to initiate the data reading controlled by the digital host. The ADAQ4003 then enters the acquisition phase and powers down. The data bits are then clocked out, MSB first, by subsequent SCK falling edges. The data is valid on both SCK edges. Although the rising edge can capture the data, a digital host using the SCK falling edge allows a faster reading rate, provided that the digital host has an acceptable hold time. After the optional 19th SCK falling edge or when CNV goes high (whichever occurs first), SDO returns to high impedance.

If multiple ADAQ4003 devices are selected at the same time, the SDO output pin handles this contention without damage or induced latch-up. Meanwhile, it is recommended to keep this contention as short as possible to limit extra power dissipation.

There must not be any digital activity on the SCK during the conversion.

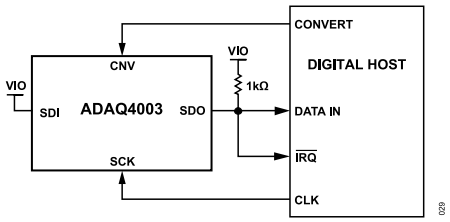

Figure 60. $\overline{CS}$ Mode, 3-Wire with Busy Indicator Connection Diagram (SDI High)

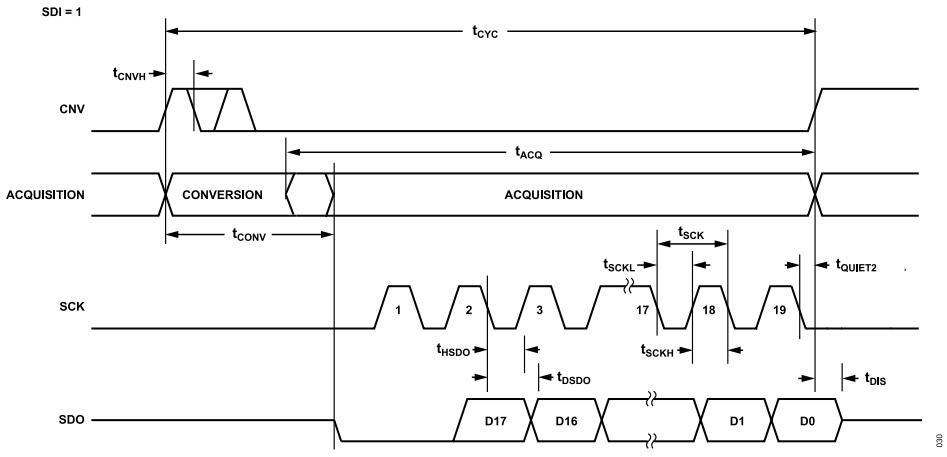

Figure 61. $\overline{CS}$ Mode, 3-Wire with Busy Indicator Serial Interface Timing Diagram (SDI High)

APPLICATIONS INFORMATION

$\overline{CS}$ MODE, 4-WIRE TURBO MODE

This mode is typically used when a single ADAQ4003 is connected to an SPI-compatible digital host. This mode provides additional time during the end of the ADC conversion process to clock out the previous conversion result, giving a lower SCK rate. The ADAQ4003 can achieve a throughput rate of 2 MSPS only when turbo mode is enabled and using a minimum SCK rate of 75 MHz. The connection diagram is shown in Figure 62, and the corresponding timing diagram is shown in Figure 63.

This mode replaces the 4-wire with busy indicator mode by programming the turbo mode bit, Bit 1 (see Table 15).

With SDI high, a rising edge on CNV initiates a conversion. The previous conversion data is available to read after the CNV rising edge. The user must wait t_{QUIET1} after CNV is brought high before bringing SDI low to clock out the previous conversion result. The user must also wait t_{QUIET2} after the last falling edge of SCK to when CNV is brought high.

When the conversion is complete, the ADAQ4003 enters the acquisition phase and powers down. The ADC result can be read by bringing its SDI input low, which consequently outputs the MSB onto SDO. The remaining data bits are then clocked by subsequent SCK falling edges. The data is valid on both SCK edges. Although the rising edge can capture the data, a digital host using the SCK falling edge allows a faster reading rate, provided that the digital host has an acceptable hold time. After the 18th SCK falling edge or when SDI goes high (whichever occurs first), SDO returns to high impedance.

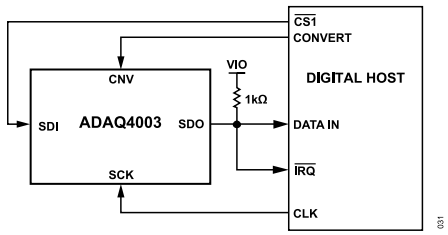

Figure 62. $\overline{CS}$ Mode, 4-Wire Turbo Mode Connection Diagram

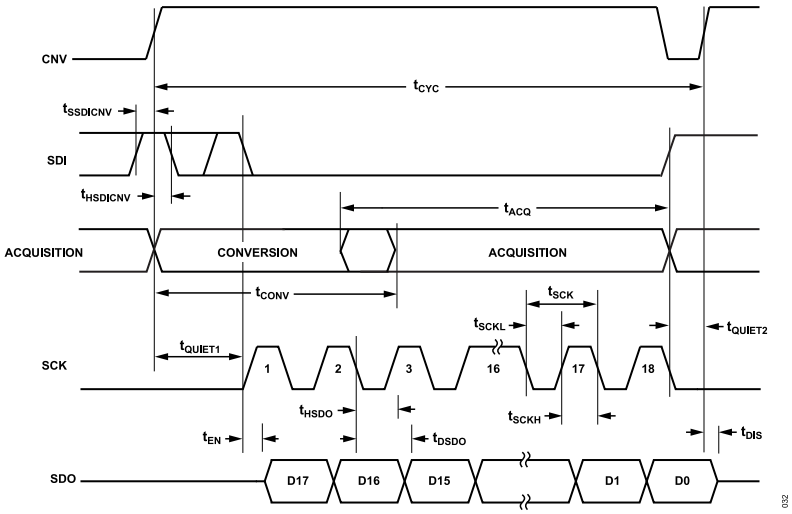

Figure 63. $\overline{CS}$ Mode, 4-Wire Turbo Mode Timing Diagram

APPLICATIONS INFORMATION

$\overline{CS}$ MODE, 4-WIRE WITHOUT BUSY INDICATOR

This mode is typically used when multiple ADAQ4003 devices are connected to an SPI-compatible digital host.

A connection diagram example using two ADAQ4003 devices is shown in Figure 64, and the corresponding timing diagram is shown in Figure 65.

With SDI high, a rising edge on CNV initiates a conversion, selects the $\overline{CS}$ mode, and forces SDO to high impedance. In this mode, CNV must be held high during the conversion phase and the subsequent data readback. If SDI and CNV are low, SDO is driven low. Prior to the minimum conversion time, SDI can select other SPI devices, such as analog multiplexers. However, SDI must be returned high before the minimum conversion time elapses and then held high for the maximum possible conversion time to avoid the generation of the busy signal indicator.

When the conversion is complete, the ADAQ4003 enters the acquisition phase and powers down. Each ADC result can be read by bringing its SDI input low, which consequently outputs the MSB onto SDO. The remaining data bits are then clocked by subsequent SCK falling edges. The data is valid on both SCK edges. Although the rising edge can capture the data, a digital host using the SCK falling edge allows a faster reading rate, provided that the digital host has an acceptable hold time. After the 18th SCK falling edge or when SDI goes high (whichever occurs first), SDO returns to high impedance and another ADAQ4003 can be read.

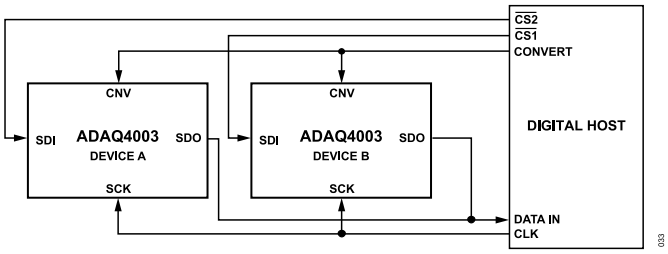

Figure 64. $\overline{CS}$ Mode, 4-Wire Without Busy Indicator Connection Diagram

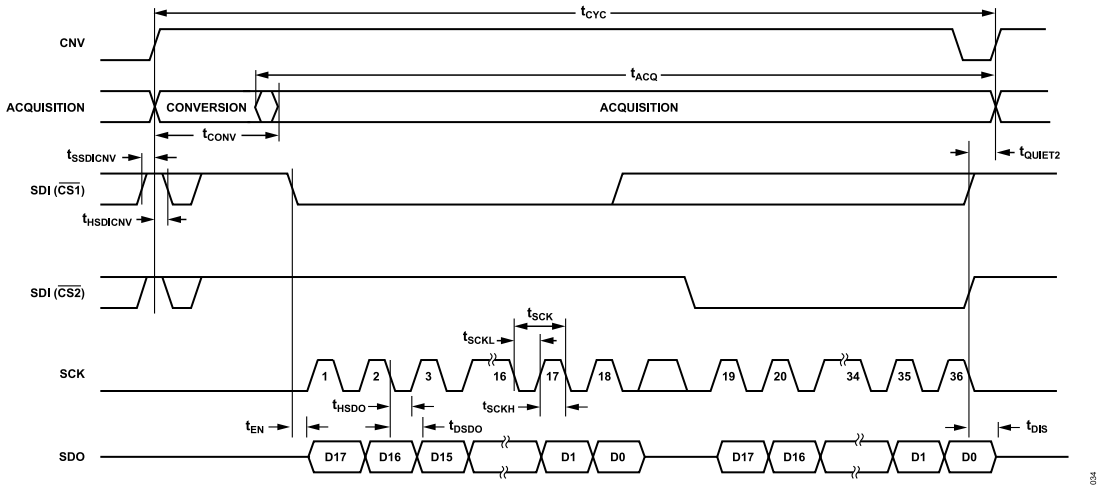

Figure 65. $\overline{CS}$ Mode, 4-Wire Without Busy Indicator Serial Interface Timing Diagram

APPLICATIONS INFORMATION

$\overline{CS}$ MODE, 4-WIRE WITH BUSY INDICATOR

This mode is typically used when a single ADAQ4003 device is connected to an SPI-compatible digital host with an interrupt input ($\overline{IRQ}$), and when it is desired to keep CNV, which samples the analog input, independent of the signal used to select the data reading. This independence is particularly important in applications where low jitter on CNV is desired.

The connection diagram is shown in Figure 66, and the corresponding timing diagram is shown in Figure 67.

With SDI high, a rising edge on CNV initiates a conversion, selects the $\overline{CS}$ mode, and forces SDO to high impedance. In this mode, CNV must be held high during the conversion phase and the subsequent data readback. If SDI and CNV are low, SDO is driven low. Prior to the minimum conversion time, SDI can select other SPI devices, such as analog multiplexers. However, SDI must be returned low before the minimum conversion time elapses and then held low for the maximum possible conversion time to guarantee the generation of the busy signal indicator.

When the conversion is complete, SDO goes from high impedance to low impedance. With a pull-up resistor of 1 kΩ on the SDO line, this transition can be used as an interrupt signal to initiate the data readback controlled by the digital host. The ADAQ4003 then enters the acquisition phase and powers down. The data bits are then clocked out, MSB first, by subsequent SCK falling edges. The data is valid on both SCK edges. Although the rising edge can capture the data, a digital host using the SCK falling edge allows a faster reading rate, provided that the digital host has an acceptable hold time. After the optional 19th SCK falling edge or when SDI goes high (whichever occurs first), SDO returns to high impedance.

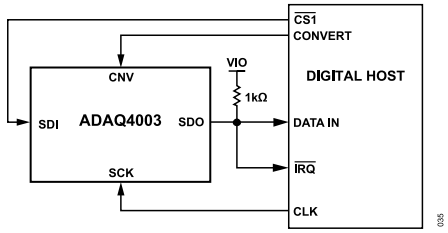

Figure 66. $\overline{CS}$ Mode, 4-Wire with Busy Indicator Connection Diagram

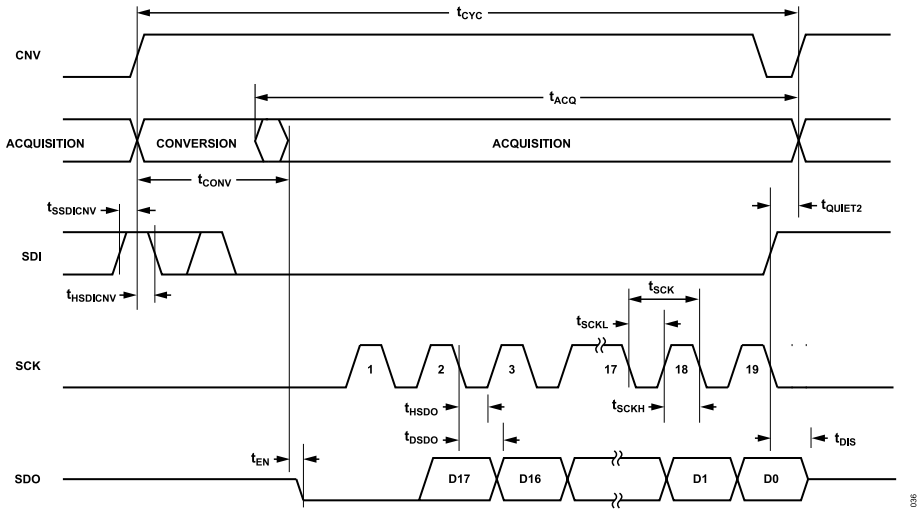

Figure 67. $\overline{CS}$ Mode, 4-Wire with Busy Indicator Serial Interface Timing Diagram

APPLICATIONS INFORMATION

DAISY-CHAIN MODE

Use this mode to daisy-chain multiple ADAQ4003 devices on a 3-wire or 4-wire serial interface. This feature is useful for reducing component count and wiring connections, for example, in isolated multiconverter applications or for systems with a limited interfacing capacity. Data readback is analogous to clocking a shift register.

A connection diagram example using two ADAQ4003 devices is shown in Figure 68, and the corresponding timing diagram is shown in Figure 69.

When SDI and CNV are low, SDO is driven low. With SCK low, a rising edge on CNV initiates a conversion, selects daisy-chain mode, and disables the busy indicator. In this mode, CNV is held high during the conversion phase and the subsequent data readback. When the conversion is complete, the MSB is output onto SDO, and the ADAQ4003 enters the acquisition phase and powers down. The remaining data bits stored in the internal shift register are clocked out of SDO by subsequent SCK falling edges. For each ADC, SDI feeds the input of the internal shift register and is clocked by the SCK rising edges. Each ADC in the daisy-chain outputs its data MSB first, and 18 × N clocks are required to read back the N ADCs. The data is valid on both SCK edges. The maximum conversion rate is reduced because of the total readback time.

It is possible to write to each ADC register in daisy-chain mode (see Figure 69). This mode requires 4-wire operation because data is clocked in on the SDI line with CNV held low. The same command byte and register data can be shifted through the entire chain to program all ADCs in the chain with the same register contents, which requires 8 × (N + 1) clocks for N ADCs. It is possible to write different register contents to each ADC in the chain by writing to the furthest ADC in the chain, first using 8 × (N + 1) clocks, and then the second furthest ADC with 8 × N clocks, and so forth until reaching the nearest ADC in the chain, which requires 16 clocks for the command and register data.

It is not possible to read register contents in daisy-chain mode. However, the six status bits can be enabled if the user wants to determine the ADC configuration. Note that enabling the status bits require six extra clocks to clock out the ADC result and the status bits per ADC in the chain. Turbo mode cannot be used in daisy-chain mode.

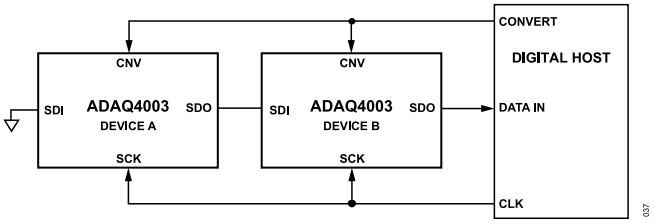

Figure 68. Daisy-Chain Mode Connection Diagram

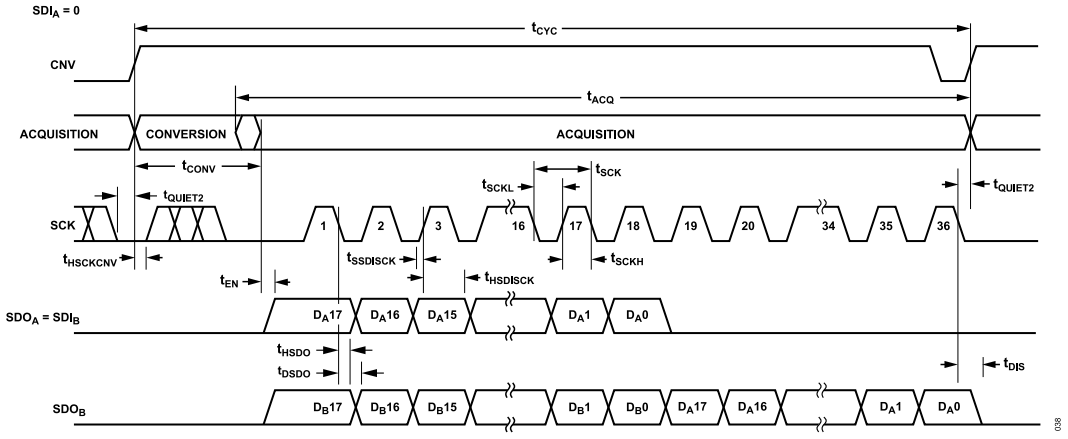

Figure 69. Daisy-Chain Mode Serial Interface Timing Diagram

APPLICATIONS INFORMATION

LAYOUT GUIDELINES

The PCB layout is critical for preserving signal integrity and achieving the expected performance from the ADAQ4003. It is recommended to design a multilayer board with an internal, clean ground plane and a separate power plane to route various supply rails beneath the ADAQ4003. Care must be taken with the placement of individual components and routing of various signals on the board. It is highly recommended to route input and output signals symmetrically while keeping the power supply circuitry away from the analog signal path. Keep the sensitive analog and digital sections separate and confined to certain areas of the board and avoid crossover of digital and analog signals.

The pinout of the ADAQ4003 eases the layout and allowing its analog signals on the left side and its digital signals on the right side. Fast switching signals, such as CNV or clocks, must not run near or crossover analog signal paths to prevent noise coupling to the ADAQ4003. Remove the ground and power planes beneath the input and output pins of ADAQ4003 to avoid undesired parasitic capacitance, especially underneath summing junction nodes (IN+ and IN−) and any floating inputs. Any undesired parasitic capacitance on the summing junction nodes tends to reduce the phase margin of the FDA and impact the distortion and linearity performance of the ADAQ4003.

The ADAQ4003 enables high channel density PCB layout by incorporating all the necessary decoupling ceramic capacitors for the reference and power supply (REF, VS+, VS−, VDD, and VIO) pins to provide a low impedance path to ground at high frequencies and to handle the transient currents so that the additional external decoupling capacitors are not required without causing any performance impact or electromagnetic interference (EMI) issues, saving board space. This performance impact was verified on the EVAL-ADAQ4003FMCZ by removing the external decoupling capacitors on the output of reference and LDO regulators that generate the on-board rails (REF, VS+, VS−, VDD, and VIO). Figure 70 shows that any spurs are buried well below −120 dB in the noise floor whether the external decoupling capacitors are used or removed. The recommended board layout is outlined in the EVAL-ADAQ4003FMCZ user guide.

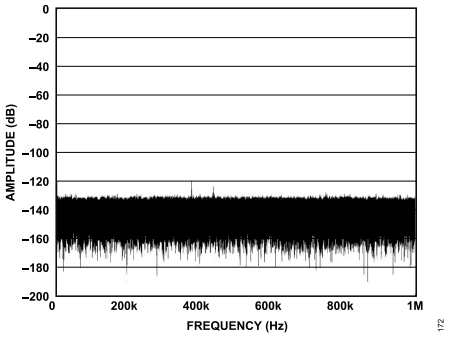

Figure 70. FFT with Shorted Inputs

OUTLINE DIMENSIONS

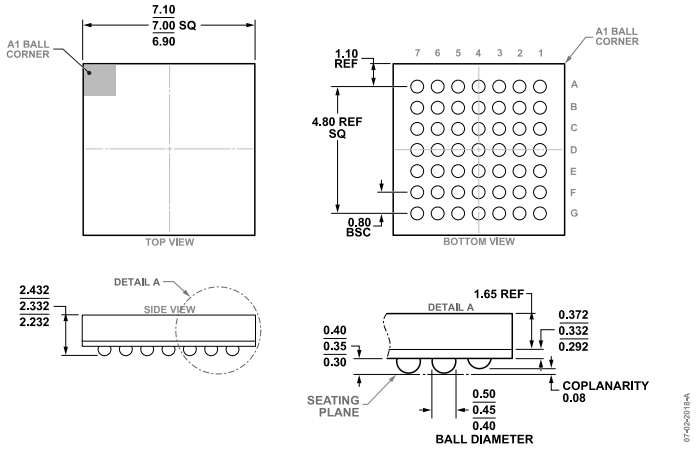

Figure 71. 49-Ball Chip Scale Package Ball Grid Array [CSP_BGA]
(BC-49-5)
Dimensions shown in millimeters

Updated: December 01, 2021

ORDERING GUIDE

Model[1]	Temperature Range	Package Description	Packing Quantity	Package Option
ADAQ4003BBCZ	-40°C to +125°C	49-Ball CSPBGA (7mm x 7mm)	Tray, 416	BC-49-5
ADAQ4003BBCZ-RL13	-40°C to +125°C	49-Ball CSPBGA (7mm x 7mm)	Reel, 2000	BC-49-5

[1] Z = RoHS Compliant Part.

EVALUATION BOARDS

Model[1, 2]	Description
EVAL-ADAQ4003FMCZ	Evaluation Board Kit

[1] Z = RoHS Compliant Part.

[2] The EVAL-ADAQ4003FMCZ evaluation board kit is compatible with the EVAL-SDP-CH1Z. See the UG-1533 for more details.

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Analog Devices Inc.:

ADAQ4003BBCZ ADAQ4003BBCZ-RL13 EVAL-ADAQ4003FMCZ ADSKPMB10-EV-FMCZ