Ultralow Distortion, Low Power, Low Noise, High Speed Op Amp

ADA4857-1/ADA4857-2

FEATURES

- **High speed**
  - **850 MHz, −3 dB bandwidth (G = +1, R_L = 1 kΩ, LFCSP)**
  - **750 MHz, −3 dB bandwidth (G = +1, R_L = 1 kΩ, SOIC)**
  - **2800 V/µs slew rate**
- **Low distortion: −88 dBc at 10 MHz (G = +1, R_L = 1 kΩ)**
- **Low power: 5 mA/amplifier at 10 V**
- **Low noise: 4.4 nV/√Hz**
- **Wide supply voltage range: 5 V to 10 V**
- **Power-down feature**
- **Available in 3 mm × 3 mm 8-lead LFCSP (single), 8-lead SOIC (single), and 4 mm × 4 mm 16-lead LFCSP (dual)**

APPLICATIONS

- **Instrumentation**
- **IF and baseband amplifiers**
- **Active filters**
- **ADC drivers**
- **DAC buffers**

CONNECTION DIAGRAMS

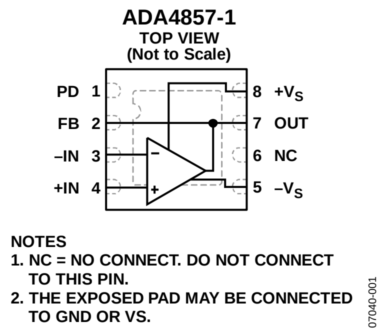

Figure 1. 8-Lead LFCSP (CP)

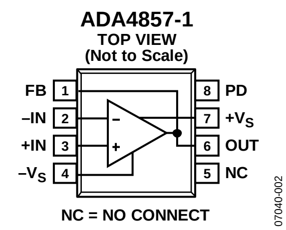

Figure 2. 8-Lead SOIC (R)

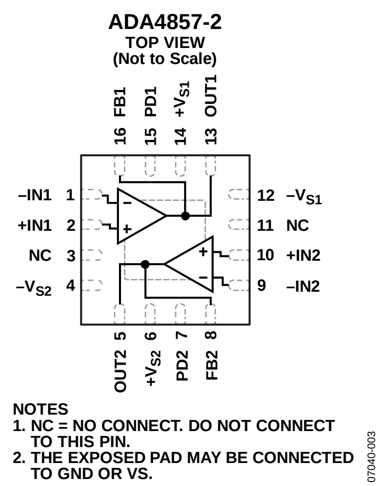

Figure 3. 16-Lead LFCSP (CP)

GENERAL DESCRIPTION

The ADA4857 is a unity-gain stable, high speed, voltage feedback amplifier with low distortion, low noise, and high slew rate. With a spurious-free dynamic range (SFDR) of −88 dBc at 10 MHz, the ADA4857 is an ideal solution for a variety of applications, including ultrasounds, ATE, active filters, and ADC drivers. The Analog Devices, Inc., proprietary next-generation XFCB process and innovative architecture enables such high performance amplifiers.

The ADA4857 has 850 MHz bandwidth, 2800 V/µs slew rate, and settles to 0.1% in 15 ns. With a wide supply voltage range (5 V to 10 V), the ADA4857 is an ideal candidate for systems that require high dynamic range, precision, and speed.

The ADA4857-1 amplifier is available in a 3 mm × 3 mm, 8-lead LFCSP and a standard 8-lead SOIC. The ADA4857-2 is available in a 4 mm × 4 mm, 16-lead LFCSP. The LFCSP features an exposed paddle that provides a low thermal resistance path to the printed circuit board (PCB). This path enables more efficient heat transfer and increases reliability. The ADA4857 works over the extended industrial temperature range (−40°C to +125°C).

Rev. D **Document Feedback**

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Technical Support **www.analog.com**

TABLE OF CONTENTS

REVISION HISTORY

1/2017—Rev. C to Rev. D

Changes to Figure 1 ... 1
Changes to Table 1 ... 3
Changes to Table 2 ... 4
Changes to Figure 5 ... 7
Added Figure 40 and Figure 43; Renumbered Sequentially ... 14
Added Figure 44, Figure 45, Figure 46, Figure 47, and Figure 48 ... 15
Changes to Power-Down Operation Section ... 17
Updated Outline Dimensions ... 20
Changes to Ordering Guide ... 21

9/2013—Rev. B to Rev. C

Changes to Figure 1 and Figure 3 ... 1
Change to Figure 5 ... 7
Change to Figure 7 ... 8
Updated Outline Dimensions ... 20
Changes to Ordering Guide ... 20

8/2011—Rev. A to Rev. B

Changes to Table 1 Conditions ... 3
Changes to Table 2 Conditions ... 4
Changes to Typical Performance Characteristics Conditions ... 9
Changes to Figure 18 ... 10
Changes to Figure 42 ... 15
Changes to Table 9 ... 16
Changes to Ordering Guide ... 20

11/2008—Rev. 0 to Rev. A

Changes to Table 5 ... 7
Changes to Table 7 ... 8
Changes to Figure 32 ... 13
Added Figure 44; Renumbered Sequentially ... 15
Changes to Layout ... 15
Changes to Table 8 ... 16
Added Active Low-Pass Filter (LFP) Section ... 17
Added Figure 48 and Figure 49; Renumbered Sequentially ... 17
Changes to Grounding Section ... 18
Exposed Paddle Notation Added to Outline Dimensions ... 19
Changes to Ordering Guide ... 20

5/2008—Revision 0: Initial Version

SPECIFICATIONS

±5 V SUPPLY

T_A = 25°C, G = 2, R_G = R_F = 499 Ω, R_S = 100 Ω for G = 1 (SOIC), R_L = 1 kΩ to ground, PD = no connect, unless otherwise noted.

Table 1.

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
DYNAMIC PERFORMANCE					
−3 dB Bandwidth (LFCSP/SOIC)	Gain (G) = 1, V_{OUT} = 0.2 V p-p	650	850/750		MHz
	G = 1, V_{OUT} = 2 V p-p		600/550		MHz
	G = 2, V_{OUT} = 0.2 V p-p		400/350		MHz
Full Power Bandwidth	G = 1, V_{OUT} = 2 V p-p, THD < −40 dBc		110		MHz
Bandwidth for 0.1 dB Flatness (LFCSP/SOIC)	G = 2, V_{OUT} = 2 V p-p, R_L = 150 Ω		75/90		MHz
Slew Rate (10% to 90%)	G = 1, V_{OUT} = 4 V step		2800		V/µs
Settling Time to 0.1%	G = 2, V_{OUT} = 2 V step		15		ns
NOISE/HARMONIC PERFORMANCE					
Harmonic Distortion	f = 1 MHz, G = 1, V_{OUT} = 2 V p-p (HD2)		−108		dBc
	f = 1 MHz, G = 1, V_{OUT} = 2 V p-p (HD3)		−108		dBc
	f = 10 MHz, G = 1, V_{OUT} = 2 V p-p (HD2)		−88		dBc
	f = 10 MHz, G = 1, V_{OUT} = 2 V p-p (HD3)		−93		dBc
	f = 50 MHz, G = 1, V_{OUT} = 2 V p-p (HD2)		−65		dBc
	f = 50 MHz, G = 1, V_{OUT} = 2 V p-p (HD3)		−62		dBc
Input Voltage Noise	f = 100 kHz		4.4		nV/√Hz
Input Current Noise	f = 100 kHz		1.5		pA/√Hz
DC PERFORMANCE					
Input Offset Voltage			±2	±4.5	mV
	T_{MIN} to T_{MAX}			±7.2	mV
Input Offset Voltage Drift	T_{MIN} to T_{MAX}		2.3	22	µV/°C
Input Bias Current			−2	−3.3	µA
	T_{MIN} to T_{MAX}			−3.8	µA
Input Bias Offset Current			50	800	nA
Open-Loop Gain	V_{OUT} = −2.5 V to +2.5 V		57		dB
PD (POWER-DOWN) PIN					
PD Input Voltage	Chip powered down		≥ (+V_S − 2)		V
	Chip powered down, T_{MIN} to T_{MAX}	≥ (+V_S − 1.7)			V
	Chip enabled		≤ (+V_S − 4.2)		V
	Chip enabled, T_{MIN} to T_{MAX}			≤ (+V_S − 5.3)	V
Turn-Off Time	50% off PD to <10% of final V_{OUT}, V_{IN} = 1 V, G = 2		55		µs
Turn-On Time	50% off PD to <10% of final V_{OUT}, V_{IN} = 1 V, G = 2		33		ns
PD Pin Leakage Current	Chip enabled		58		µA
	Chip powered down		80		µA
INPUT CHARACTERISTICS					
Input Resistance	Common mode		8		MΩ
	Differential mode		4		MΩ
Input Capacitance	Common mode		2		pF
Input Common-Mode Voltage Range			±4		V
Common-Mode Rejection Ratio	V_{CM} = ±1 V	−78	−86		dB
	V_{CM} = −3.6 V to +3.7 V, T_{MIN} to T_{MAX}	−70			dB

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
OUTPUT CHARACTERISTICS					
Output Overdrive Recovery Time	V_{IN} = ±2.5 V, G = 2		10		ns
Output Voltage Swing					
High	R_L = 1 kΩ		$+V_S$ − 1		V
	R_L = 1 kΩ, T_{MIN} to T_{MAX}	$+V_S$ − 1.3			V
	R_L = 100 Ω		$+V_S$ − 1.3		V
	R_L = 100 Ω, T_{MIN} to T_{MAX}	$+V_S$ − 2			V
Low	R_L = 1 kΩ		$−V_S$ + 1		V
	R_L = 1 kΩ, T_{MIN} to T_{MAX}			$−V_S$ + 1.3	V
	R_L = 100 Ω		$−V_S$ + 1.3		V
	R_L = 100 Ω, T_{MIN} to T_{MAX}			$−V_S$ + 3	V
Output Current			50		mA
Short-Circuit Current	Sinking and sourcing		125		mA
Capacitive Load Drive	30% overshoot, G = 2		10		pF
POWER SUPPLY					
Operating Range		4.5		10.5	V
Quiescent Current			5	5.5	mA
Quiescent Current (Power Down)	PD ≥ V_{CC} − 2 V		350	450	μA
Positive Power Supply Rejection	$+V_S$ = 4.5 V to 5.5 V, $−V_S$ = −5 V	−59	−62		dB
Negative Power Supply Rejection	$+V_S$ = 5 V, $−V_S$ = −4.5 V to −5.5 V	−65	−68		dB

+5 V SUPPLY

T_A = 25°C, G = 2, R_F = R_G = 499 Ω, R_S = 100 Ω for G = 1 (SOIC), R_L = 1 kΩ to midsupply, PD = no connect, unless otherwise noted.

Table 2.

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
DYNAMIC PERFORMANCE					
−3 dB Bandwidth (LFCSP/SOIC)	G = 1, V_{OUT} = 0.2 V p-p	595	800/750		MHz
	G = 1, V_{OUT} = 2 V p-p		500/400		MHz
	G = 2, V_{OUT} = 0.2 V p-p		360/300		MHz
Full Power Bandwidth	G = 1, V_{OUT} = 2 V p-p, THD < −40 dBc		95		MHz
Bandwidth for 0.1 dB Flatness (LFCSP/SOIC)	G = 2, V_{OUT} = 2 V p-p, R_L = 150 Ω		50/40		MHz
Slew Rate (10% to 90%)	G = 1, V_{OUT} = 2 V step		1500		V/μs
Settling Time to 0.1%	G = 2, V_{OUT} = 2 V step		15		ns
NOISE/HARMONIC PERFORMANCE					
Harmonic Distortion	f = 1 MHz, G = 1, V_{OUT} = 2 V p-p (HD2)		−92		dBc
	f = 1 MHz, G = 1, V_{OUT} = 2 V p-p (HD3)		−90		dBc
	f = 10 MHz, G = 1, V_{OUT} = 2 V p-p (HD2)		−81		dBc
	f = 10 MHz, G = 1, V_{OUT} = 2 V p-p (HD3)		−71		dBc
	f = 50 MHz, G = 1, V_{OUT} = 2 V p-p (HD2)		−69		dBc
	f = 50 MHz, G = 1, V_{OUT} = 2 V p-p (HD3)		−55		dBc
Input Voltage Noise	f = 100 kHz		4.4		nV/√Hz
Input Current Noise	f = 100 kHz		1.5		pA/√Hz
DC PERFORMANCE					
Input Offset Voltage			±1	±4.2	mV
	T_{MIN} to T_{MAX}			±6.4	mV
Input Offset Voltage Drift	T_{MIN} to T_{MAX}		4.6	23	μV/°C
Input Bias Current			−1.7	−3.3	μA
	T_{MIN} to T_{MAX}			−4.1	μA
Input Bias Offset Current			50	800	nA
Open-Loop Gain	V_{OUT} = 1.25 V to 3.75 V		57		dB

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
PD (POWER-DOWN) PIN					
PD Input Voltage	Chip powered down		≥ $(+V_S - 2)$		V
	Chip powered down, T_{MIN} to T_{MAX}	≥ $(+V_S - 1.4)$			V
	Chip enabled		≤ $(+V_S - 4.2)$		V
	Chip enabled, T_{MIN} to T_{MAX}			≤ $(+V_S - 4.8)$	V
Turn-Off Time	50% off PD to <10% of final V_{OUT}, V_{IN} = 1 V, G = 2		38		µs
Turn-On Time	50% off PD to <10% of final V_{OUT}, V_{IN} = 1 V, G = 2		30		ns
PD Pin Leakage Current	Chip enable		8		µA
	Chip powered down		30		µA
INPUT CHARACTERISTICS					
Input Resistance	Common mode		8		MΩ
	Differential mode		4		MΩ
Input Capacitance	Common mode		2		pF
Input Common-Mode Voltage Range			1 to 4		V
Common-Mode Rejection Ratio	V_{CM} = 2 V to 3 V	−76	−84		dB
	V_{CM} = 1.3 V to 3.7 V, T_{MIN} to T_{MAX}	−70			dB
OUTPUT CHARACTERISTICS					
Overdrive Recovery Time	G = 2		15		ns
Output Voltage Swing					
High	R_L = 1 kΩ		$+V_S - 1$		V
	R_L = 1 kΩ, T_{MIN} to T_{MAX}	$+V_S - 1.3$			V
	R_L = 100 Ω		$+V_S - 1.1$		V
	R_L = 100 Ω, T_{MIN} to T_{MAX}	$+V_S - 1.7$			V
Low	R_L = 1 kΩ		$-V_S + 1$		V
	R_L = 1 kΩ, T_{MIN} to T_{MAX}			$-V_S + 1.3$	V
	R_L = 100 Ω		$-V_S + 1.1$		V
	R_L = 100 Ω, T_{MIN} to T_{MAX}			$-V_S + 1.6$	V
Output Current			50		mA
Short-Circuit Current	Sinking and sourcing		75		mA
Capacitive Load Drive	30% overshoot, G = 2		10		pF
POWER SUPPLY					
Operating Range		4.5		10.5	V
Quiescent Current			4.5	5	mA
Quiescent Current (Power Down)	PD ≥ V_{CC} − 2 V		250	350	µA
Positive Power Supply Rejection	$+V_S$ = 4.5 V to 5.5 V, $-V_S$ = 0 V	−58	−62		dB
Negative Power Supply Rejection	$+V_S$ = 5 V, $-V_S$ = −0.5 V to +0.5 V	−65	−68		dB

ABSOLUTE MAXIMUM RATINGS

Table 3.

Parameter	Rating
Supply Voltage	11 V
Power Dissipation	See Figure 4
Common-Mode Input Voltage	$-V_S + 0.7$ V to $+V_S - 0.7$ V
Differential Input Voltage	$\pm V_S$
Exposed Paddle Voltage	$-V_S$
Storage Temperature Range	−65°C to +125°C
Operating Temperature Range	−40°C to +125°C
Lead Temperature (Soldering, 10 sec)	300°C
Junction Temperature	150°C

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

THERMAL RESISTANCE

θ_{JA} is specified for the worst-case conditions, that is, θ_{JA} is specified for device soldered in circuit board for surface-mount packages.

Table 4.

Package Type	θ_{JA}	θ_{JC}	Unit
8-Lead SOIC	115	15	°C/W
8-Lead LFCSP	94.5	34.8	°C/W
16-Lead LFCSP	68.2	19	°C/W

MAXIMUM POWER DISSIPATION

The maximum safe power dissipation for the ADA4857 is limited by the associated rise in junction temperature (T_J) on the die. At approximately 150°C, which is the glass transition temperature, the properties of the plastic change. Even temporarily exceeding this temperature limit may change the stresses that the package exerts on the die, permanently shifting the parametric performance of the ADA4857. Exceeding a junction temperature of 175°C for an extended period can result in changes in silicon devices, potentially causing degradation or loss of functionality.

The power dissipated in the package (P_D) is the sum of the quiescent power dissipation and the power dissipated in the die due to the ADA4857 drive at the output. The quiescent power is the voltage between the supply pins (V_S) times the quiescent current (I_S).

$$P_D = \textit{Quiescent Power} + (\textit{Total Drive Power} - \textit{Load Power})$$

$$P_D = \left(V_S \times I_S\right) + \left(\frac{V_S}{2} \times \frac{V_{OUT}}{R_L}\right) - \frac{{V_{OUT}}^2}{R_L}$$

RMS output voltages must be considered. If R_L is referenced to $-V_S$, as in single-supply operation, the total drive power is $V_S \times I_{OUT}$. If the rms signal levels are indeterminate, consider the worst case, when $V_{OUT} = V_S/4$ for R_L to midsupply.

$$P_D = \left(V_S \times I_S\right) + \frac{\left(V_S/4\right)^2}{R_L}$$

In single-supply operation with R_L referenced to $-V_S$, the worst case is $V_{OUT} = V_S/2$.

Airflow increases heat dissipation, effectively reducing θ_{JA}. In addition, more metal directly in contact with the package leads and exposed paddle from metal traces, through holes, ground, and power planes reduces θ_{JA}.

Figure 4 shows the maximum power dissipation in the package vs. the ambient temperature for the SOIC and LFCSP packages on a JEDEC standard 4-layer board. θ_{JA} values are approximations.

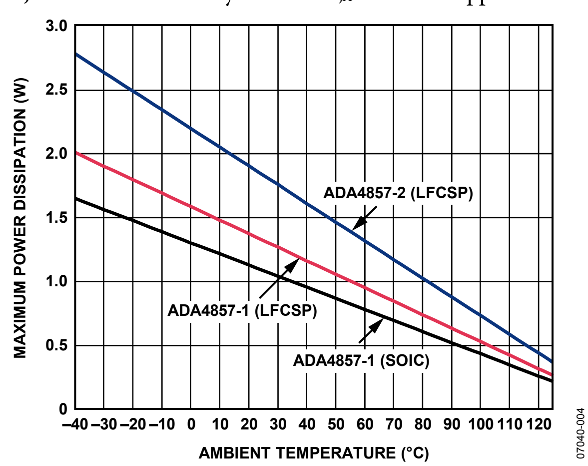
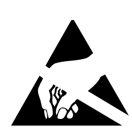


Figure 4. Maximum Power Dissipation vs. Temperature for a 4-Layer Board

ESD CAUTION



ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATIONS AND FUNCTION DESCRIPTIONS

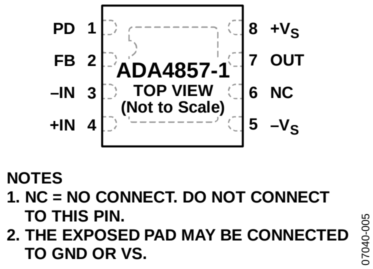


Figure 5. 8-Lead LFCSP Pin Configuration

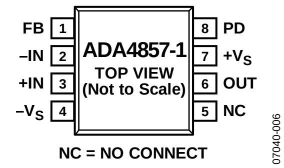


Figure 6. 8-Lead SOIC Pin Configuration

Table 5. 8-Lead LFCSP Pin Function Descriptions

Pin No.	Mnemonic	Description
1	PD	Power Down.
2	FB	Feedback.
3	−IN	Inverting Input.
4	+IN	Noninverting Input.
5	$-V_S$	Negative Supply.
6	NC	No Connect.
7	OUT	Output.
8	$+V_S$	Positive Supply.
EP	GND or V_S	Exposed Pad. The exposed pad may be connected to GND or V_S.

Table 6. 8-Lead SOIC Pin Function Descriptions

Pin No.	Mnemonic	Description
1	FB	Feedback.
2	−IN	Inverting Input.
3	+IN	Noninverting Input.
4	$-V_S$	Negative Supply.
5	NC	No Connect.
6	OUT	Output.
7	$+V_S$	Positive Supply.
8	PD	Power Down.

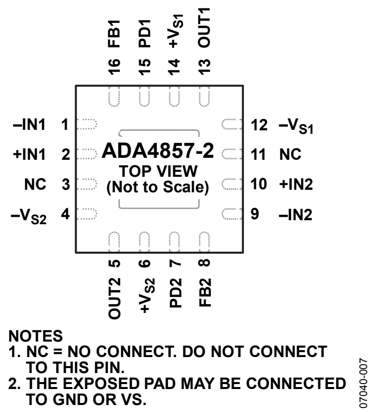


Figure 7. 16-Lead LFCSP Pin Configuration

Table 7. 16-Lead LFCSP Pin Function Descriptions

Pin No.	Mnemonic	Description
1	−IN1	Inverting Input 1.
2	+IN1	Noninverting Input 1.
3, 11	NC	No Connect.
4	$-V_{S2}$	Negative Supply 2.
5	OUT2	Output 2.
6	$+V_{S2}$	Positive Supply 2.
7	PD2	Power Down 2.
8	FB2	Feedback 2.
9	−IN2	Inverting Input 2.
10	+IN2	Noninverting Input 2.
12	$-V_{S1}$	Negative Supply 1.
13	OUT1	Output 1.
14	$+V_{S1}$	Positive Supply 1.
15	PD1	Power Down 1.
16	FB1	Feedback 1.
EP	GND or V_S	Exposed Pad. The exposed pad may be connected to GND or V_S.

TYPICAL PERFORMANCE CHARACTERISTICS

T = 25°C, G = +1, R_F = 0 Ω, and, R_G open, R_S = 100 Ω for SOIC, (for G = +2, R_F = R_G = 499 Ω), unless otherwise noted.

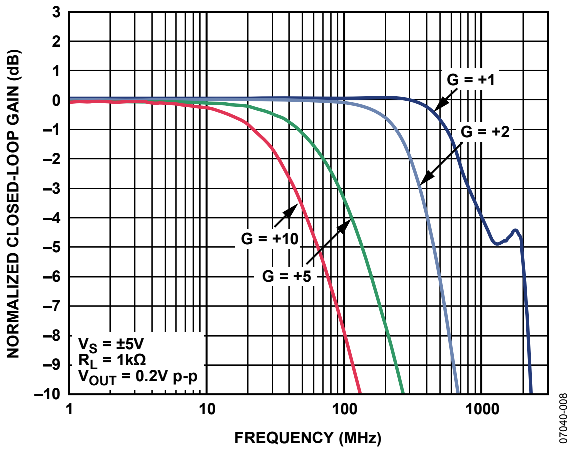


Figure 8. Small Signal Frequency Responses for Various Gains (LFCSP)

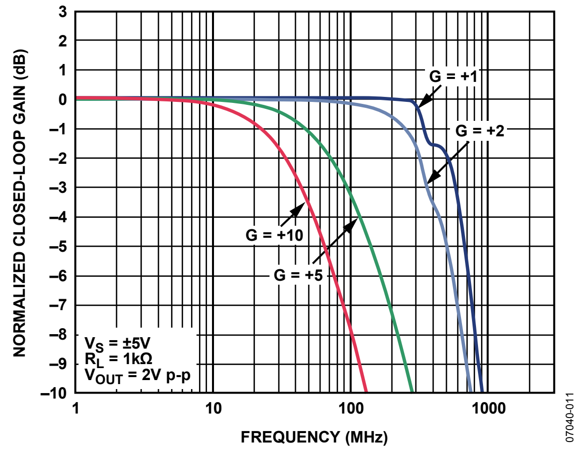


Figure 11. Large Signal Frequency Responses for Various Gains (LFCSP)

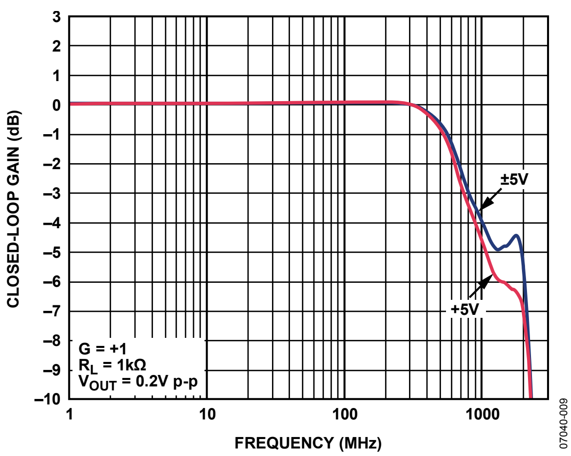


Figure 9. Small Signal Frequency Response for Various Supply Voltages (LFCSP)

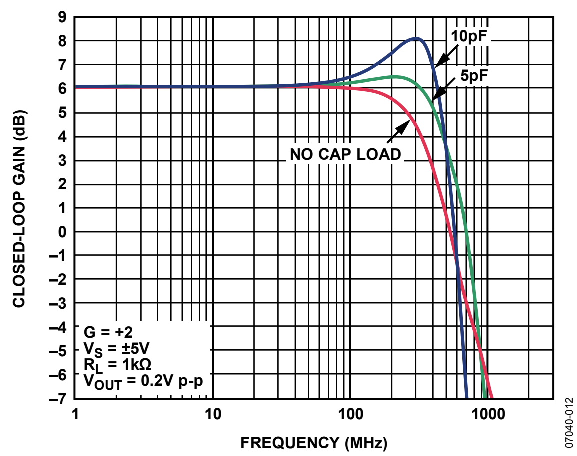


Figure 12. Small Signal Frequency Response for Various Capacitive Loads (LFCSP)

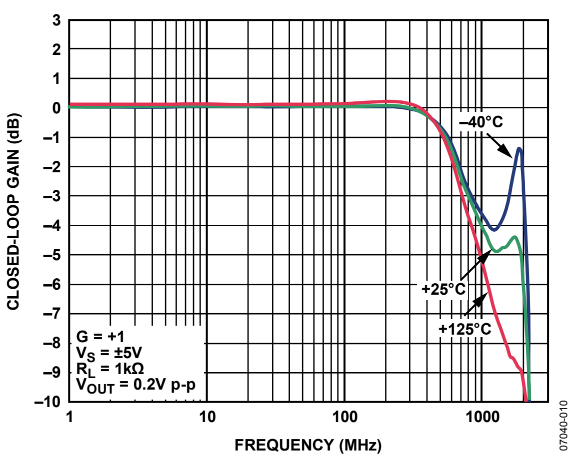


Figure 10. Small Signal Frequency Response for Various Temperatures (LFCSP)

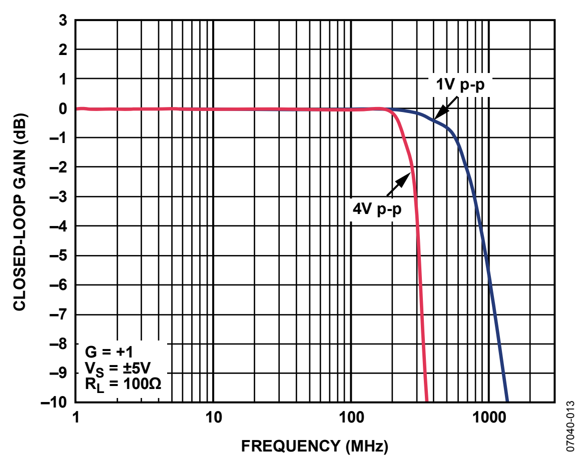


Figure 13. Large Signal Frequency Response vs. V_{OUT} (LFCSP)

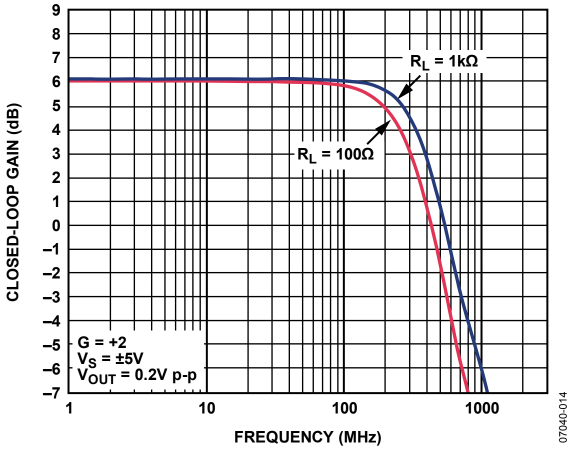


Figure 14. Small Signal Frequency Response for Various Resistive Loads (LFCSP)

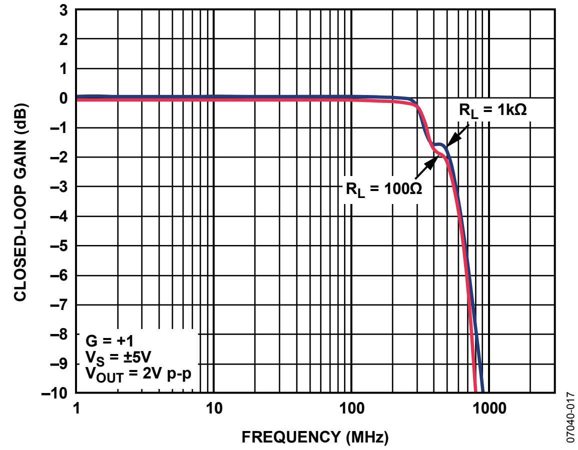


Figure 17. Large Signal Frequency Response for Various Resistive Loads (LFCSP)

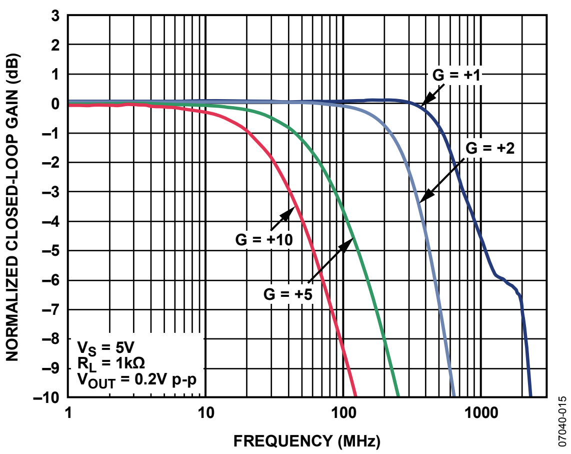


Figure 15. Small Signal Frequency Response for Various Gains (LFCSP)

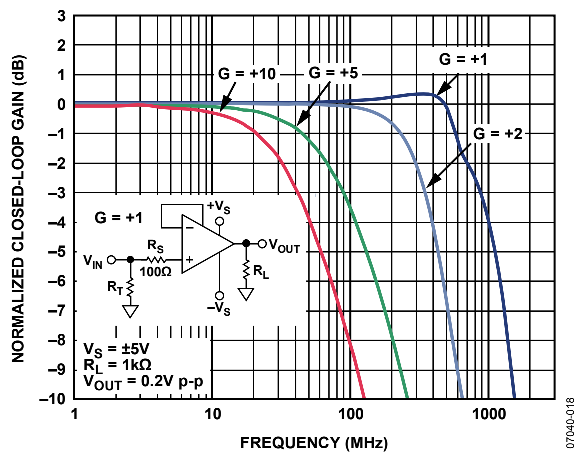


Figure 18. Small Signal Frequency Response for Various Gains (SOIC), $R_S = 100\ \Omega$ for G = +1

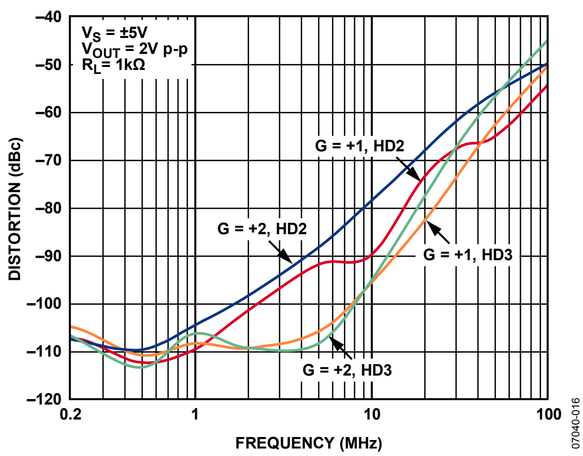


Figure 16. Harmonic Distortion vs. Frequency and Gain (LFCSP)

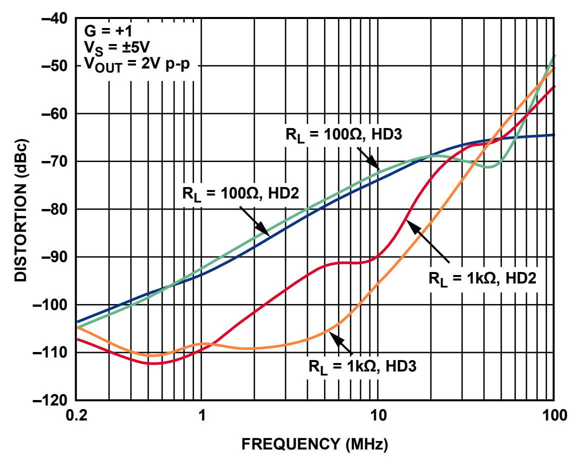


Figure 19. Harmonic Distortion vs. Frequency and Load (LFCSP)

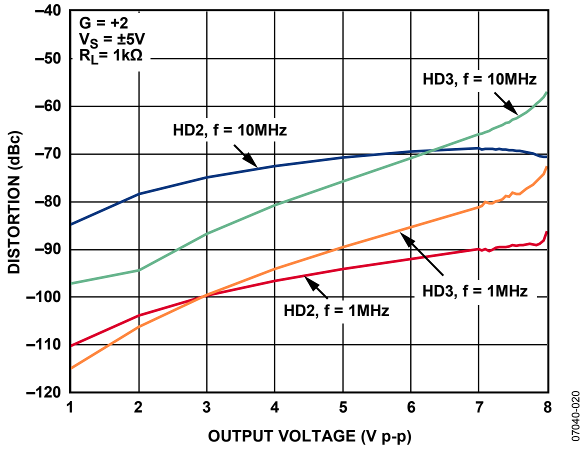


Figure 20. Harmonic Distortion vs. Output Voltage

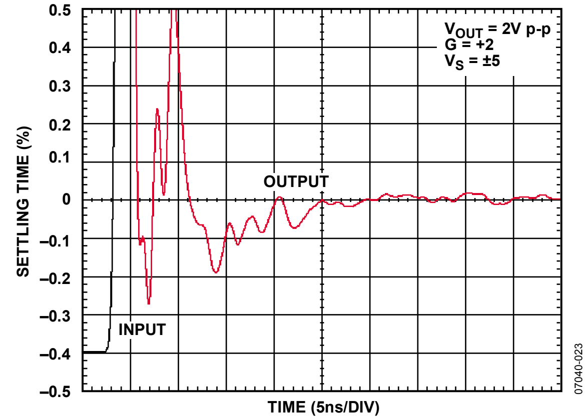


Figure 23. Short-Term Settling Time (LFCSP)

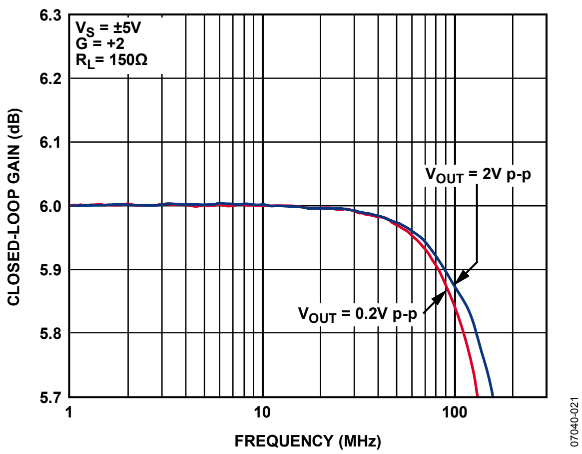


Figure 21. 0.1 dB Flatness vs. Frequency for Various Output Voltages (SOIC)

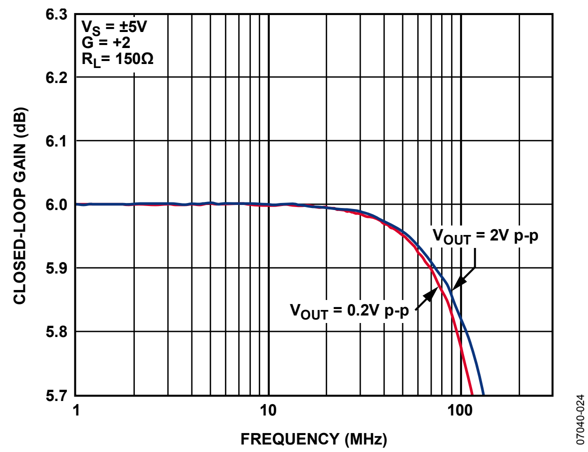


Figure 24. 0.1 dB Flatness vs. Frequency for Various Output Voltages (LFCSP)

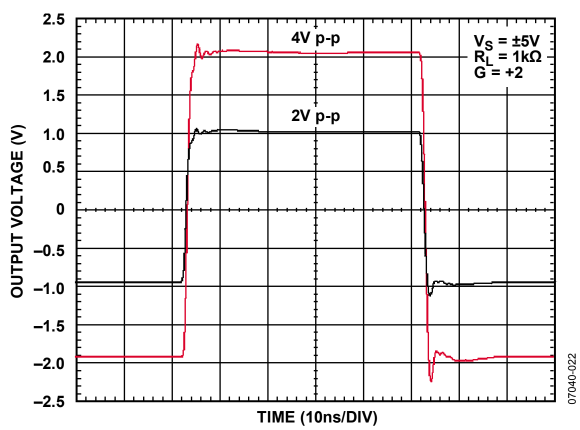


Figure 22. Large Signal Transient Response for Various Output Voltages (SOIC)

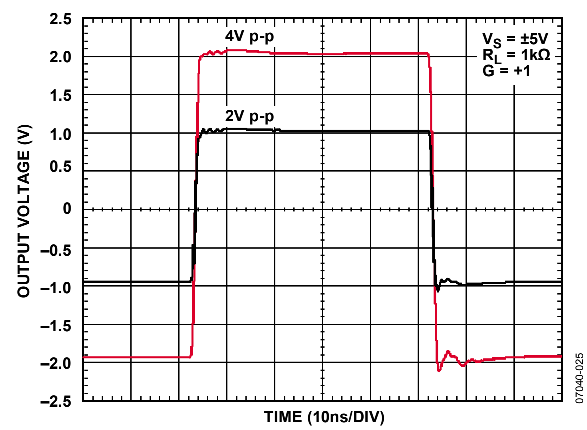


Figure 25. Large Signal Transient Response for Various Output Voltages (LFCSP)

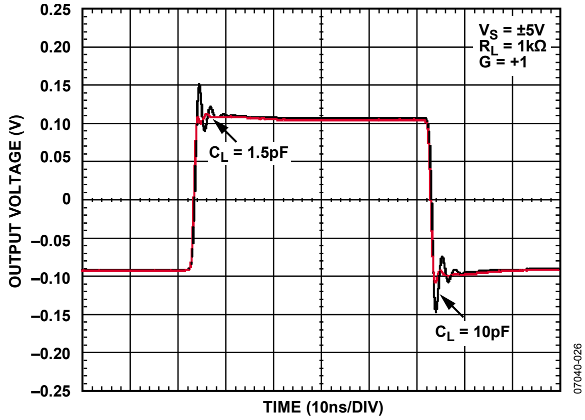


Figure 26. Small Signal Transient Response for Various Capacitive Loads (LFCSP)

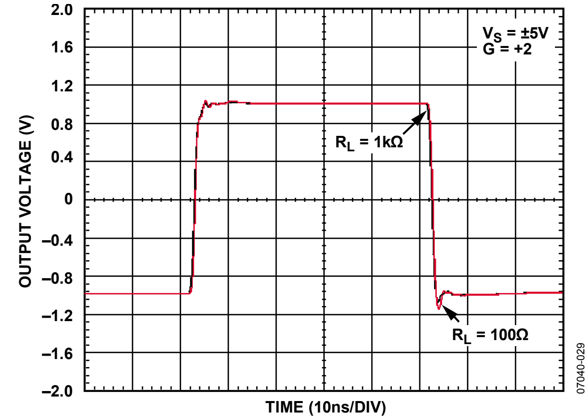


Figure 29. Large Signal Transient Response for Various Load Resistances (SOIC)

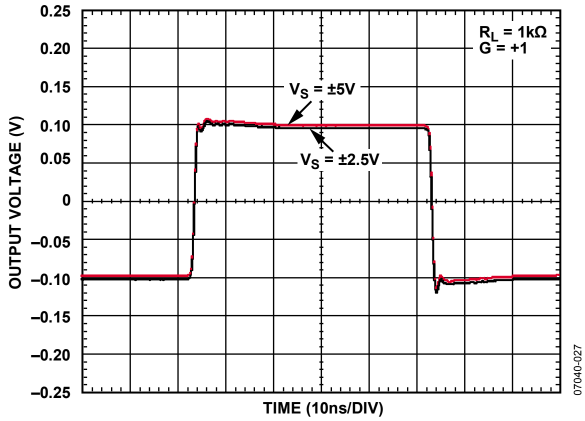


Figure 27. Small Signal Transient Response for Various Supply Voltages (LFCSP)

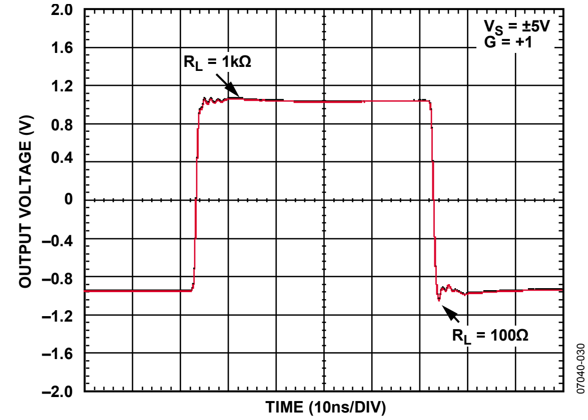


Figure 30. Large Signal Transient Response for Various Load Resistances (LFCSP)

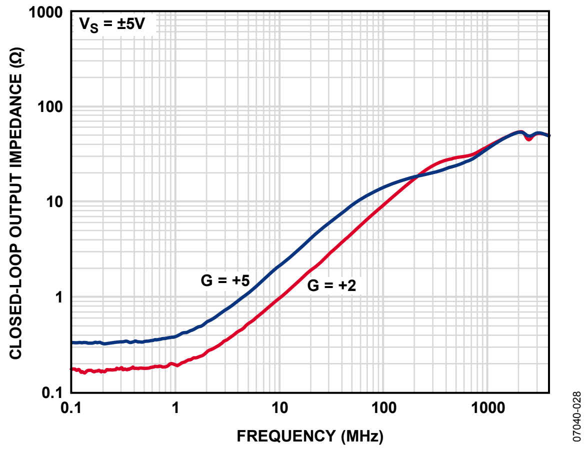


Figure 28. Closed-Loop Output Impedance vs. Frequency for Various Gains

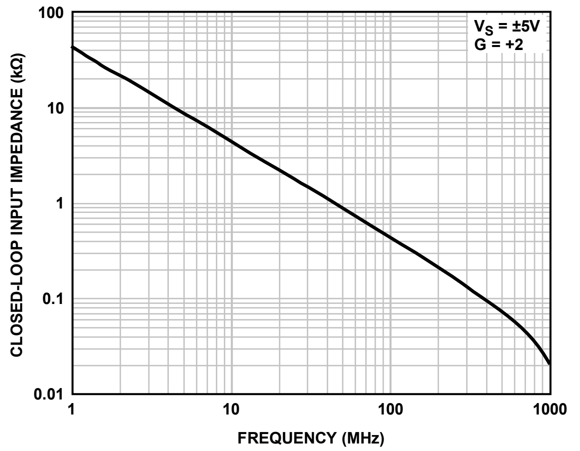


Figure 31. Closed-Loop Input Impedance vs. Frequency

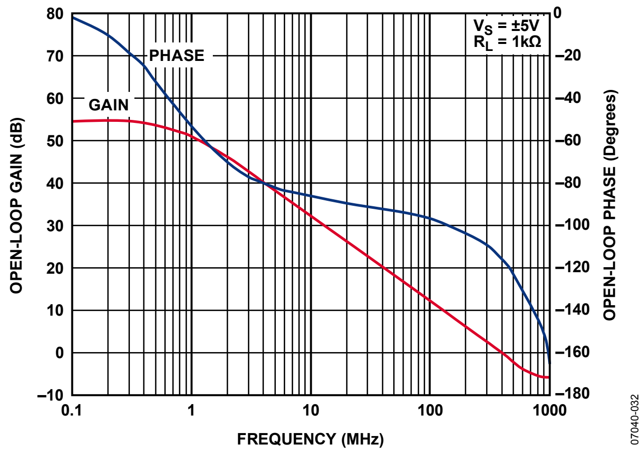


Figure 32. Open-Loop Gain and Phase vs. Frequency

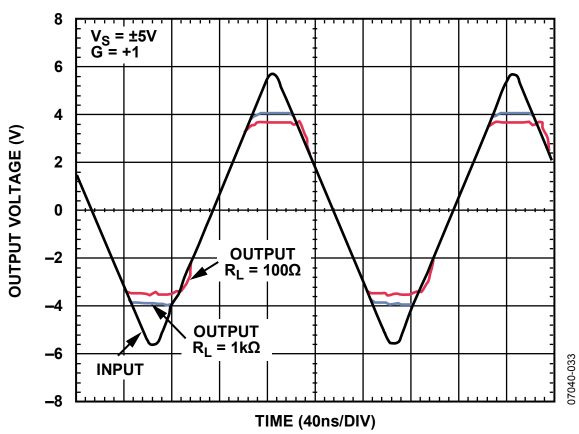


Figure 33. Input Overdrive Recovery for Various Resistive Loads

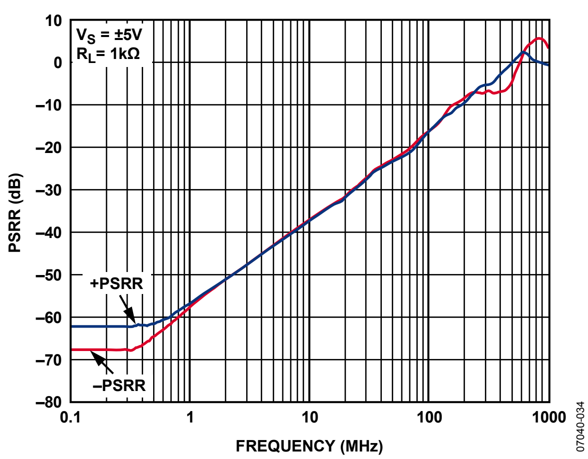


Figure 34. Power Supply Rejection Ratio (PSRR) vs. Frequency

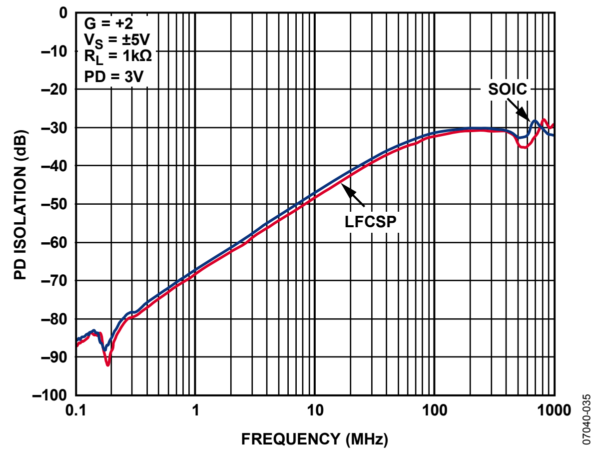


Figure 35. PD Isolation vs. Frequency

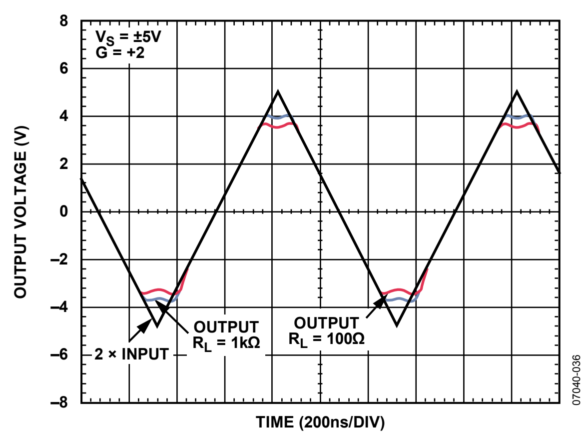


Figure 36. Output Overdrive Recovery for Various Resistive Loads

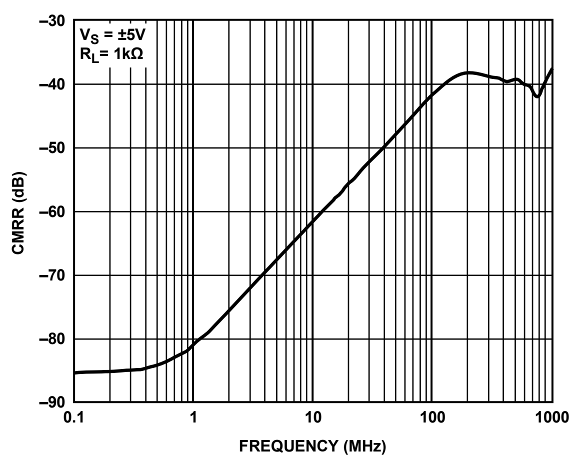


Figure 37. Common-Mode Rejection Ratio (CMRR) vs. Frequency

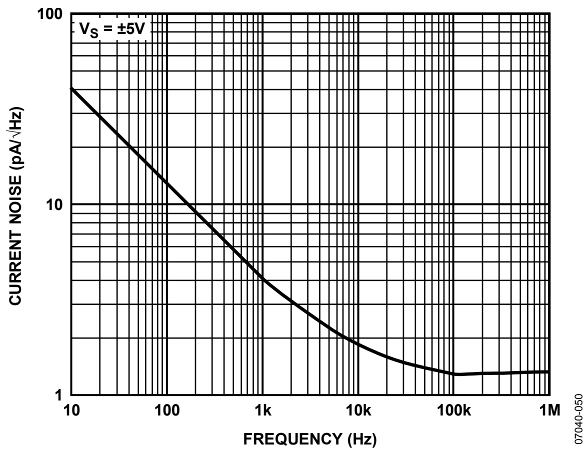


Figure 38. Input Current Noise vs. Frequency

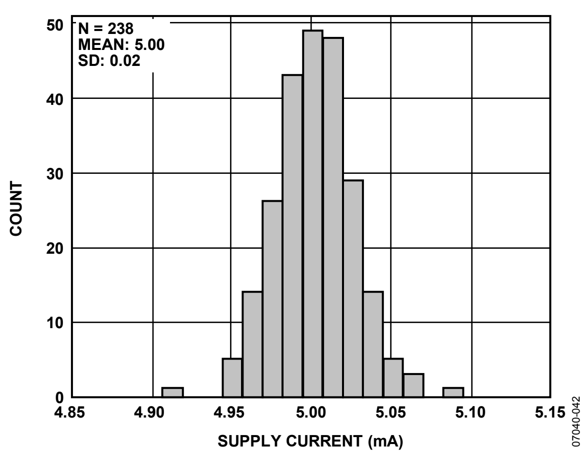


Figure 39. Supply Current

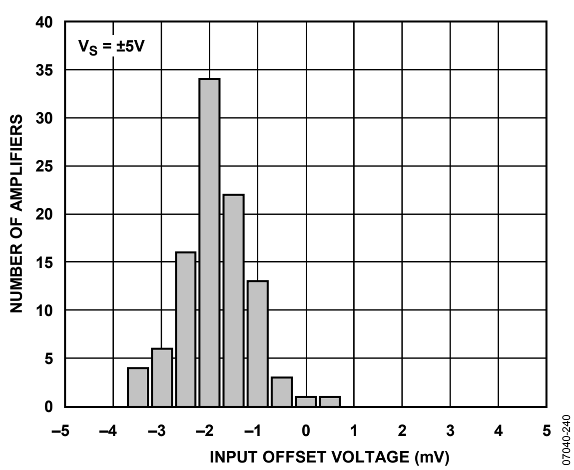


Figure 40. Input Offset Voltage Distribution, $V_S = \pm5$ V

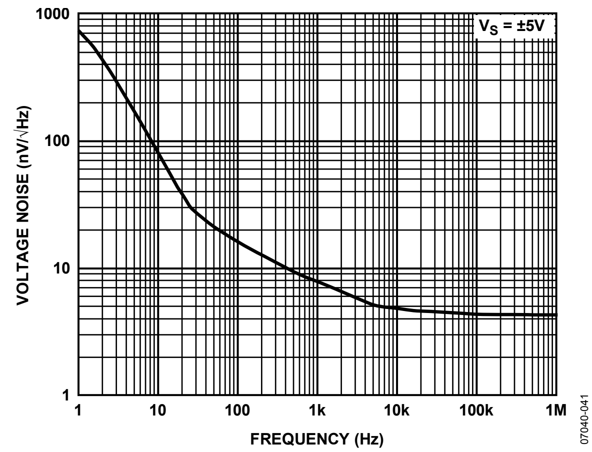


Figure 41. Input Voltage Noise vs. Frequency

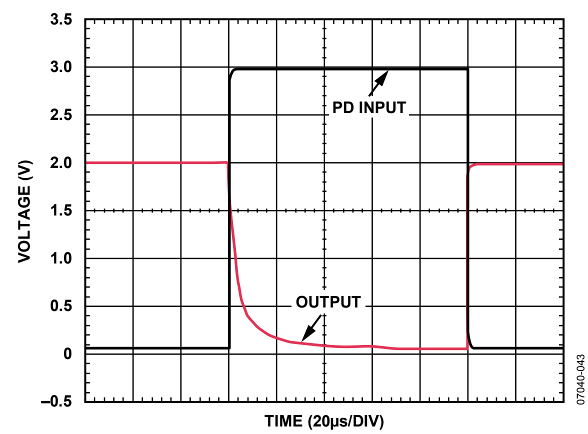


Figure 42. Disable/Enable Switching Speed

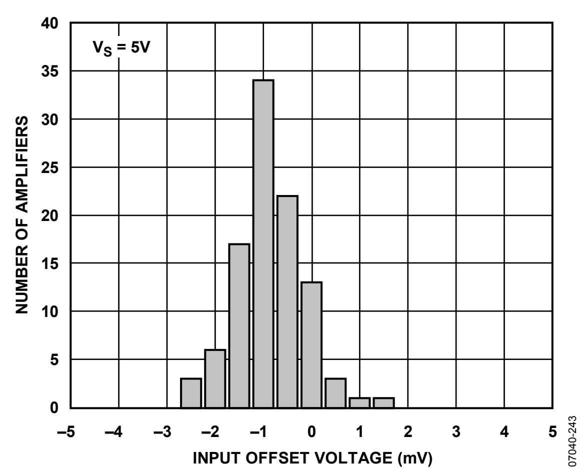


Figure 43. Input Offset Voltage Distribution, $V_S = 5$ V

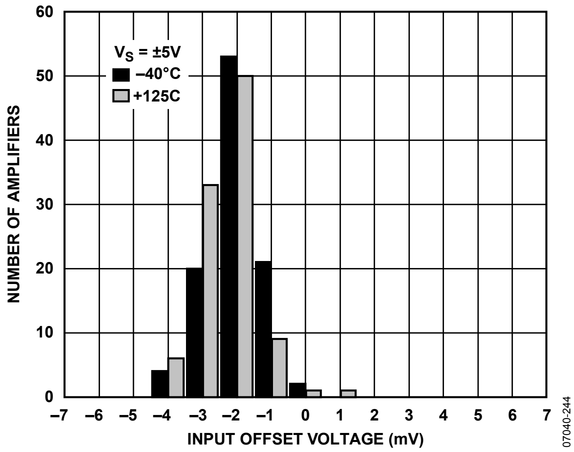


Figure 44. Input Offset Voltage Distribution over Temperature, $V_S = \pm 5$ V

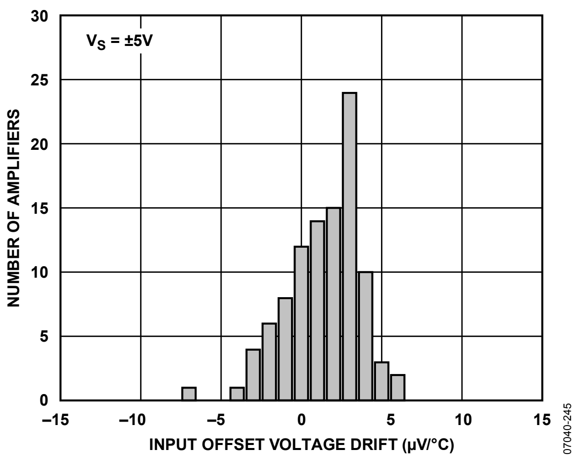


Figure 45. Input Offset Voltage Drift Distribution, $V_S = \pm 5$ V

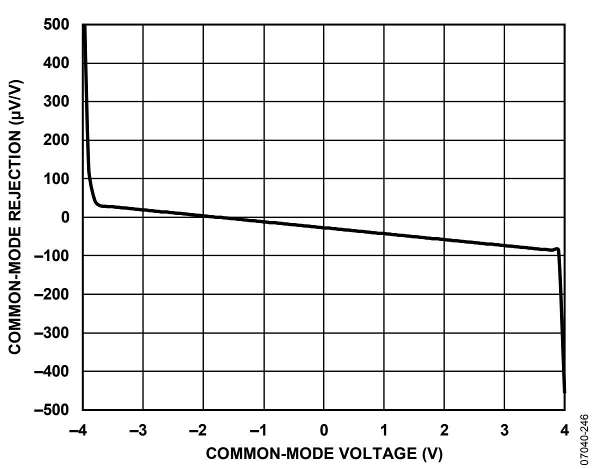


Figure 46. Common-Mode Rejection vs. Common-Mode Voltage

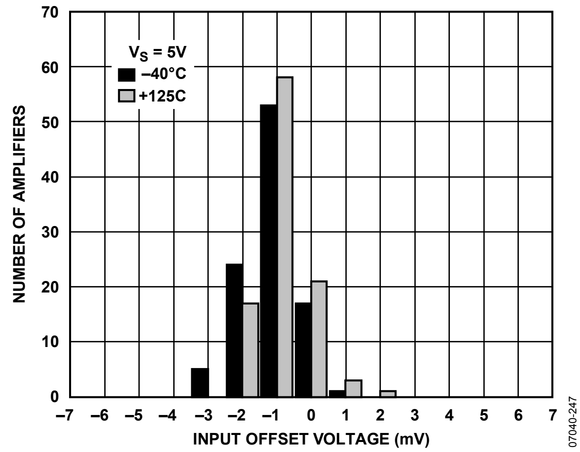


Figure 47. Input Offset Voltage Distribution over Temperature, $V_S = 5$ V

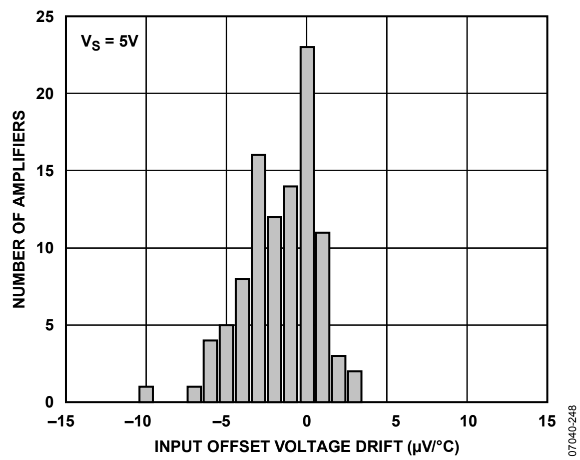


Figure 48. Input Offset Voltage Drift Distribution, $V_S = 5$ V

TEST CIRCUITS

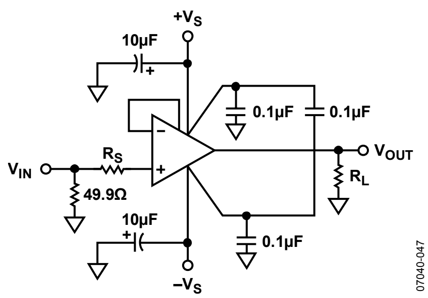


Figure 49. Noninverting Load Configuration

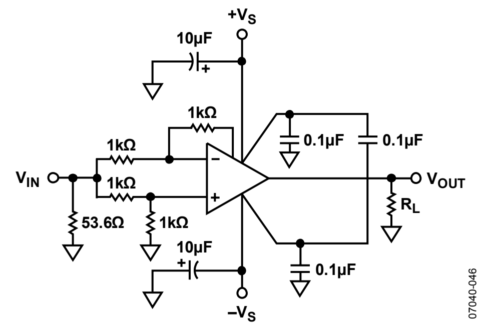


Figure 52. Common-Mode Rejection

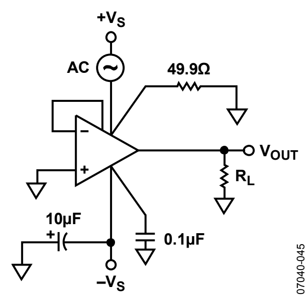


Figure 50. Positive Power Supply Rejection

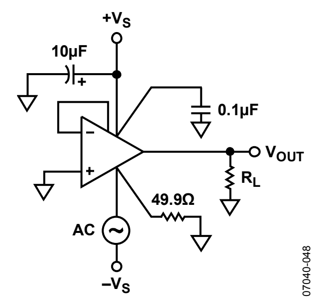


Figure 53. Negative Power Supply Rejection

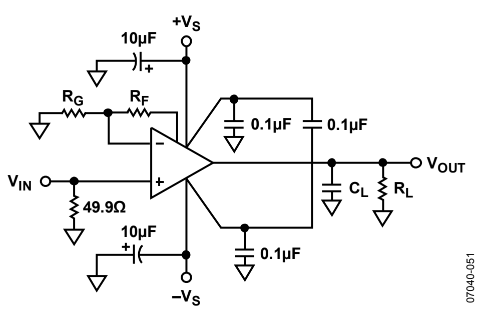


Figure 51. Typical Capacitive Load Configuration (LFCSP)

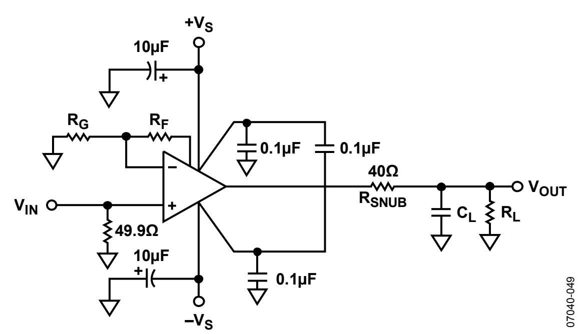


Figure 54. Typical Capacitive Load Configuration (SOIC)

APPLICATIONS INFORMATION

POWER-DOWN OPERATION

The PD pin powers down the chip, reducing the quiescent current and the overall power consumption. To enable the device, pull the PD pin low. Table 8 provides the PD pin voltages that enable the correct operation at different supplies. These voltages are applicable for ambient temperature only. Consult Table 1 and Table 2 when designing for use at the full operating temperature range.

Note that PD does not put the output in a high-Z state, which means that the ADA4857 must not be used as a multiplexer.

Table 8. PD Operation Table Guide

	Supply Voltage		
Condition	**±5 V**	**±2.5 V**	**+5 V**
Enabled	≤+0.8 V	≤−1.7 V	≤+0.8 V
Powered down	≥+3 V	≥+0.5 V	≥+3 V

CAPACITIVE LOAD CONSIDERATIONS

When driving a capacitive load using the SOIC package, R_{SNUB} reduces the peaking (see Figure 54). An optimum resistor value of 40 Ω is found to maintain the peaking within 1 dB for any capacitive load up to 40 pF.

RECOMMENDED VALUES FOR VARIOUS GAINS

Table 9 provides a useful reference for determining various gains and associated performance. R_F and R_G are kept low to minimize their contribution to the overall noise performance of the amplifier.

Table 9. Various Gain and Recommended Resistor Values Associated with Conditions; V_S = ±5 V, T_A = 25°C, R_L = 1 kΩ, R_T = 49.9 Ω

Gain	R_S (Ω) (CSP/SOIC)	R_F (Ω)	R_G (Ω)	−3 dB SS BW (MHz) (CSP/SOIC)	Slew Rate (V/µs), V_{OUT} = 2 V Step	ADA4857 Voltage Noise (nV/√Hz), RTO	Total System Noise (nV/√Hz), RTO
+1	0/100	0	N/A	850/750	2350	4.4	4.49
+2	0/0	499	499	360/320	1680	8.8	9.89
+5	0/0	499	124	90/89	516	22.11	23.49
+10	0/0	499	56.2	43/40	213	43.47	45.31

ACTIVE LOW-PASS FILTER (LPF)

Active filters are used in many applications such as antialiasing filters and high frequency communication IF strips. With a 410 MHz gain bandwidth product and high slew rate, the ADA4857-2 is an ideal candidate for active filters. Figure 55 shows the frequency response of 90 MHz and 45 MHz LPFs. In addition to the bandwidth requirements, the slew rate must be capable of supporting the full power bandwidth of the filter. In this case, a 90 MHz bandwidth with a 2 V p-p output swing requires at least 2800 V/μs.

The circuit shown in Figure 56 is a 4-pole, Sallen-Key LPF. The filter comprises two identical cascaded Sallen-Key LPF sections, each with a fixed gain of G = 2. The net gain of the filter is equal to G = 4 or 12 dB. The actual gain shown in Figure 55 is 12 dB. This does not take into account the output voltage being divided in half by the series matching termination resistor, R_T, and the load resistor.

Setting the resistors equal to each other greatly simplifies the design equations for the Sallen-Key filter. To achieve 90 MHz, the value of R must be set to 182 Ω. However, if the value of R is doubled, the corner frequency is cut in half to 45 MHz. This would be an easy way to tune the filter by simply multiplying the value of R (182 Ω) by the ratio of 90 MHz and the new corner frequency in megahertz.

Figure 55 shows the output of each stage is of the filter and the two different filters corresponding to R = 182 Ω and R = 365 Ω. Resistor values are kept low for minimal noise contribution, offset voltage, and optimal frequency response. Due to the low capacitance values used in the filter circuit, the PCB layout and minimization of parasitics is critical. A few picofarads can detune the corner frequency, f_c of the filter. The capacitor values shown in Figure 56 actually incorporate some stray PCB capacitance.

Capacitor selection is critical for optimal filter performance. Capacitors with low temperature coefficients, such as NPO ceramic capacitors and silver mica, are good choices for filter elements.

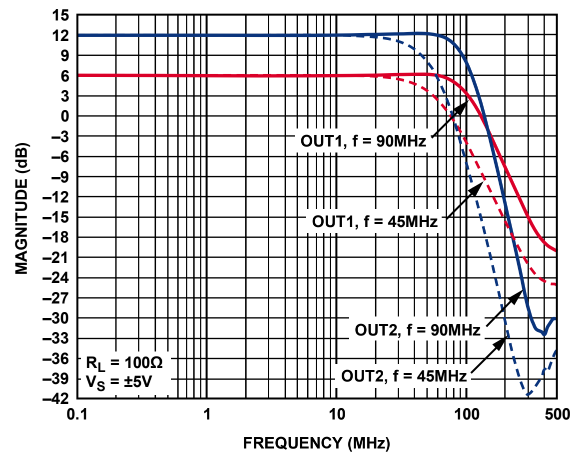


Figure 55. Low-Pass Filter Response

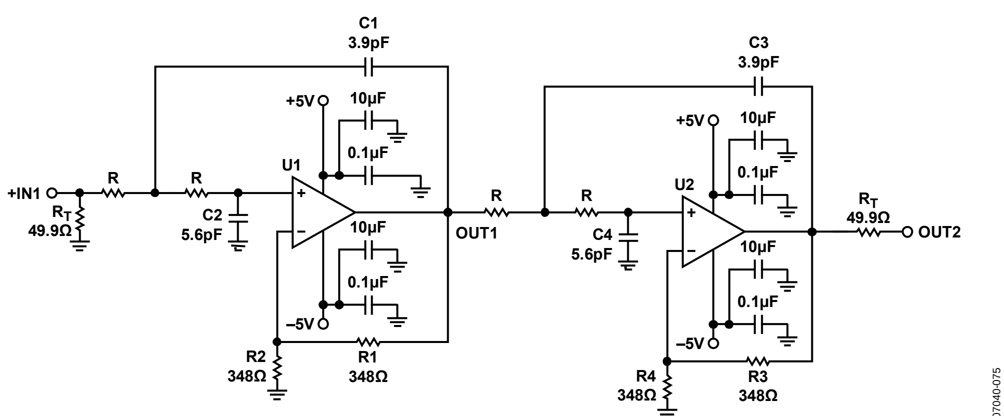


Figure 56. 4-Pole, Sallen-Key Low-Pass Filter (ADA4857-2)

NOISE

To analyze the noise performance of an amplifier circuit, identify the noise sources and determine if the source has a significant contribution to the overall noise performance of the amplifier. To simplify the noise calculations, noise spectral densities were used rather than actual voltages to leave bandwidth out of the expressions (noise spectral density, which is generally expressed in nV/√Hz, is equivalent to the noise in a 1 Hz bandwidth).

The noise model shown in Figure 57 has six individual noise sources: the Johnson noise of the three resistors, the operational amplifier voltage noise, and the current noise in each input of the amplifier. Each noise source has its own contribution to the noise at the output. Noise is generally referred to input (RTI), but it is often easier to calculate the noise referred to the output (RTO) and then divide by the noise gain to obtain the RTI noise.

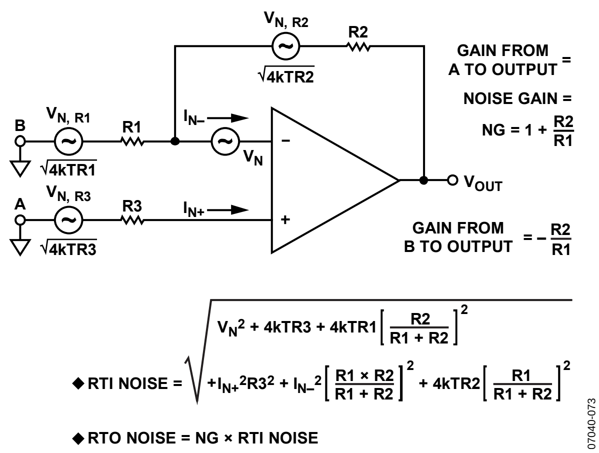


Figure 57. Operational Amplifier Noise Analysis Model

All resistors have Johnson noise that is calculated by

$$\sqrt{(4kBTR)}$$

where:
k is Boltzmann's Constant (1.38×10^{-23} J/K).
B is the bandwidth in Hertz.
T is the absolute temperature in Kelvin.
R is the resistance in ohms.

A simple relationship that is easy to remember is that a 50 Ω resistor generates a Johnson noise of 1 nV/√Hz at 25°C.

In applications where noise sensitivity is critical, care must be taken not to introduce other significant noise sources to the amplifier. Each resistor is a noise source. Attention to the following areas is critical to maintain low noise performance: design, layout, and component selection. A summary of noise performance for the amplifier and associated resistors can be seen in Table 9.

CIRCUIT CONSIDERATIONS

Careful and deliberate attention to detail when laying out the ADA4857 board yields optimal performance. Power supply bypassing, parasitic capacitance, and component selection all contribute to the overall performance of the amplifier.

PCB LAYOUT

Because the ADA4857 can operate up to 850 MHz, it is essential that RF board layout techniques be employed. All ground and power planes under the pins of the ADA4857 must be cleared of copper to prevent the formation of parasitic capacitance between the input pins to ground and the output pins to ground. A single mounting pad on the SOIC footprint can add as much as 0.2 pF of capacitance to ground if the ground plane is not cleared from under the mounting pads. The low distortion pinout of the ADA4857 increases the separation distance between the inputs and the supply pins, which improves the second harmonics. In addition, the feedback pin reduces the distance between the output and the inverting input of the amplifier, which helps minimize the parasitic inductance and capacitance of the feedback path, reducing ringing and peaking.

POWER SUPPLY BYPASSING

Power supply bypassing for the ADA4857 was optimized for frequency response and distortion performance. Figure 49 shows the recommended values and location of the bypass capacitors. The 0.1 µF bypassing capacitors must be placed as close as possible to the supply pins. Power supply bypassing is critical for stability, frequency response, distortion, and PSR performance. The capacitor between the two supplies helps improve PSR and distortion performance. The 10 µF electrolytic capacitors must be close to the 0.1 µF capacitors; however, it is not as critical. In some cases, additional paralleled capacitors can help improve frequency and transient response.

GROUNDING

Ground and power planes must be used where possible. Ground and power planes reduce the resistance and inductance of the power planes and ground returns. The returns for the input, output terminations, bypass capacitors, and R_G must all be kept as close to the ADA4857 as possible. The output load ground and the bypass capacitor grounds must be returned to the same point on the ground plane to minimize parasitic trace inductance, ringing, and overshoot and to improve distortion performance. The ADA4857 LFSCP packages feature an exposed paddle. For optimum electrical and thermal performance, solder this paddle to the ground plane or the power plane. For more information on high speed circuit design, see *A Practical Guide to High-Speed Printed-Circuit-Board Layout* at www.analog.com.

OUTLINE DIMENSIONS

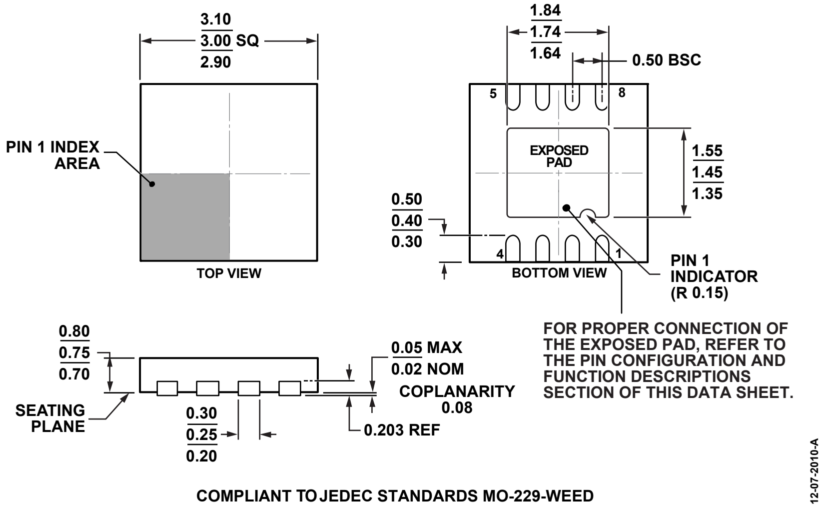


Figure 58. 8-Lead Lead Frame Chip Scale Package [LFCSP]
3 mm × 3 mm Body and 0.75 mm Package Height (CP-8-13)
Dimensions shown in millimeters

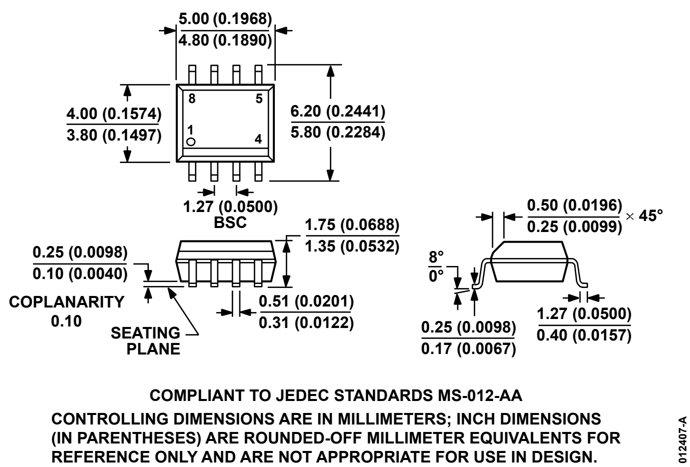


Figure 59. 8-Lead Standard Small Outline Package [SOIC_N]
(R-8)
Dimensions shown in millimeters and (inches)

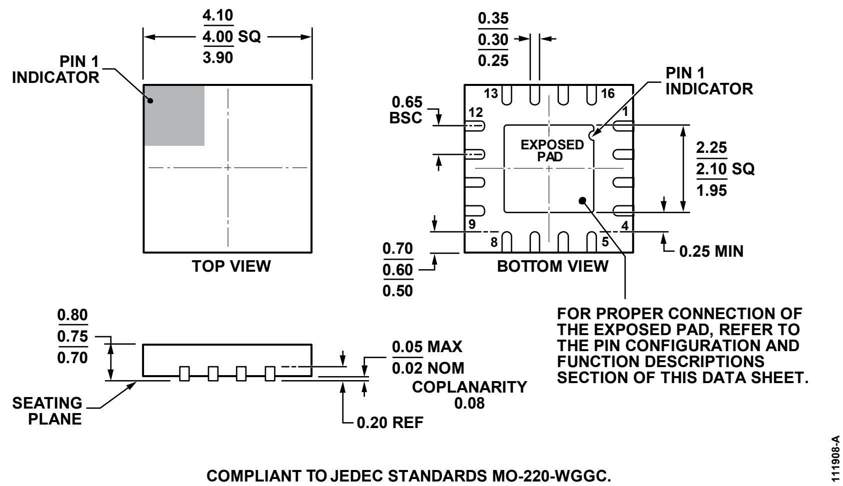


Figure 60. 16-Lead Lead Frame Chip Scale Package [LFCSP]
4 mm × 4 mm Body and 0.75 mm Package Height
(CP-16-23)
Dimensions shown in millimeters

ORDERING GUIDE

Model[1]	Temperature Range	Package Description	Package Option	Ordering Quantity	Branding
ADA4857-1YCPZ-R2	–40°C to +125°C	8-Lead LFCSP	CP-8-13	250	H15
ADA4857-1YCPZ-RL	–40°C to +125°C	8-Lead LFCSP	CP-8-13	5,000	H15
ADA4857-1YCPZ-R7	–40°C to +125°C	8-Lead LFCSP	CP-8-13	1,500	H15
ADA4857-1YRZ	–40°C to +125°C	8-Lead SOIC_N	R-8	98	
ADA4857-1YRZ-R7	–40°C to +125°C	8-Lead SOIC_N	R-8	2,500	
ADA4857-2YCPZ-R2	–40°C to +125°C	16-Lead LFCSP	CP-16-23	250	
ADA4857-2YCPZ-RL	–40°C to +125°C	16-Lead LFCSP	CP-16-23	5,000	
ADA4857-2YCPZ-R7	–40°C to +125°C	16-Lead LFCSP	CP-16-23	1,500	
ADA4857-2YCP-EBZ		Evaluation Board			

[1] Z = RoHS Compliant Part.