12-Bit, 80 MSPS/105 MSPS ADC

AD9432

FEATURES

On-chip reference and track-and-hold
On-chip input buffer
Power dissipation: 850 mW typical at 105 MSPS
500 MHz analog bandwidth
SNR: 67 dB @ 49 MHz AIN at 105 MSPS
SFDR: 80 dB @ 49 MHz AIN at 105 MSPS
2.0 V p-p analog input range
5.0 V supply operation
3.3 V CMOS/TTL outputs
Twos complement output format

APPLICATIONS

Communications
Base stations and zero-IF subsystems
Wireless local loop (WLL)
Local multipoint distribution service (LMDS)
HDTV broadcast cameras and film scanners

GENERAL INTRODUCTION

The AD9432 is a 12-bit, monolithic sampling analog-to-digital converter (ADC) with an on-chip track-and-hold circuit and is optimized for high speed conversion and ease of use. The product operates up to a 105 MSPS conversion rate with outstanding dynamic performance over its full operating range.

The ADC requires only a single 5.0 V power supply and a 105 MHz encode clock for full performance operation. No external reference or driver components are required for many applications. The digital outputs are TTL-/CMOS-compatible, and a separate output power supply pin supports interfacing with 3.3 V logic. The encode input supports either differential or single-ended mode and is TTL-/CMOS-compatible.

Fabricated on an advanced BiCMOS process, the AD9432 is available in a 52-lead low profile quad flat package (LQFP) and in a 52-lead thin quad flat package (TQFP_EP). The AD9432 is specified over the industrial temperature range of −40°C to +85°C.

FUNCTIONAL BLOCK DIAGRAM

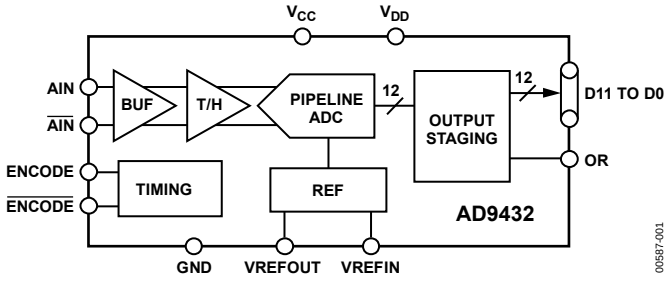

Figure 1.

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SPECIFICATIONS

V_{DD} = 3.3 V, V_{CC} = 5.0 V; external reference; differential encode input, unless otherwise noted.

Table 1.

Parameter	Temp	Test Level	80 MSPS Min	80 MSPS Typ	80 MSPS Max	105 MSPS Min	105 MSPS Typ	105 MSPS Max	Unit
RESOLUTION				12			12		Bits
DC ACCURACY									
Differential Nonlinearity (DNL)	25°C	I	−0.75	±0.25	+0.75	−0.75	±0.25	+0.75	LSB
	Full	VI	−1.0	±0.5	+1.0	−1.0	±0.5	+1.0	LSB
Integral Nonlinearity (INL)	25°C	I	−1.0	±0.5	+1.0	−1.0	±0.5	+1.0	LSB
	Full	VI	−1.5	±1.0	+1.5	−1.5	±1.0	+1.5	LSB
No Missing Codes	Full	VI		Guaranteed			Guaranteed		
Gain Error[1]	25°C	I	−5	+2	+7	−5	+2	+7	% FS
Gain Tempco[1]	Full	V		150			150		ppm/°C
ANALOG INPUTS (AIN, $\overline{AIN}$)									
Input Voltage Range	Full	V		2			2		V p-p
Common-Mode Voltage	Full	V		3.0			3.0		V
Input Offset Voltage	Full	VI	−5	±0	+5	−5	±0	+5	mV
Input Resistance	Full	VI	2	3	4	2	3	4	kΩ
Input Capacitance	25°C	V		4			4		pF
Analog Bandwidth, Full Power	25°C	V		500			500		MHz
ANALOG REFERENCE									
Output Voltage	Full	VI	2.4	2.5	2.6	2.4	2.5	2.6	V
Tempco	Full	V		50			50		ppm/°C
Input Bias Current	Full	VI		15	50		15	50	µA
SWITCHING PERFORMANCE									
Maximum Conversion Rate	Full	VI	80			105			MSPS
Minimum Conversion Rate	Full	IV			1			1	MSPS
Encode Pulse Width High (t_{EH})	25°C	IV	4.0	6.2		4.0	4.8		ns
Encode Pulse Width Low (t_{EL})	25°C	IV	4.0	6.2		4.0	4.8		ns
Aperture Delay (t_A)	25°C	V		2.0			2.0		ns
Aperture Uncertainty (Jitter)	25°C	V		0.25			0.25		ps rms
Output Valid Time (t_V)[2]	Full	VI	3.0	5.3		3.0	5.3		ns
Output Propagation Delay (t_{PD})[2]	Full	VI		5.5	8.0		5.5	8.0	ns
Output Rise Time (t_R)[2]	Full	V		2.1			2.1		ns
Output Fall Time (t_F)[2]	Full	V		1.9			1.9		ns
Out-of-Range Recovery Time	25°C	V		2			2		ns
Transient Response Time	25°C	V		2			2		ns
Latency	Full	IV		10			10		Cycles
DIGITAL INPUTS									
Encode Input Common Mode	Full	V		1.6			1.6		V
Differential Input (ENCODE, $\overline{ENCODE}$)	Full	V		750			750		mV
Single-Ended Input									
Logic 1 Voltage	Full	IV	2.0			2.0			V
Logic 0 Voltage	Full	IV			0.8			0.8	V
Input Resistance	Full	VI	3	5	8	3	5	8	kΩ
Input Capacitance	25°C	V		4.5			4.5		pF
DIGITAL OUTPUTS									
Logic 1 Voltage (V_{DD} = 3.3 V)	Full	VI	V_{DD} − 0.05			V_{DD} − 0.05			V
Logic 0 Voltage (V_{DD} = 3.3 V)	Full	VI			0.05			0.05	V
Output Coding				Twos complement			Twos complement		

Parameter	Temp	Test Level	80 MSPS Min	80 MSPS Typ	80 MSPS Max	105 MSPS Min	105 MSPS Typ	105 MSPS Max	Unit
POWER SUPPLY									
Power Dissipation[3]	Full	VI		790	1000		850	1100	mW
I_{VCC}	Full	VI		158	200		170	220	mA
I_{VDD}	Full	VI		9.5	12.2		12.5	16	mA
Power Supply Rejection Ratio (PSRR)	25°C	I	−5	+0.5	+5	−5	+0.5	+5	mV/V
DYNAMIC PERFORMANCE[4]									
Signal-to-Noise Ratio (SNR) (Without Harmonics)									
f_{IN} = 10 MHz	25°C	I	65.5	67.5		65.5	67.5		dB
f_{IN} = 40 MHz	25°C	I	65	67.2			67.2		dB
f_{IN} = 49 MHz	25°C	I		67.0		64	67.0		dB
f_{IN} = 70 MHz	25°C	V		66.1			66.1		dB
Signal-to-Noise and Distortion (SINAD) Ratio (with Harmonics)									
f_{IN} = 10 MHz	25°C	I	65	67.2		65	67.2		dB
f_{IN} = 40 MHz	25°C	I	64.5	66.9			66.9		dB
f_{IN} = 49 MHz	25°C	I		66.7		63	66.7		dB
f_{IN} = 70 MHz	25°C	V		65.8			65.8		dB
Effective Number of Bits (ENOB)									
f_{IN} = 10 MHz	25°C	V		11.0			11.0		Bits
f_{IN} = 40 MHz	25°C	V		10.9			10.9		Bits
f_{IN} = 49 MHz	25°C	V		10.9			10.9		Bits
f_{IN} = 70 MHz	25°C	V		10.7			10.7		Bits
Second-Order and Third-Order Harmonic Distortion									
f_{IN} = 10 MHz	25°C	I	−75	−85		−75	−85		dBc
f_{IN} = 40 MHz	25°C	I	−73	−85			−83		dBc
f_{IN} = 49 MHz	25°C	I		−83		−72	−80		dBc
f_{IN} = 70 MHz	25°C	V		−80			−78		dBc
Worst Other Harmonic or Spur (Excluding Second-Order and Third-Order Harmonics)									
f_{IN} = 10 MHz	25°C	I	−80	−90		−80	−90		dBc
f_{IN} = 40 MHz	25°C	I	−80	−90			−90		dBc
f_{IN} = 49 MHz	25°C	I		−90		−80	−90		dBc
f_{IN} = 70 MHz	25°C	V		−90			−90		dBc
Two-Tone Intermodulation Distortion (IMD)									
f_{IN1} = 29.3 MHz; f_{IN2} = 30.3 MHz	25°C	V		−75			−75		dBc
f_{IN1} = 70.3 MHz; f_{IN2} = 71.3 MHz	25°C	V		−66			−66		dBc

[1] Gain error and gain temperature coefficients are based on the ADC only (with a fixed 2.5 V external reference and a 2 V p-p differential analog input).
[2] t_V and t_{PD} are measured from the transition points of the ENCODE input to the 50%/50% levels of the digital output swing. The digital output load during testing is not to exceed an ac load of 10 pF or a dc current of ±40 µA. Rise and fall times are measured from 10% to 90%.
[3] Power dissipation measured with encode at rated speed and a dc analog input (outputs static, I_{VDD} = 0).
[4] SNR/harmonics based on an analog input voltage of –0.5 dBFS referenced to a 2 V full-scale input range.

TIMING DIAGRAM

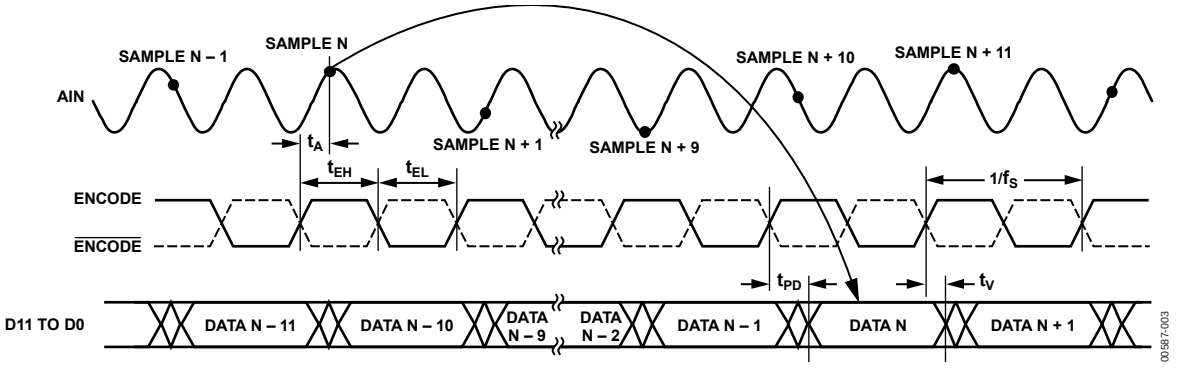


Figure 2. Timing Diagram

ABSOLUTE MAXIMUM RATINGS

Table 2.

Parameter	Rating
V_{DD}	6 V
V_{CC}	6 V
Analog Inputs	−0.5 V to V_{CC} + 0.5 V
Digital Inputs	−0.5 V to V_{DD} + 0.5 V
VREFIN	−0.5 V to V_{CC} + 0.5 V
Digital Output Current	20 mA
Operating Temperature Range	−55°C to +125°C
Storage Temperature Range	−65°C to +150°C
Maximum Junction Temperature	150°C
Maximum Case Temperature	150°C

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

EXPLANATION OF TEST LEVELS

I 100% production tested.
II 100% production tested at 25°C and sample tested at specified temperatures.
III Sample tested only.
IV Parameter is guaranteed by design and characterization testing.
V Parameter is a typical value only.
VI 100% production tested at 25°C; guaranteed by design and characterization testing for industrial temperature range.

THERMAL CHARACTERISTICS

Table 3 lists AD9432 thermal characteristics for simulated typical performance in a 4-layer JEDEC board, horizontal orientation.

Table 3. Thermal Resistance

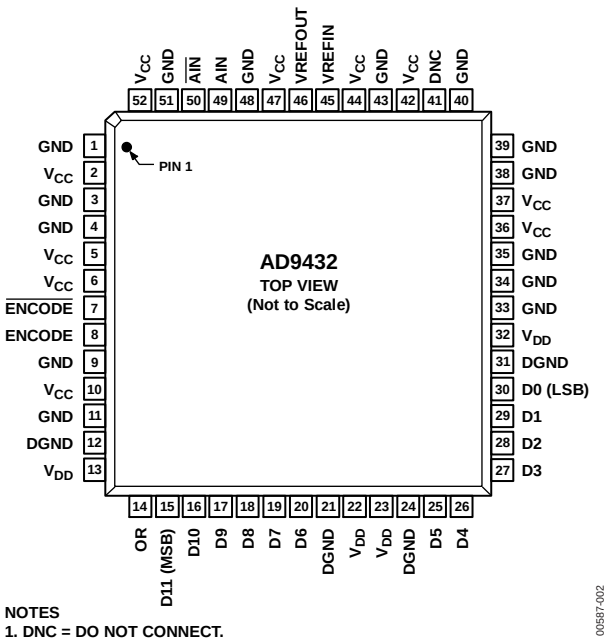
Package Type	θ_{JA}	θ_{JMA}	θ_{JC}	Unit
52-Lead LQFP (ST-52)				
No Airflow	50			°C/W
52-Lead TQFP_EP (SV-52-2)[1]			2	°C/W
No Airflow	19.3			°C/W
1.0 m/s Airflow		16		°C/W

[1] Bottom of package (soldered exposed pad).

ESD CAUTION

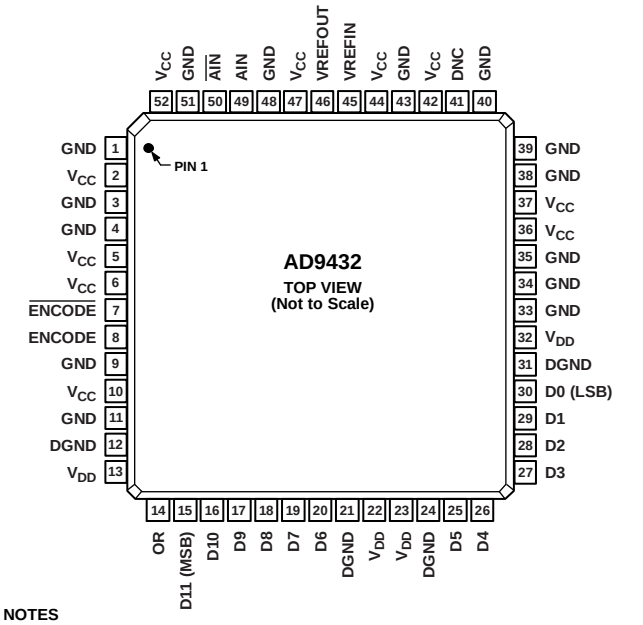
ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATIONS AND FUNCTION DESCRIPTIONS



NOTES
1. DNC = DO NOT CONNECT.

Figure 3. Pin Configuration, LQFP



NOTES
1. ALTHOUGH NOT REQUIRED IN ALL APPLICATIONS, THE EXPOSED PADDLE ON THE UNDERSIDE OF THE PACKAGE SHOULD BE SOLDERED TO THE GROUND PLANE. SOLDERING THE EXPOSED PADDLE TO THE PCB INCREASES THE RELIABILITY OF THE SOLDER JOINTS, MAXIMIZING THE THERMAL CAPABILITY OF THE PACKAGE.

Figure 4. Pin Configuration, TQFP_EP

Table 4. Pin Function Descriptions

Pin No.	Mnemonic	Description
1, 3, 4, 9, 11, 33, 34, 35, 38, 39, 40, 43, 48, 51	GND	Analog Ground.
2, 5, 6, 10, 36, 37, 42, 44, 47, 52	V_{CC}	Analog Supply (5 V).
7	$\overline{\text{ENCODE}}$	Encode Clock for ADC, Complementary.
8	ENCODE	Encode Clock for ADC, True. ADC samples on rising edge of ENCODE.
12, 21, 24, 31	DGND	Digital Output Ground.
13, 22, 23, 32	V_{DD}	Digital Output Power Supply (2.7 V to 3.6 V).
14	OR	Out-of-Range Output.
15 to 20, 25 to 30	D11 to D6, D5 to D0	Digital Output.
41	DNC	Do Not Connect.
45	VREFIN	Reference Input for ADC (2.5 V Typical). Bypass with 0.1 µF capacitor to ground.
46	VREFOUT	Internal Reference Output (2.5 V Typical).
49	AIN	Analog Input, True.
50	$\overline{\text{AIN}}$	Analog Input, Complementary.
	Exposed Pad (TQFP_EP)	Although not required in all applications, the exposed paddle on the underside of the TQFP_EP package should be soldered to the ground plane. Soldering the exposed paddle to the PCB increases the reliability of the solder joints, maximizing the thermal capability of the package.

TYPICAL PERFORMANCE CHARACTERISTICS

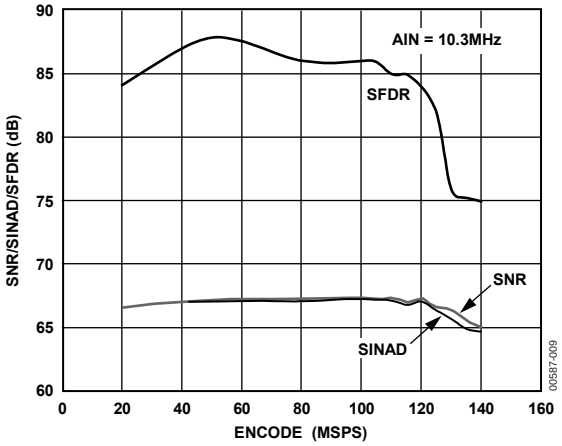


Figure 5. SNR/SINAD/SFDR vs. f_S, f_{IN} = 10.3 MHz

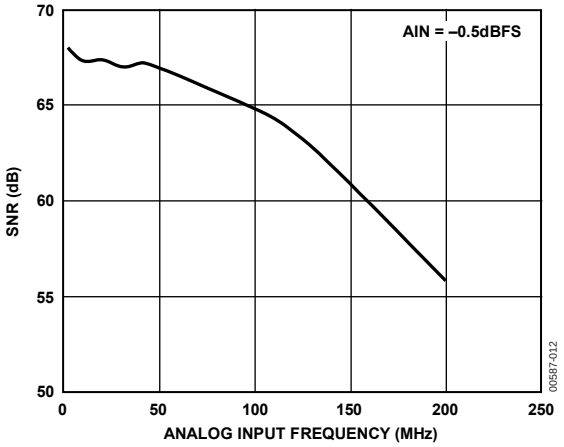


Figure 8. SNR vs. f_{IN}, Encode = 105 MSPS

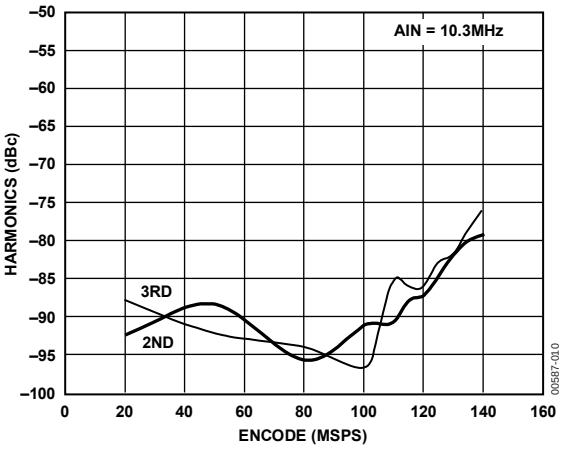


Figure 6. Second-Order and Third-Order Harmonics vs. f_S, f_{IN} = 10.3 MHz

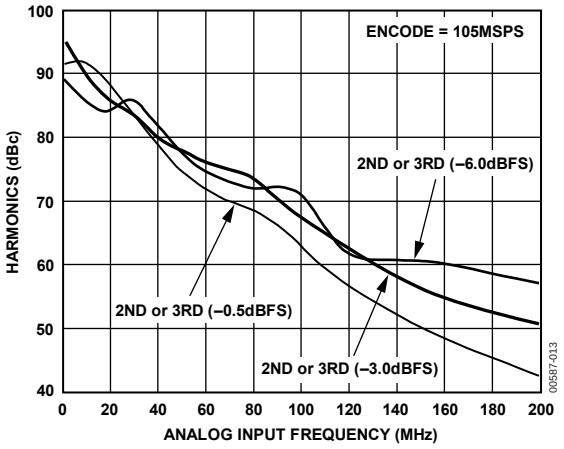


Figure 9. Second-Order and Third-Order Harmonics vs. f_{IN}, f_S = 105 MSPS

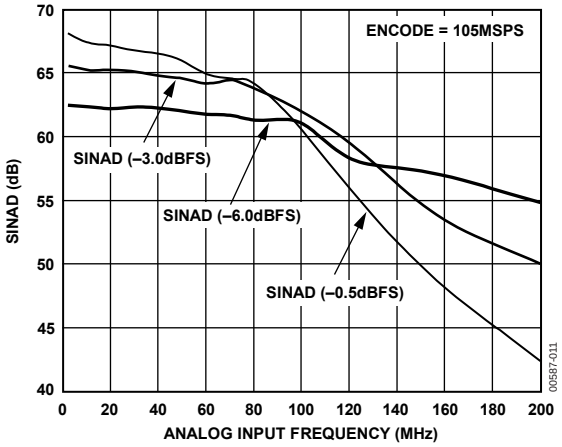


Figure 7. SINAD vs. f_{IN}, f_S = 105 MSPS

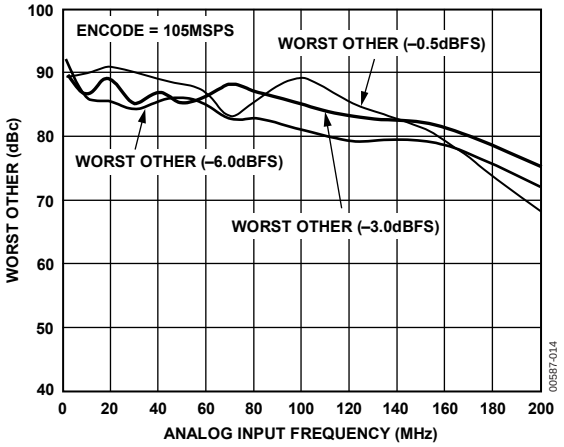


Figure 10. Worst Other (Excluding Second-Order and Third-Order Harmonics) vs. f_{IN}, f_S = 105 MSPS

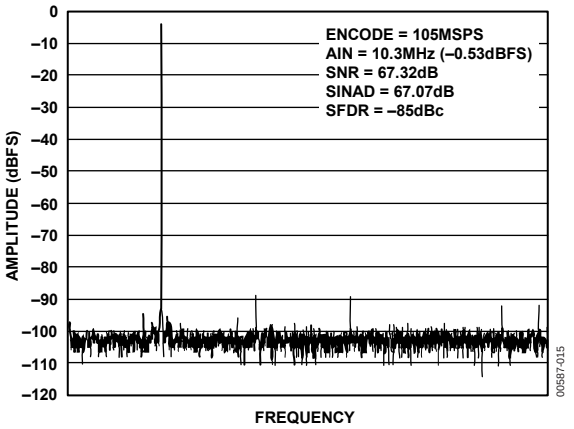


Figure 11. FFT: f_S = 105 MSPS, f_{IN} = 10.3 MHz

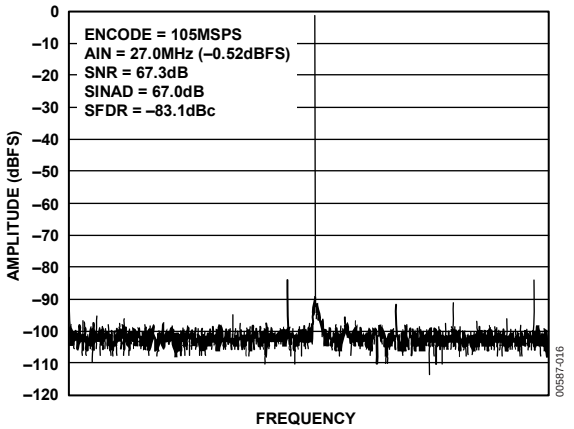


Figure 12. FFT: f_S = 105 MSPS, f_{IN} = 27 MHz

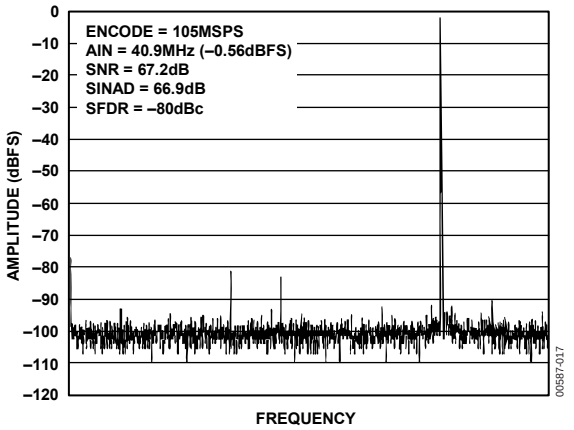


Figure 13. FFT: f_S = 105 MSPS, f_{IN} = 40.9 MHz

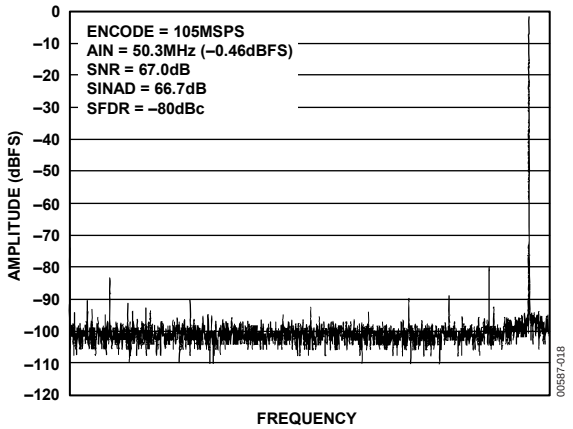


Figure 14. FFT: f_S = 105 MSPS, f_{IN} = 50.3 MHz

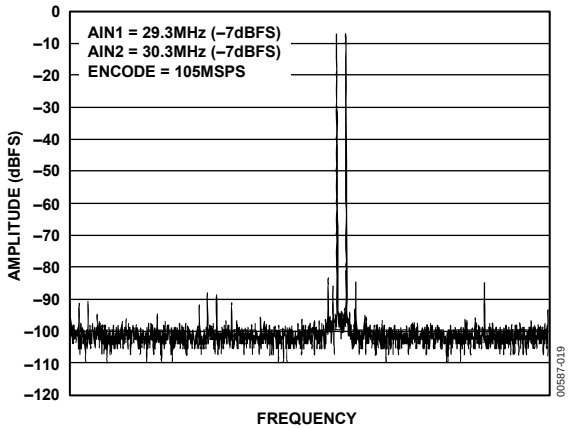


Figure 15. Two-Tone FFT, Wideband: f_S = 105 MSPS, AIN1 = 29.3 MHz, AIN2 = 30.3 MHz

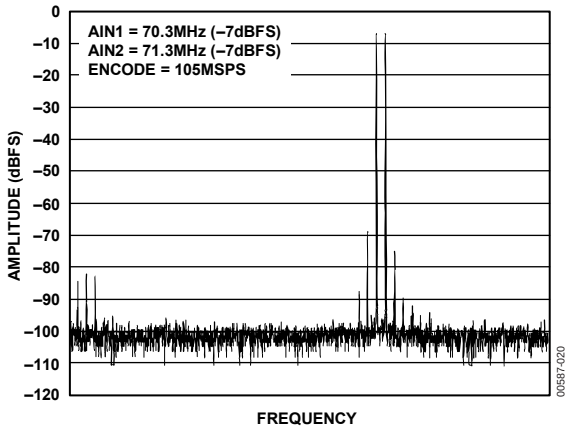


Figure 16. Two-Tone FFT, Wideband: f_S = 105 MSPS, AIN1 = 70.3 MHz, AIN2 = 71.3 MHz

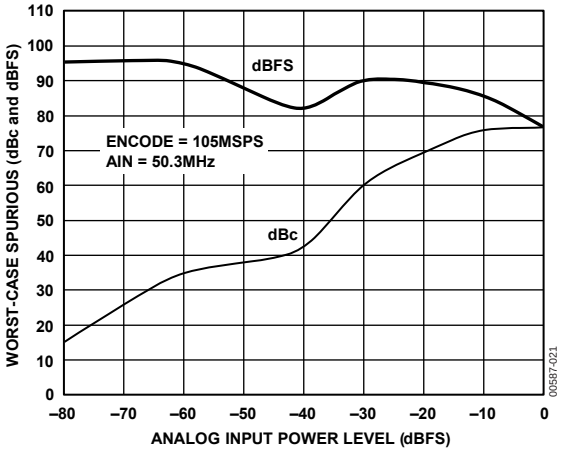


Figure 17. Single-Tone SFDR, f_S = 105 MSPS, f_{IN} = 50.3 MHz

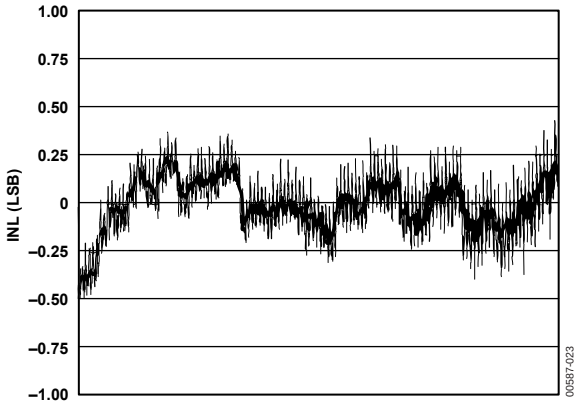


Figure 19. Integral Nonlinearity, f_S = 105 MSPS

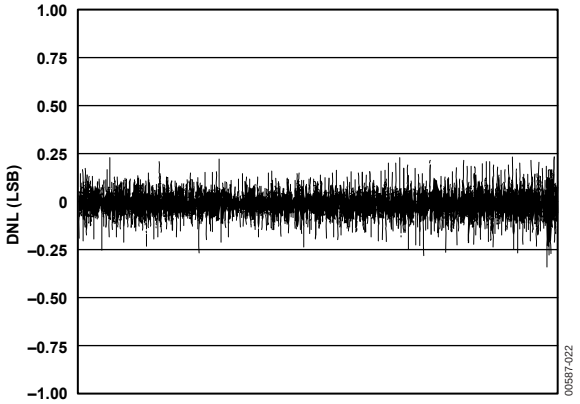


Figure 18. Differential Nonlinearity, f_S = 105 MSPS

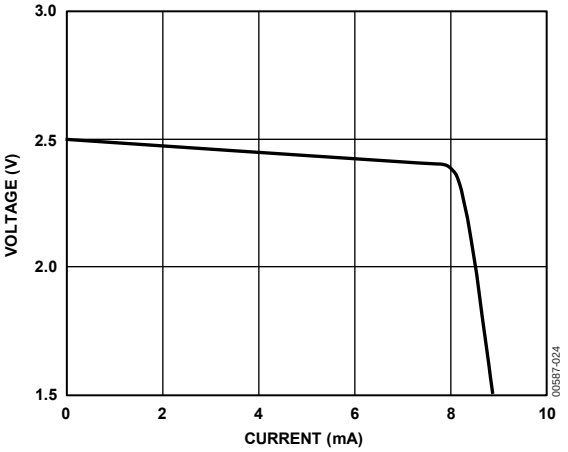


Figure 20. Voltage Reference Output vs. Current Load

TERMINOLOGY

Analog Bandwidth
The analog input frequency at which the spectral power of the fundamental frequency (as determined by the FFT analysis) is reduced by 3 dB.

Aperture Delay
The delay between a differential crossing of ENCODE and ENCODE and the instant at which the analog input is sampled.

Aperture Uncertainty (Jitter)
The sample-to-sample variation in aperture delay.

Differential Nonlinearity (DNL)
The deviation of any code from an ideal 1 LSB step.

Effective Number of Bits (ENOB)
The effective number of bits (ENOB) is calculated from the measured SNR based on the following equation:

$$ENOB = \frac{SNR_{MEASURED} - 1.76\ \text{dB} + 20\ \log\left(\frac{Full-Scale\ Amplitude}{Input\ Amplitude}\right)}{6.02}$$

Encode Pulse Width/Duty Cycle
Pulse width high is the minimum amount of time that the encode pulse should be left in the Logic 1 state to achieve the rated performance. Pulse width low is the minimum amount of time that the encode pulse should be left in the Logic 0 state. At a given clock rate, these specifications define an acceptable encode duty cycle.

Harmonic Distortion
The ratio of the rms signal amplitude fundamental frequency to the rms signal amplitude of a single harmonic component (second, third, and so on); reported in dBc.

Integral Nonlinearity (INL)
The deviation of the transfer function from a reference line measured in fractions of 1 LSB using a "best straight line" determined by a least square curve fit.

Maximum Conversion Rate
The maximum encode rate at which parametric testing is performed.

Minimum Conversion Rate
The encode rate at which the SNR of the lowest analog signal frequency drops by no more than 3 dB below the guaranteed limit.

Output Propagation Delay
The delay between a differential crossing of ENCODE and ENCODE and the time when all output data bits are within valid logic levels.

Power Supply Rejection Ratio (PSRR)
The ratio of a change in input offset voltage to a change in power supply voltage.

Signal-to-Noise and Distortion (SINAD) Ratio
The ratio of the rms signal amplitude (set at 1 dB below full scale) to the rms value of the sum of all other spectral components, including harmonics but excluding dc.

Signal-to-Noise Ratio (SNR)
The ratio of the rms signal amplitude (set at 1 dB below full scale) to the rms value of the sum of all other spectral components, excluding the first five harmonics and dc.

Spurious-Free Dynamic Range (SFDR)
The ratio of the rms signal amplitude to the rms value of the peak spurious spectral component. The peak spurious component may or may not be a harmonic. May be reported in dBc (degrades as signal level is lowered) or in dBFS (always related back to converter full scale).

Two-Tone Intermodulation Distortion Rejection
The ratio of the rms value of either input tone (f_1, f_2) to the rms value of the worst third-order intermodulation product; reported in dBc. Products are located at $2f_1 - f_2$ and $2f_2 - f_1$.

Two-Tone SFDR
The ratio of the rms value of either input tone (f_1, f_2) to the rms value of the peak spurious component. The peak spurious component may or may not be an IMD product. May be reported in dBc (degrades as signal level is lowered) or in dBFS (always related back to converter full scale).

Worst Other Spur
The ratio of the rms signal amplitude to the rms value of the worst spurious component (excluding the second-order and third-order harmonic); reported in dBc.

EQUIVALENT CIRCUITS

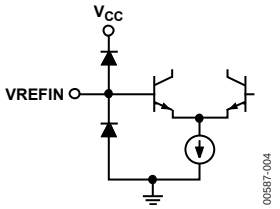


Figure 21. Voltage Reference Input Circuit

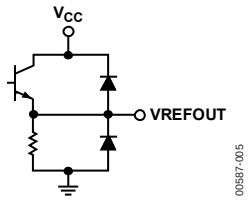


Figure 22. Voltage Reference Output Circuit

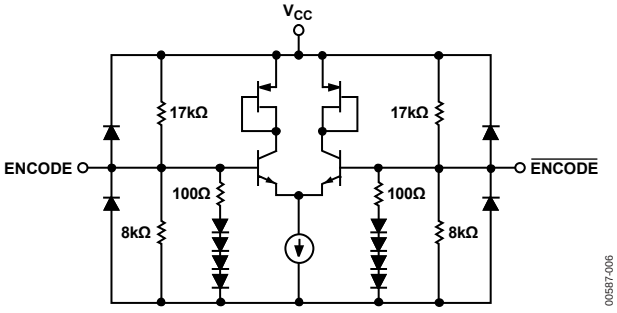


Figure 23. Encode Input Circuit

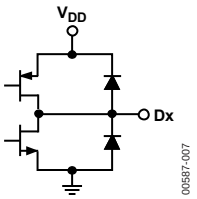


Figure 24. Digital Output Circuit

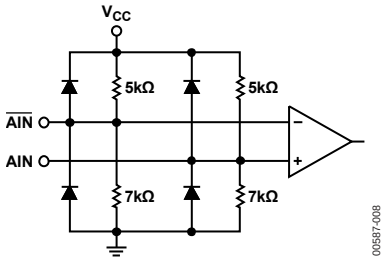


Figure 25. Analog Input Circuit

THEORY OF OPERATION

The AD9432 is a 12-bit pipeline converter that uses a switched-capacitor architecture. Optimized for high speed, this converter provides flat dynamic performance up to frequencies near Nyquist. DNL transitional errors are calibrated at final test to a typical accuracy of 0.25 LSB or less.

ANALOG INPUT

The analog input to the AD9432 is a differential buffer. The input buffer is self-biased by an on-chip resistor divider that sets the dc common-mode voltage to a nominal 3 V (see the Equivalent Circuits section). Rated performance is achieved by driving the input differentially. The minimum input offset voltage is obtained when driving from a source with a low differential source impedance, such as a transformer in ac applications. Capacitive coupling at the inputs increases the input offset voltage by as much as ±25 mV. Driving the ADC single-ended degrades performance. For best dynamic performance, impedances at AIN and $\overline{\text{AIN}}$ should match.

Special care was taken in the design of the analog input section of the AD9432 to prevent damage and corruption of data when the input is overdriven. The nominal input range is 2 V p-p. Each analog input is 1 V p-p when driven differentially.

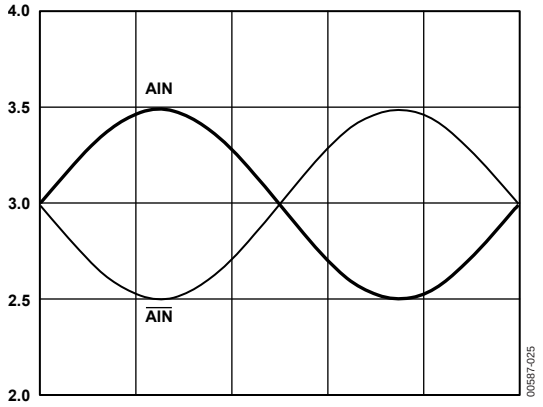


Figure 26. Full-Scale Analog Input Range

ENCODE INPUT

Any high speed ADC is extremely sensitive to the quality of the sampling clock provided by the user. A track-and-hold circuit is essentially a mixer, and any noise, distortion, or timing jitter on the clock is combined with the desired signal at the ADC output. For this reason, considerable care has been taken in the design of the encode input of the AD9432, and the user is advised to give commensurate thought to the clock source. The encode input supports differential or single-ended mode and is fully TTL-/CMOS-compatible.

Note that the encode inputs cannot be driven directly from PECL level signals (V_{IHD} is 3.5 V maximum). PECL level signals can easily be accommodated by ac coupling, as shown in Figure 27. Good performance is obtained using an MC10EL16 translator in the circuit to drive the encode inputs.

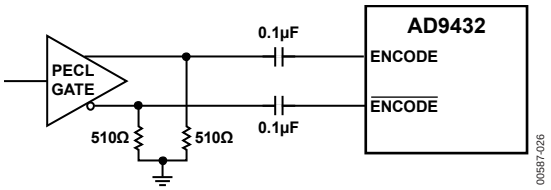


Figure 27. AC Coupling to Encode Inputs

ENCODE VOLTAGE LEVEL DEFINITION

The voltage level definitions for driving ENCODE and $\overline{\text{ENCODE}}$ in single-ended and differential mode are shown in Figure 28.

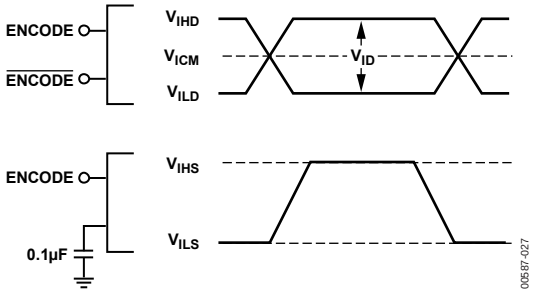


Figure 28. Differential and Single-Ended Input Levels

Table 5. Encode Inputs

Input	Min	Nominal	Max
Differential Signal Amplitude (V_{ID})	500 mV	750 mV	
High Differential Input Voltage (V_{IHD})			3.5 V
Low Differential Input Voltage (V_{ILD})	0 V		
Common-Mode Input (V_{ICM})	1.25 V	1.6 V	
High Single-Ended Voltage (V_{IHS})	2 V		3.5 V
Low Single-Ended Voltage (V_{ILS})	0 V		0.8 V

Often, the cleanest clock source is a crystal oscillator producing a pure sine wave. In this configuration, or with any roughly symmetrical clock input, the input can be ac-coupled and biased to a reference voltage that also provides the encode. This ensures that the reference voltage is centered on the encode signal.

DIGITAL OUTPUTS

The digital outputs are 3.3 V (2.7 V to 3.6 V) TTL-/CMOS-compatible for lower power consumption. The output data format is twos complement (see Table 6).

Table 6. Twos Complement Output Coding (V_{REF} = 2.5 V)

Code	AIN − $\overline{\text{AIN}}$ (V)	Digital Output
+2047	1.000	0111 1111 1111
…	…	…
0	0	0000 0000 0000
−1	−0.00049	1111 1111 1111
…	…	…
−2048	−1.000	1000 0000 0000

The out-of-range (OR) output is logic low for normal operation. During any clock cycle when the ADC output data (Dx) reaches positive or negative full scale (+2047 or −2048), the OR output goes high. The OR output is internally generated each clock cycle. It has the same pipeline latency and propagation delay as the ADC output data and remains high until the output data reflects an in-range condition. The ADC output bits (Dx) do not roll over and, therefore, remain at positive or negative full scale (+2047 or −2048) while the OR output is high.

VOLTAGE REFERENCE

A stable and accurate 2.5 V voltage reference is built into the AD9432 (VREFOUT). In normal operation, the internal reference is used by strapping Pin 45 to Pin 46 and placing a 0.1 µF decoupling capacitor at VREFIN.

The input range can be adjusted by varying the reference voltage applied to the AD9432. No appreciable degradation in performance occurs when the reference is adjusted ±5%. The full-scale range of the ADC tracks reference voltage changes linearly.

TIMING

The AD9432 provides latched data outputs, with 10 pipeline delays. Data outputs are included or available one propagation delay (t_{PD}) after the rising edge of the encode command (see Figure 2). The length of the output data lines and the loads placed on them should be minimized to reduce transients within the AD9432; these transients can detract from the dynamic performance of the converter.

The minimum guaranteed conversion rate of the AD9432 is 1 MSPS. At internal clock rates below 1 MSPS, dynamic performance may degrade. Therefore, input clock rates below 1 MHz should be avoided.

During initial power-up, or whenever the clock to the AD9432 is interrupted, the output data will not be accurate for 200 ns or 10 clock cycles, whichever is longer.

APPLICATIONS INFORMATION

USING THE AD8138 TO DRIVE THE AD9432

The AD8138 differential output op amp can be used to drive the AD9432 in dc-coupled applications. The AD8138 was specifically designed for ADC driver applications. Superior SNR performance is maintained up to analog frequencies of 30 MHz. The AD8138 op amp provides single-ended-to-differential conversion, which allows for a low cost alternative to transformer coupling for ac applications, as well.

The circuit in Figure 29 was breadboarded, and the measured performance is shown in Figure 30 and Figure 31. These figures are for ±5 V supplies at the AD8138; with a single 5 V supply at the AD8138, performance dropped by about 1 dB to 2 dB.

Figure 30 shows SNR and SINAD for a −1 dBFS analog input frequency varied from 2 MHz to 40 MHz with an encode rate of 105 MSPS. The measurements are for nominal conditions at room temperature. Figure 31 shows the second-order and third-order harmonic distortion performance under the same conditions.

The dc common-mode voltage for the AD8138 outputs can be adjusted via the V_{OCM} input to provide the 3 V common-mode voltage that the AD9432 inputs require.

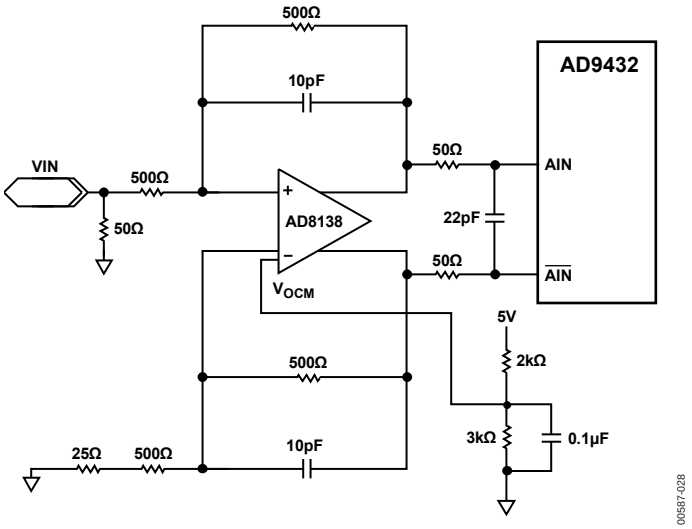


Figure 29. AD8138/AD9432 Schematic

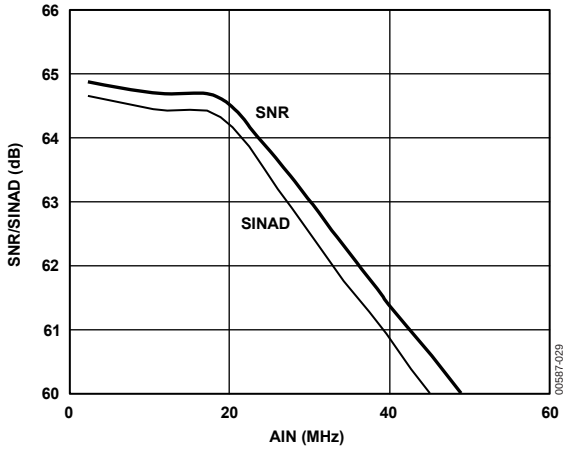


Figure 30. Measured SNR and SINAD (Encode = 105 MSPS)

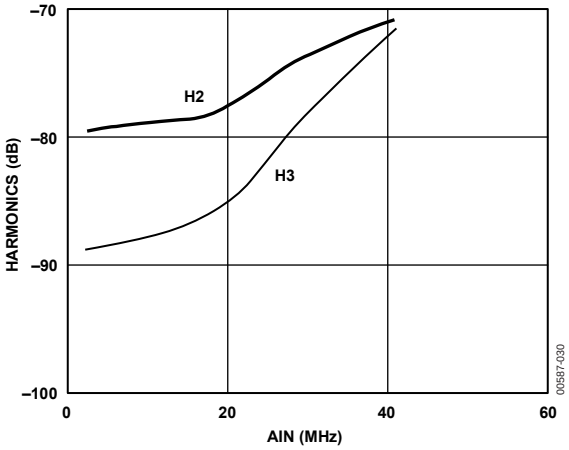
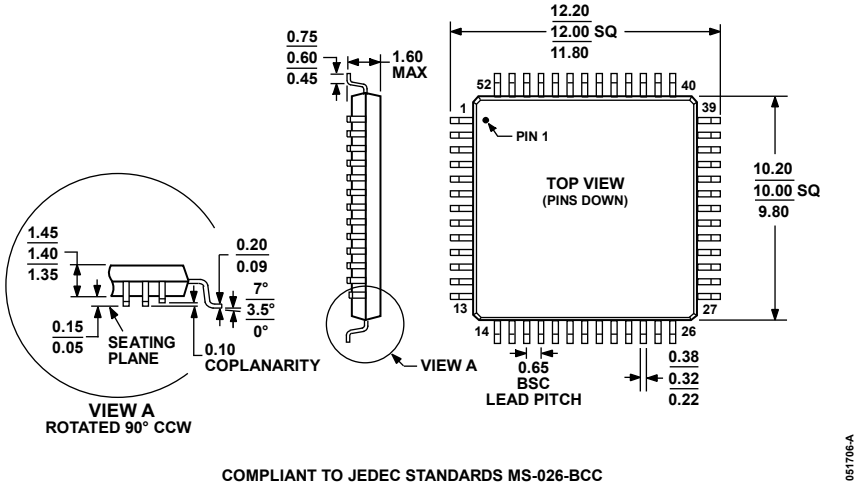


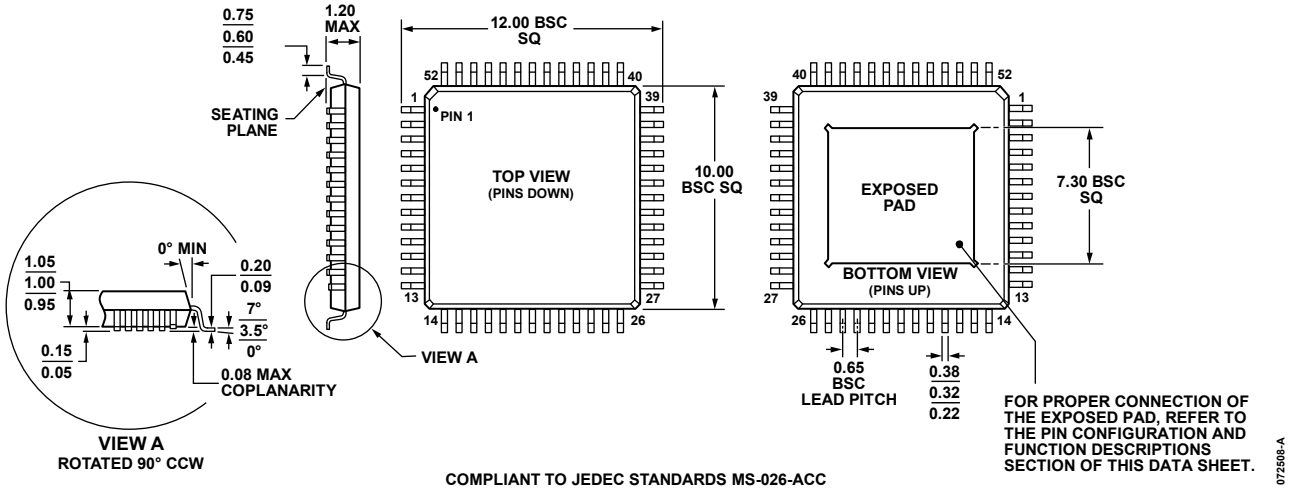
Figure 31. Measured Second-Order and Third-Order Harmonic Distortion (Encode = 105 MSPS)

OUTLINE DIMENSIONS



COMPLIANT TO JEDEC STANDARDS MS-026-BCC

Figure 32. 52-Lead Low Profile Quad Flat Package [LQFP]
(ST-52)
Dimensions shown in millimeters



COMPLIANT TO JEDEC STANDARDS MS-026-ACC

Figure 33. 52-Lead Thin Quad Flat Package, Exposed Pad [TQFP_EP]
(SV-52-2)
Dimensions shown in millimeters

ORDERING GUIDE

Model	Temperature Range	Package Description	Package Option
AD9432BSTZ-80[1]	–40°C to +85°C	52-Lead Low Profile Quad Flat Package [LQFP]	ST-52
AD9432BSTZ-105[1]	–40°C to +85°C	52-Lead Low Profile Quad Flat Package [LQFP]	ST-52
AD9432BSVZ-80[1]	–40°C to +85°C	52-Lead Thin Quad Flat Package, Exposed Pad [TQFP_EP]	SV-52-2
AD9432BSVZ-105[1]	–40°C to +85°C	52-Lead Thin Quad Flat Package, Exposed Pad [TQFP_EP]	SV-52-2

[1] Z = RoHS Compliant Part.

D00587-0-6/09(F)

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AD9432BSTZ-80 AD9432BSVZ-80 AD9432BSVZ-105 AD9432BSTZ-105