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REVISION HISTORY**4/2022—Rev. D to Rev. E**

Updated Format (Universal).....	1
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SPECIFICATIONS

DC SPECIFICATIONS

$AV_{DD} = 3\text{ V}$, $DrV_{DD} = 3\text{ V}$; $T_{MIN} = -40^{\circ}\text{C}$, $T_{MAX} = +85^{\circ}\text{C}$; external 1.25 V voltage reference and rated encode frequency used, unless otherwise noted.

Table 1.

Parameter	Temp	Test Level	AD9214-65			AD9214-80			AD9214-105			Unit
			Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
RESOLUTION			10			10			10			Bits
ACCURACY												
No Missing Codes	25°C	VI	Guaranteed			Guaranteed			Guaranteed			
	Full	VI	Guaranteed			Guaranteed			Guaranteed			
Offset Error	Full	VI	-18	0	+18	-18		+18	-18	0	+18	LSB
Gain Error ¹	25°C	I	-2		+8	-2		+8	-2		+8	%FS
Differential Nonlinearity ²	25°C	I	-1.0	±0.5	+1.0	-1.0	±0.5	+1.2	-1.0	±0.08	+1.5	LSB
(DNL)	Full	V	-1.0		+1.2	-1.0		+1.4			+1.7	LSB
Integral Nonlinearity ²	25°C	I	-1.35	±0.75	+1.35	-1.5	±0.75	+1.5	-2.2	±1.5	+2.2	LSB
(INL)	Full	V	-1.9		+1.9	-1.8		+1.8	-2.5		+2.5	LSB
TEMPERATURE DRIFT												
Offset Error	Full	V	16			16			16			ppm/°C
Gain Error ¹	Full	V	150			150			150			ppm/°C
Reference Voltage	Full	V	80			80			80			ppm/°C
REFERENCE (REF)												
Internal Reference Voltage	25°C	VI	1.18	1.23	1.28	1.18	1.23	1.28	1.18	1.23	1.28	V
Output Current ³	Full	V	200			200			200			μA
Input Current ⁴	Full	V	123			123			123			μA
Input Resistance	Full	V	10			10			10			kΩ
ANALOG INPUTS (A_{IN} , \bar{A}_{IN})												
Differential Input Range	Full	V	1 or 2									V p-p
Common-Mode Voltage	Full	V	$AV_{DD}/3$			$AV_{DD}/3$			$AV_{DD}/3$			V
Differential Input Resistance ⁵	Full	V	20			20			20			kΩ
Differential Input Capacitance	Full	V	5			5			5			pF
POWER SUPPLY												
Supply Voltages												
AV_{DD}	Full	IV	2.7		3.6	2.7		3.6	2.7		3.6	V
DrV_{DD}	Full	IV	2.7		3.6	2.7		3.6	2.7		3.6	V
Supply Current												
I_{AVDD} ($AV_{DD} = 3.0\text{ V}$) ⁶	Full	VI	64		75	90		105	95		110	mA
Power-Down Current ⁷												
I_{AVDD} ($AV_{DD} = 3.0\text{ V}$)	Full	VI	10		15	10		15	10		15	mA
Power Consumption ⁸	Full	VI	190		220	250		300	285		325	mW
PSRR	25°C	I	±0.5			±1			±1			LSB/V
	Full	V	±2			±2			±2			mV/V

¹ Gain error and gain temperature coefficient are based on the ADC only (with a fixed 1.25 V external reference).

² Measured with 1 V A_{IN} range for AD9214-80 and AD9214-105. Measured with 2 V A_{IN} range for AD9214-65.

³ REFSense externally connected to AGND, REF is configured as an output for the internal reference voltage.

⁴ REFSense externally connected to AV_{DD} , REF is configured as an input for the external reference voltage.

⁵ 10 kΩ to $AV_{DD}/3$ on each input.

SPECIFICATIONS

Table 1.

Parameter	Temp	Test Level	AD9214-65			AD9214-80			AD9214-105			Unit
			Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	

⁶ I_{AVDD} is measured with an analog input of 10.3 MHz, 0.5 dBFS, sine wave, rated encode rate, and PWRDN = 0. See the [Typical Performance Characteristics](#) section and [Applying the AD9214](#) section for I_{DrVDD} .

⁷ Power-down supply currents measured with PWRDN = 1; rated encode rate, A_{IN} = full-scale dc input.

⁸ Power consumption measured with A_{IN} = full-scale dc input.

DIGITAL SPECIFICATIONS

$AV_{DD} = 3\text{ V}$, $DrV_{DD} = 3\text{ V}$; $T_{MIN} = -40^{\circ}\text{C}$, $T_{MAX} = +85^{\circ}\text{C}$.

Table 2.

			AD9214-65			AD9214-80			AD9214-105			
Parameter	Temp	Test Level	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Unit
DIGITAL INPUTS ¹												
Logic "1" Voltage	Full	IV	2.0			2.0			2.0			V
Logic "0" Voltage	Full	IV			0.8			0.8			0.8	V
Input Capacitance	Full	V		2.0			2.0			2.0		pF
DIGITAL OUTPUTS ²												
Logic Compatibility				CMOS/T TL			CMOS/T TL			CMOS/T TL		V
Logic "1" Voltage	Full	VI	DrV _{DD} – 50 mV			DrV _{DD} – 50 mV			DrV _{DD} – 50 mV			V
Logic "0" Voltage	Full	VI			50			50			50	mV

¹ Digital Inputs include ENCODE and PWRDN.

² Digital Outputs include D0–D9 and OR.

AC SPECIFICATIONS

AC specifications based on a 1.0 V p-p full-scale input range for the AD9214-80 and AD9214-105, and a 2.0 V p-p full-scale input range for the AD9214-65. An external reference is used. $AV_{DD} = 3\text{ V}$, $DrV_{DD} = 3\text{ V}$; ENCODE = maximum conversion rate; $T_{MIN} = -40^{\circ}\text{C}$, $T_{MAX} = +85^{\circ}\text{C}$; external 1.25 V voltage reference used, unless otherwise noted.

Table 3.

		Test Level	AD9214-65			AD9214-80			AD9214-105			Unit
Parameter	Temp		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
SNR												
Analog Input @ -0.5 dBFS												
10 MHz	25°C	I	55.5	58.3		56.0	58.1		51.0	53.0		dB
39 MHz	25°C	I		57.1		55.0	57.1		50.5	53.0		dB
51 MHz	25°C	V					55.0			53.0		dB
70 MHz	25°C	V					54.0			52.6		dB
SINAD												
Analog Input @ -0.5 dBFS												
10 MHz	25°C	I	55.0	57.8		55.5	57.6		50.0	52.0		dB
39 MHz	25°C	I		56.7		54.5	56.7		50.0	52.0		dB
51 MHz	25°C	V					54.5			52.0		dB
70 MHz	25°C	V								52.0		dB
EFFECTIVE NUMBER OF BITS												

SPECIFICATIONS

Table 3.

Parameter	Temp	Test Level	AD9214-65			AD9214-80			AD9214-105			Unit
			Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
Analog Input @ -0.5 dBFS												
10 MHz	25°C	I	8.9	9.3		9.0	9.3		8.4			Bit
39 MHz	25°C	I		9.2		8.8	9.2		8.4			Bit
51 MHz	25°C	V					8.8		8.4			Bit
70 MHz	25°C	V					8.5		8.4			Bit
SECOND HARMONIC DISTORTION												
Analog Input @ -0.5 dBFS												
10 MHz	25°C	I	-66	-79		-64	-74		-62	-68		dBc
39 MHz	25°C	I		-75		-63	-76		-62	-71		dBc
51 MHz	25°C	V					-72			-64		dBc
70 MHz	25°C	V					-65			-62		dBc
THIRD HARMONIC DISTORTION												
Analog Input @ -0.5 dBFS												
10 MHz	25°C	I	-63.5	-71		-63	-72		-59	-64		dBc
39 MHz	25°C	I		-70		-63	-74		-59	-67		dBc
51 MHz	25°C	V					-78			-71		dBc
70 MHz	25°C	V								-65		dBc
SFDR												
Analog Input @ -0.5 dBFS												
10 MHz	25°C	I	63.5	71		63	71		57	62		dBc
39 MHz	25°C	I		70		63	71		57	62		dBc
51 MHz	25°C	V					67			62		dBc
70 MHz	25°C	V					64			62		dBc
TWO-TONE INTERMOD DISTORTION ¹												
Analog Input @ -0.5 dBFS	25°C	V		76			74			72		dBFS
ANALOG INPUT BANDWIDTH	25°C	V		300			300			300		MHz

¹ F1 = 29.3 MHz, F2 = 30.3 MHz.

SWITCHING SPECIFICATIONS

$AV_{DD} = 3\text{ V}$, $DrV_{DD} = 3\text{ V}$; ENCODE = maximum conversion rate; $T_{MIN} = -40^{\circ}\text{C}$, $T_{MAX} = +85^{\circ}\text{C}$; external 1.25 V voltage reference used, unless otherwise noted.

Table 4.

Parameter	Temp	Test Level	AD9214-65			AD9214-80			AD9214-105			Unit
			Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
ENCODE INPUT PARAMETERS ¹												
Maximum Conversion Rate	Full	VI	65			80			105			MSPS
Minimum Conversion Rate	Full	IV			20			20			20	MSPS
Encode Pulse Width High (t_{EH})	Full	IV	6.0			5.0			3.8			ns
Encode Pulse Width Low (t_{EL})	Full	IV	6.0			5.0			3.8			ns
Aperture Delay (t_A)	25°C	V		2.0			2.0			2.0		ns
Aperture Uncertainty (Jitter)	25°C	V		3			3			3		ps rms
DATA OUTPUT PARAMETERS												
Pipeline Delays	Full	IV		5			5			5		Clock Cycle
Output Valid Time (t_{V}) ¹	Full	V	3.0	4.5		3.0	4.5		3.0	4.5		ns

SPECIFICATIONS

Table 4.

Parameter	Temp	Test Level	AD9214-65			AD9214-80			AD9214-105			Unit
			Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
Output Propagation Delay ¹ (t_{PD})	Full	V		4.5	6.0		4.5	6.0		4.5	6.0	ns
TRANSIENT RESPONSE TIME	25°C	V		5			5			5		ns
OUT-OF-RANGE RECOVERY TIME	25°C	V		5			5			5		ns

¹ t_V and t_{PD} are measured from the 1.5 V level of the ENCODE input to the 50% levels of the digital output swing. The digital output load during test is not to exceed an ac load of 5 pF or a dc current of $\pm 40 \mu\text{A}$.

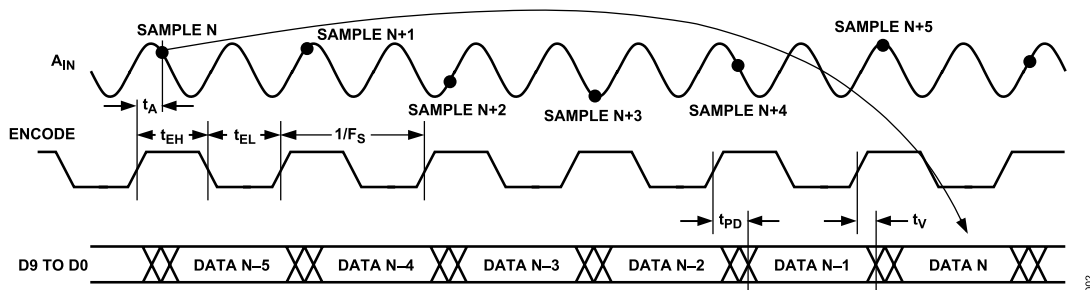


Figure 2. Timing Diagram

ABSOLUTE MAXIMUM RATINGS

Table 5.

Parameter	Rating
Electrical	
AV _{DD} Voltage	4 V max
DrV _{DD} Voltage	4 V max
Analog Input Voltage	-0.5 V to AV _{DD} + 0.5 V
Analog Input Current	0.4 mA
Digital Input Voltage	-0.5 V to AV _{DD} + 0.5 V
Digital Output Current	20 mA max
REF Input Voltage	-0.5 V to AV _{DD} + 0.5 V
Environmental ¹	
Operating Temperature Range (Ambient)	-40°C to +125°C
Maximum Junction Temperature	150°C
Lead Temperature (Soldering, 10 sec)	150°C
Storage Temperature Range (Ambient)	-65°C to +150°C

¹ Typical thermal impedances (package = 28 SSOP); $\theta_{JA} = 49^{\circ}\text{C/W}$. These measurements were taken on a six-layer board in still air with a solid ground plane.

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

EXPLANATION OF TEST LEVELS

Table 6.

Level	Description
I	100% production tested.
II	100% production tested at 25°C and guaranteed by design and characterization at specified temperatures.
III	Sample tested only.
IV	Parameter is guaranteed by design and characterization testing.
V	Parameter is a typical value only.
VI	100% production tested at 25°C and guaranteed by design and characterization for industrial temperature range.

ESD CAUTION



ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

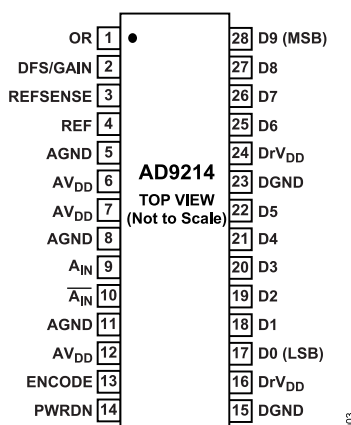


Figure 3. Pin Configuration

Table 7. Pin Function Descriptions

Pin No.	Mnemonic	Description
1	OR	CMOS Output; Out-of-Range Indicator. Logic HIGH indicates the analog input voltage was outside the converter's range for the current output data.
2	DFS/GAIN	Data Format Select and Gain Mode Select. Connect externally to AVDD for twos complement data format and 1 V p-p analog input range. Connect externally to AGND for Offset Binary data format and 1 V p-p analog input range. Connect externally to REF (Pin 4) for twos complement data format and 2 V p-p analog input range. Floating this pin will configure the device for Offset Binary data format and a 2 V p-p analog input range.
3	REFSENSE	Reference Mode Select Pin for the ADC. This pin is normally connected externally to AGND, which enables the internal 1.25 V reference, and configures REF (Pin 4) as an analog reference output pin. Connecting REFSense externally to AVDD disables the internal reference, and configures REF (Pin 4) as an external reference input. In this case, the user must drive REF with a clean and accurate 1.25 V ($\pm 5\%$) reference input.
4	REF	Reference input or output as configured by REFSense (Pin 3). When configured as an output (REFSENSE = AGND), the internal reference (nominally 1.25 V) is enabled and is available to the user on this pin. When configured as an input (REFSENSE = AVDD), the user must drive REF with a clean and accurate 1.25 V ($\pm 5\%$) reference. This pin should be bypassed to AGND with an external 0.1 μ F capacitor, whether it is configured as an input or output.
5, 8, 11	AGND	Analog Ground.
6, 7, 12	AVDD	Analog Power Supply, Nominally 3 V.
9	A _{IN}	Positive terminal of the differential analog input for the ADC.
10	A _{IN}	Negative terminal of the differential analog input for the ADC. This pin can be left open if operating in single-ended mode, but it is preferable to match the impedance seen at the positive terminal (see Driving the Analog Inputs).
13	ENCODE	Encode Clock for the ADC. The AD9214 samples the analog signal on the rising edge of ENCODE.
14	PWRDN	CMOS-compatible power-down mode select, Logic LOW for normal operation; Logic HIGH for power-down mode (digital outputs in high impedance state). PWRDN has an internal 10 k Ω pull-down resistor to ground.
15, 23	DGND	Digital Output Ground.
16, 24	DrVDD	Digital Output Driver Power Supply. Nominally 2.5 V to 3.6 V.
17 to 22, 25 to 28	D0 (LSB) to D5, D6 to D9 (MSB)	CMOS Digital Outputs of ADC.

TYPICAL PERFORMANCE CHARACTERISTICS

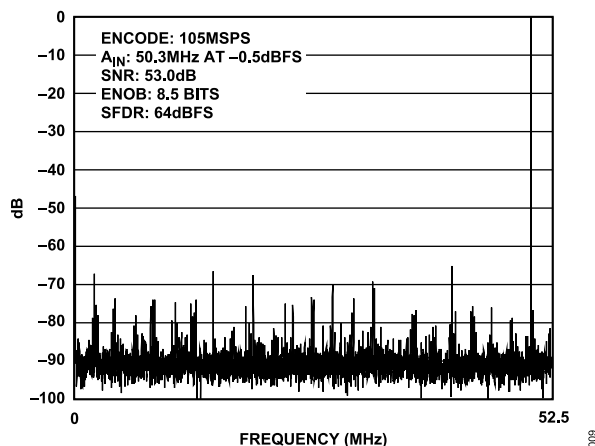


Figure 4. FFT: $f_S = 105$ MSPS, $f_{IN} = \sim 50.3$ MHz; $A_{IN} = -0.5$ dBFS Differential, 1 V p-p Analog Input Range

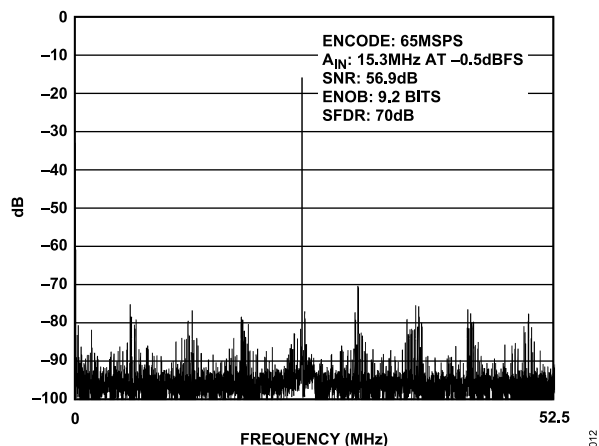


Figure 7. FFT: $f_S = 65$ MSPS, $f_{IN} = 15.3$ MHz (2 V p-p) with AD8138 Driving A_{IN}

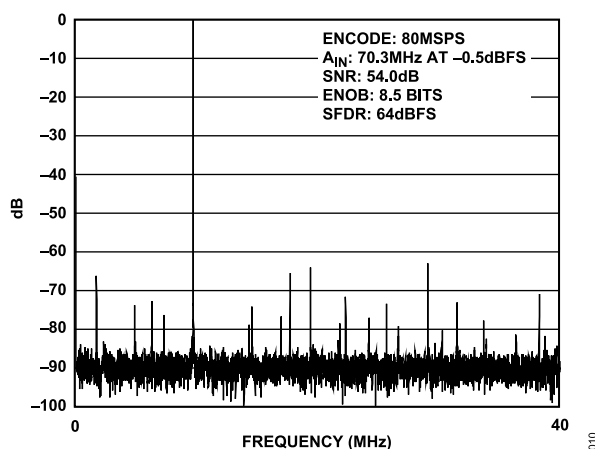


Figure 5. FFT: $f_S = 80$ MSPS, $f_{IN} = 70$ MHz; $A_{IN} = -0.5$ dBFS, 1 V p-p Analog Input Range

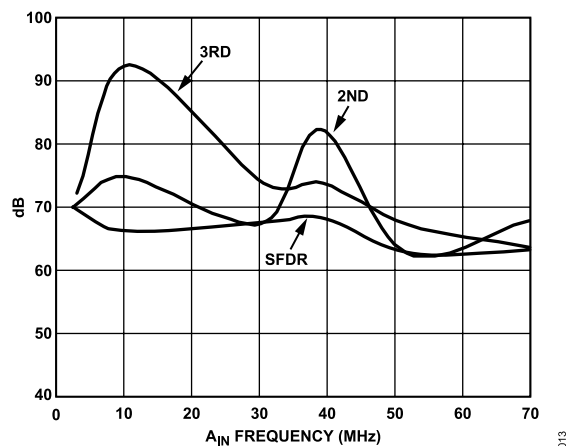


Figure 8. Harmonic Distortion (Second and Third) and SFDR vs. A_{IN} Frequency (1 V p-p, $f_S = 105$ MSPS)

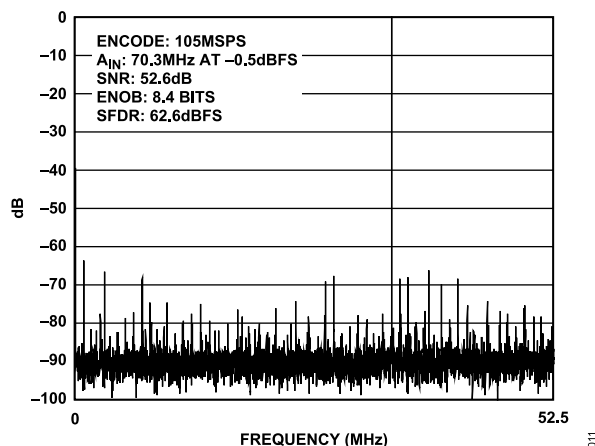


Figure 6. FFT: $f_S = 105$ MSPS; $f_{IN} = 70$ MHz (1 V p-p)

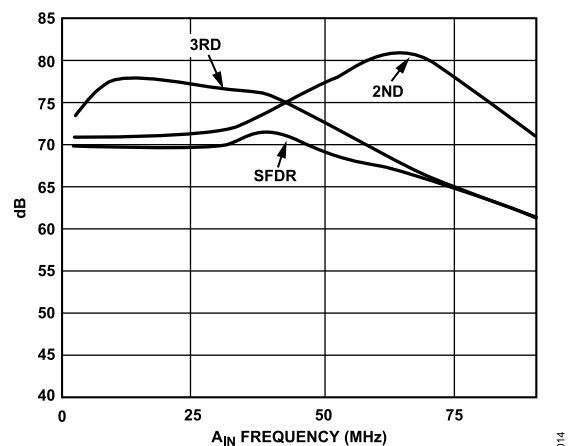


Figure 9. Harmonic Distortion (Second and Third) and SFDR vs. A_{IN} Frequency (1 V p-p, $f_S = 80$ MSPS)

TYPICAL PERFORMANCE CHARACTERISTICS

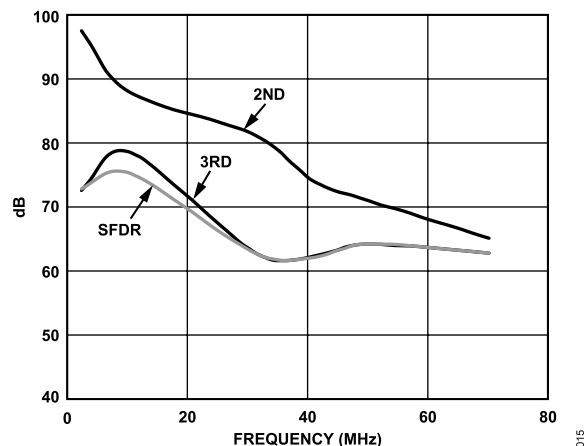


Figure 10. Harmonic Distortion (Second and Third) and SFDR vs. A_{IN} Frequency (1 V p-p and 2 V p-p, $f_s = 65$ MSPS)

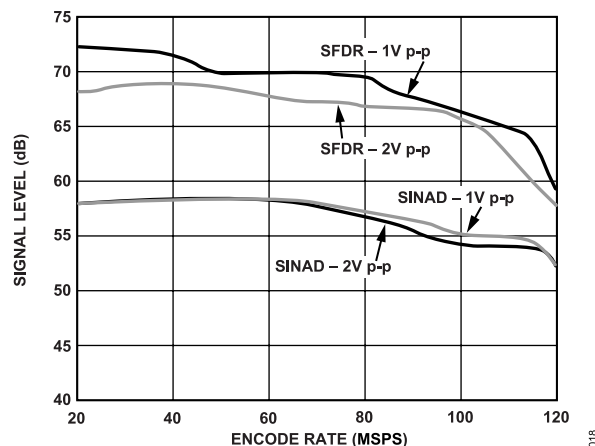


Figure 13. SINAD and SFDR vs. Encode Rate ($f_{IN} = 10.3$ MHz; 1 V p-p and 2 V p-p)

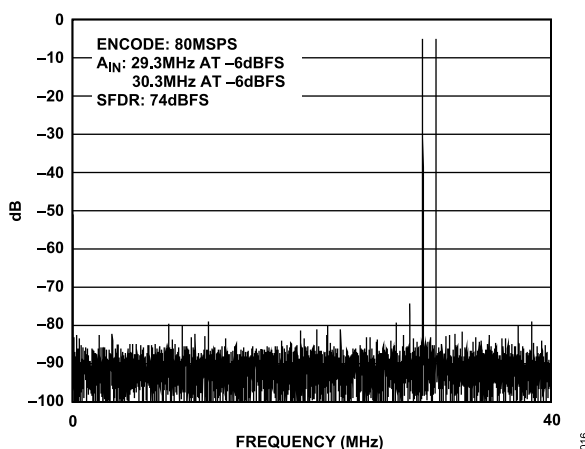


Figure 11. Two-Tone Intermodulation Distortion (29.3 MHz, 30.3 MHz; 1 V p-p, $f_s = 80$ MSPS)

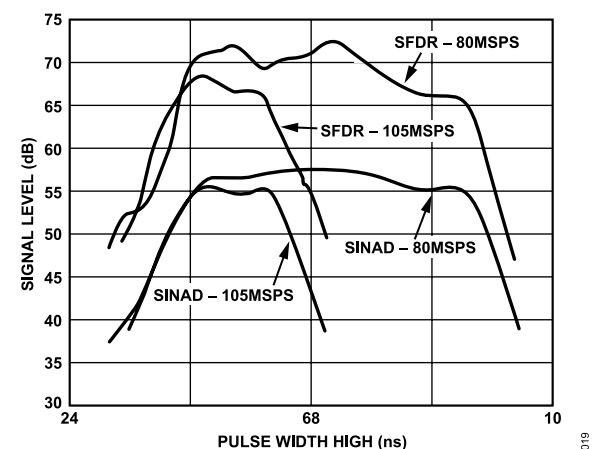


Figure 14. SINAD and SFDR vs. Encode Pulse Width High (1 V p-p)

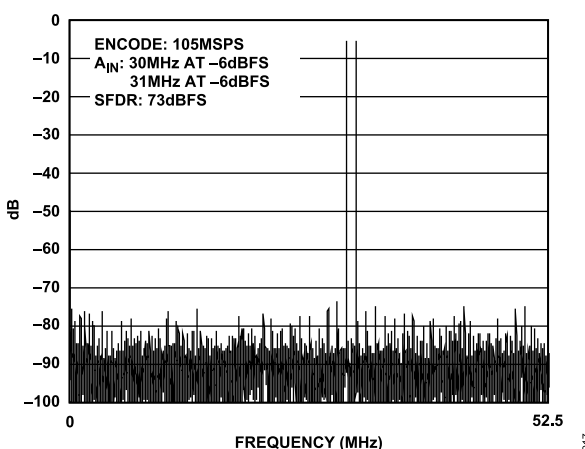


Figure 12. Two-Tone Intermodulation Distortion (30 MHz and 31 MHz; 1 V p-p, $f_s = 105$ MSPS)

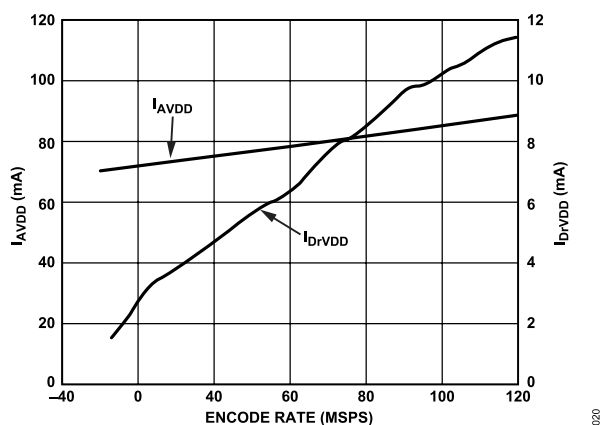


Figure 15. I_{AVDD} and I_{DRVDD} vs. Encode Rate ($f_{AIN} = 10.3$ MHz, -0.5 dBFS, and -3 dBFS) C_{LOAD} on Digital Outputs ~ 7 pF

TYPICAL PERFORMANCE CHARACTERISTICS

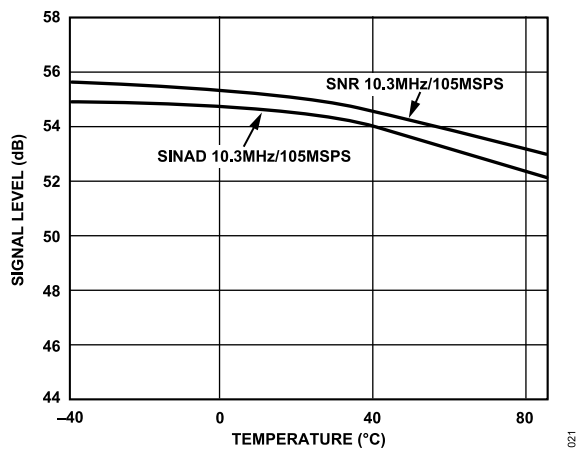


Figure 16. SINAD/SNR vs. Temperature ($f_{AIN} = 10.3 \text{ MHz}$, $f_{ENCODE} = 105 \text{ MSPS}$, 1 V p-p)

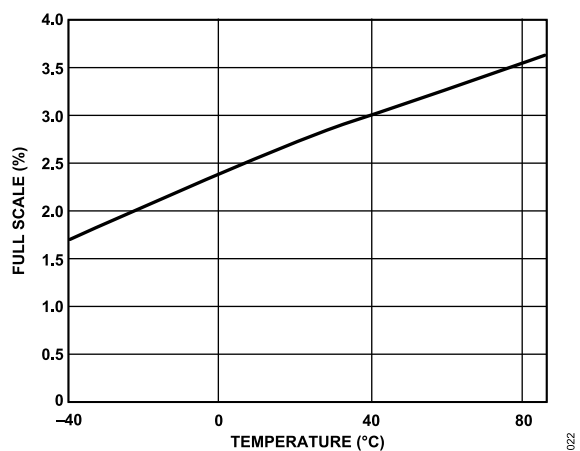


Figure 17. ADC Gain vs. Temperature (with External 1.25 V Reference)

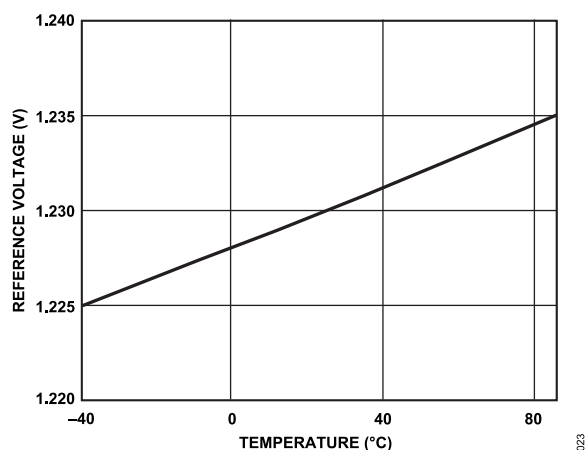


Figure 18. ADC Reference vs. Temperature (with 200 μA Load)

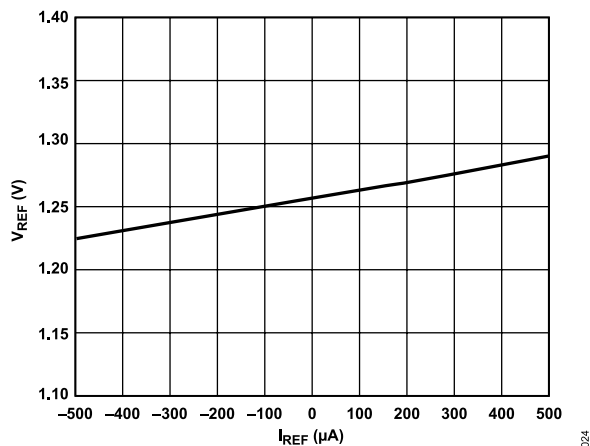


Figure 19. ADC Reference vs. Current Load

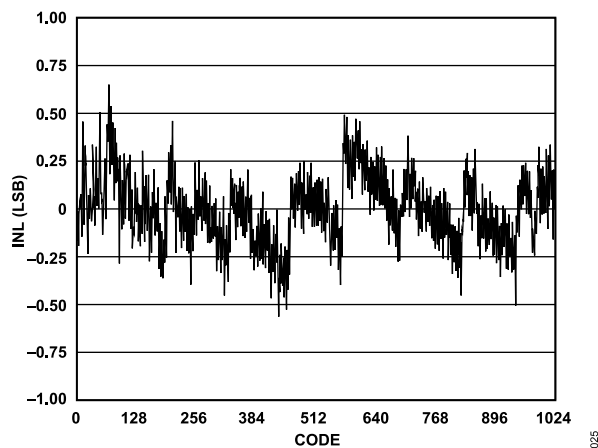


Figure 20. INL @ 80 MSPS

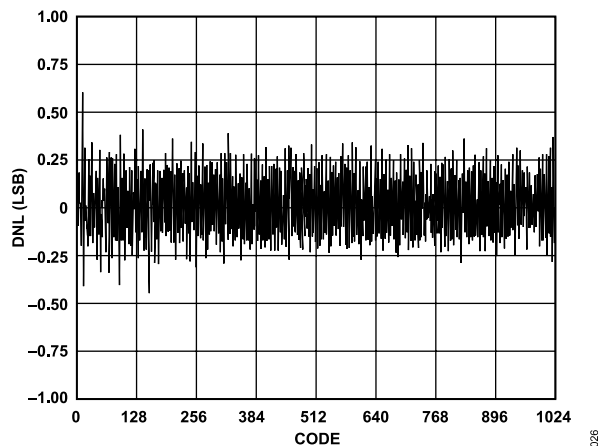


Figure 21. DNL @ 80 MSPS

EQUIVALENT CIRCUITS

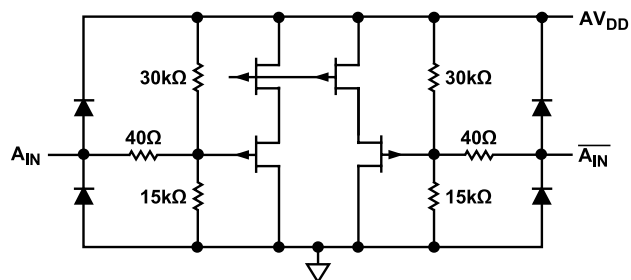


Figure 22. Analog Input Stage

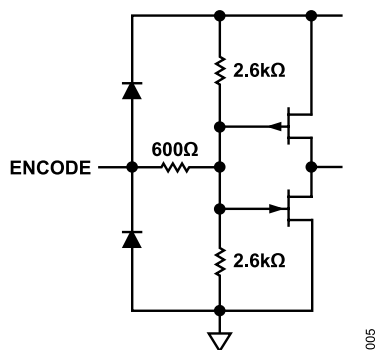


Figure 23. Encode Inputs

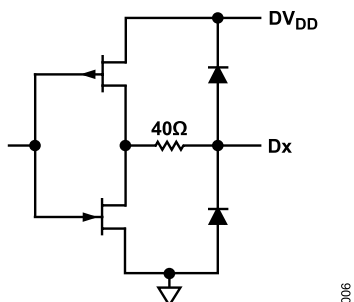


Figure 24. Digital Output Stage

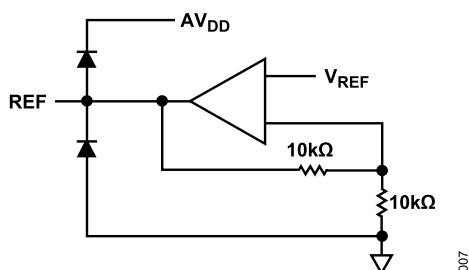


Figure 25. REF Configured as an Output

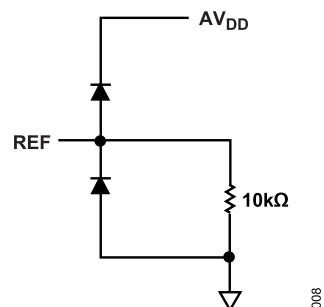


Figure 26. REF Configured as an Input

TERMINOLOGY

Analog Bandwidth

The analog input frequency at which the spectral power of the fundamental frequency (as determined by the FFT analysis) is reduced by 3 dB.

Aperture Delay

The delay between the 50% point of the rising edge of the ENCODE command and the instant at which the analog input is sampled.

Aperture Uncertainty (Jitter)

The sample-to-sample variation in aperture delay.

Differential Analog Input Resistance, Differential Analog Input Capacitance, and Differential Analog Input Impedance

The real and complex impedances measured at each analog input port. The resistance is measured statically and the capacitance and differential input impedances are measured with a network analyzer.

Differential Analog Input Voltage Range

The peak-to-peak differential voltage that must be applied to the converter to generate a full-scale response. Peak differential voltage is computed by observing the voltage on a single pin and subtracting the voltage from the other pin, which is 180 degrees out of phase. Peak-to-peak differential is computed by rotating the inputs phase 180 degrees and taking the peak measurement again. Then the difference is computed between both peak measurements.

Differential Nonlinearity

The deviation of any code width from an ideal 1 LSB step.

Effective Number of Bits

The effective number of bits (ENOB) is calculated from the measured SNR based on the equation:

$$ENOB = \frac{SINAD_{MEASURED} - 1.76 \text{ dB} + 20 \log\left(\frac{Full \text{ Scale}}{Actual}\right)}{6.02}$$

Encode Pulse Width/Duty Cycle

Pulse width high is the minimum amount of time that the ENCODE pulse should be left in Logic "1" state to achieve rated performance; pulse width low is the minimum time ENCODE pulse should be left in low state. See timing implications of changing t_{ENCH} in text. At a given clock rate, these specs define an acceptable Encode duty cycle.

Full-Scale Input Power

Expressed in dBm. Computed using the following equation:

$$Power_{FULLSCALE} = 10 \log \left(\frac{\left(\frac{V_{FULLSCALE}^2}{Z_{INPUT}} \right)_{rms}}{0.001} \right)$$

Gain Error

Gain error is the difference between the measured and ideal full scale input voltage range of the ADC.

Harmonic Distortion, Second

The ratio of the rms signal amplitude to the rms value of the second harmonic component, reported in dBc.

Harmonic Distortion, Third

The ratio of the rms signal amplitude to the rms value of the third harmonic component, reported in dBc.

Integral Nonlinearity

The deviation of the transfer function from a reference line measured in fractions of 1 LSB using a "best straight line" determined by a least square curve fit.

Minimum Conversion Rate

The encode rate at which the SNR of the lowest analog signal frequency drops by no more than 3 dB below the guaranteed limit.

Maximum Conversion Rate

The encode rate at which parametric testing is performed.

Output Propagation Delay

The delay between a differential crossing of ENCODE and ENCODE and the time when all output data bits are within valid logic levels.

Noise (for any range within the ADC):

$$V_{NOISE} = \sqrt{Z \times 0.001 \times 10^{\frac{FS_{dBm} - SNR_{dBc} - Signal_{dBFS}}{10}}}$$

where:

Z is the input impedance.

FS is the full-scale of the device for the frequency in question.

SNR is the value for the particular input level.

$Signal$ is the signal level within the ADC reported in dB below full-scale. This value includes both thermal and quantization noise.

Power Supply Rejection Ratio (PSRR)

The ratio of a change in input offset voltage to a change in power supply voltage.

Signal-to-Noise-and-Distortion (SINAD)

The ratio of the rms signal amplitude (set 0.5 dB below full scale) to the rms value of the sum of all other spectral components, including harmonics but excluding dc.

TERMINOLOGY

Signal-to-Noise Ratio (without Harmonics)

The ratio of the rms signal amplitude (set at 0.5 dB below full scale) to the rms value of the sum of all other spectral components, excluding the first five harmonics and dc.

Spurious-Free Dynamic Range (SFDR)

The ratio of the rms signal amplitude to the rms value of the peak spurious spectral component. The peak spurious component may or may not be a harmonic. May be reported in dBc (that is, degrades as signal level is lowered), or dBFS (always related back to converter full scale).

Two-Tone Intermodulation Distortion Rejection

The ratio of the rms value of either input tone to the rms value of the worst third order intermodulation product; reported in dBc.

Two-Tone SFDR

The ratio of the rms value of either input tone to the rms value of the peak spurious component. The peak spurious component may or may not be an intermodulation distortion product. May be reported in dBc (that is, degrades as signal level is lowered), or in dBFS (always related back to converter full scale).

Worst Other Spur

The ratio of the rms signal amplitude to the rms value of the worst spurious component (excluding the second and third harmonic) reported in dBc.

Transient Response Time

Transient response is defined as the time it takes for the ADC to reacquire the analog input after a transient from 10% above negative full scale to 10% below positive full scale.

Out-of-Range Recovery Time

Out-of-range recovery time is the time it takes for the ADC to reacquire the analog input after a transient from 10% above positive full scale to 10% above negative full scale, or from 10% below negative full scale to 10% below positive full scale.

THEORY OF OPERATION

The AD9214 architecture is a bit-per-stage pipeline converter utilizing switch capacitor techniques. These stages determine the 7 MSBs and drive a 3-bit flash. Each stage provides sufficient overlap and error correction allowing optimization of comparator accuracy. The input buffer is differential and both inputs are internally biased. This allows the most flexible use of ac or dc and differential or single-ended input modes. The output staging block aligns the data, carries out the error correction and feeds the data to output buffers. The output buffers are powered from a separate supply, allowing support of different logic families. During power-down, the outputs go to a high impedance state.

APPLYING THE AD9214

Encoding the AD9214

Any high-speed A/D converter is extremely sensitive to the quality of the sampling clock provided by the user. A Track/ Hold circuit is essentially a mixer. Any noise, distortion, or timing jitter on the clock will be combined with the desired signal at the A/D output. For that reason, considerable care has been taken in the design of the ENCODE input of the AD9214, and the user is advised to give commensurate thought to the clock source. The ENCODE input is fully TTL/CMOS compatible, and should normally be driven directly from a low jitter, crystal-controlled TTL/CMOS oscillator.

The ENCODE input is internally biased, allowing the user to ac-couple in the clock signal. The cleanest clock source is often a crystal oscillator producing a pure sine wave. Figure 27 illustrates ac coupling such a source to the ENCODE input.

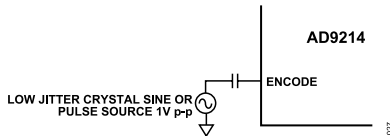


Figure 27. AC-Coupled Encode Circuit

Reference Circuit

The reference circuit of the AD9214 is configured by REFSENSE (Pin 3). By externally connecting REFSENSE to AGND, the ADC is configured to use the internal reference (~ 1.25 V), and the REF pin connection (Pin 4) is configured as an output for the internal reference voltage.

If REFSENSE is externally connected to AV_{DD} , the ADC is configured to use an external reference. In this mode, the REF pin is configured as a reference input, and must be driven by an external 1.25 V reference.

In either configuration, the analog input voltage range (either 1 V p-p or 2 V p-p as determined by DFS/Gain) will track the reference voltage linearly, and an external bypass capacitor should be connected between REF and AGND to reduce noise on the reference. In practice, no appreciable degradation in performance occurs when an external reference is adjusted $\pm 5\%$.

DFS/GAIN

The DFS/GAIN (Data Format Select/Gain) input (Pin 2) controls both the output data format and gain (analog input voltage range) of the ADC. The table below describes its operation.

Table 8. Data Format and Gain Configuration

External DFS/GAIN Connection	Differential Analog Input Voltage Range	Output Data Format
AGND	1 V p-p	Offset Binary
AV_{DD}	1 V p-p	Twos Complement
REF	2 V p-p	Twos Complement
Floating	2 V p-p	Offset Binary

Driving the Analog Inputs

The analog input to the AD9214 is a differential buffer. As shown in the equivalent circuits, each of the differential inputs is internally dc biased at $\sim AV_{DD}/3$ to allow ac-coupling of the analog input signal. The analog signal may be dc-coupled as well. In this case, the dc load will be equivalent to ~ 10 k Ω to $AV_{DD}/3$, and the dc common-mode level of the analog signals should be within the range of $AV_{DD}/3 \pm 200$ mV. For best dynamic performance, impedances at A_{IN} and \bar{A}_{IN} should match.

Driving the analog input differentially optimizes ac performance, minimizing even order harmonics and taking advantage of common-mode rejection of noise. A differential signal may be transformer-coupled, as illustrated in Figure 28, or driven from a high-performance differential amplifier such as the AD8138 illustrated in Figure 29.

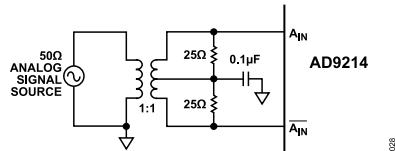


Figure 28. Single-Ended-to-Differential Conversion Using a Transformer

Special care was taken in the design of the analog input section of the AD9214 to prevent damage and corruption of data when the input is overdriven. The optimal input range is 1.0 V p-p, but the AD9214 can support a 2.0 V p-p input range with some degradation in performance (see Table 8).

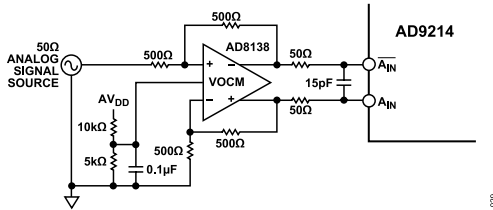


Figure 29. DC-Coupled Analog Input Circuit

THEORY OF OPERATION

POWER SUPPLIES

The AD9214 has two power supplies, AV_{DD} and DrV_{DD} . AV_{DD} and AGND supply power to all the analog circuitry, the inputs and the internal timing and digital error correction circuits. AV_{DD} supply current will vary slightly with encode rate, as noted in the Typical Performance Characteristics section.

DrV_{DD} and DGND supply only the CMOS digital outputs, allowing the user to adjust the voltage level to match downstream logic.

DrV_{DD} current will vary depending on the voltage level, external loading capacitance, and the encode frequency. Designs that minimize external load capacitance will reduce power consumption and reduce supply noise that may affect ADC performance. The maximum DrV_{DD} current can be calculated as

$$I_{DrVDD} = V_{DrVDD} \times C_{LOAD} \times f_{encode} \times N$$

where N is the number of output bits, 10 in the case of the AD9214.

This maximum current is for the condition of every output bit switching on every clock cycle, which can only occur for a full-scale square wave at the Nyquist frequency, $f_{ENCODE}/2$. In practice, I_{DrVDD} will be the average number of output bits switching, which will be determined by the encode rate and the characteristics of the analog input signal. The performance curves section provides a reference of I_{DrVDD} versus encode rate for a 10.3 MHz sine wave driving the analog input.

Both power supply connections should be decoupled to ground at or near the package connections, using high quality, ceramic chip capacitors. A single ground plane is recommended for all ground (AGND and DGND) connections.

The PWRDN control pin configures the AD9214 for a sleep mode when it is logic HIGH. PWRDN floats logic LOW for normal operation. In sleep mode, the ADC is not active, and will consume less power. When switching from sleep mode to normal operation, the ADC will need ~15 clock cycles to recover to valid output data.

Digital Outputs

Care must be taken when designing the data receivers for the AD9214. It is recommended that the digital outputs drive a series resistor (for example, 100 Ω) followed by a gate like the 74LCX821. To minimize capacitive loading, there should be only one gate on each output pin. An example of this is shown in the evaluation board schematic in Figure 30. The series resistors should be placed as close to the AD9214 as possible to limit the amount of current that can flow into the output stage. These switching currents are confined between ground (DGND) and the DrV_{DD} pins. Standard TTL gates should be avoided since they can appreciably add to the dynamic switching currents of the AD9214. It should also be noted that extra capacitive loading will increase output timing and invalidate timing specifications. Digital output timing is guaranteed with 10 pF loads.

LAYOUT INFORMATION

The schematic of the evaluation board (Figure 30) represents a typical implementation of the AD9214. A multilayer board is recommended to achieve best results. It is highly recommended that high quality, ceramic chip capacitors be used to decouple each supply pin to ground directly at the device. The pinout of the AD9214 facilitates ease of use in the implementation of high frequency, high resolution design practices. All of the digital outputs and their supply and ground pin connections are segregated to one side of the package, with the inputs on the opposite side for isolation purposes.

Care should be taken when routing the digital output traces. To prevent coupling through the digital outputs into the analog portion of the AD9214, minimal capacitive loading should be placed on these outputs. It is recommended that a fan-out of only one gate should be used for all AD9214 digital outputs.

The layout of the encode circuit is equally critical. Any noise received on this circuitry will result in corruption in the digitization process and lower overall performance. The Encode clock must be isolated from the digital outputs and the analog inputs.

EVALUATION BOARD

The AD9214 evaluation board offers designers an easy way to evaluate device performance. The user must supply an analog input signal, encode clock reference, and power supplies. The digital outputs of the AD9214 are latched on the evaluation board, and are available with a data ready signal at a 40-pin edge connector. Refer to the evaluation board and Schematic sections, and Table 11.

Power Connections

Power to the board is supplied via three detachable, 4-pin power strips (U4, U9, and U10). These 12 pins should be driven as outlined in the Table 9.

Table 9. Power Supply Connections for AD9214

Pin	Designator	External Supply Required
1	LVC	3 V
3	5 V	5 V (optional Z1 supply)
5	–5 V	–5 V (optional Z1 supply)
7	VCC	3 V
9	VDD	3 V
11	DAC	5 V
2, 4, 6, 8, 10, 12	GND	Ground

Note that the +5 V and –5 V supplies are optional, and only required if the user adds differential op amp Z1 to the board.

Reference Circuit

The evaluation board is configured at assembly to use the AD9214's on-board reference. To supply an external reference, the user must connect the REFSENSE pin to VCC by removing the

THEORY OF OPERATION

jumper block connecting E25 to E26, and placing it between E19 and E24. In this configuration, an external 1.25 V reference must be connected to jumper connection E23. Jumper connections E19 to E21, E24, and resistors R13 to R14 are omitted at assembly, and not used in the evaluation of the AD9214.

Gain/Data Format

The evaluation board is assembled with the DFS/GAIN pin connected to ground; this configures the AD9214 for a 1 V p-p analog input range, and offset binary data format. The user may remove this jumper and replace it to make one of the connections described in the table below to configure the AD9214 for different gain and output data format options.

Table 10. Data Format and Gain Configuration for Evaluation Board

DFS/GAIN Jumper Placement	DFS/GAIN Connection	Differential AIN Range	Output Data Format
E18 to E12	AGND	1 V p-p	Offset Binary
E16 to E11	AVDD	1 V p-p	Twos Complement
E15 to E14	REF	2 V p-p	Twos Complement
E17 to E13	Floating	2 V p-p	Offset Binary

Power-Down

The evaluation board is configured at assembly so that the PWRDN input floats low for normal operating condition. The user may add a jumper between option holes E5 and E6 to connect PWRDN to AVCC, configuring the AD9214 for power-down mode.

Encode Signal and Distribution

The encode input signal should drive SMB connector J5, which has an on-board 50 Ω termination. A standard CMOS compatible pulse source is recommended. Alternatively, the user can adjust the dc level of an ac-coupled clock source by adding resistor R11, normally omitted. J5 drives the AD9214 ENCODE input and one gate of U12, which buffers and distributes the clock signal to the on-board latch (U3), the reconstruction DAC (U11), and the output data connector (U2). The board comes assembled with timing options optimized for the DAC and latch; the user may invert the DR signal at Pin 37 of edge connector U2 by removing the jumper block between E34 and E35, and reinstalling it between E35 and E36.

Analog Input

The analog input signal is connected to the evaluation board by SMB connector J1. As configured at assembly, the signal is ac coupled by capacitor C10 to transformer T1. This 1:1 transformer provides a 50 Ω termination for connector J1 via 25 Ω resistors R1 and R4. T1 also converts the signal at J1 into a differential signal for the analog inputs of the AD9214. Resistor R3, normally omitted, can be used to terminate J1 if the transformer is removed.

The user can reconfigure the board to drive the AD9214 single-endedly by removing the jumper block between E1 and E3, and

replacing it between E3 and E2. In this configuration, capacitor C2 stabilizes the self-bias of $\overline{A_{IN}}$, and resistor R2 provides a matched impedance for a 50 Ω source at J1.

Transformer T1 can be bypassed by moving the jumper normally between E40 and E38 to connect E40 to E37, and moving the jumper normally between E39 and E10 to connect E7 to E10. In this configuration, the analog input of the AD9214 is driven single ended, directly from J1; and R3 (normally omitted) should be installed to terminate any cable connected to J1.

Using the AD8138

An optional driver circuit for the analog input, based on the AD8138 differential amplifier, is included in the layout of the AD9214 evaluation board. This portion of the evaluation circuit is not populated when the board is manufactured, but can be easily be added by the user. Resistors R5, R16, R18, and R25 are the feedback network that sets the gain of the AD8138. Resistors R23 and R24 set the common-mode voltage at the output of the op amp. Resistors R27 and R28, and capacitor C15, form a low-pass filter at the output of the AD8138, limiting its noise contribution into the AD9214.

Once the drive circuit is populated, the user should remove the jumper block normally between E40 and E38, and place it between E40 and E41. This will ac-couple the analog input signal from SMB connector J1 to the AD8138 drive circuit. The user will also need to remove the jumper blocks that normally connect E39 to E10 and E1 to E3 to remove transformer T1 from the circuit.

DAC Reconstruction Circuit

The data available at output connector U2 is also reconstructed by DAC U11, the AD9752. This 12-bit, high-speed digital-to-analog converter is included as a tool in setting up and debugging the evaluation board. It should not be used to measure the performance of the AD9214, as its performance will not accurately reflect the performance of the ADC. The DAC's output, available at J2, will drive 50 Ω . The user can add a jumper block between E8 and E9 to activate the SLEEP function of the DAC.

SCHEMATIC

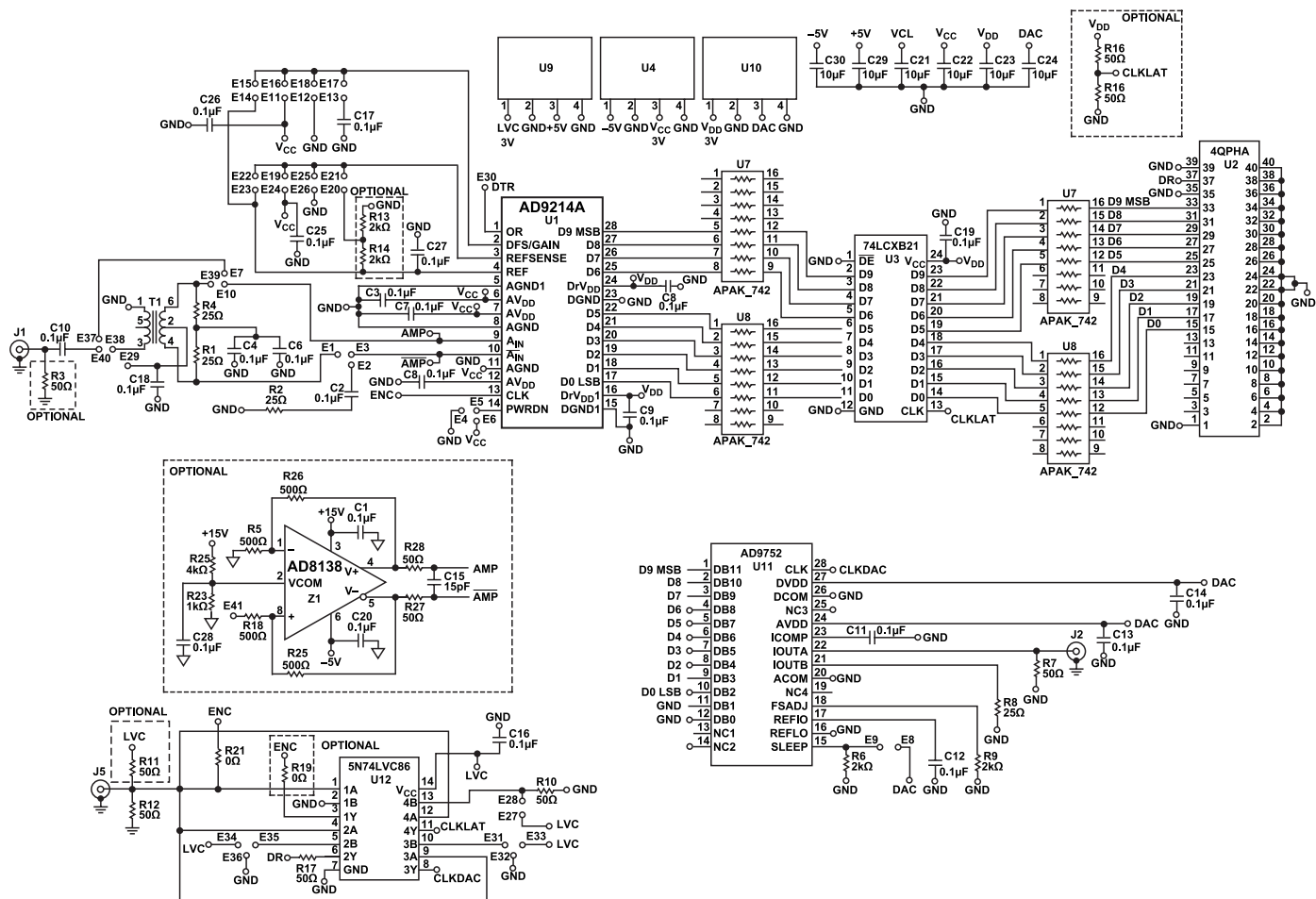


Figure 30. PCB Schematic

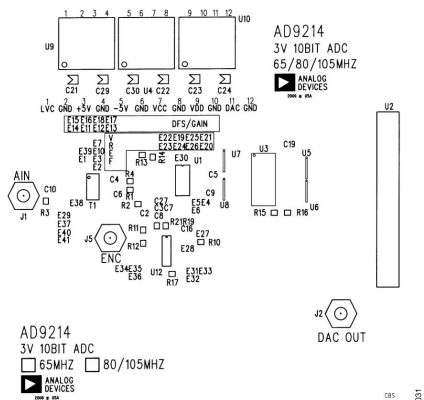


Figure 31. PCB Top Side Silkscreen

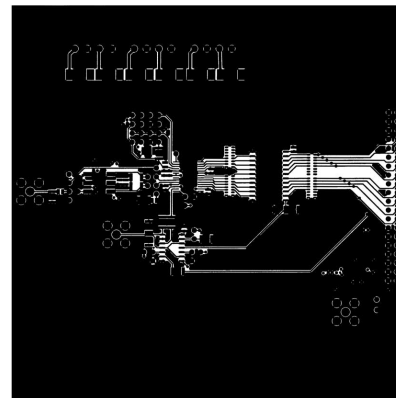


Figure 32. PCB Top Side Copper

SCHEMATIC

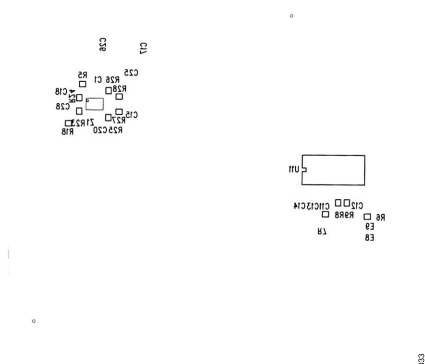


Figure 33. PCB Bottom Side Silkscreen

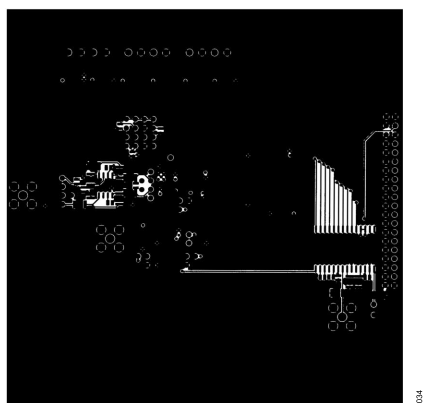


Figure 34. PCB Bottom Side Copper

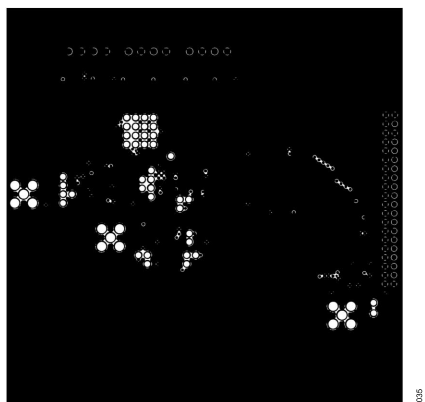


Figure 35. PCB Ground Layer—Layer TBD

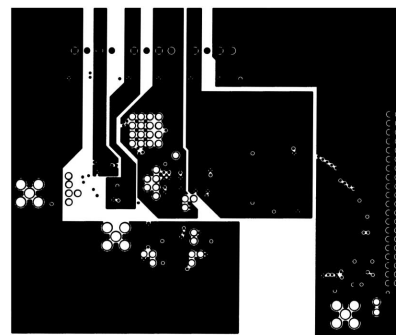


Figure 36. PCB Power Layers—Layers 3 and 4

SCHEMATIC

Table 11. AD9214/PCB Bill of Material

Number	Quantity	Reference Designator	Device	Package	Value
1	1	N/A	PCB		
2	19	C1 to C3, C5 to C14, C16 to C20, C25 to C28	Capacitor	603	0.1 μ F
3	4	C21 to C24	Capacitor	CAPTAJD	10 μ F
4	11	C4	Capacitor	603	0.01 μ F
5	4	R1, R2, R4, R8	Resistor	1206	25 Ω
6	4	R7, R10, R12, R17	Resistor	1206	50 Ω
7	4	U5 to U8	Resistor	RPAK_742	100 Ω
8	1	R21	Resistor	1206	0 Ω
9	2	R6, R9	Resistor	1206	2000 Ω
10	37	E1 to E6, E8 to E9, E11 to E27, E29, E31 to E41	Test Points Jumper Connections		TSW-120-07-G-S SMT-100-BK-G
11	3	J1, J2, J5	Connector	SMB	51-52-220
12	1	U12	Clock Chip	SOIC	SN74LVC86
13	1	U11	DAC	SOIC	AD9752
14	1	U3	Latch	SOIC	74LCX821
15	1	U1	ADC/DUT	SOIC	AD9214
16	1	U2	40-Pin Header		Samtec TSW-120-07-G-D
17	1	T1	Transformer		Mini Circuits ADT1-1WT
18	3	U4, U9, U10	Power Strip Power Connector		Newark 95F5966 25.602.5453.0
19 ¹	3	C1, C20, C28	Capacitor	603	0.1 μ F
20 ¹	2	C30, C29	Capacitor	CAPTAJD	10 μ F
21 ¹	1	C15	Capacitor	603	15 pF
22 ¹	4	R5, R18, R25, R26	Resistor	1206	500 Ω
23 ¹	1	R23	Resistor	1206	1 k Ω
24 ¹	1	R24	Resistor	1206	4 k Ω
25 ¹	3	R11, R15, R16	Resistor	1206	User Select
26 ¹	2	R13, R14	Resistor	1206	N/A
27 ¹	3	R27, R28, R3	Resistor	1206	50 Ω
28 ¹	1	R19	Resistor	1206	0 Ω
29 ¹	1	Z1	Op Amp	SOIC	AD8138

¹ This item is included in the PCB design, but is omitted at assembly.

OUTLINE DIMENSIONS

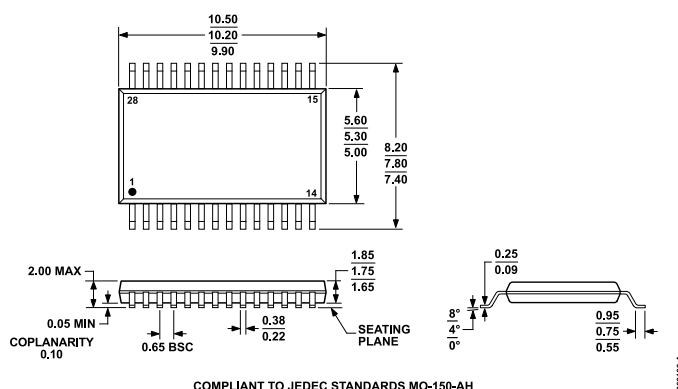


Figure 37. 28-Lead Shrink Small Outline Package (RS-28)
 Dimensions shown in inches and millimeters

Updated: April 05, 2022

ORDERING GUIDE

Model ¹	Temperature Range	Package Description	Packing Quantity	Package Option
AD9214BRSZ-105	-40°C to +85°C	28-Lead SSOP	Tube	RS-28
AD9214BRSZ-65	-40°C to +85°C	28-Lead SSOP	Tube	RS-28
AD9214BRSZ-80	-40°C to +85°C	28-Lead SSOP	Tube	RS-28
AD9214BRSZ-RL105	-40°C to +85°C	28-Lead SSOP	Reel, 1500	RS-28
AD9214BRSZ-RL65	-40°C to +85°C	28-Lead SSOP	Reel, 1500	RS-28
AD9214BRSZ-RL80	-40°C to +85°C	28-Lead SSOP	Reel, 1500	RS-28

¹ Z = RoHS Compliant Part.

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