High Performance, Low Power, Rail-to-Rail Precision Instrumentation Amplifier

FEATURES

- Low power: 368 μA maximum quiescent current
- Rail-to-rail output
- Low noise and distortion
  - 8 nV/√Hz maximum input voltage noise at 1 kHz
  - 0.15 μV p-p RTI noise (G = 100)
  - 0.5 ppm nonlinearity with 2 kΩ load (G = 1)
- Excellent ac specifications
  - 80 dB minimum CMRR at 10 kHz (G = 1)
  - 2.2 MHz bandwidth (G = 1)
- High precision dc performance (AD8422BRZ)
  - 150 dB minimum CMRR (G = 1000)
  - 0.04% maximum gain error (G = 1000)
  - 0.3 μV/°C maximum input offset drift
  - 0.5 nA maximum input bias current
- Wide supply range
  - 4.6 V to 36 V single supply
  - ±2.3 V to ±18 V dual supply
- Input overvoltage protection: 40 V from opposite supply
- Gain range: 1 to 1000
- Available in 8-lead LFCSP, 8-lead MSOP, and 8-lead SOIC_N

APPLICATIONS

- Medical instrumentation
- Industrial process controls
- Strain gages
- Transducer interfaces
- Precision data acquisition systems
- Channel-isolated systems
- Portable instrumentation

TYPICAL APPLICATION DIAGRAM

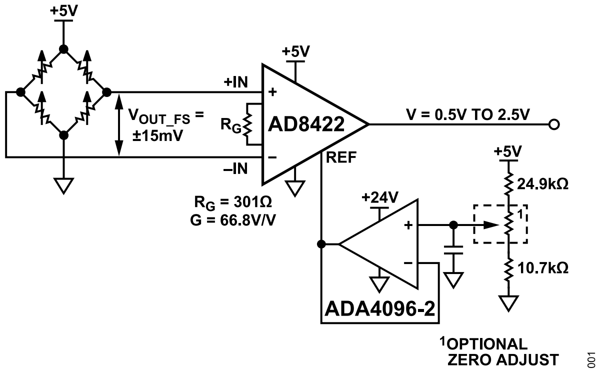

Figure 1. Bridge Amplifier with Output Zero Adjust

GENERAL DESCRIPTION

The AD8422 is a high precision, low power, low noise, rail-to-rail instrumentation amplifier that delivers the best performance per unit microampere in the industry. The AD8422 processes signals with ultralow distortion performance that is load independent over its full output range.

The AD8422 is the third generation development of the industry-standard AD620. The AD8422 employs new process technologies and design techniques to achieve higher dynamic range and lower errors than its predecessors, while consuming less than one-third of the power. The AD8422 uses the high performance pinout introduced by the AD8221.

Very low bias current makes the AD8422 error free with high source impedance, allowing multiple sensors to be multiplexed to the inputs. Low voltage noise and low current noise make the AD8422 an ideal choice for measuring a Wheatstone bridge.

The wide input range and rail-to-rail output of the AD8422 bring all of the benefits of a high performance in-amp to single-supply applications. Whether using high or low supply voltages, the power savings make the AD8422 an excellent choice for high channel count or power sensitive applications.

The AD8422 uses robust input protection that ensures reliability without sacrificing noise performance. The AD8422 has high ESD immunity, and the inputs are protected from continuous voltages up to 40 V from the opposite supply rail.

A single resistor sets the gain from 1 to 1000. The reference pin can be used to apply a precise offset to the output voltage.

The AD8422 is specified from −40°C to +85°C for the 8-lead MSOP and the 8-lead SOIC_N and from −40°C to +125°C for the 8-lead LFCSP.

Rev. C

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REVISION HISTORY

11/2022—Rev. B to Rev. C

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SPECIFICATIONS

SOIC_N

V_S = ±15 V, V_{REF} = 0 V, V_{+IN} = 0 V, V_{-IN} = 0 V, T_A = 25°C, G = 1, and R_L = 2 kΩ, unless otherwise noted.

Table 1.

Parameter	Test Conditions/ Comments	AD8422ARZ			AD8422BRZ			Unit
		Min	Typ	Max	Min	Typ	Max	
COMMON-MODE REJECTION RATIO								
CMRR DC to 60 Hz with 1 kΩ Source Imbalance	V_{CM} = −10 V to +10 V							
G = 1		86			94			dB
G = 10		106			114			dB
G = 100		126			134			dB
G = 1000		146			150			dB
Over Temperature, G = 1	T = −40°C to +85°C	83			89			dB
CMRR at 10 kHz	V_{CM} = −10 V to +10 V							
G = 1		80			80			dB
G = 10		90			95			dB
G = 100		100			100			dB
G = 1000		100			100			dB
NOISE[1]								
Voltage Noise, 1 kHz								
Input Voltage Noise, e_{NI}	V_{IN+}, V_{IN-}, V_{REF} = 0 V			8			8	nV/√Hz
Output Voltage Noise, e_{NO}			80			80		nV/√Hz
Peak to Peak, RTI	f = 0.1 Hz to 10 Hz							
G = 1			2			2		µV p-p
G = 10			0.5			0.5		µV p-p
G = 100 to 1000			0.15			0.15		µV p-p
Current Noise	f = 1 kHz		90			90	110	fA/√Hz
	f = 0.1 Hz to 10 Hz		8			8		pA p-p
VOLTAGE OFFSET[2]								
Input Offset, V_{OSI}	V_S = ±2.3 V to ±15 V			60			25	µV
Over Temperature	T = −40°C to +85°C			70			40	µV
Average Temperature Coefficient				0.4			0.3	µV/°C
Output Offset, V_{OSO}	V_S = ±2.3 V to ±15 V			300			150	µV
Over Temperature	T = −40°C to +85°C			500			300	µV
Average Temperature Coefficient				5			2	µV/°C
Offset RTI vs. Supply (PSR)	V_S = ±2.3 V to ±18 V							
G = 1		90	110		100	120		dB
G = 10		110	130		120	140		dB
G = 100		124	150		140	160		dB
G = 1000		130	150		140	160		dB
INPUT CURRENT								
Input Bias Current	V_S = ±2.3 V to ±15 V		0.5	1		0.2	0.5	nA
Over Temperature	T = −40°C to +85°C			2			1	nA
Average Temperature Coefficient			4			4		pA/°C
Input Offset Current	V_S = ±2.3 V to ±15 V		0.2	0.3		0.1	0.15	nA
Over Temperature	T = −40°C to +85°C			0.8			0.3	nA
Average Temperature Coefficient			1			1		pA/°C
REFERENCE INPUT								

SPECIFICATIONS

Table 1. (Continued)

Parameter	Test Conditions/ Comments	AD8422ARZ			AD8422BRZ			Unit
		Min	Typ	Max	Min	Typ	Max	
R_{IN}			20			20		kΩ
I_{IN}	V_{IN+}, V_{IN-}, V_{REF} = 0 V		35	50		35	50	µA
Voltage Range		$-V_S$		$+V_S$	$-V_S$		$+V_S$	V
Gain to Output			1			1		V/V
DYNAMIC RESPONSE								
Small Signal −3 dB Bandwidth								
G = 1			2200			2200		kHz
G = 10			850			850		kHz
G = 100			120			120		kHz
G = 1000			12			12		kHz
Settling Time 0.01%	10 V step							
G = 1			13			13		µs
G = 10			13			13		µs
G = 100			12			12		µs
G = 1000			80			80		µs
Settling Time 0.001%	10 V step							
G = 1			15			15		µs
G = 10			15			15		µs
G = 100			15			15		µs
G = 1000			160			160		µs
Slew Rate	G = 1 to 100	0.8			0.8			V/µs
GAIN[3]	G = 1 + (19.8 kΩ/R_G)							
Gain Range		1		1000	1		1000	V/V
Gain Error	V_{OUT} ± 10 V							
G = 1				0.03			0.01	%
G = 10				0.2			0.04	%
G = 100				0.2			0.04	%
G = 1000				0.2			0.04	%
Gain Nonlinearity	V_{OUT} = −10 V to +10 V							
G = 1	R_L = 2 kΩ		0.5	5		0.5	5	ppm
G = 10			2	5		2	5	ppm
G = 100			4	10		4	10	ppm
G = 1000			10	20		10	20	ppm
Gain vs. Temperature								
G = 1				5			1	ppm/°C
G > 1				−80			–80	ppm/°C
INPUT								
Input Impedance								
Differential			200||2			200||2		GΩ||pF
Common Mode			200||2			200||2		GΩ||pF
Input Operating Voltage Range[4, 5]	V_S = ±2.3 V to ±18 V	$-V_S + 1.2$		$+V_S - 1.5$	$-V_S + 1.2$		$+V_S - 1.5$	V
Over Temperature	T = −40°C to +85°C	$-V_S + 1.2$		$+V_S - 1.5$	$-V_S + 1.2$		$+V_S - 1.5$	V
OUTPUT								
Output Swing, R_L = 10 kΩ	V_S = ±15 V	$-V_S + 0.2$		$+V_S - 0.2$	$-V_S + 0.2$		$+V_S - 0.2$	V
Over Temperature	T = −40°C to +85°C	$-V_S + 0.25$		$+V_S - 0.25$	$-V_S + 0.25$		$+V_S - 0.25$	V
Output Swing, R_L = 10 kΩ	V_S = ±2.3 V	$-V_S + 0.12$		$+V_S - 0.12$	$-V_S + 0.12$		$+V_S - 0.12$	V
Over Temperature	T = −40°C to +85°C	$-V_S + 0.13$		$+V_S - 0.13$	$-V_S + 0.13$		$+V_S - 0.13$	V

SPECIFICATIONS

Table 1. (Continued)

Parameter	Test Conditions/ Comments	AD8422ARZ			AD8422BRZ			Unit
		Min	Typ	Max	Min	Typ	Max	
Output Swing, R_L = 2 kΩ	V_S = ±15 V	$-V_S + 0.25$		$+V_S - 0.25$	$-V_S + 0.25$		$+V_S - 0.25$	V
Over Temperature[6]	T = −40°C to +85°C	$-V_S + 0.3$		$+V_S - 1.4$	$-V_S + 0.3$		$+V_S - 1.4$	V
Output Swing, R_L = 2 kΩ	V_S = ±2.3 V	$-V_S + 0.16$		$+V_S - 0.16$	$-V_S + 0.16$		$+V_S - 0.16$	V
Over Temperature	T = −40°C to +85°C	$-V_S + 0.2$		$+V_S - 0.2$	$-V_S + 0.2$		$+V_S - 0.2$	V
Short-Circuit Current			20			20		mA
POWER SUPPLY								
Operating Range	Dual-supply operation	±2.3		±18	±2.3		±18	V
	Single-supply operation	4.6		36	4.6		36	V
Quiescent Current			338	368		338	368	µA
Over Temperature	T = −40°C to +85°C			400			400	µA
TEMPERATURE RANGE								
Specified Performance		–40		+85	–40		+85	°C
Operating Range[7]		–40		+125	–40		+125	°C

[1] Total RTI noise = $\sqrt{(e_{NI}^2 + (e_{NO}/G)^2)}$.

[2] Total RTI V_{OS} = $(V_{OSI}) + (V_{OSO}/G)$.

[3] Gain does not include the effects of the external resistor, R_G.

[4] One input grounded. G = 1.

[5] Only specified to guarantee linear output voltage. If linear bias current is required, use the following voltage range: $-V_S + 2$ V to $+V_S - 2.2$ V. See Figure 19 and Figure 20.

[6] Output current limited at cold temperatures. See Figure 34.

[7] See Typical Performance Characteristics for expected operation between 85°C and 125°C.

MSOP

V_S = ±15 V, V_{REF} = 0 V, V_{+IN} = 0 V, V_{-IN} = 0 V, T_A = 25°C, G = 1, and R_L = 2 kΩ, unless otherwise noted.

Table 2.

Parameter	Test Conditions/ Comments	AD8422ARMZ			AD8422BRMZ			Unit
		Min	Typ	Max	Min	Typ	Max	
COMMON-MODE REJECTION RATIO								
CMRR DC to 60 Hz with 1 kΩ Source Imbalance	V_{CM} = −10 V to +10 V							
G = 1		86			90			dB
G = 10		106			110			dB
G = 100		126			130			dB
G = 1000		146			150			dB
Over Temperature, G = 1	T = −40°C to +85°C	83			86			
CMRR at 10 kHz	V_{CM} = −10 V to +10 V							
G = 1		80			80			dB
G = 10		90			95			dB
G = 100		100			100			dB
G = 1000		100			100			dB
NOISE[1]								
Voltage Noise, 1 kHz								
Input Voltage Noise, e_{NI}	V_{IN+}, V_{IN-}, V_{REF} = 0 V			8			8	nV/√Hz
Output Voltage Noise, e_{NO}			80			80		nV/√Hz
Peak to Peak, RTI	f = 0.1 Hz to 10 Hz							

SPECIFICATIONS

Table 2. (Continued)

Parameter	Test Conditions/ Comments	AD8422ARMZ Min	AD8422ARMZ Typ	AD8422ARMZ Max	AD8422BRMZ Min	AD8422BRMZ Typ	AD8422BRMZ Max	Unit
G = 1			2			2		μV p-p
G = 10			0.5			0.5		μV p-p
G = 100 to 1000			0.15			0.15		μV p-p
Current Noise	f = 1 kHz		90			90	110	fA/√Hz
	f = 0.1 Hz to 10 Hz		8			8		pA p-p
VOLTAGE OFFSET[2]								
Input Offset, V_{OSI}	V_S = ±2.3 V to ±15 V			70			50	μV
Over Temperature	T = −40°C to +85°C			110			75	μV
Average Temperature Coefficient				0.6			0.4	μV/°C
Output Offset, V_{OSO}	V_S = ±2.3 V to ±15 V			300			150	μV
Over Temperature	T = −40°C to +85°C			500			300	μV
Average Temperature Coefficient				5			2	μV/°C
Offset RTI vs. Supply (PSR)	V_S = ±2.3 V to ±18 V							
G = 1		90	110		100	120		dB
G = 10		110	130		120	140		dB
G = 100		124	150		140	160		dB
G = 1000		130	150		140	160		dB
INPUT CURRENT								
Input Bias Current	V_S = ±2.3 V to ±15 V		0.5	1		0.2	0.5	nA
Over Temperature	T = −40°C to +85°C			2			1	nA
Average Temperature Coefficient			4			4		pA/°C
Input Offset Current	V_S = ±2.3 V to ±15 V		0.2	0.3		0.1	0.15	nA
Over Temperature	T = −40°C to +85°C			0.8			0.3	nA
Average Temperature Coefficient			1			1		pA/°C
REFERENCE INPUT								
R_{IN}			20			20		kΩ
I_{IN}	V_{IN+}, V_{IN-}, V_{REF} = 0 V		35	50		35	50	μA
Voltage Range		$-V_S$		$+V_S$	$-V_S$		$+V_S$	V
Gain to Output			1			1		V/V
DYNAMIC RESPONSE								
Small Signal −3 dB Bandwidth								
G = 1			2200			2200		kHz
G = 10			850			850		kHz
G = 100			120			120		kHz
G = 1000			12			12		kHz
Settling Time 0.01%	10 V step							
G = 1			13			13		μs
G = 10			13			13		μs
G = 100			12			12		μs
G = 1000			80			80		μs
Settling Time 0.001%	10 V step							
G = 1			15			15		μs
G = 10			15			15		μs
G = 100			15			15		μs
G = 1000			160			160		μs
Slew Rate	G = 1 to 100	0.8			0.8			V/μs
GAIN[3]	G = 1 + (19.8 kΩ/R_G)							

SPECIFICATIONS

Table 2. (Continued)

Parameter	Test Conditions/ Comments	AD8422ARMZ			AD8422BRMZ			Unit
		Min	Typ	Max	Min	Typ	Max	
Gain Range		1		1000	1		1000	V/V
Gain Error	V_{OUT} ± 10 V							
G = 1				0.03			0.01	%
G = 10				0.2			0.04	%
G = 100				0.2			0.04	%
G = 1000				0.2			0.04	%
Gain Nonlinearity	$V_{OUT} = -10$ V to +10 V							
G = 1	R_L = 2 kΩ		0.5	5		0.5	5	ppm
G = 10			2	5		2	5	ppm
G = 100			4	10		4	10	ppm
G = 1000			10	20		10	20	ppm
Gain vs. Temperature								
G = 1				5			1	ppm/°C
G > 1				−80			−80	ppm/°C
INPUT								
Input Impedance								
Differential			200‖2			200‖2		GΩ‖pF
Common Mode			200‖2			200‖2		GΩ‖pF
Input Operating Voltage Range[4, 5]	V_S = ±2.3 V to ±18 V	$-V_S + 1.2$		$+V_S - 1.5$	$-V_S + 1.2$		$+V_S - 1.5$	V
Over Temperature	T = −40°C to +85°C	$-V_S + 1.2$		$+V_S - 1.5$	$-V_S + 1.2$		$+V_S - 1.5$	V
OUTPUT								
Output Swing, R_L = 10 kΩ	V_S = ±15 V	$-V_S + 0.2$		$+V_S - 0.2$	$-V_S + 0.2$		$+V_S - 0.2$	V
Over Temperature	T = −40°C to +85°C	$-V_S + 0.25$		$+V_S - 0.25$	$-V_S + 0.25$		$+V_S - 0.25$	V
Output Swing, R_L = 10 kΩ	V_S = ±2.3 V	$-V_S + 0.12$		$+V_S - 0.12$	$-V_S + 0.12$		$+V_S - 0.12$	V
Over Temperature	T = −40°C to +85°C	$-V_S + 0.13$		$+V_S - 0.13$	$-V_S + 0.13$		$+V_S - 0.13$	V
Output Swing, R_L = 2 kΩ	V_S = ±15 V	$-V_S + 0.25$		$+V_S - 0.25$	$-V_S + 0.25$		$+V_S - 0.25$	V
Over Temperature[6]	T = −40°C to +85°C	$-V_S + 0.3$		$+V_S - 1.4$	$-V_S + 0.3$		$+V_S - 1.4$	V
Output Swing, R_L = 2 kΩ	V_S = ±2.3 V	$-V_S + 0.16$		$+V_S - 0.16$	$-V_S + 0.16$		$+V_S - 0.16$	V
Over Temperature	T = −40°C to +85°C	$-V_S + 0.2$		$+V_S - 0.2$	$-V_S + 0.2$		$+V_S - 0.2$	V
Short-Circuit Current			20			20		mA
POWER SUPPLY								
Operating Range	Dual-supply operation	±2.3		±18	±2.3		±18	V
	Single-supply operation	4.6		36	4.6		36	V
Quiescent Current			338	368		338	368	µA
Over Temperature	T = −40°C to +85°C			400			400	µA
TEMPERATURE RANGE								
Specified Performance		−40		+85	−40		+85	°C
Operating Range[7]		−40		+125	−40		+125	°C

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[1] Total RTI Noise = $\sqrt{(e_{NI}^2 + (e_{NO}/G)^2)}$.

[2] Total RTI $V_{OS} = (V_{OSI}) + (V_{OSO}/G)$.

[3] Gain does not include the effects of the external resistor, R_G.

[4] One input grounded. G = 1.

[5] Only specified to guarantee linear output voltage. If linear bias current is required, use the following voltage range: $-V_S + 2$ V to $+V_S - 2.2$ V. See Figure 19 and Figure 20.

[6] Output current limited at cold temperatures. See Figure 34.

[7] See Typical Performance Characteristics for expected operation between 85°C and 125°C.

SPECIFICATIONS

LFCSP

V_S = ±15 V, V_{REF} = 0 V, V_{+IN} = 0 V, V_{-IN} = 0 V, T_A = 25°C, G = 1, and R_L = 2 kΩ, unless otherwise noted.

Table 3.

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
COMMON-MODE REJECTION RATIO					
CMRR DC to 60 Hz with 1 kΩ Source Imbalance	V_{CM} = −10 V to +10 V				
G = 1		86			dB
G = 10		106			dB
G = 100		126			dB
G = 1000		146			dB
Over Temperature, G = 1	T = −40°C to +125°C	83			
CMRR at 10 kHz	V_{CM} = −10 V to +10 V				
G = 1		80			dB
G = 10		90			dB
G = 100		100			dB
G = 1000		100			dB
NOISE[1]					
Voltage Noise, 1 kHz					
Input Voltage Noise, e_{NI}	V_{IN+}, V_{IN-}, V_{REF} = 0 V			8	nV/√Hz
Output Voltage Noise, e_{NO}			80		nV/√Hz
Peak to Peak, RTI	f = 0.1 Hz to 10 Hz				
G = 1			2		μV p-p
G = 10			0.5		μV p-p
G = 100 to 1000			0.15		μV p-p
Current Noise	f = 1 kHz		90		fA/√Hz
	f = 0.1 Hz to 10 Hz		8		pA p-p
VOLTAGE OFFSET[2]					
Input Offset, V_{OSI}	V_S = ±2.3 V to ±15 V			70	μV
Over Temperature	T = −40°C to +125°C			110	μV
Average Temperature Coefficient				0.9	μV/°C
Output Offset, V_{OSO}	V_S = ±2.3 V to ±15 V			300	μV
Over Temperature	T = −40°C to +125°C			500	μV
Average Temperature Coefficient				5	μV/°C
Offset RTI vs. Supply (PSR)	V_S = ±2.3 V to ±18 V				
G = 1		90	110		dB
G = 10		110	130		dB
G = 100		124	150		dB
G = 1000		130	150		dB
INPUT CURRENT					
Input Bias Current	V_S = ±2.3 V to ±15 V		0.5	1	nA
Over Temperature	T = −40°C to +125°C			2	nA
Average Temperature Coefficient			4		pA/°C
Input Offset Current	V_S = ±2.3 V to ±15 V		0.2	0.3	nA
Over Temperature	T = −40°C to +125°C			0.8	nA
Average Temperature Coefficient			1		pA/°C
REFERENCE INPUT					
R_{IN}			20		kΩ
I_{IN}	V_{IN+}, V_{IN-}, V_{REF} = 0 V		35	50	μA
Voltage Range		$-V_S$		$+V_S$	V

SPECIFICATIONS

Table 3. (Continued)

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
Gain to Output			1		V/V
DYNAMIC RESPONSE					
Small Signal −3 dB Bandwidth					
G = 1			2200		kHz
G = 10			850		kHz
G = 100			120		kHz
G = 1000			12		kHz
Settling Time 0.01%	10 V step				
G = 1			13		µs
G = 10			13		µs
G = 100			12		µs
G = 1000			80		µs
Settling Time 0.001%	10 V step				
G = 1			15		µs
G = 10			15		µs
G = 100			15		µs
G = 1000			160		µs
Slew Rate	G = 1 to 100	0.8			V/µs
GAIN[3]	G = 1 + (19.8 kΩ/R_G)				
Gain Range		1		1000	V/V
Gain Error	V_{OUT} ± 10 V				
G = 1				0.03	%
G = 10				0.2	%
G = 100				0.2	%
G = 1000				0.2	%
Gain Nonlinearity	V_{OUT} = −10 V to +10 V				
G = 1	R_L = 2 kΩ		0.5	5	ppm
G = 10			2	5	ppm
G = 100			4	10	ppm
G = 1000			10	20	ppm
Gain vs. Temperature	T = −40°C to +125°C				
G = 1				1	ppm/°C
G > 1				−80	ppm/°C
INPUT					
Input Impedance					
Differential			200||2		GΩ||pF
Common Mode			200||2		GΩ||pF
Input Operating Voltage Range[4, 5]	V_S = ±2.3 V to ±18 V	$-V_S + 1.2$		$+V_S - 1.5$	V
Over Temperature	T = −40°C to +125°C	$-V_S + 1.2$		$+V_S - 1.5$	V
OUTPUT					
Output Swing, R_L = 10 kΩ	V_S = ±15 V	$-V_S + 0.2$		$+V_S - 0.2$	V
Over Temperature	T = −40°C to +125°C	$-V_S + 0.28$		$+V_S - 0.28$	V
Output Swing, R_L = 10 kΩ	V_S = ±2.3 V	$-V_S + 0.12$		$+V_S - 0.12$	V
Over Temperature	T = −40°C to +125°C	$-V_S + 0.14$		$+V_S - 0.14$	V
Output Swing, R_L = 2 kΩ	V_S = ±15 V	$-V_S + 0.25$		$+V_S - 0.25$	V
Over Temperature[6]	T = −40°C to +125°C	$-V_S + 0.35$		$+V_S - 1.43$	V
Output Swing, R_L = 2 kΩ	V_S = ±2.3 V	$-V_S + 0.16$		$+V_S - 0.16$	V
Over Temperature	T = −40°C to +125°C	$-V_S + 0.21$		$+V_S - 0.21$	V

SPECIFICATIONS

Table 3. (Continued)

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
Short-Circuit Current			20		mA
POWER SUPPLY					
Operating Range	Dual-supply operation	±2.3		±18	V
	Single-supply operation	4.6		36	V
Quiescent Current			338	368	μA
Over Temperature	T = −40°C to +125°C			450	μA
TEMPERATURE RANGE					
Specified Performance		−40		+125	°C
Operating Range		−40		+125	°C

[1] Total RTI Noise = $\sqrt{(e_{NI}^2 + (e_{NO}/G)^2)}$.

[2] Total RTI V_{OS} = (V_{OSI}) + (V_{OSO}/G).

[3] Gain does not include the effects of the external resistor, R_G.

[4] One input grounded. G = 1.

[5] Only specified to guarantee linear output voltage. If linear bias current is required, use the following voltage range: $-V_S + 2$ V to $+V_S - 2.2$ V. See Figure 19 and Figure 20.

[6] Output current limited at cold temperatures. See Figure 34.

ABSOLUTE MAXIMUM RATINGS

Table 4.

Parameter	Rating
Supply Voltage	±2.3 V to ±18 V
Output Short-Circuit Current Duration	Indefinite
Maximum Voltage at −IN or +IN[1]	$-V_S + 40$ V
Minimum Voltage at −IN or +IN	$+V_S - 40$ V
Maximum Voltage at REF	$\pm V_S \pm 0.3$ V
Temperature	
Storage Range	−65°C to +150°C
Operating Range	−40°C to +125°C
Maximum Junction	150°C

[1] For voltages beyond these limits, use input protection resistors. See the Theory of Operation section for more information.

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

THERMAL RESISTANCE

Thermal performance is directly linked to printed circuit board (PCB) design and operating environment. Careful attention to PCB thermal design is required.

θ_{JA} is the junction to ambient thermal resistance, and θ_{JC} is the junction to case thermal resistance.

Table 5. Thermal Resistance

Package	θ_{JA}[1]	θ_{JC}	Unit
R-8	113	51	°C/W
RM-8	151	59	°C/W
CP-8-19	55	59	°C/W

[1] θ_{JA} is specified for a device in free air using a 4-layer JEDEC PCB.

ELECTROSTATIC DISCHARGE (ESD) RATINGS

The following ESD information is provided for handling of ESD-sensitive devices in an ESD-protected area only.

Human body model (HBM) per ESDA/JEDEC JS-001-2011.

Charged device model (CDM) per JESD22-C101.

Machine model (MM) per JESD22-A115. MM voltage values are for characterization only.

ESD Ratings for AD8422

Table 6. AD8422, 8-Lead SOIC_N, 8-Lead MSOP, and 8-Lead LFCSP

ESD Model	Withstand Threshold	Class
HBM	2.5 kV	2
CDM	1.25 kV	IV
MM	100 V	Not applicable

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATIONS AND FUNCTION DESCRIPTIONS

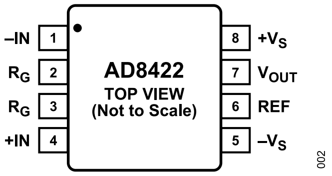
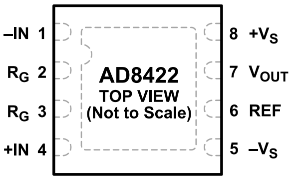


Figure 2. 8-Lead MSOP and 8-Lead SOIC_N Pin Configuration



NOTES
1. EXPOSED PAD. CONNECT THE EXPOSED PAD TO $–V_S$ OR LEAVE IT UNCONNECTED.

Figure 3. 8-Lead LFCSP Pin Configuration

Table 7. Pin Function Descriptions

Pin No.	Mnemonic	Description
1	−IN	Negative Input Terminal.
2, 3	R_G	Gain Setting Terminals. Place resistor across the R_G pins to set the gain. $G = 1 + (19.8\ k\Omega/R_G)$. Do not connect anything else to these pins. The minimum allowed value of R_G is 19.8 Ω.
4	+IN	Positive Input Terminal.
5	$−V_S$	Negative Power Supply Terminal.
6	REF	Reference Voltage Terminal. Drive this terminal with a low impedance voltage source to level shift the output.
7	V_{OUT}	Output Terminal.
8	$+V_S$	Positive Power Supply Terminal.
	EPAD	Exposed Pad. Connect the exposed pad to $−V_S$ or leave it unconnected.

TYPICAL PERFORMANCE CHARACTERISTICS

T = 25°C, V_S = ±15, V_{REF} = 0 V, R_L = 10 kΩ, unless otherwise noted.

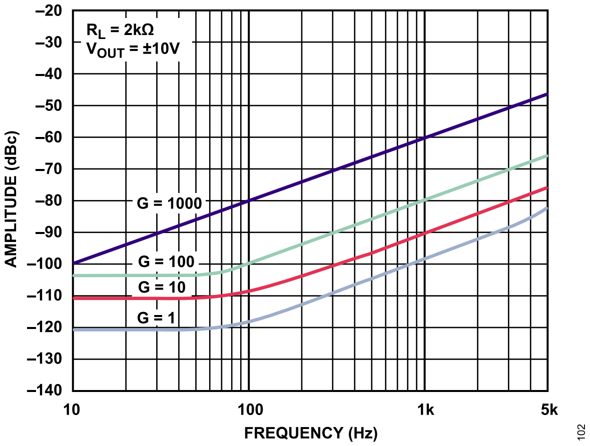


Figure 4. Total Harmonic Distortion vs. Frequency

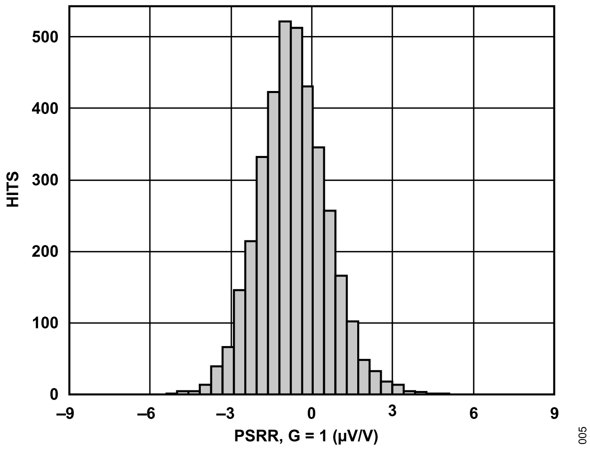


Figure 7. Typical Distribution of PSRR (G = 1)

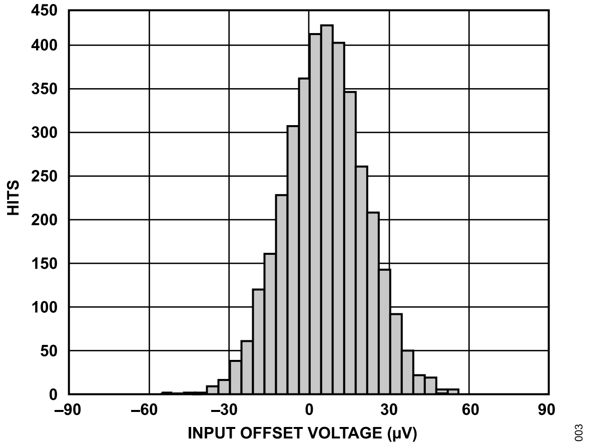


Figure 5. Typical Distribution of Input Offset Voltage

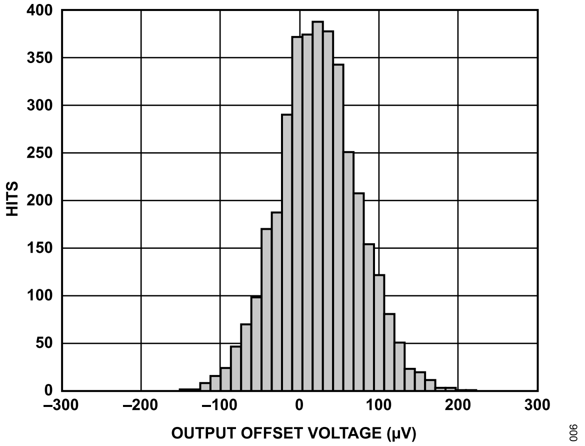


Figure 8. Typical Distribution of Output Offset Voltage

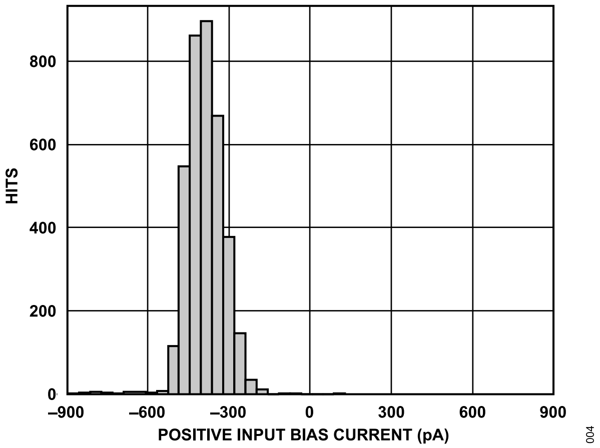


Figure 6. Typical Distribution of Input Bias Current

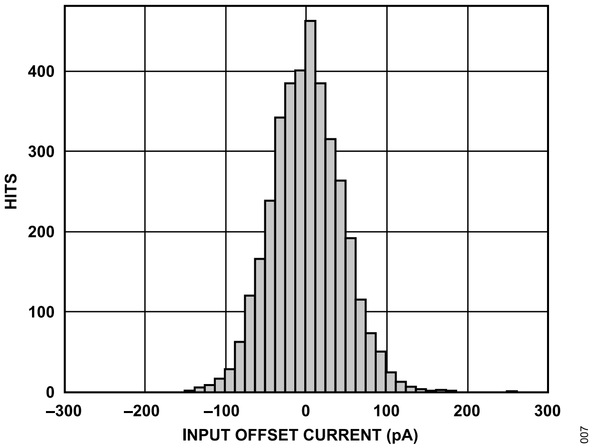


Figure 9. Typical Distribution of Input Offset Current

TYPICAL PERFORMANCE CHARACTERISTICS

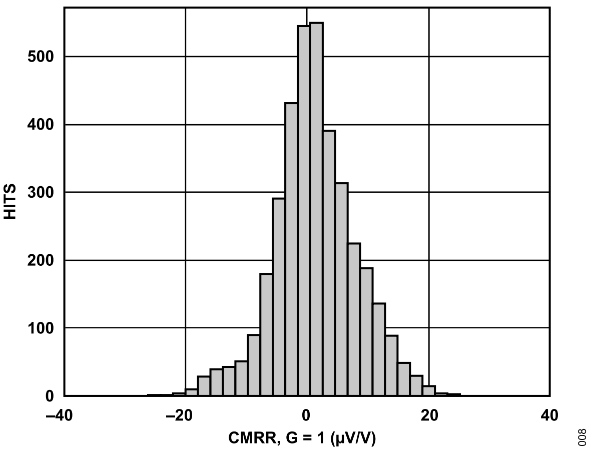


Figure 10. Typical Distribution of CMRR (G = 1)

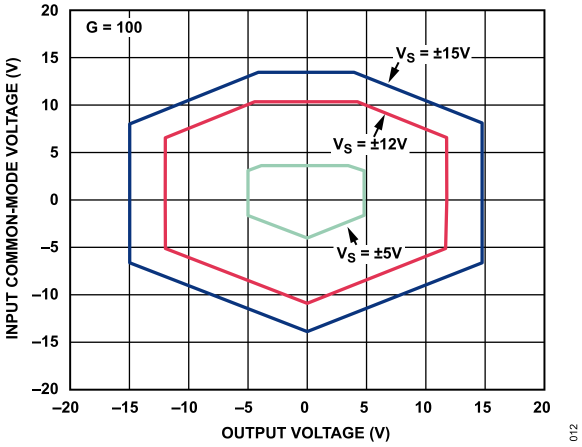


Figure 13. Input Common-Mode Voltage vs. Output Voltage (G = 100), V_S = ±15 V, V_S = ±12 V, V_S = ±5 V

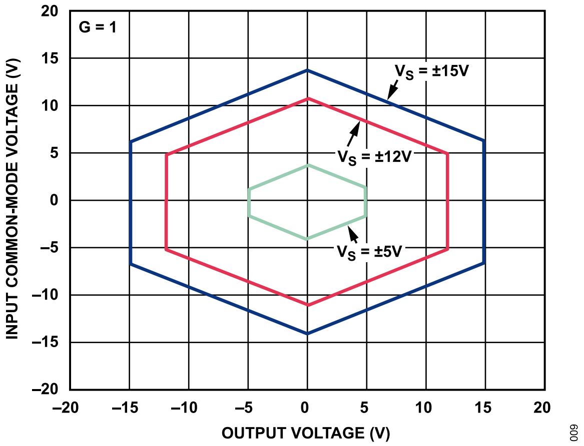


Figure 11. Input Common-Mode Voltage vs. Output Voltage (G = 1), V_S = ±15 V, V_S = ±12 V, V_S = ±5 V

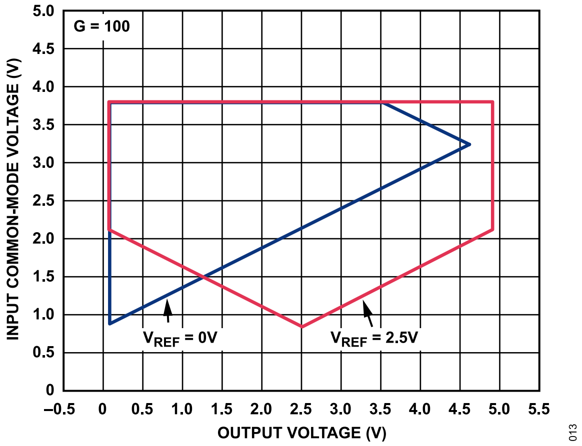


Figure 14. Input Common-Mode Voltage vs. Output Voltage (G = 100), Single-Supply, V_S = 5 V

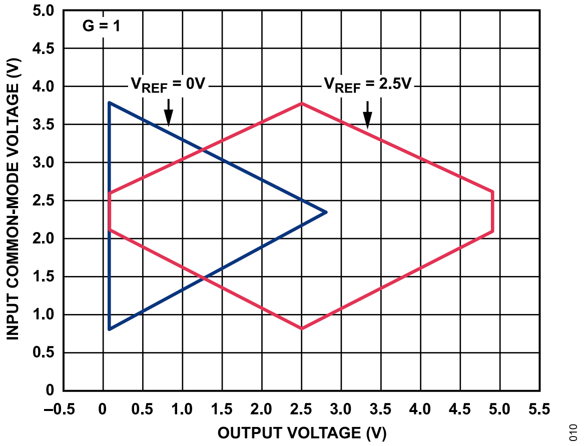


Figure 12. Input Common-Mode Voltage vs. Output Voltage (G = 1), Single-Supply, V_S = 5 V

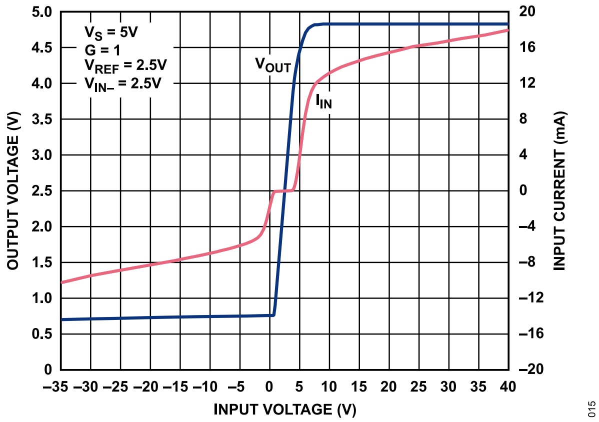


Figure 15. Input Overvoltage Performance; G = 1, V_S = 5 V

TYPICAL PERFORMANCE CHARACTERISTICS

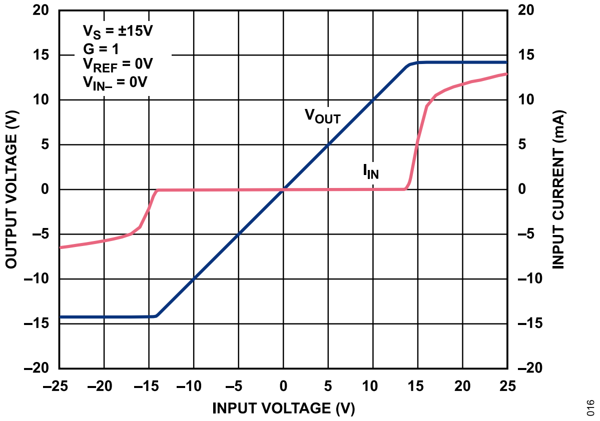


Figure 16. Input Overvoltage Performance; G = 1, V_S = ±15 V

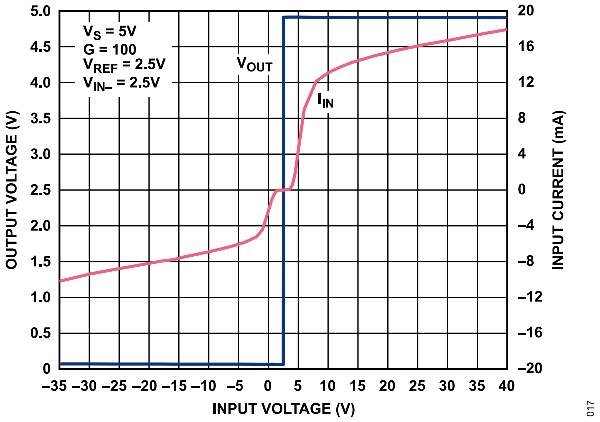


Figure 17. Input Overvoltage Performance; G = 100, V_S = 5 V

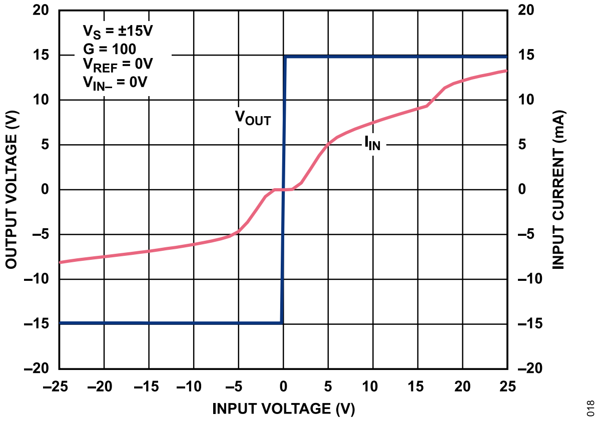


Figure 18. Input Overvoltage Performance; G = 100, V_S = ±15 V

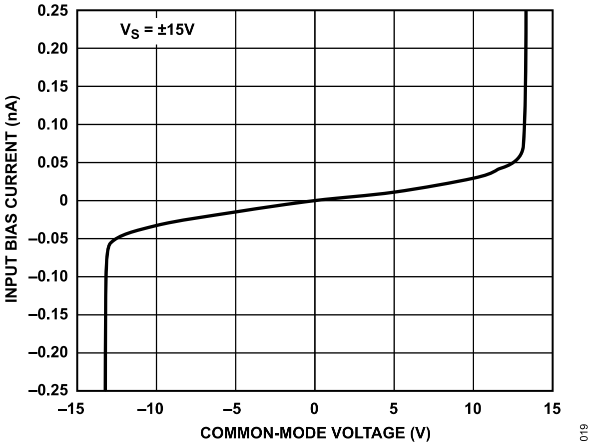


Figure 19. Input Bias Current vs. Common-Mode Voltage, V_S = ±15 V

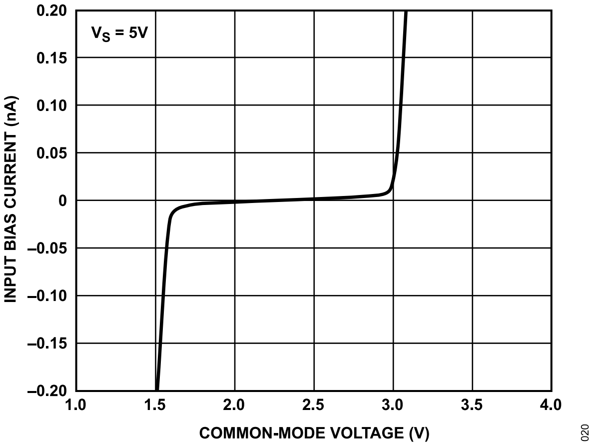


Figure 20. Input Bias Current vs. Common-Mode Voltage, V_S = 5 V

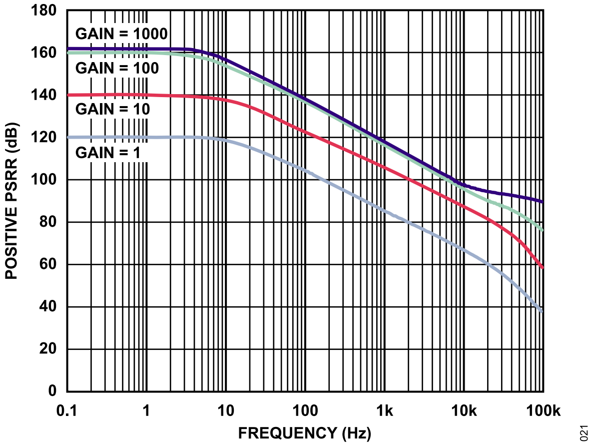


Figure 21. Positive PSRR vs. Frequency

TYPICAL PERFORMANCE CHARACTERISTICS

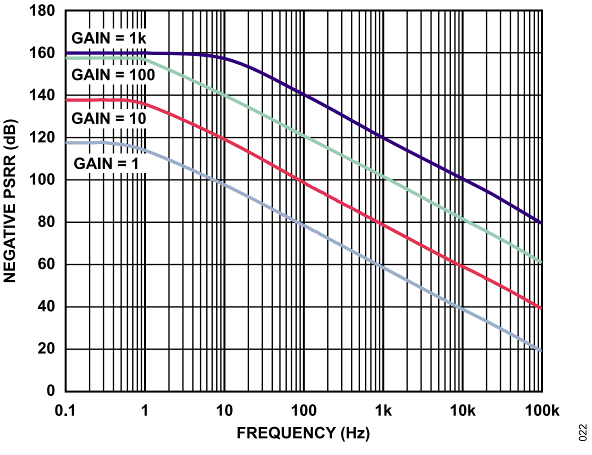


Figure 22. Negative PSRR vs. Frequency

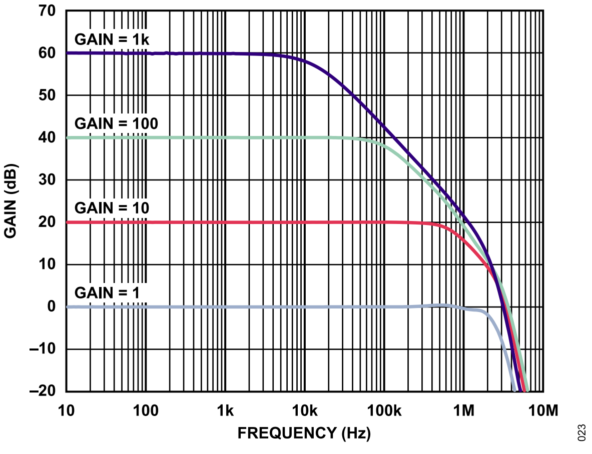


Figure 23. Gain vs. Frequency

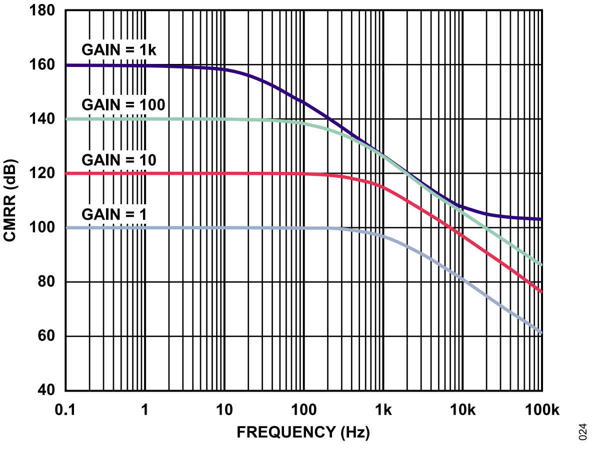


Figure 24. CMRR vs. Frequency

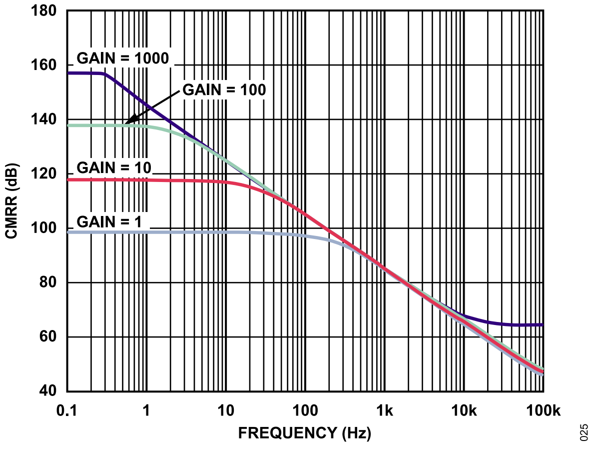


Figure 25. CMRR vs. Frequency, 1 kΩ Source Imbalance

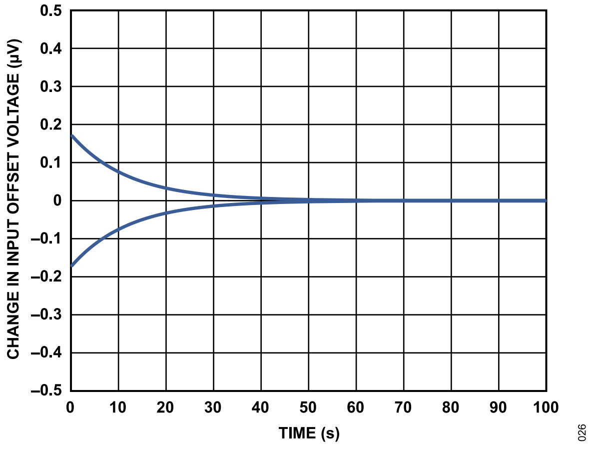


Figure 26. Change in Input Offset Voltage (V_{OSI}) vs. Warm-Up Time

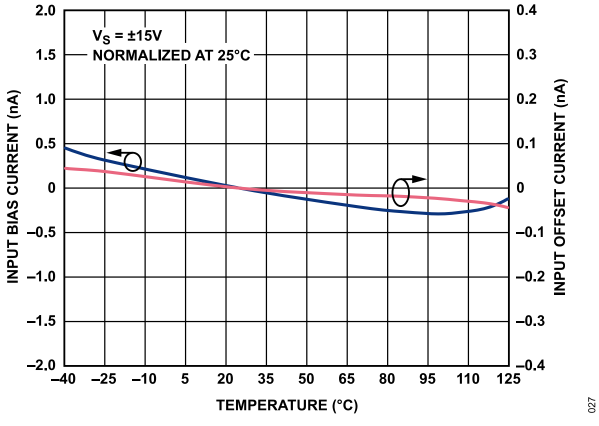


Figure 27. Input Bias Current and Input Offset Current vs. Temperature

TYPICAL PERFORMANCE CHARACTERISTICS

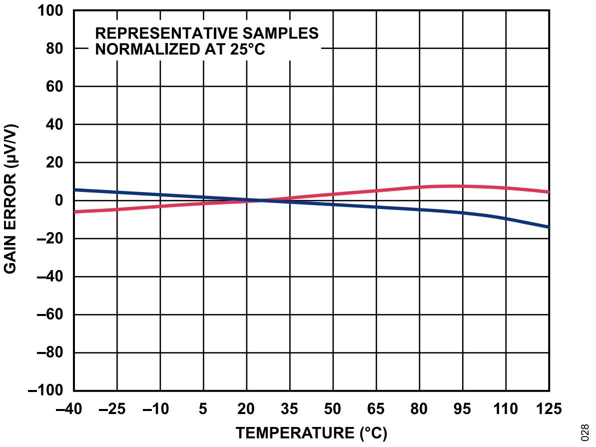


Figure 28. Gain vs. Temperature (G = 1)

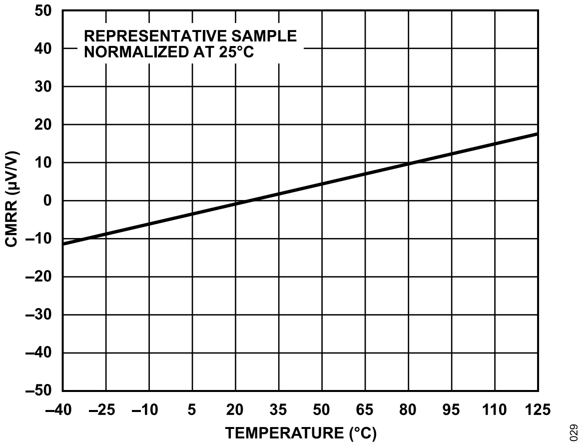


Figure 29. CMRR vs. Temperature (G = 1), Normalized at 25°C

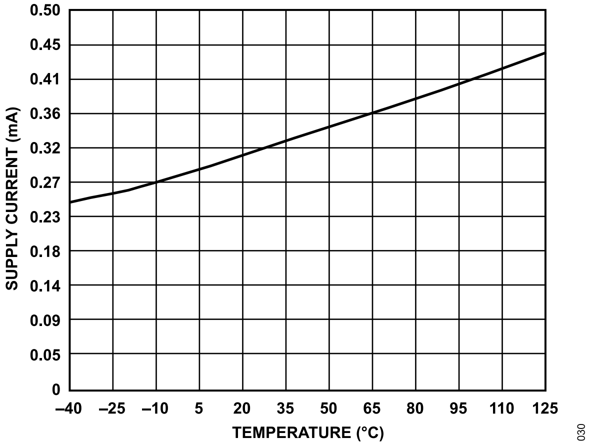


Figure 30. Supply Current vs. Temperature (G = 1)

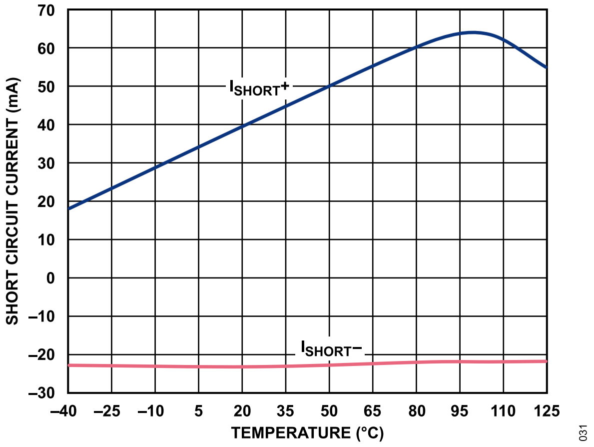


Figure 31. Short-Circuit Current vs. Temperature (G = 1)

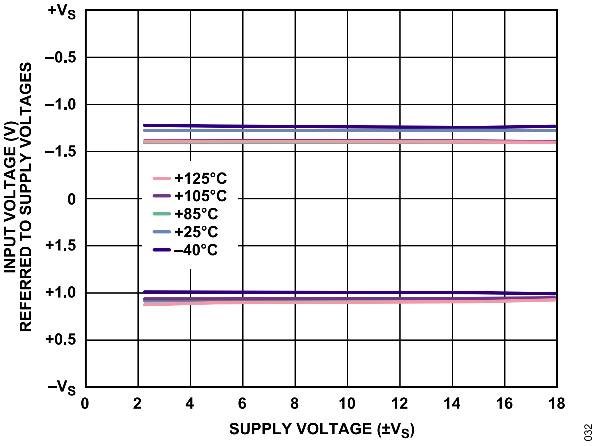


Figure 32. Input Voltage vs. Supply Voltage

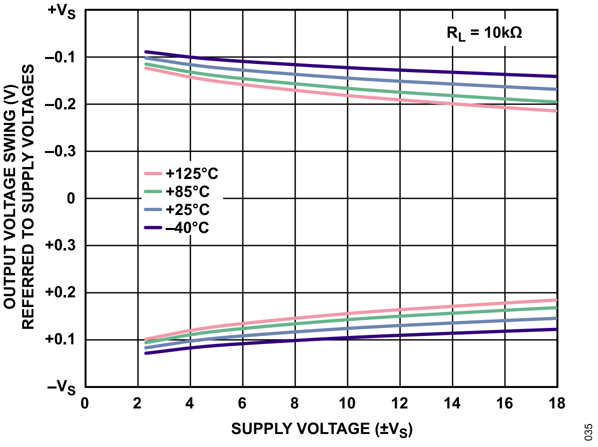


Figure 33. Output Voltage Swing vs. Supply Voltage, R_L = 10 kΩ

TYPICAL PERFORMANCE CHARACTERISTICS

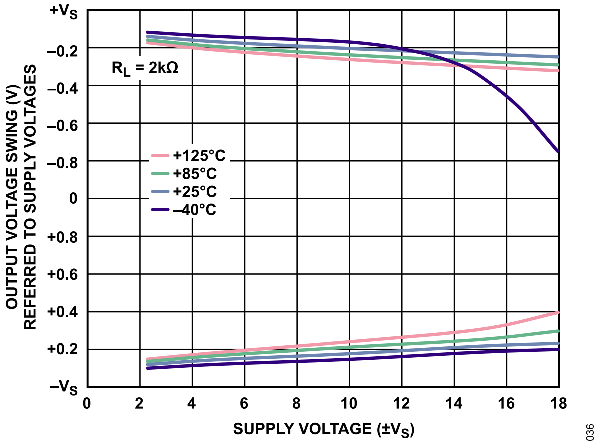


Figure 34. Output Voltage Swing vs. Supply Voltage, R_L = 2 kΩ

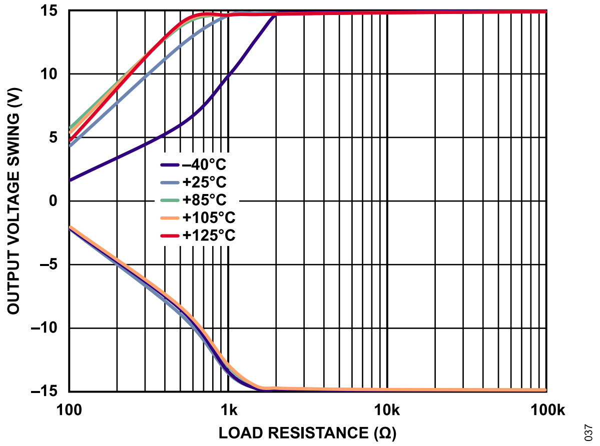


Figure 35. Output Voltage Swing vs. Load Resistance

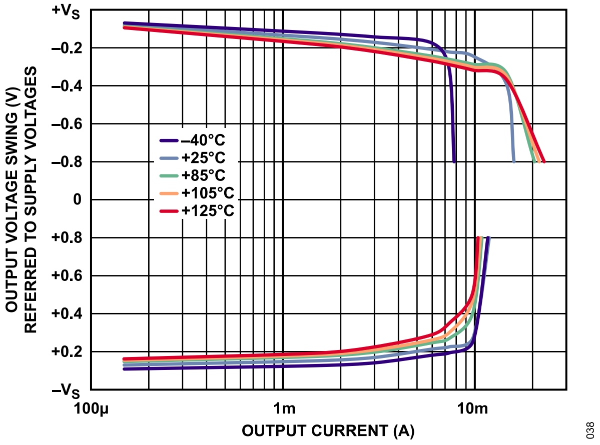


Figure 36. Output Voltage Swing vs. Output Current

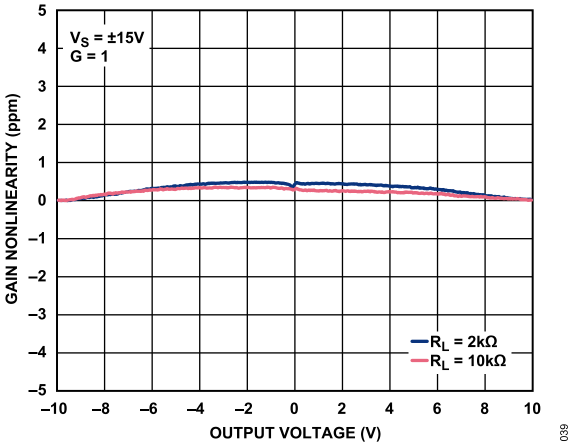


Figure 37. Gain Nonlinearity (G = 1)

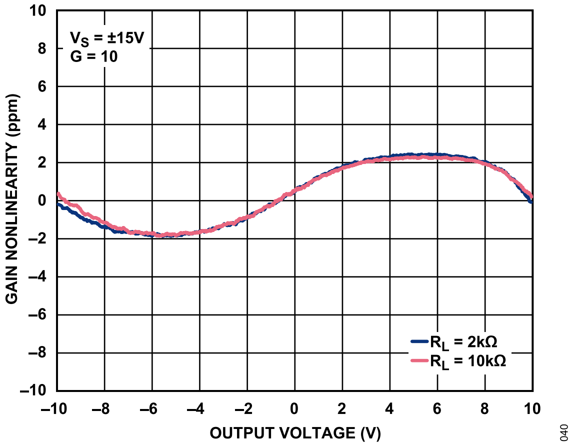


Figure 38. Gain Nonlinearity (G = 10)

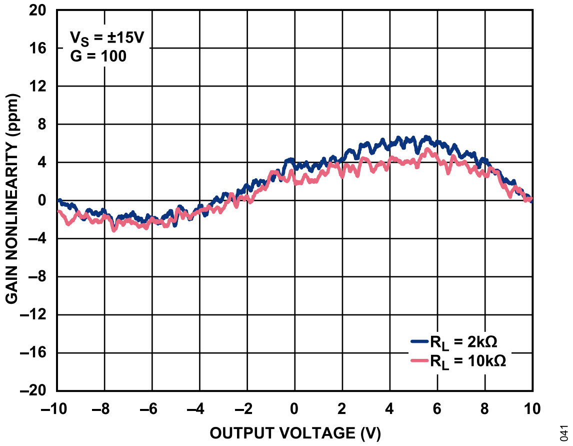


Figure 39. Gain Nonlinearity (G = 100)

TYPICAL PERFORMANCE CHARACTERISTICS

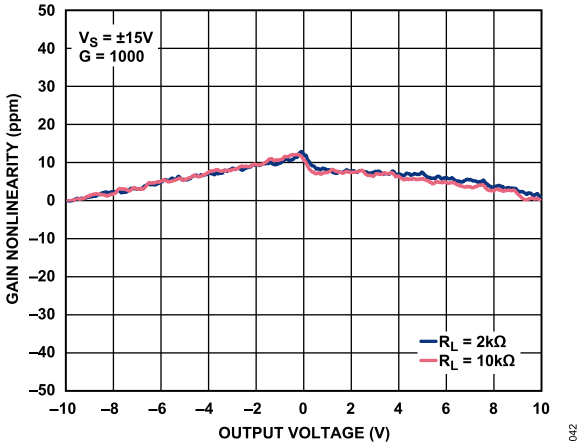


Figure 40. Gain Nonlinearity (G = 1000)

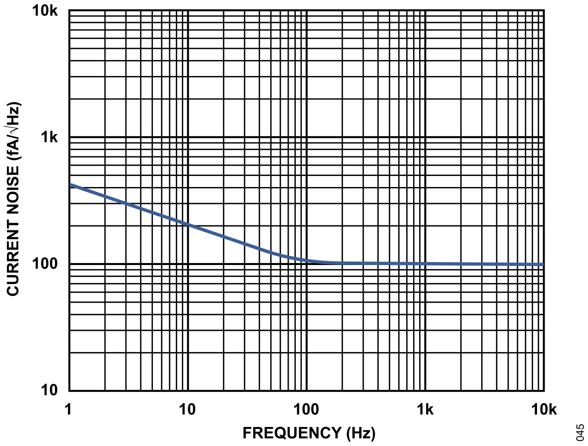


Figure 43. Current Noise Spectral Density vs. Frequency

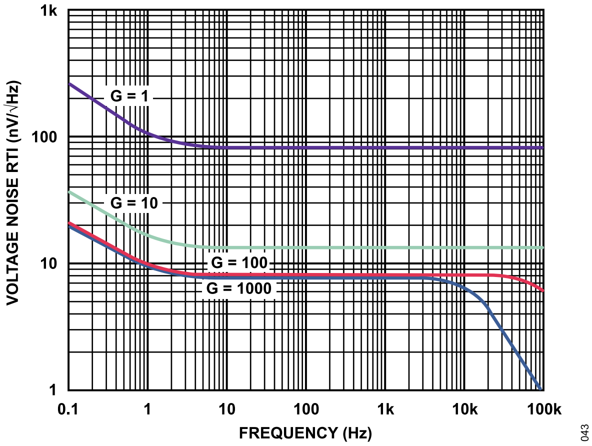


Figure 41. Voltage Noise Spectral Density vs. Frequency

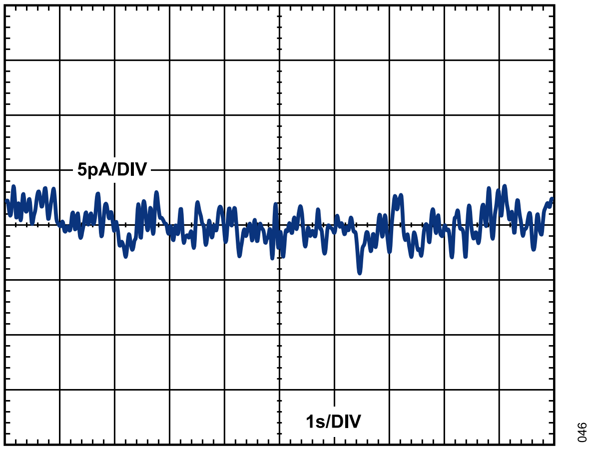


Figure 44. 0.1 Hz to 10 Hz Current Noise

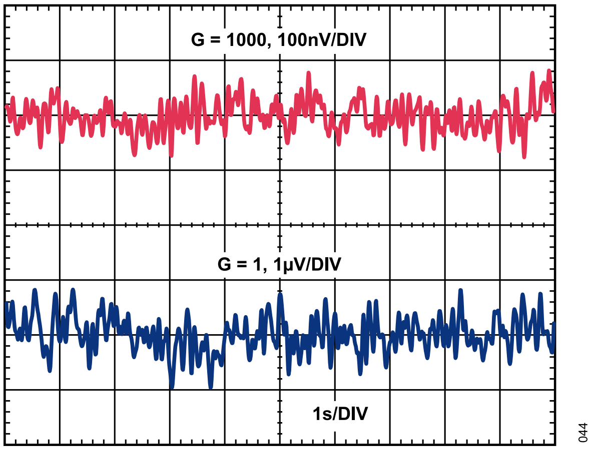


Figure 42. 0.1 Hz to 10 Hz RTI Voltage Noise (G = 1, G = 1000)

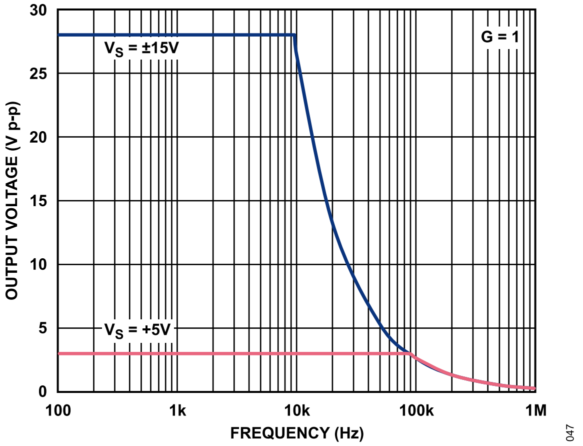


Figure 45. Large Signal Frequency Response

TYPICAL PERFORMANCE CHARACTERISTICS

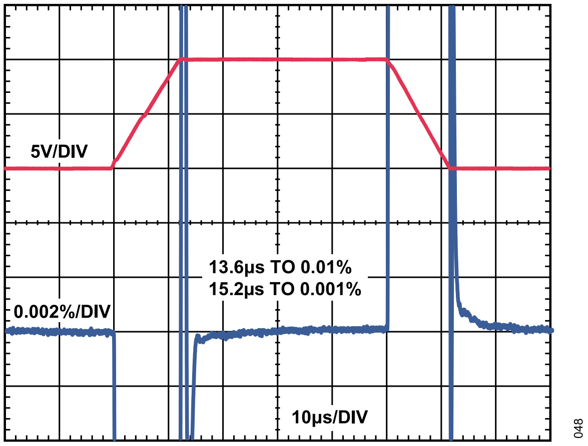


Figure 46. Large Signal Pulse Response and Settling Time (G = 1), 10 V Step, V_S = ±15 V, R_L = 2 kΩ, C_L = 100 pF

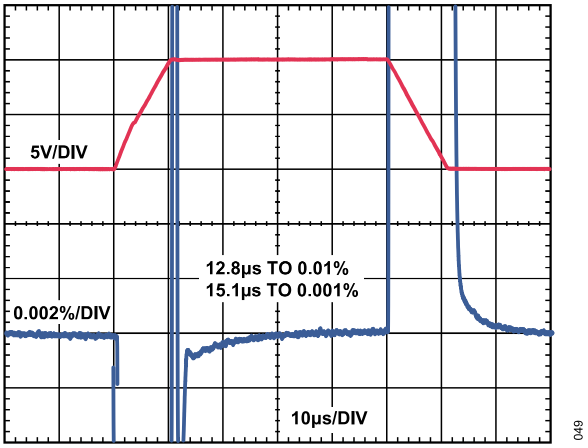


Figure 47. Large Signal Pulse Response and Settling Time (G = 10), 10 V Step, V_S = ±15 V, R_L = 2 kΩ, C_L = 100 pF

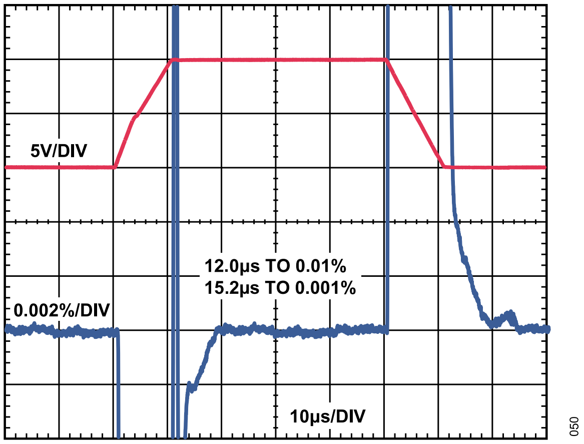


Figure 48. Large Signal Pulse Response and Settling Time (G = 100), 10 V Step, V_S = ±15 V, R_L = 2 kΩ, C_L = 100 pF

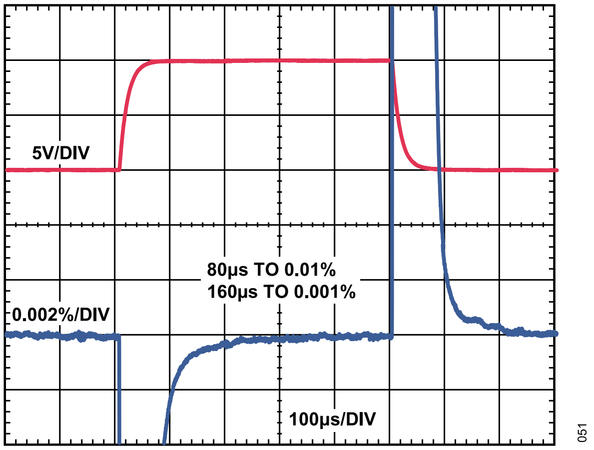


Figure 49. Large Signal Pulse Response and Settling Time (G = 1000), 10 V Step, V_S = ±15 V, R_L = 2 kΩ, C_L = 100 pF

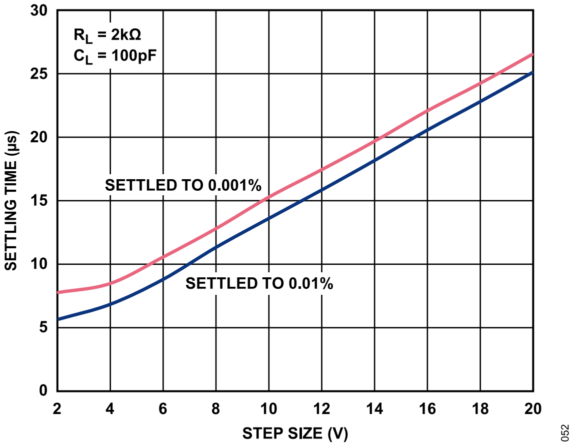


Figure 50. Settling Time vs. Step Size (G = 1)

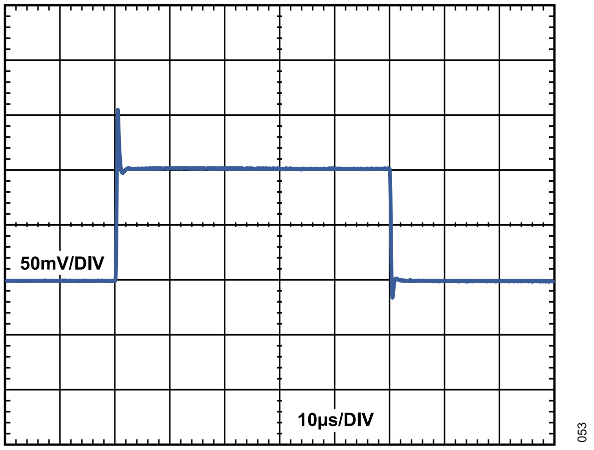


Figure 51. Small Signal Pulse Response (G = 1), R_L = 2 kΩ, C_L = 100 pF

TYPICAL PERFORMANCE CHARACTERISTICS

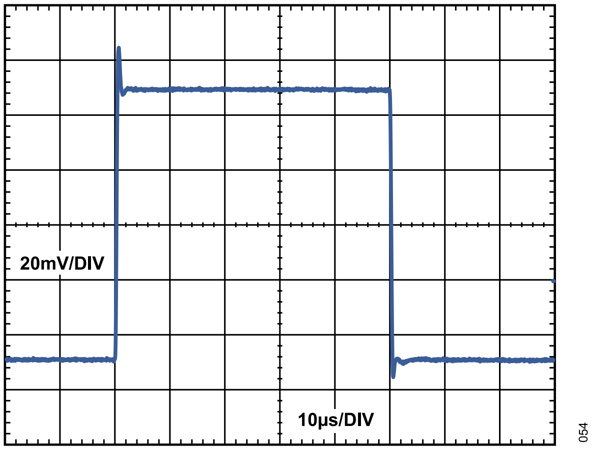


Figure 52. Small Signal Pulse Response (G = 10), R_L = 2 kΩ, C_L = 100 pF

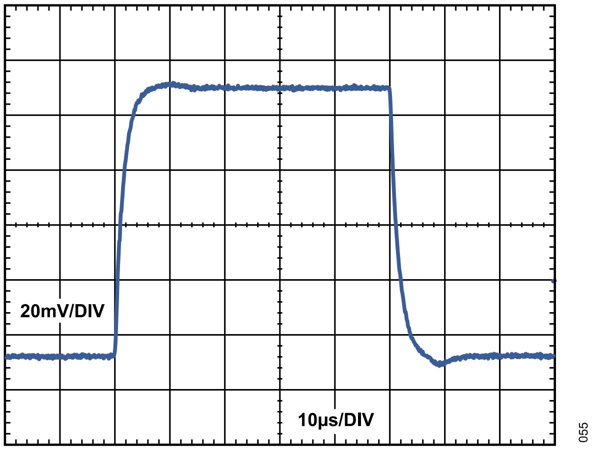


Figure 53. Small Signal Pulse Response (G = 100), R_L = 2 kΩ, C_L = 100 pF

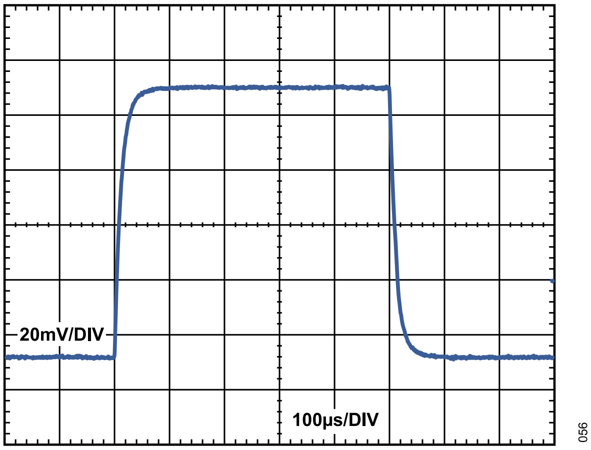


Figure 54. Small Signal Pulse Response (G = 1000), R_L = 2 kΩ, C_L = 100 pF

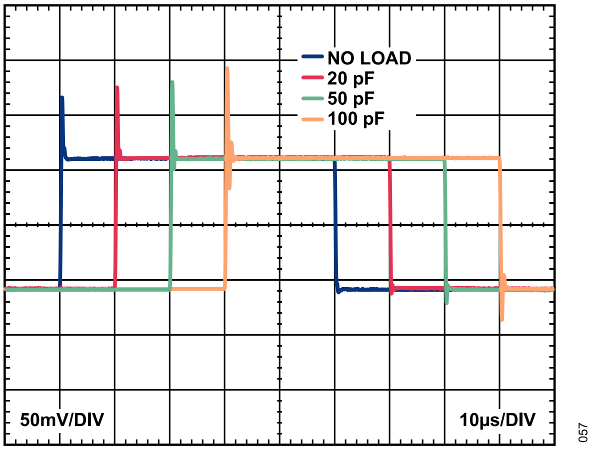


Figure 55. Small Signal Pulse Response with Various Capacitive Loads (G = 1), R_L = No Load

THEORY OF OPERATION

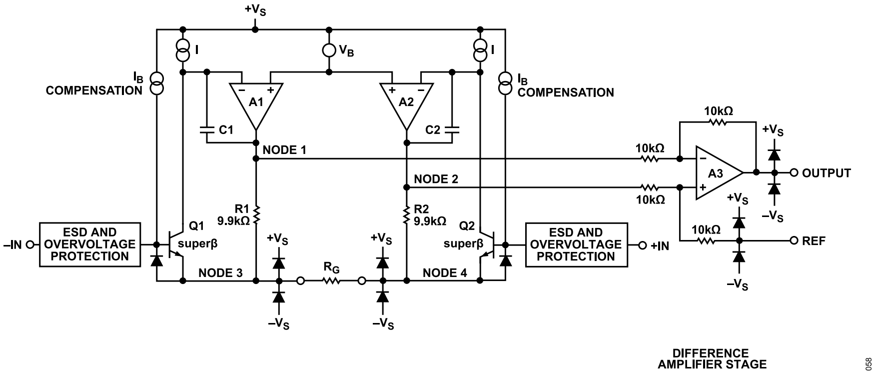


Figure 56. Simplified Schematic

ARCHITECTURE

The AD8422 is based on the classic 3-op-amp instrumentation amplifier topology. This topology has two stages: a preamplifier to provide differential amplification followed by a difference amplifier that removes the common-mode voltage. Figure 56 shows a simplified schematic of the AD8422.

Topologically, Q1, A1, R1 and Q2, A2, R2 can be viewed as precision current feedback amplifiers that maintain a fixed current in the emitters of Q1 and Q2. Any change in the input signal forces the output voltages of A1 and A2 to change accordingly and maintain the Q1 and Q2 current at the correct value. This causes a precise diode drop from –IN and +IN to Node 3 and Node 4, respectively, so that the differential signal applied to the inputs is replicated across the R_G pins. Any current through R_G must also flow through R1 and R2, creating the gained differential voltage between Node 1 and Node 2.

The amplified differential signal and the common-mode signal are applied to a difference amplifier that rejects the common-mode voltage but preserves the amplified differential voltage.

Laser-trimmed resistors allow for a highly accurate in-amp with a gain error of less than 0.01% and a CMRR that exceeds 94 dB (G = 1). The supply current is precisely trimmed to reduce uncertainties due to part-to-part variations in power dissipation and noise. The high performance pinout and special attention to design and layout allow for high CMRR across a wide frequency and temperature range. Using superbeta input transistors and bias current compensation, the AD8422 offers extremely high input impedance and low bias current, as well as very low voltage noise while using only 300 µA supply current. The overvoltage protection scheme allows the input to go 40 V from the opposite rail at all gains without compromising the noise performance.

The transfer function of the AD8422 is

$$V_{OUT} = G \times (V_{IN+} - V_{IN-}) + V_{REF} \quad (1)$$

where:

$$G = 1 + \frac{19.8\ \text{k}\Omega}{R_G} \quad (2)$$

GAIN SELECTION

Placing a resistor across the R_G terminals sets the gain of the AD8422 that can be calculated by referring to Table 8 or by using the following gain equation:

$$R_G = \frac{19.8\ \text{k}\Omega}{G - 1} \quad (3)$$

The AD8422 defaults to G = 1 when no gain resistor is used. Add the tolerance and gain drift of the R_G resistor to the specifications of the AD8422 to determine the total gain accuracy of the system. When the gain resistor is not used, gain error and gain drift are minimal.

Table 8. Gains Achieved Using 1% Resistors

1% Standard Table Value of R_G (Ω)	Calculated Gain
19.6 k	2.010
4.99 k	4.968
2.21 k	9.959
1.05 k	19.86
402	50.25
200	100.0
100	199.0
39.2	506.1
20	991.0

R_G Power Dissipation

The AD8422 duplicates the differential voltage across its inputs onto the R_G resistor. Choose an R_G resistor size that is sufficient to handle the expected power dissipation at ambient temperature.

REFERENCE TERMINAL

The output voltage of the AD8422 is developed with respect to the potential on the reference terminal. This can be used to apply a precise offset to the output signal. For example, a voltage source can be tied to the REF pin to level shift the output, allowing the AD8422 to drive a unipolar analog-to-digital converter (ADC). The REF pin is protected with ESD diodes and must not exceed either $+V_S$ or $-V_S$ by more than 0.3 V.

THEORY OF OPERATION

For best performance, maintain a source impedance to the REF terminal that is below 1 Ω. As shown in Figure 56, the reference terminal, REF, is at one end of a 10 kΩ resistor. Additional impedance at the REF terminal adds to this 10 kΩ resistor and results in amplification of the signal connected to the positive input.

The amplification from the additional R_{REF} can be calculated as

$2(10\ k\Omega + R_{REF})/(20\ k\Omega + R_{REF})$

Only the positive signal path is amplified; the negative path is unaffected. This uneven amplification degrades CMRR.

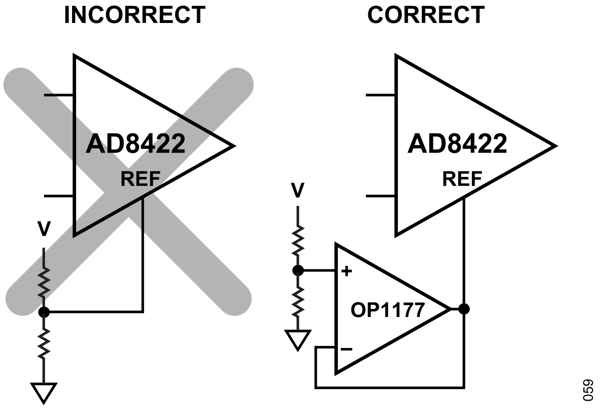


Figure 57. Driving the Reference Pin (REF)

INPUT VOLTAGE RANGE

The 3-op-amp architecture of the AD8422 applies gain in the first stage before removing common-mode voltage with the difference amplifier stage. Internal nodes between the first and second stages (Node 1 and Node 2 in Figure 56) experience a combination of a gained signal, a common-mode signal, and a diode drop. The voltage supplies can limit the combined signal, even when the individual input and output signals are not limited. Figure 11 through Figure 14 show this limitation in detail.

LAYOUT

To ensure optimum performance of the AD8422 at the PCB level, take care in the design of the board layout. To aid in this task, the pins of the AD8422 are arranged in a logical manner.

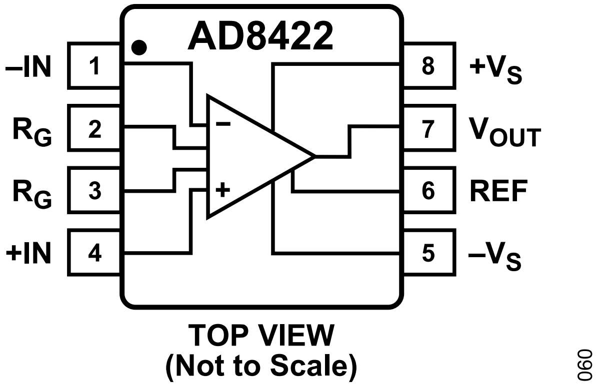


Figure 58. Pinout Diagram

Common-Mode Rejection Ratio over Frequency

Poor layout can cause some of the common-mode signals to be converted to differential signals before reaching the in-amp. Such conversions occur when one input path has a frequency response that is different from the other. To maintain high CMRR over frequency, closely match the input source impedance and capacitance of each path. Place additional source resistance in the input path (for example, for input protection) close to the in-amp inputs, which minimizes their interaction with parasitic capacitance from the PCB traces.

Parasitic capacitance at the gain setting pins (R_G) can also affect CMRR over frequency. If the board design has a component at the gain setting pins (for example, a switch or jumper), choose a component such that the parasitic capacitance is as small as possible.

Power Supplies and Grounding

Use a stable dc voltage to power the instrumentation amplifier. Noise on the supply pins can adversely affect performance.

Place a 0.1 μF capacitor as close as possible to each supply pin. Because the length of the bypass capacitor leads is critical at high frequency, surface-mount capacitors are recommended. A parasitic inductance in the bypass ground trace works against the low impedance created by the bypass capacitor. As shown in Figure 59, a 10 μF capacitor can be used farther away from the device. For larger value capacitors, intended to be effective at lower frequencies, the current return path distance is less critical. In most cases, this capacitor can be shared by other local precision integrated circuits.

THEORY OF OPERATION

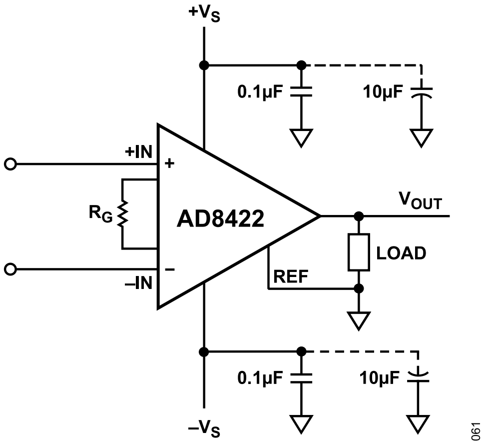


Figure 59. Supply Decoupling, REF, and Output Referred to Local Ground

A ground plane layer is helpful to reduce parasitic inductances. This minimizes voltage drops with changes in current. The area of the current path is directly proportional to the magnitude of parasitic inductances and, therefore, the impedance of the path at high frequencies. Large changes in currents in an inductive decoupling path or ground return create unwanted effects due to the coupling of such changes into the amplifier inputs.

Because load currents flow from the supplies, connect the load at the same physical location as the bypass capacitor grounds.

Reference Pin

The output voltage of the AD8422 is developed with respect to the potential on the reference terminal. Ensure that REF is tied to the appropriate local ground.

INPUT BIAS CURRENT RETURN PATH

The input bias current of the AD8422 must have a dc return path to ground. When using a floating source without a current return path, such as a thermocouple, create a current return path, as shown in Figure 60.

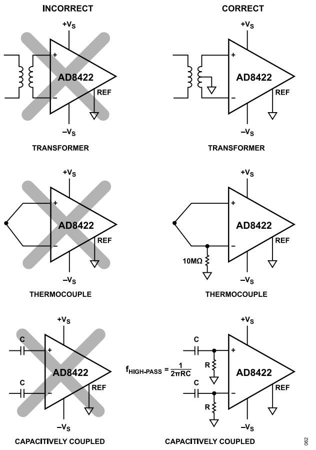


Figure 60. Creating an Input Bias Current Return Path

INPUT VOLTAGES BEYOND THE SUPPLY RAILS

Many instrumentation amplifiers specify excellent CMRR and input impedance, but in a real system, the performance suffers because of the external components required for input protection. The AD8422 has very robust inputs. It typically does not need additional input protection. Input voltages can be up to 40 V from the opposite supply rail without damage to the part. For example, with a +5 V positive supply and a 0 V negative supply, the part can safely withstand voltages from −35 V to +40 V. Unlike some other instrumentation amplifiers, the part can handle large differential input voltages even when the part is in high gain.

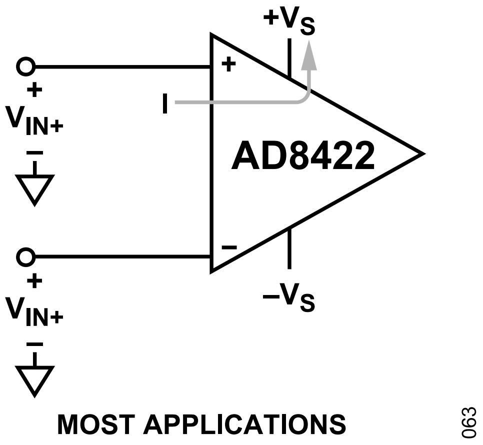


Figure 61. Input Overvoltage Protection with no External Components

For input voltages less than 40 V from the opposite rail, no input protection is required.

Keep the rest of the AD8422 terminals within the supplies. All terminals of the AD8422 are protected against ESD.

Input Voltages Beyond the Maximum Ratings

For applications where the AD8422 encounters voltages beyond the limits in the Absolute Maximum Ratings section, external protection is required. This external protection depends on the duration of the overvoltage event and the noise performance required.

For short-lived events, transient protectors such as metal oxide varistors (MOVs) may be all that is required.

For longer events, use resistors in series with the inputs combined with diodes. To avoid worsening bias current performance, low leakage diodes, such as the BAV199 or FJH1100s, are recommended. The diodes prevent the voltage at the input of the amplifier from exceeding the maximum ratings, while the resistors limit the current into the diodes. Because most external diodes can easily handle 100 mA or more, resistor values do not have to be large. Therefore, the protection resistance has minimal impact on noise performance.

THEORY OF OPERATION

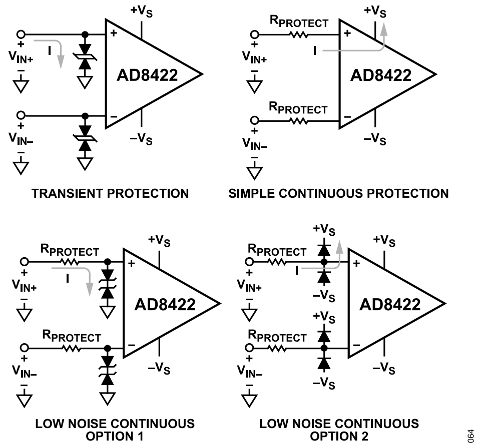


Figure 62. Input Protection Options for Input Voltages Beyond Absolute Maximum Ratings

At the expense of some noise performance, another solution is to use series resistors. In the overvoltage case, current into the inputs of the AD8422 is internally limited to a safe value for the amplifier. Although the AD8422 inputs must still be kept within the Absolute Maximum Ratings, the I × R drop across the protection resistor increases the maximum voltage that the system can withstand to the following values:

For positive input signals,

$$V_{MAX\_NEW} = (40\ \text{V} + Negative\ Supply) + I_{IN} \times R_{PROTECT} \quad (4)$$

For negative input signals,

$$V_{MIN\_NEW} = (Positive\ Supply - 40\ \text{V}) - I_{OUT} \times R_{PROTECT} \quad (5)$$

Overvoltage performance is shown in Figure 15, Figure 16, Figure 17, and Figure 18. With gains greater than 100 and supply voltages less than ±2.5 V, overdrive voltages beyond the rails may cause the output to invert as far as the REF pin voltage.

RF INTERFERENCE (RFI)

RF rectification is often a problem when amplifiers are used in applications that have strong RF signals. The disturbance can appear as a small dc offset voltage. High frequency signals can be filtered with a low-pass RC network placed at the input of the instrumentation amplifier, as shown in Figure 63.

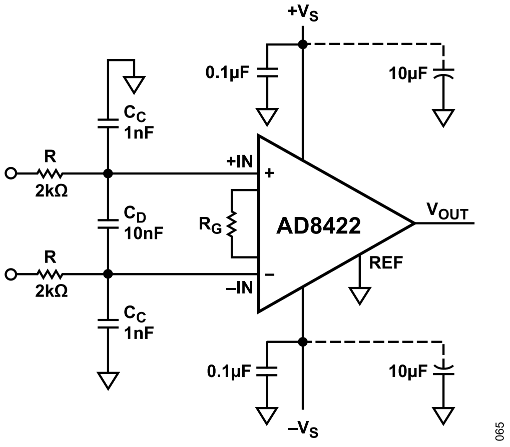


Figure 63. RFI Suppression

The filter limits the input signal bandwidth, according to the following relationship:

$$FilterFrequency_{DIFF} = \frac{1}{2\pi R(2C_D + C_C)} \quad (6)$$

$$FilterFrequency_{CM} = \frac{1}{2\pi RC_C} \quad (7)$$

where $C_D \geq 10\ C_C$.

C_D affects the difference signal, and C_C affects the common-mode signal. Choose values of R and C_C that minimize RFI. A mismatch between R × CC at the positive input and R × CC at the negative input degrades the CMRR of the AD8422. By using a value of C_D that is one order of magnitude larger than C_C, the effect of the mismatch is reduced, and performance is improved.

Resistors add noise; therefore, the choice of the resistor and capacitor values depends on the desired tradeoff between noise, input impedance at high frequencies, and RF immunity. The resistors used for the RFI filter can be the same as those used for input protection.

APPLICATIONS INFORMATION

PRECISION BRIDGE CONDITIONING

With its high CMRR, low drift, and rail-to-rail output, the AD8422 is an excellent choice for conditioning a signal from a Wheatstone bridge. With appropriate supply voltages, the gain and reference pin voltage can be adjusted to match the full-scale bridge output to any desired output range, such as 0 V to 5 V. Figure 64 shows a circuit to convert a bridge signal into a 4 mA to 20 mA output using the AD8276 low power, precision difference amplifier, and the ADA4096-2 low power, rail-to-rail input and output, overvoltage protected op amp. With high precision bridge circuits, care must be taken to compensate offsets and temperature errors. For example, if the voltage at the REF pin is used to compensate for the bridge offset, ensure that the AD8422 is within its operating range for the maximum expected offset. If the zero-adjust potentiometer is excluded, connect the positive op amp input to the center of the 24.9 kΩ, 10.7 kΩ divider, which is at 1.5 V. If lower supply voltages are used for the AD8276 and the ADA4096-2, ensure that the desired output voltage of the AD8276 is within its output range, and V_L is within the input and output range of the ADA4096-2. The transistor must have sufficient breakdown voltage and I_C. Low cost transistors, such as the BC847 or 2N5210, are recommended.

PROCESS CONTROL ANALOG INPUT

In process control systems such as programmable logic controllers (PLC) and distributed control systems (DCS), analog variables typically occur in just a few standard voltage or current ranges, including 4 mA to 20 mA and ±10 V. Variables within these input ranges must often be gained or attenuated and level shifted to match a specific ADC input range such as 0 V to 5 V. The circuit in Figure 65 shows one way this can be done with a single AD8422. Low power, overvoltage protection, and high precision make the AD8422 a good match for process control applications, and high input impedance, low bias current, and low current noise allow significant source resistance with minimum additional errors.

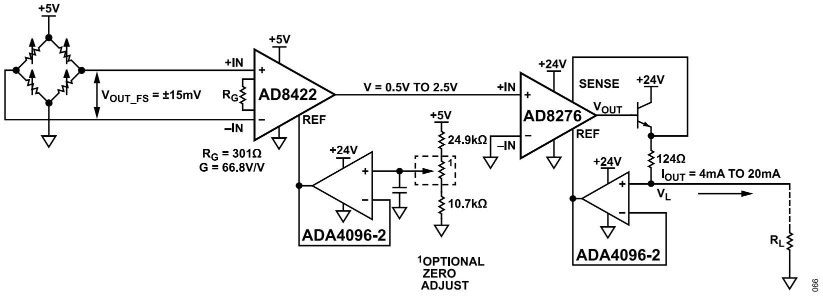


Figure 64. Bridge Circuit with 4 mA to 20 mA Output

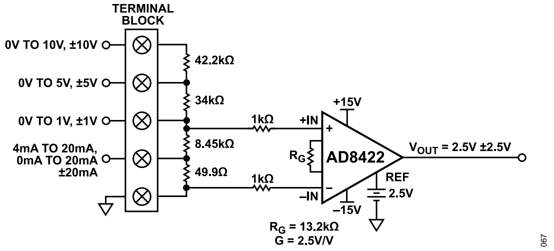
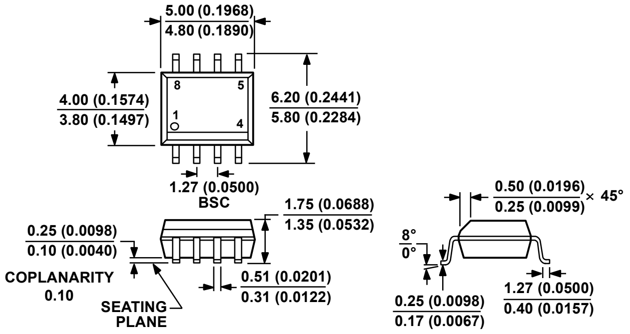


Figure 65. Process Control Analog Input

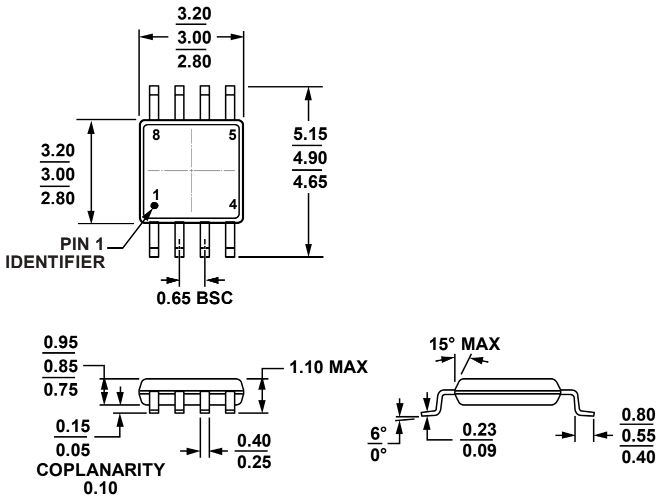
OUTLINE DIMENSIONS



COMPLIANT TO JEDEC STANDARDS MS-012-AA

CONTROLLING DIMENSIONS ARE IN MILLIMETERS; INCH DIMENSIONS (IN PARENTHESES) ARE ROUNDED-OFF MILLIMETER EQUIVALENTS FOR REFERENCE ONLY AND ARE NOT APPROPRIATE FOR USE IN DESIGN.

Figure 66. 8-Lead Standard Small Outline Package [SOIC_N]
Narrow Body
(R-8)
Dimensions shown in millimeters and (inches)



COMPLIANT TO JEDEC STANDARDS MO-187-AA

Figure 67. 8-Lead Mini Small Outline Package [MSOP]
(RM-8)
Dimensions shown in millimeters

OUTLINE DIMENSIONS

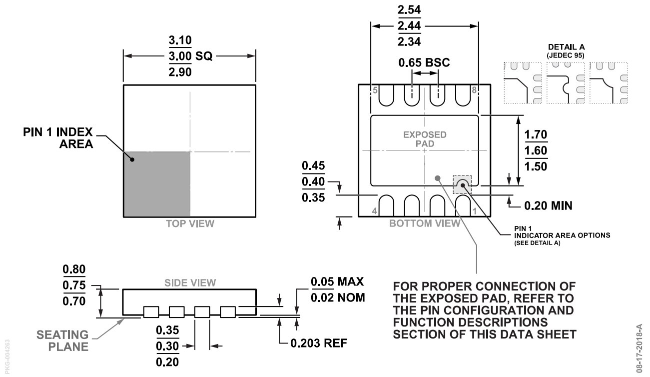


Figure 68. 8-Lead Lead Frame Chip Scale Package [LFCSP]
3 mm × 3 mm Body and 0.75 mm Package Height
(CP-8-19)
Dimensions shown in millimeters

Updated: September 19, 2022

ORDERING GUIDE

Model[1]	Temperature Range	Package Description	Packing Quantity	Package Option	Marking Code
AD8422ACPZ-R7	-40°C to +125°C	8-Lead LFCSP (3mm x 3mm w/ EP)	Reel, 1500	CP-8-19	A4K
AD8422ACPZ-RL	-40°C to +125°C	8-Lead LFCSP (3mm x 3mm w/ EP)	Reel, 5000	CP-8-19	A4K
AD8422ARMZ	-40°C to +85°C	8-Lead MSOP		RM-8	Y4U
AD8422ARMZ-R7	-40°C to +85°C	8-Lead MSOP	Reel, 1000	RM-8	Y4U
AD8422ARMZ-RL	-40°C to +85°C	8-Lead MSOP	Reel, 3000	RM-8	Y4U
AD8422ARZ	-40°C to +85°C	8-Lead SOIC		R-8	
AD8422ARZ-R7	-40°C to +85°C	8-Lead SOIC	Reel, 1000	R-8	
AD8422ARZ-RL	-40°C to +85°C	8-Lead SOIC	Reel, 2500	R-8	
AD8422BRMZ	-40°C to +85°C	8-Lead MSOP		RM-8	Y4V
AD8422BRMZ-R7	-40°C to +85°C	8-Lead MSOP	Reel, 1000	RM-8	Y4V
AD8422BRMZ-RL	-40°C to +85°C	8-Lead MSOP	Reel, 3000	RM-8	Y4V
AD8422BRZ	-40°C to +85°C	8-Lead SOIC		R-8	
AD8422BRZ-R7	-40°C to +85°C	8-Lead SOIC	Reel, 1000	R-8	
AD8422BRZ-RL	-40°C to +85°C	8-Lead SOIC	Reel, 2500	R-8	

[1] Z = RoHS Compliant Part.

Mouser Electronics

Authorized Distributor

Click to View Pricing, Inventory, Delivery & Lifecycle Information:

Analog Devices Inc.:

AD8422BRMZ AD8422ARZ AD8422ARMZ AD8422BRMZ-R7 AD8422ARMZ-R7 AD8422ARZ-RL AD8422BRZ-RL AD8422ARZ-R7 AD8422BRZ-R7 AD8422BRZ AD8422ARMZ-RL AD8422BRMZ-RL AD8422ACPZ-RL AD8422ACPZ-R7 EVAL-AD8422ACPZ