3 nV/√Hz, Low Power Instrumentation Amplifier

Known Good Die

AD8421-KGD

FEATURES

Low power: 2.3 mA maximum quiescent current
Low noise
- **3.2 nV/√Hz maximum input voltage noise at 1 kHz**
- **200 fA/√Hz typical current noise spectral density at 1 kHz**

Excellent ac specifications
- **10 MHz typical small signal bandwidth (gain = 1 and gain = 10)**
- **2 MHz typical small signal bandwidth (gain = 100)**
- **0.6 μs typical settling time to 0.001% (gain = 10)**
- **80 dB minimum CMRR at 20 kHz (gain = 1)**
- **35 V/μs typical slew rate**

High precision dc performance
- **84 dB minimum CMRR DC to 60 Hz with 1 kΩ source imbalance (gain = 1)**
- **0.9 μV/°C maximum input offset voltage, average temperature coefficient**
- **5 ppm/°C maximum gain vs. temperature (gain = 1)**
- **2 nA maximum input bias current**

Inputs protected to 40 V from opposite supply
±2.5 V to ±18 V dual supply (+5 V to +36 V single supply)
Gain set with a single resistor (gain = 1 to 10,000)
Known Good Die (KGD): these die are fully guaranteed to data sheet specification.

APPLICATIONS

Medical instrumentation
Precision data acquisition
Microphone preamplification
Vibration analysis
Multiplexed input applications
ADC driver

GENERAL DESCRIPTION

The AD8421-KGD is a low cost, low power, low noise, ultralow bias current, high speed instrumentation amplifier that is ideally suited for a broad spectrum of signal conditioning and data acquisition applications. This device features high CMRR, allowing the device to extract low level signals in the presence of high frequency common-mode noise over a wide temperature range.

FUNCTIONAL BLOCK DIAGRAM

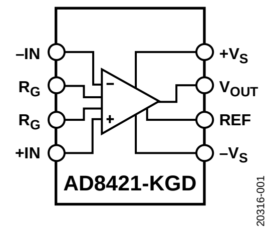

Figure 1.

The 10 MHz small signal bandwidth, 35 V/μs slew rate, and 0.6 μs settling time to 0.001% (gain = 10) allow the AD8421-KGD to amplify high speed signals and excel in applications that require high channel count, multiplexed systems. Even at higher gains, the current feedback architecture maintains high performance. For example, at gain = 100, the bandwidth is 2 MHz and the settling time is 0.8 μs.

The AD8421-KGD has excellent distortion performance, making this device suitable for use in demanding applications such as vibration analysis.

The AD8421-KGD delivers 3 nV/√Hz input voltage noise and 200 fA/√Hz current noise spectral density with only 2 mA quiescent current, making the device an ideal choice for measuring low level signals. For applications with high source impedance, the AD8421-KGD employs innovative process technology and design techniques to provide noise performance that is limited only by the sensor.

The AD8421-KGD uses unique protection methods to ensure robust inputs while still maintaining low noise. This protection allows input voltages up to 40 V from the opposite supply rail without damage to the device.

A single resistor sets the gain from 1 to 10,000. The reference pin can be used to apply a precise offset to the output voltage.

The AD8421-KGD is specified from −40°C to +85°C and operational to 125°C.

Additional application and technical information can be found in the AD8421 data sheet.

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TABLE OF CONTENTS

Features ... 1
Applications ... 1
General Description ... 1
Functional Block Diagram ... 1
Revision History ... 2
Specifications ... 3
Absolute Maximum Ratings ... 6
ESD Caution ... 6
Pin Configuration and Function Descriptions ... 7
Outline Dimensions ... 8
Die Specifications and Assembly Recommendations ... 8
Ordering Guide ... 8

REVISION HISTORY

9/2019—Revision 0: Initial Version

SPECIFICATIONS

Supply voltage (V_S) = ±15 V, REF voltage (V_{REF}) = 0 V, T_A = 25°C, gain = 1, and load resistance (R_L) = 2 kΩ, unless otherwise noted.

Table 1.

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
COMMON-MODE REJECTION RATIO (CMRR)					
CMRR DC to 60 Hz with 1 kΩ Source Imbalance	Common-mode voltage (V_{CM}) = −10 V to +10 V				
Gain = 1		84			dB
Gain = 10		104			dB
Gain = 100		124			dB
Gain = 1000		134			dB
Over Temperature, Gain = 1	T_A = −40°C to +85°C	80			dB
CMRR at 20 kHz	V_{CM} = −10 V to +10 V				
Gain = 1		80			dB
Gain = 10		90			dB
Gain = 100		100			dB
Gain = 1000		100			dB
NOISE					
Voltage Noise, 1 kHz[1]	+IN voltage (V_{+IN}), −IN voltage (V_{-IN}) = 0 V				
Input Voltage Noise, e_{ni}			3	3.2	nV/√Hz
Output Voltage Noise, e_{no}				60	nV/√Hz
Peak to Peak, Referred to Input (RTI)	Frequency = 0.1 Hz to 10 Hz				
Gain = 1			2		μV p-p
Gain = 10			0.5		μV p-p
Gain = 100 to 1000			0.07		μV p-p
Current Noise					
Spectral Density	Frequency = 1 kHz		200		fA/√Hz
Peak to Peak, RTI	Frequency = 0.1 Hz to 10 Hz		18		pA p-p
VOLTAGE OFFSET[2]					
Input Offset Voltage, V_{OSI}	V_S = ±5 V to ±15 V			70	μV
Over Temperature	T_A = −40°C to +85°C			135	μV
Average Temperature Coefficient				0.9	μV/°C
Output Offset Voltage, V_{OSO}				600	μV
Over Temperature	T_A = −40°C to +85°C			1	mV
Average Temperature Coefficient				9	μV/°C
Offset RTI vs. Supply (Power Supply Ratio)	V_S = ±2.5 V to ±18 V				
Gain = 1		90	120		dB
Gain = 10		110	120		dB
Gain = 100		124	130		dB
Gain = 1000		130	140		dB
INPUT CURRENT					
Input Bias Current			1	2	nA
Over Temperature	T_A = −40°C to +85°C			8	nA
Average Temperature Coefficient			50		pA/°C
Input Offset Current			0.5	2	nA
Over Temperature	T_A = −40°C to +85°C			3	nA
Average Temperature Coefficient			1		pA/°C

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
DYNAMIC RESPONSE					
Small Signal Bandwidth	−3 dB				
Gain = 1			10		MHz
Gain = 10			10		MHz
Gain = 100			2		MHz
Gain = 1000			0.2		MHz
Settling Time to 0.01%	10 V step				
Gain = 1			0.7		μs
Gain = 10			0.4		μs
Gain = 100			0.6		μs
Gain = 1000			5		μs
Settling Time to 0.001%	10 V step				
Gain = 1			1		μs
Gain = 10			0.6		μs
Gain = 100			0.8		μs
Gain = 1000			6		μs
Slew Rate					
Gain = 1 to 100			35		V/μs
GAIN[3]	Gain = 1 + (9.9 kΩ/R_G)				
Gain Range		1		10,000	V/V
Gain Error	Output voltage (V_{OUT}) = ±10 V				
Gain = 1				0.05	%
Gain = 10 to 1000				0.3	%
Gain Nonlinearity	V_{OUT} = −10 V to +10 V				
Gain = 1	R_L ≥ 2 kΩ			1	ppm
	R_L = 600 Ω		1	3	ppm
Gain = 10 to 1000	R_L ≥ 600 Ω		30	50	ppm
	V_{OUT} = −5 V to +5 V		5	10	ppm
Gain vs. Temperature[3]					
Gain = 1				5	ppm/°C
Gain > 1				−50	ppm/°C
INPUT					
Input Impedance					
Differential			30‖3		GΩ‖pF
Common Mode			30‖3		GΩ‖pF
Input Operating Voltage Range[4]	V_S = ±2.5 V to ±18 V	$-V_S + 2.3$		$+V_S - 1.8$	V
Over Temperature	T_A = −40°C	$-V_S + 2.5$		$+V_S - 2.0$	V
	T_A = 85°C	$-V_S + 2.1$		$+V_S - 1.8$	V
OUTPUT	R_L = 2 kΩ				
Output Swing	V_S = ±2.5 V to ±18 V	$-V_S + 1.2$		$+V_S - 1.6$	V
Over Temperature	T_A = −40°C to +85°C	$-V_S + 1.2$		$+V_S - 1.6$	V
Short-Circuit Current			65		mA
REFERENCE INPUT					
Input Reference, R_{IN}			20		kΩ
Input Current, I_{IN}	V_{+IN}, V_{-IN} = 0 V		20	24	μA
Voltage Range		$-V_S$		$+V_S$	V
Reference Gain to Output			1 ± 0.0001		V/V

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
POWER SUPPLY					
Operating Range	Dual supply	±2.5		±18	V
	Single supply	5		36	V
Quiescent Current			2	2.3	mA
Over Temperature	T_A = −40°C to +85°C			2.6	mA
TEMPERATURE RANGE					
For Specified Performance		−40		+85	°C
Operational[5]		−40		+125	°C

[1] Total voltage noise = $\sqrt{(e_{ni}^2 + (e_{no}/Gain)^2 + e_{RG}^2)}$, where e_{RG} is the external gain resistor noise. See the AD8421 data sheet for more information.
[2] Total RTI $V_{OS} = (V_{OSI}) + (V_{OSO}/Gain)$.
[3] These specifications do not include the tolerance of the external gain setting resistor, R_G. For Gain > 1, add R_G errors to the specifications given in this table.
[4] Input operating voltage range of the AD8421-KGD input stage only. The input range can depend on the common-mode voltage, differential voltage, gain, and reference voltage. See the AD8421 data sheet for more details.
[5] See the AD8421 data sheet for expected operation between 85°C and 125°C.

ABSOLUTE MAXIMUM RATINGS

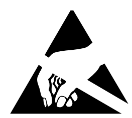
Table 2.

Parameter	Rating
Supply Voltage	±18 V
Output Short-Circuit Current Duration	Indefinite
Maximum Voltage at −IN or +IN[1]	$-V_S + 40$ V
Minimum Voltage at −IN or +IN	$+V_S - 40$ V
Maximum Voltage at REF[2]	$+V_S + 0.3$ V
Minimum Voltage at REF	$-V_S - 0.3$ V
Storage Temperature Range	−65°C to +150°C
Operating Temperature Range	−40°C to +125°C
Maximum Junction Temperature	150°C
Electrostatic Discharge (ESD)	
Human Body Model	2 kV
Charged Device Model	1.25 kV
Machine Model	0.2 kV

[1] For voltages beyond these limits, use input protection resistors. See the AD8421 data sheet for more information.
[2] There are ESD protection diodes from the reference input to each supply. Therefore, REF cannot be driven beyond the supplies in the same way that +IN and −IN can. See the AD8421 data sheet for more information.

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

ESD CAUTION



ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

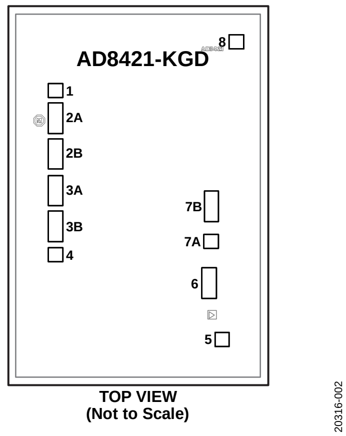


Figure 2. Pad Configuration

Table 3. Pad Function Descriptions[1]

Pad No.	Mnemonic	Pad Type	X-Axis (µm)	Y-Axis (µm)	Description
1	−IN	Single	−548.2	+376	Negative Input Pad.
2A	R_G	Double	−548.2	+241	Gain Setting Pad.
2B	R_G	Double	−548.2	+66	Gain Setting Pad.
3A	R_G	Double	−548.2	−112	Gain Setting Pad.
3B	R_G	Double	−548.2	−287	Gain Setting Pad.
4	+IN	Single	−548.2	−422	Positive Input Pad.
5	$-V_S$	Single	+566.4	−841	Negative Power Supply Pad.
6	REF	Double	+502	−565.8	Reference Voltage Pad.
7A	V_{OUT}	Single	+512	−359.5	Output Pad.
7B	V_{OUT}	Double	+512	−191.6	Output Pad.
8	$+V_S$	Single	+635.8	+929	Positive Power Supply Pad.

[1] To minimize gain errors introduced by the bond wires, use Kelvin connections between the chip and the gain resistor, R_G, by connecting Pad 2A and Pad 2B in parallel to one end of R_G and by connecting Pad 3A and Pad 3B in parallel to the other end of R_G. For unity-gain applications where R_G is not required, Pad 2A and Pad 2B must be bonded together as well as Pad 3A and Pad 3B.

OUTLINE DIMENSIONS

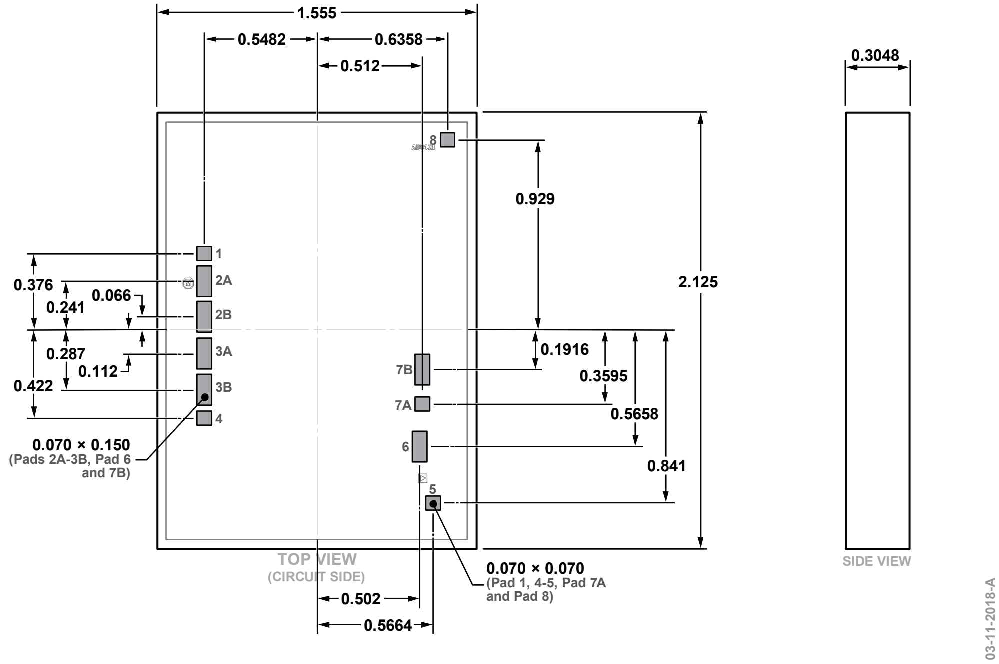


Figure 3. 8-Pad Bare Die [CHIP]
(C-8-15)
Dimensions shown in millimeters

DIE SPECIFICATIONS AND ASSEMBLY RECOMMENDATIONS

Table 4. Die Specifications

Parameter	Value	Unit
Scribe Line Width	90 × 90	µm
Die Size	1555 × 2125	µm
Thickness	304.8	µm
Backside	None[1]	Not applicable
Passivation	Doped oxide/silicon (Si)/Nitrogen (N)	Not applicable
Bond Pads (Minimum)	70 × 70	µm
Bond Pad Composition	1.0 Aluminum (Al)/Si, 0.5 Copper (Cu)	%

[1] If connecting the backside to a voltage potential, tie the backside to $-V_S$. Otherwise, leave the backside floating.

Table 5. Assembly Recommendations

Assembly Component	Recommendation
Die Attach	No special requirements
Bonding Method	Gold ball or aluminum wedge
Bonding Sequence	Any

ORDERING GUIDE

Model[1]	Temperature Range	Package Description	Package Option
AD8421-KGD-WP	−40°C to +85°C	8-Pad Bare Die [CHIP], Waffle Pack	C-8-15

[1] The AD8421-KGD-WP is a RoHS compliant part.

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