325 MHz, 8 × 8 Buffered Video Crosspoint Switches

Data Sheet

AD8108/AD8109

FEATURES

- 8 × 8 high speed nonblocking switch arrays
  - AD8108: G = 1
  - AD8109: G = 2
- Serial or parallel programming of switch array
- Serial data out allows daisy-chaining of multiple 8 × 8 arrays to create larger switch arrays
- Output disable allows connection of multiple devices
- Pin-compatible with AD8110/AD8111 16 × 8 switch arrays
- For 16 × 16 arrays see AD8116
- Complete solution
  - Buffered inputs
  - Eight output amplifiers
    - AD8108 (G = 1)
    - AD8109 (G = 2)
  - Drives 150 Ω loads
- Excellent video performance
  - 60 MHz 0.1 dB gain flatness
  - 0.02%/0.02° differential gain/differential phase error (R_L = 150 Ω)
- Excellent ac performance
  - −3 dB bandwidth: 325 MHz (AD8108), 250 MHz (AD8109)
  - Slew rate: 400 V/µs (AD8108), 480 V/µs (AD8109)
- Low power of 45 mA
- Low all hostile crosstalk of −83 dB at 5 MHz
- Reset pin allows disabling of all outputs (connected through a capacitor to ground provides power-on reset capability)
- Excellent ESD rating: exceeds 4000 V human body model
- 80-lead LQFP (12 mm × 12 mm)

APPLICATIONS

- Routing of high speed signals including
  - Composite video (NTSC, PAL, S, SECAM)
  - Component video (YUV, RGB)
  - Compressed video (MPEG, Wavelet)
  - 3-level digital video (HDB3)

GENERAL DESCRIPTION

The AD8108/AD8109 are high speed 8 × 8 video crosspoint switch matrices. They offer a −3 dB signal bandwidth greater than 250 MHz and channel switch times of less than 25 ns with 1% settling. With −83 dB of crosstalk and −98 dB isolation (at 5 MHz), the AD8108/AD8109 are useful in many high speed applications. The differential gain and differential phase of better than 0.02% and 0.02°, respectively, along with 0.1 dB flatness out to 60 MHz, make the AD8108/AD8109 ideal for video signal switching.

FUNCTIONAL BLOCK DIAGRAM

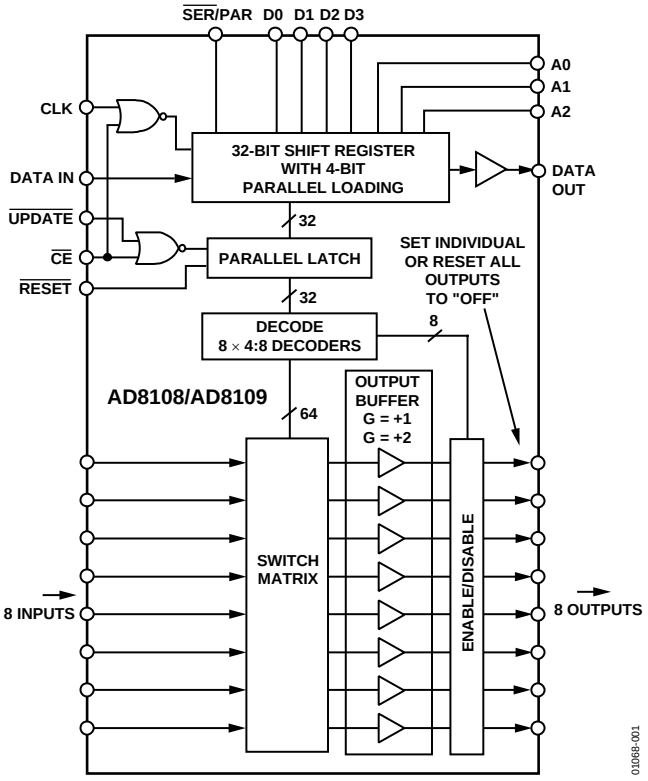

Figure 1. Functional Block Diagram

The AD8108 and AD8109 include eight independent output buffers that can be placed into a high impedance state for paralleling crosspoint outputs so that off channels do not load the output bus. The AD8108 has a gain of 1, while the AD8109 offers a gain of 2. They operate on voltage supplies of ±5 V while consuming only 45 mA of idle current. The channel switching is performed via a serial digital control (which can accommodate daisy-chaining of several devices) or via a parallel control allowing updating of an individual output without reprogramming the entire array.

The AD8108/AD8109 is packaged in an 80-lead LQFP and is available over the extended industrial temperature range of −40°C to +85°C.

Rev. C

Document Feedback

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9/2005—Rev. A to Rev. B

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1/2002—Rev. 0 to Rev. A

Changed MQFP to LQFP ... Universal
Updated Outline Dimensions ... 27

10/1997—Revision 0: Initial Version

SPECIFICATIONS

V_S = ±5 V, T_A = +25°C, R_L = 1 kΩ, unless otherwise noted.

Table 1.

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit	Reference
DYNAMIC PERFORMANCE						
−3 dB Bandwidth	200 mV p-p, R_L = 150 Ω	240/150	325/250		MHz	Figure 1, Figure 13
	2 V p-p, R_L = 150 Ω		140/160		MHz	Figure 1, Figure 13
Propagation Delay	2 V p-p, R_L = 150 Ω		5		ns	
Slew Rate	2 V Step, R_L = 150 Ω		400/480		V/µs	
Settling Time	0.1%, 2 V Step, R_L = 150 Ω		40		ns	Figure 15, Figure 18
Gain Flatness	0.05 dB, 200 mV p-p, R_L = 150 Ω		60/50		MHz	Figure 1, Figure 13
	0.05 dB, 2 V p-p, R_L = 150 Ω		60/50		MHz	Figure 1, Figure 13
	0.1 dB, 200 mV p-p, R_L = 150 Ω		70/65		MHz	Figure 1, Figure 13
	0.1 dB, 2 V p-p, R_L = 150 Ω		80/50		MHz	Figure 1, Figure 13
NOISE/DISTORTION PERFORMANCE						
Differential Gain Error	NTSC or PAL, R_L = 1 kΩ		0.01		%	
	NTSC or PAL, R_L = 150 Ω		0.02		%	
Differential Phase Error	NTSC or PAL, R_L = 1 kΩ		0.01		Degrees	
	NTSC or PAL, R_L = 150 Ω		0.02		Degrees	
Crosstalk, All Hostile	f = 5 MHz		−83/−85		dB	Figure 8, Figure 14
	f = 10 MHz		−76/−83		dB	Figure 8, Figure 14
Off Isolation, Input-Output	f = 5 MHz, R_L =150 Ω, one channel		−98/−102		dB	Figure 23, Figure 29
Input Voltage Noise	0.01 MHz to 50 MHz		15		nV/√Hz	Figure 20, Figure 26
DC PERFORMANCE						
Gain Error	R_L = 1 kΩ		0.04/0.1	0.07/0.5	%	
	R_L = 150 Ω		0.15/0.25		%	
Gain Matching	No load, channel-channel			0.02/1.0	%	
	R_L = 1 kΩ, channel-channel			0.09/1.0	%	
Gain Temperature Coefficient			0.5/8		ppm/°C	
OUTPUT CHARACTERISTICS						
Output Impedance	DC, enabled		0.2		Ω	Figure 24, Figure 30
	Disabled		10/0.001		MΩ	Figure 21, Figure 27
Output Disable Capacitance	Disabled		2		pF	
Output Leakage Current	Disabled, AD8108 only		1/NA		µA	
Output Voltage Range	No load	±2.5	±3		V	
Output Current		20	40		mA	
Short-Circuit Current			65		mA	
INPUT CHARACTERISTICS						
Input Offset Voltage	Worst case (all configurations)		5	20	mV	Figure 35, Figure 41
	Temperature coefficient		12		µV/°C	Figure 36, Figure 42
Input Voltage Range		±2.5/±1.25	±3/±1.5		V	
Input Capacitance	Any switch configuration		2.5		pF	
Input Resistance		1	10		MΩ	
Input Bias Current	Per output selected		2	5	µA	
SWITCHING CHARACTERISTICS						
Enable On Time			60		ns	
Switching Time, 2 V Step	50% $\overline{\text{UPDATE}}$ to 1% settling		25		ns	
Switching Transient (Glitch)	Measured at output		20/30		mV p-p	Figure 22, Figure 28

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit	Reference
POWER SUPPLIES						
Supply Current	AVCC, outputs enabled, no load		33		mA	
	AVCC, outputs disabled		10		mA	
	AVEE, outputs enabled, no load		33		mA	
	AVEE, outputs disabled		10		mA	
	DVCC		10		mA	
Supply Voltage Range			±4.5 to ±5.5		V	
PSRR	f = 100 kHz		73/78		dB	Figure 19, Figure 25
	f = 1 MHz		55/58		dB	
OPERATING TEMPERATURE RANGE						
Temperature Range	Operating (still air)		−40 to +85		°C	
θ_{JA}	Operating (still air)		48		°C/W	

TIMING CHARACTERISTICS (SERIAL)

Table 2. Timing Characteristics

Parameter	Symbol	Min	Typ	Max	Unit
Serial Data Setup Time	t_1	20			ns
CLK Pulse Width	t_2	100			ns
Serial Data Hold Time	t_3	20			ns
CLK Pulse Separation, Serial Mode	t_4	100			ns
CLK to $\overline{\text{UPDATE}}$ Delay	t_5	0			ns
$\overline{\text{UPDATE}}$ Pulse Width	t_6	50			ns
CLK to DATA OUT Valid, Serial Mode	t_7			180	ns
Propagation Delay, $\overline{\text{UPDATE}}$ to Switch On or Off	–			8	ns
Data Load Time, CLK = 5 MHz, Serial Mode	–		6.4		µs
CLK, $\overline{\text{UPDATE}}$ Rise and Fall Times	–			100	ns
$\overline{\text{RESET}}$ Time	–	200			ns

Table 3. Logic Levels

V_{IH}	V_{IL}	V_{OH}	V_{OL}	I_{IH}	I_{IL}	I_{OH}	I_{OL}
$\overline{\text{RESET}}$, SER/PAR CLK, DATA IN, $\overline{\text{CE}}$, $\overline{\text{UPDATE}}$	$\overline{\text{RESET}}$, SER/PAR CLK, DATA IN, $\overline{\text{CE}}$, $\overline{\text{UPDATE}}$	DATA OUT	DATA OUT	$\overline{\text{RESET}}$, SER/PAR CLK, DATA IN, $\overline{\text{CE}}$, $\overline{\text{UPDATE}}$	$\overline{\text{RESET}}$, SER/PAR CLK, DATA IN, $\overline{\text{CE}}$, $\overline{\text{UPDATE}}$	DATA OUT	DATA OUT
2.0 V min	0.8 V max	2.7 V min	0.5 V max	20 µA max	−400 µA min	−400 µA max	3.0 mA min

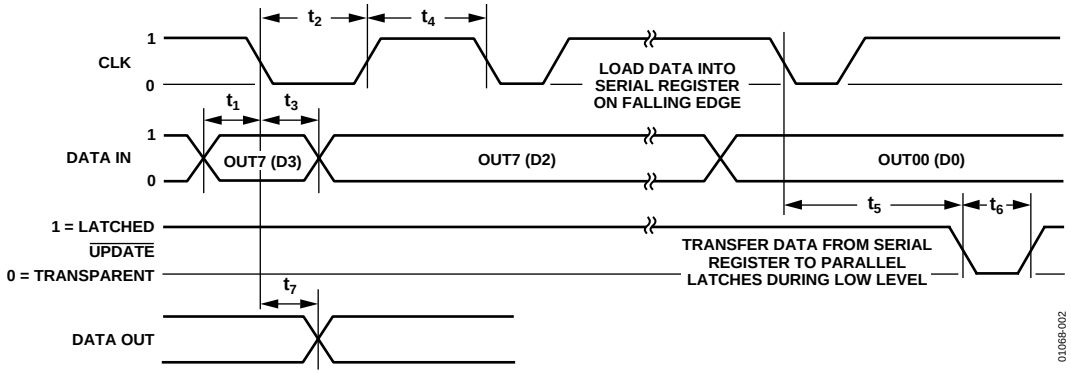


Figure 2. Timing Diagram, Serial Mode

TIMING CHARACTERISTICS (PARALLEL)

Table 4. Timing Characteristics

Parameter	Symbol	Min	Typ	Max	Unit
Data Setup Time	t_1	20			ns
CLK Pulse Width	t_2	100			ns
Data Hold Time	t_3	20			ns
CLK Pulse Separation	t_4	100			ns
CLK to $\overline{\text{UPDATE}}$ Delay	t_5	0			ns
$\overline{\text{UPDATE}}$ Pulse Width	t_6	50			ns
Propagation Delay, $\overline{\text{UPDATE}}$ to Switch On or Off	–			8	ns
CLK, $\overline{\text{UPDATE}}$ Rise and Fall Times	–			100	ns
$\overline{\text{RESET}}$ Time	–	200			ns

Table 5. Logic Levels

V_{IH}	V_{IL}	V_{OH}	V_{OL}	I_{IH}	I_{IL}	I_{OH}	I_{OL}
$\overline{\text{RESET}}$, $\overline{\text{SER}}$/PAR CLK, D0, D1, D2, D3, A0, A1, A2 $\overline{\text{CE}}$, $\overline{\text{UPDATE}}$	$\overline{\text{RESET}}$, $\overline{\text{SER}}$/PAR CLK, D0, D1, D2, D3, A0, A1, A2 $\overline{\text{CE}}$, $\overline{\text{UPDATE}}$	DATA OUT	DATA OUT	$\overline{\text{RESET}}$, $\overline{\text{SER}}$/PAR CLK, D0, D1, D2, D3, A0, A1, A2 $\overline{\text{CE}}$, $\overline{\text{UPDATE}}$	$\overline{\text{RESET}}$ $\overline{\text{SER}}$/PAR CLK, D0, D1, D2, D3, A0, A1, A2 $\overline{\text{CE}}$, $\overline{\text{UPDATE}}$	DATA OUT	DATA OUT
2.0 V min	0.8 V max	2.7 V min	0.5 V max	20 µA max	−400 µA min	−400 µA max	3.0 mA min

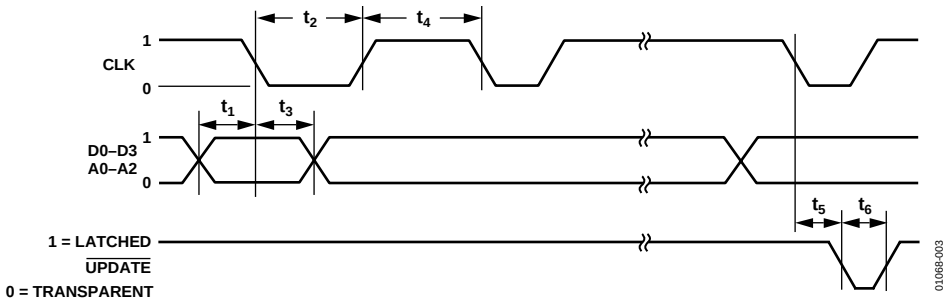


Figure 3. Timing Diagram, Parallel Mode

Table 6. Operation Truth Table

CE	$\overline{\text{UPDATE}}$	CLK	DATA IN	DATA OUT	$\overline{\text{RESET}}$	$\overline{\text{SER}}$\PAR	Operation/Comment
1	X	X	X	X	X	X	No change in logic.
0	1	f	$Data_i$	$Data_{i-32}$	1	0	The data on the serial DATA IN line is loaded into serial register. The first bit clocked into the serial register appears at DATA OUT 32 clocks later.
0	1	f	D0 … D3, A0 … A2	Not applicable in parallel mode	1	1	The data on the parallel data lines, D0 to D3, are loaded into the 32-bit serial shift register location addressed by A0 to A2.
0	0	X	X…	X	1	X	Data in the 32-bit shift register transfers into the parallel latches that control the switch array. Latches are transparent.
X	X	X	X	X	0	X	Asynchronous operation. All outputs are disabled. Remainder of logic is unchanged.

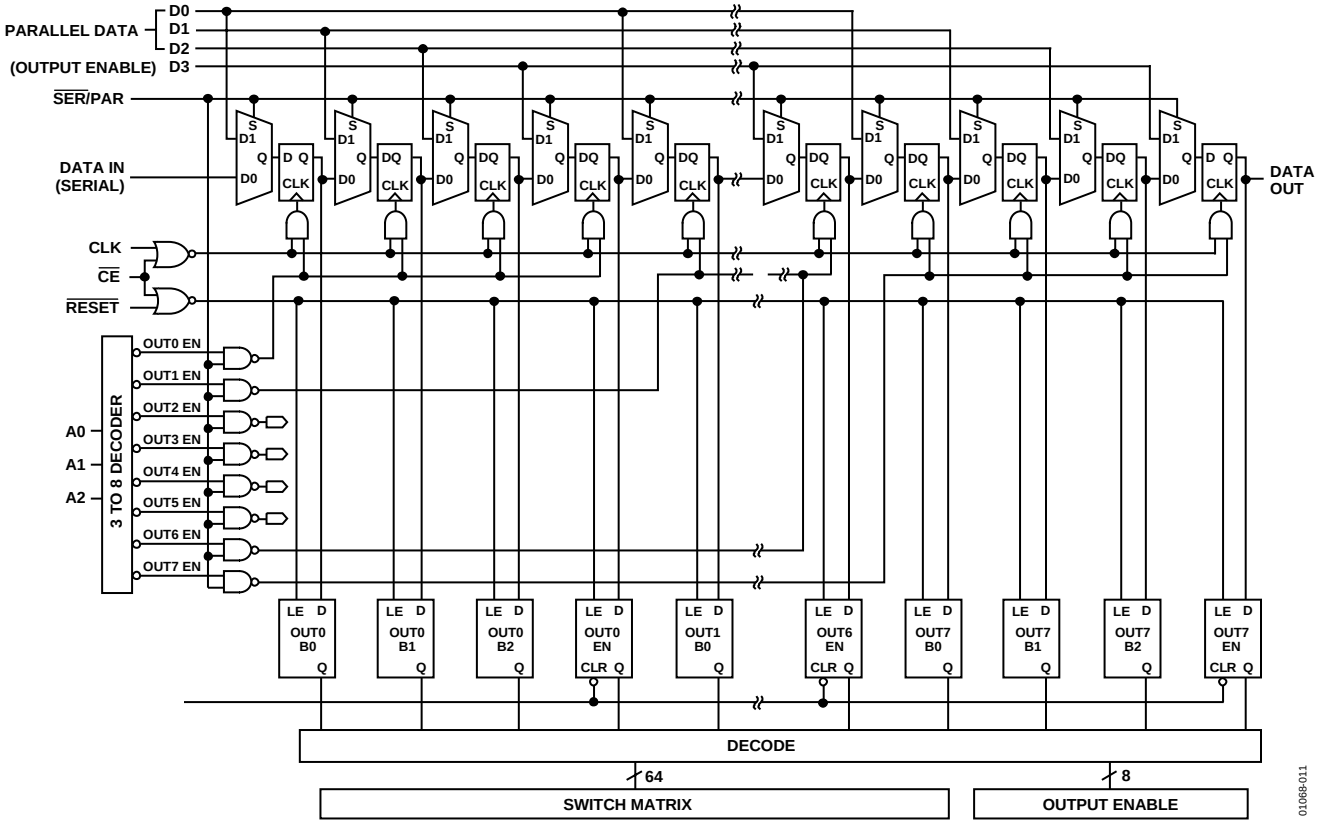


Figure 4. Logic Diagram

ABSOLUTE MAXIMUM RATINGS

Table 7.

Parameter	Rating
Supply Voltage	12.0 V
Internal Power Dissipation[1]	
AD8108/AD8109 80-Lead Plastic LQFP (ST)	2.6 W
Input Voltage	$\pm V_S$
Output Short-Circuit Duration	Observe power derating curves
Storage Temperature Range[2]	−65°C to +125°C

[1] Specification is for device in free air (T_A = 25°C). 80-lead plastic LQFP (ST): θ_{JA} = 48°C/W.
[2] Maximum reflow temperatures are to JEDEC industry standard J-STD-020.

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

MAXIMUM POWER DISSIPATION

The maximum power that can be safely dissipated by the AD8108/AD8109 is limited by the associated rise in junction temperature. The maximum safe junction temperature for plastic encapsulated devices is determined by the glass transition temperature of the plastic, approximately 125°C. Temporarily exceeding this limit may cause a shift in parametric performance due to a change in the stresses exerted on the die by the package. Exceeding a junction temperature of 125°C for an extended period can result in device failure.

While the AD8108/AD8109 are internally short-circuit protected, this may not be sufficient to guarantee that the maximum junction temperature (125°C) is not exceeded under all conditions. To ensure proper operation, it is necessary to observe the maximum power derating curves shown in Figure 5.

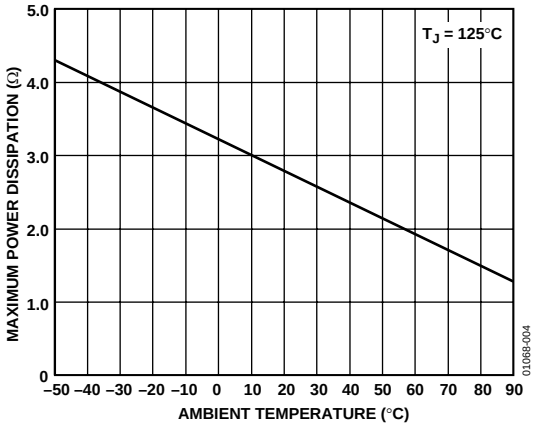


Figure 5. Maximum Power Dissipation vs. Temperature

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

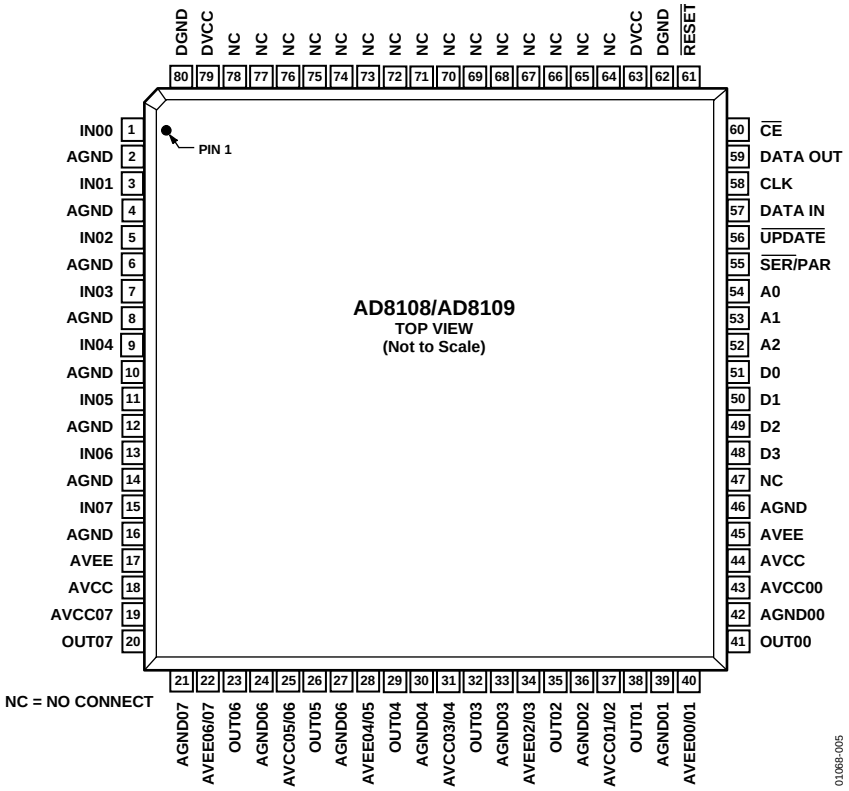


Figure 6. Pin Configuration

Table 8. Pin Function Descriptions

Pin No.	Mnemonic	Description
1, 3, 5, 7, 9, 11, 13, 15	INxx	Analog Inputs. xx = Channels 00 through 07.
57	DATA IN	Serial Data Input, TTL Compatible.
58	CLK	Clock, TTL Compatible. Falling edge triggered.
59	DATA OUT	Serial Data Output, TTL Compatible.
56	UPDATE	Enable (Transparent) Low. Allows serial register to connect directly to switch matrix. Data latched when high.
61	$\overline{\text{RESET}}$	Disable Outputs, Active Low.
60	$\overline{\text{CE}}$	Chip Enable, Enable Low. Must be low to clock in and latch data.
55	$\overline{\text{SER}}$/PAR	Selects Serial Data Mode, Low or Parallel, High. Must be connected.
41, 38, 35, 32, 29, 26, 23, 20	OUTyy	Analog Outputs. yy = Channels 00 through 07.
2, 4, 6, 8, 10, 12, 14, 16, 46	AGND	Analog Ground for Inputs and Switch Matrix.
63, 79	DVCC	5 V for Digital Circuitry
62, 80	DGND	Ground for Digital Circuitry
17, 45	AVEE	−5 V for Inputs and Switch Matrix.
18, 44	AVCC	+5 V for Inputs and Switch Matrix.
42, 39, 36, 33, 30, 27, 24, 21	AGNDxx	Ground for Output Amp. xx = Output Channels 00 through 07. Must be connected.
43, 37, 31, 25, 19	AVCCxx/yy	+5 V for Output Amplifier that is Shared by Channels xx and yy. Must be connected.
40, 34, 28, 22	AVEExx/yy	−5 V for Output Amplifier that is Shared by Channels xx and yy. Must be connected.
54	A0	Parallel Data Input, TTL Compatible (output select LSB).
53	A1	Parallel Data Input, TTL Compatible (output select).
52	A2	Parallel Data Input, TTL Compatible (output select MSB).
51	D0	Parallel Data Input, TTL Compatible (input select LSB).
50	D1	Parallel Data Input, TTL Compatible (input select).
49	D2	Parallel Data Input, TTL Compatible (input select MSB).
48	D3	Parallel Data Input, TTL Compatible (output enable).
47, 64 to 78	NC	No Connect.

TYPICAL PERFORMANCE CHARACTERISTICS

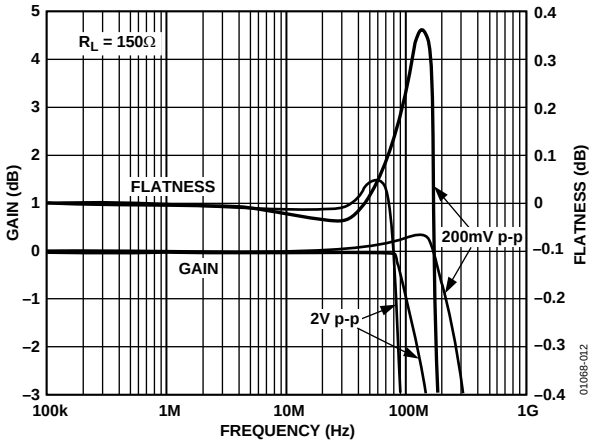


Figure 7. AD8108 Frequency Response

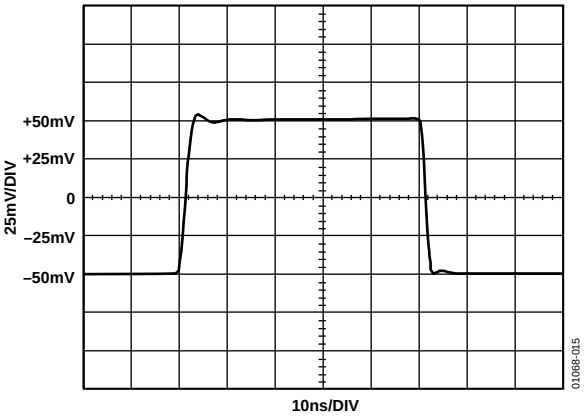


Figure 10. AD8108 Step Response, 100 mV Step

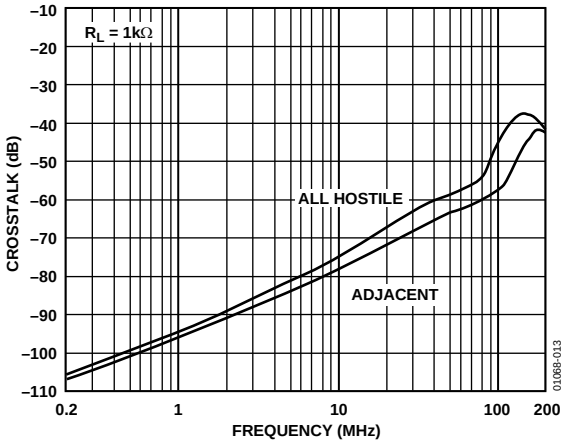


Figure 8. AD8108 Crosstalk vs. Frequency

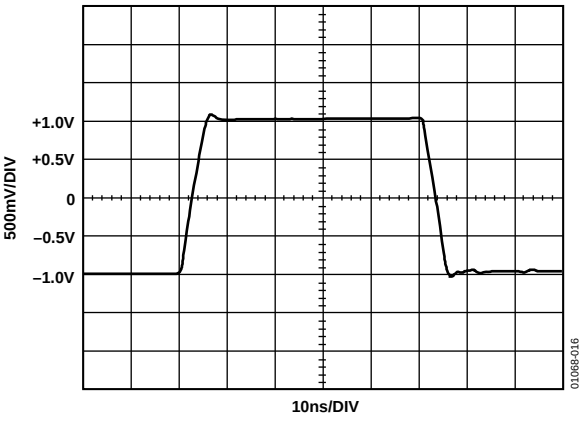


Figure 11. AD8108 Step Response, 2 V Step

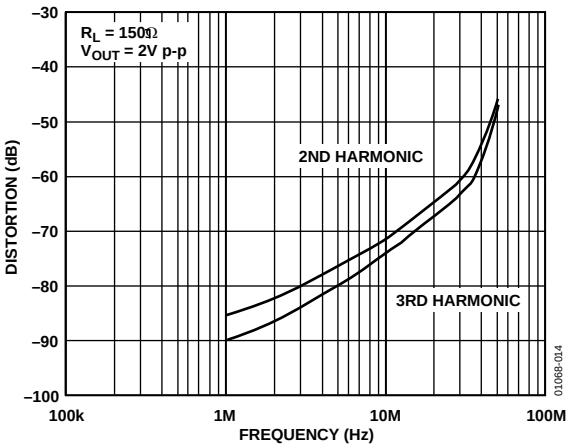


Figure 9. AD8108 Distortion vs. Frequency

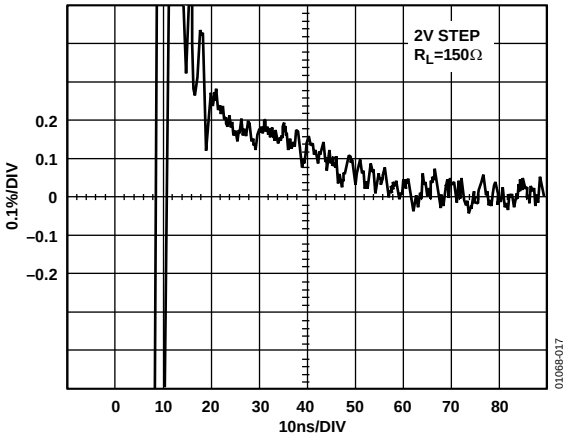


Figure 12. AD8108 Settling Time

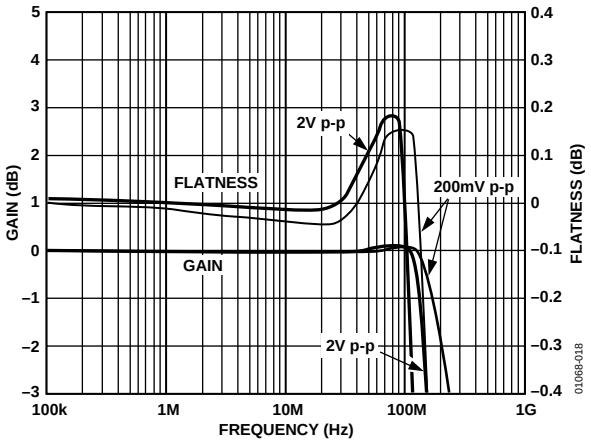


Figure 13. AD8109 Frequency Response

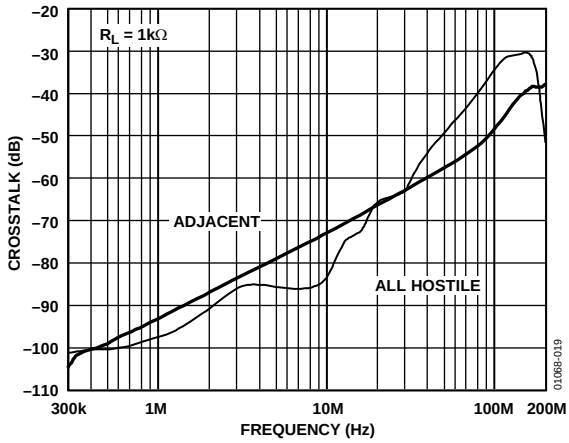


Figure 14. AD8109 Crosstalk vs. Frequency

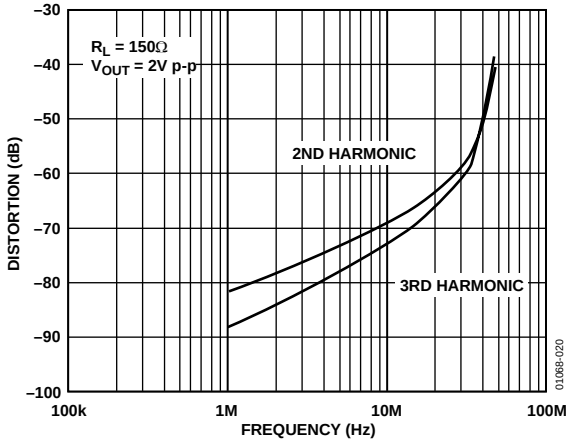


Figure 15. AD8109 Distortion vs. Frequency

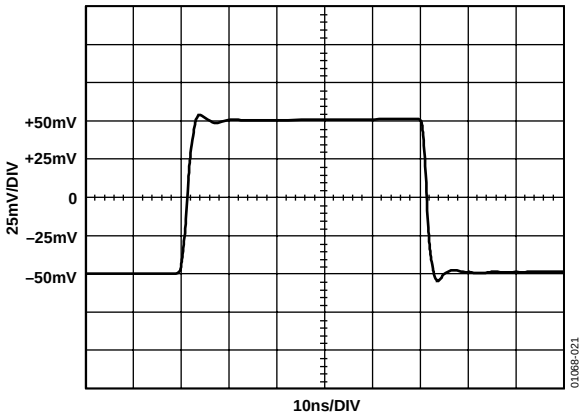


Figure 16. AD8109 Step Response, 100 mV Step

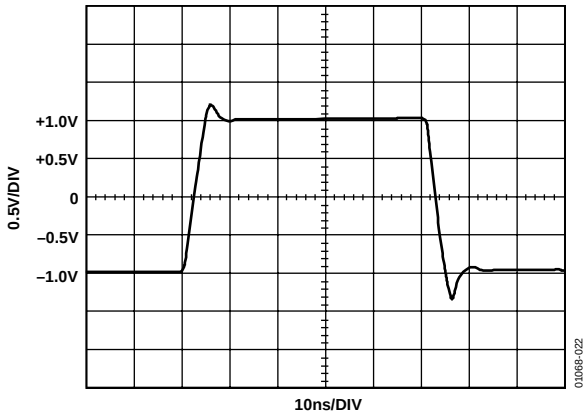


Figure 17. AD8109 Step Response, 2 V Step

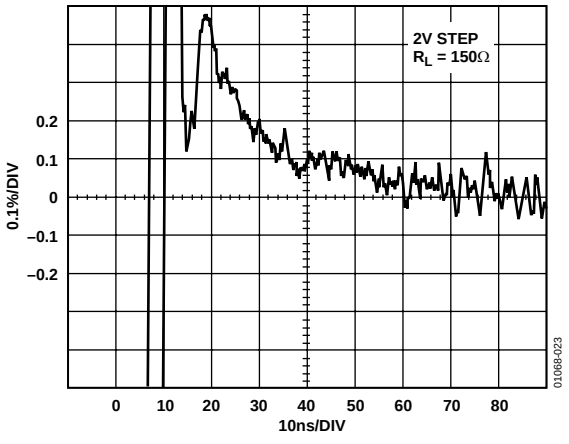


Figure 18. AD8109 Settling Time

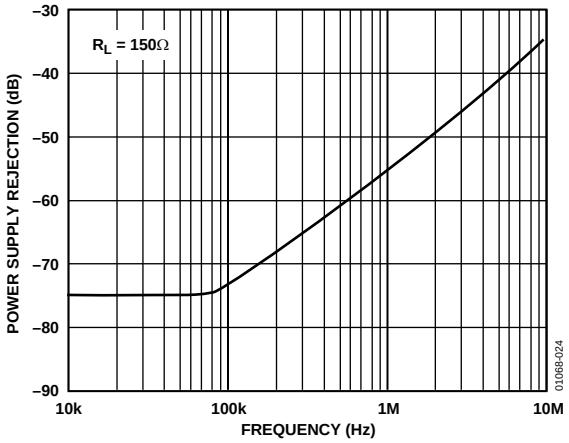


Figure 19. AD8108 PSRR vs. Frequency

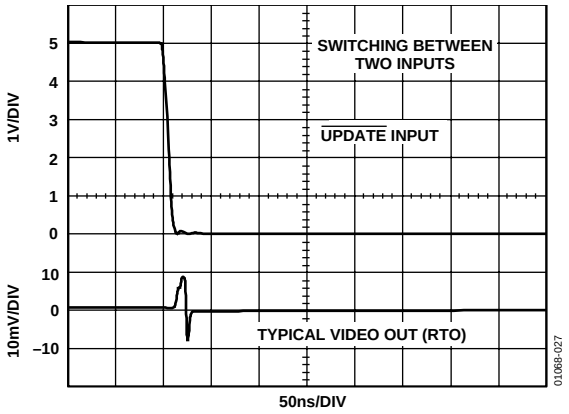


Figure 22. AD8108 Switching Transient (Glitch)

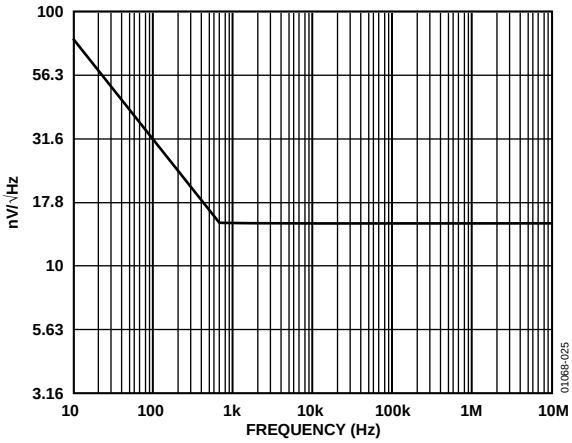


Figure 20. AD8108 Voltage Noise vs. Frequency

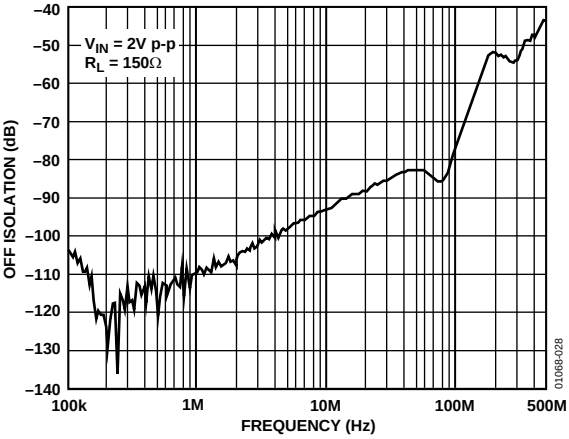


Figure 23. AD8108 Off Isolation, Input-Output

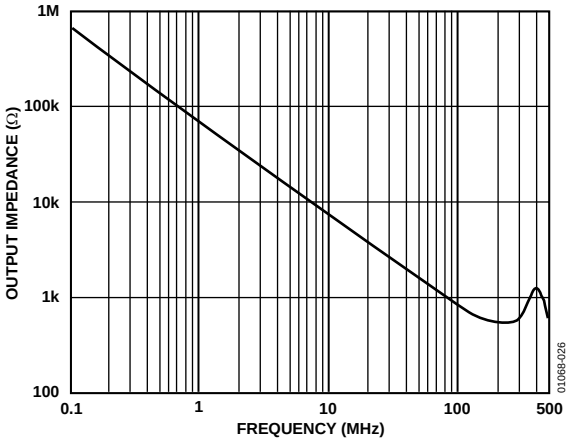


Figure 21. AD8108 Output Impedance, Disabled

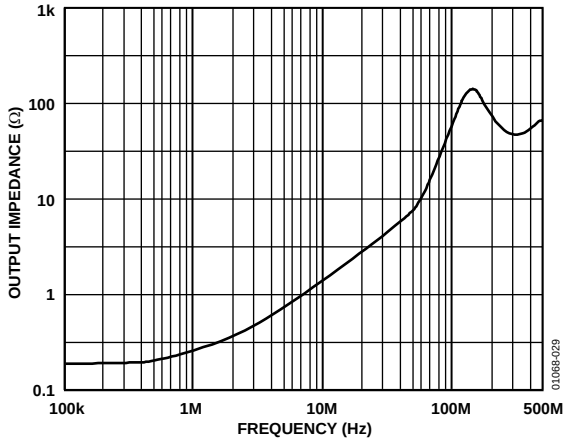


Figure 24. AD8108 Output Impedance, Enabled

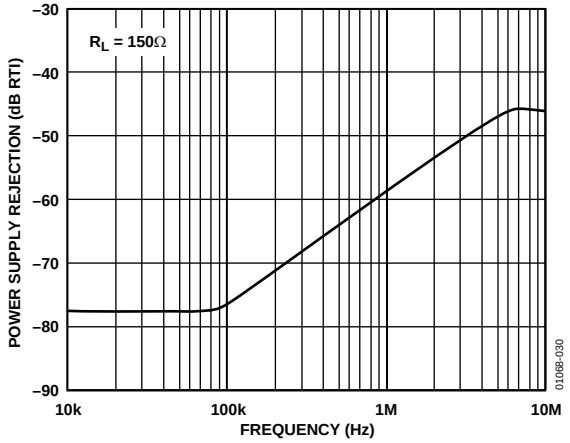


Figure 25. AD8109 PSRR vs. Frequency

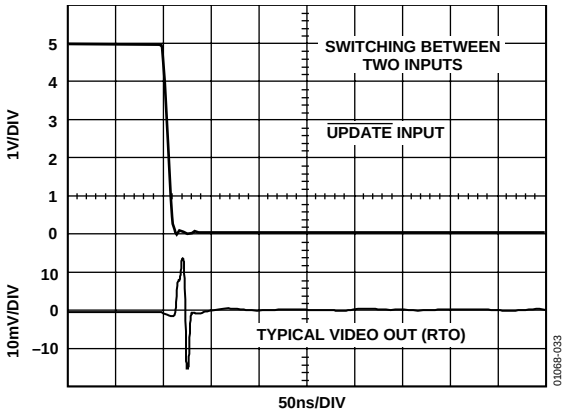


Figure 28. AD8109 Switching Transient (Glitch)

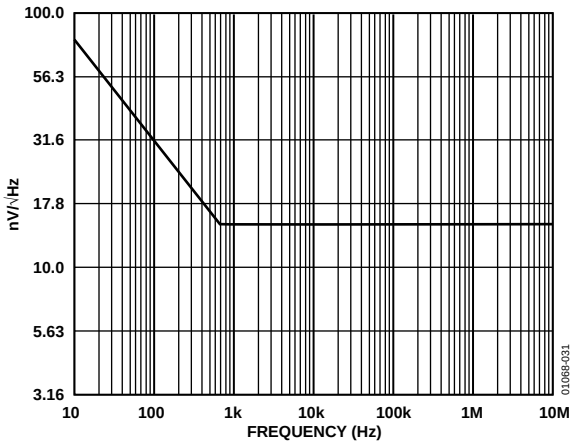


Figure 26. AD8109 Voltage Noise vs. Frequency

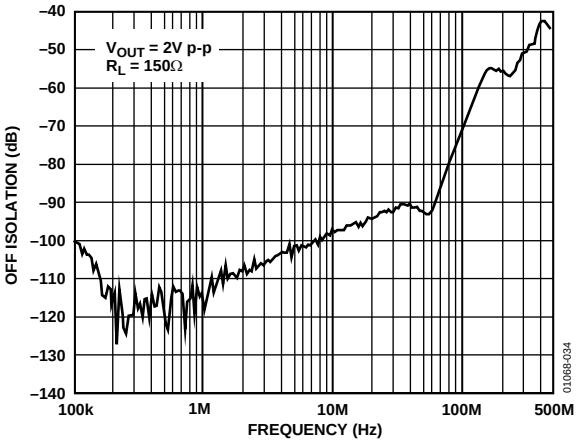


Figure 29. AD8109 Off Isolation, Input-Output

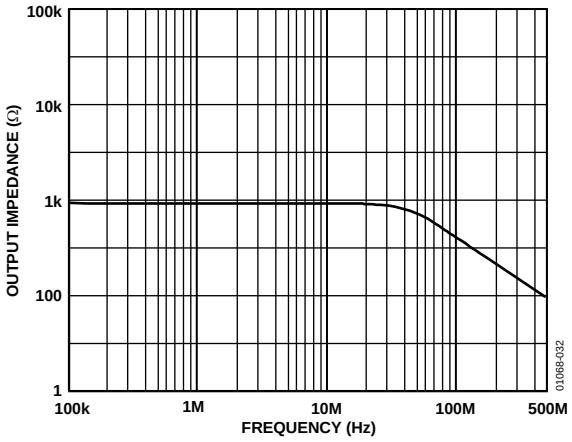


Figure 27. AD8109 Output Impedance, Disabled

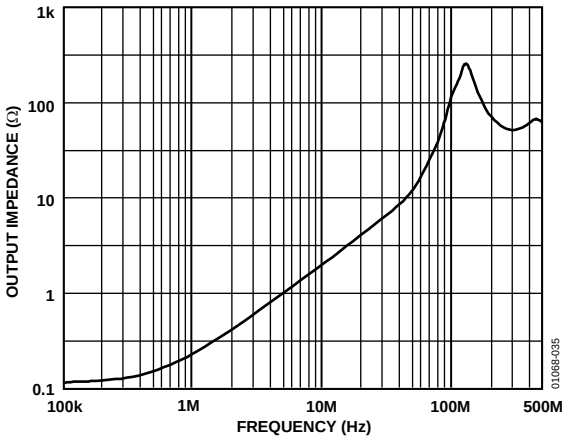


Figure 30. AD8109 Output Impedance, Enabled

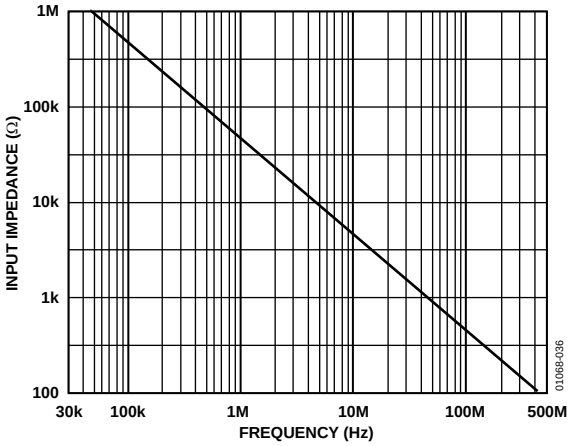


Figure 31. AD8108 Input Impedance vs. Frequency

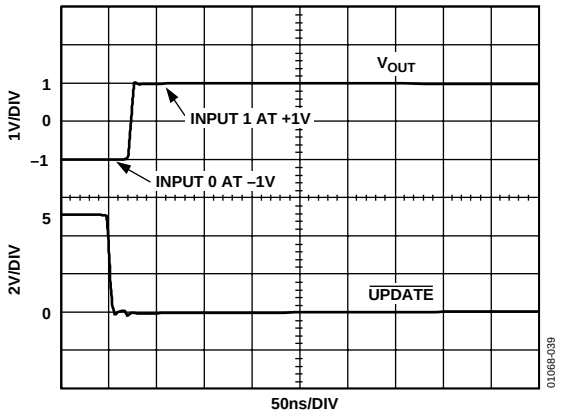


Figure 34. AD8108 Switching Time

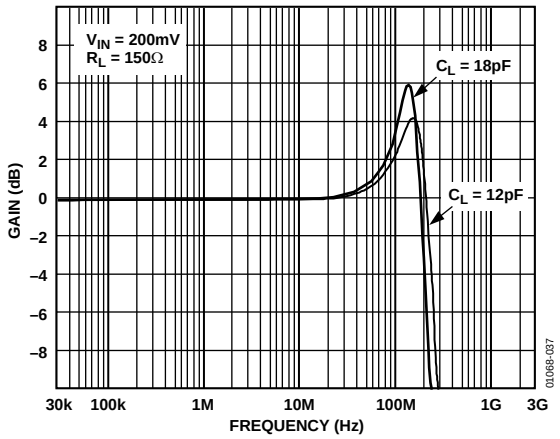


Figure 32. AD8108 Frequency Response vs. Capacitive Load

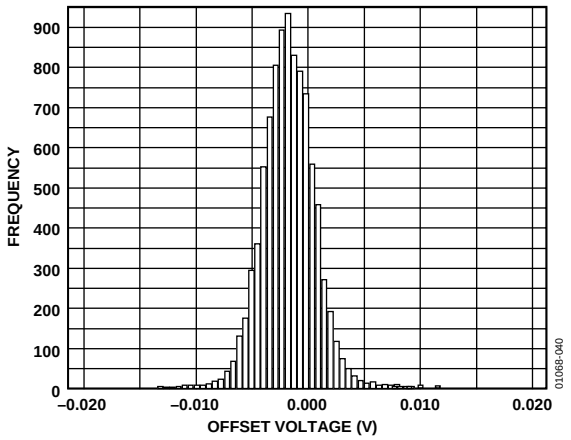


Figure 35. AD8108 Offset Voltage Distribution

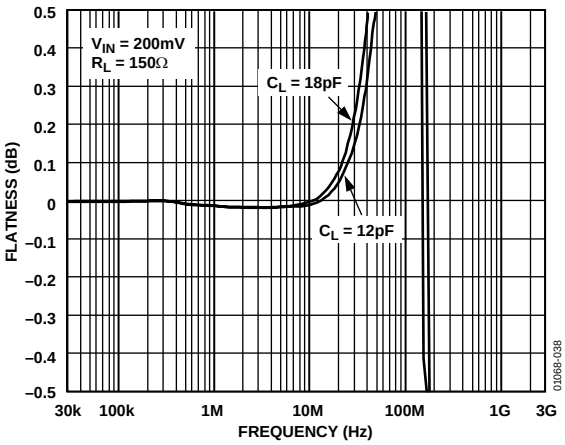


Figure 33. AD8108 Flatness vs. Capacitive Load

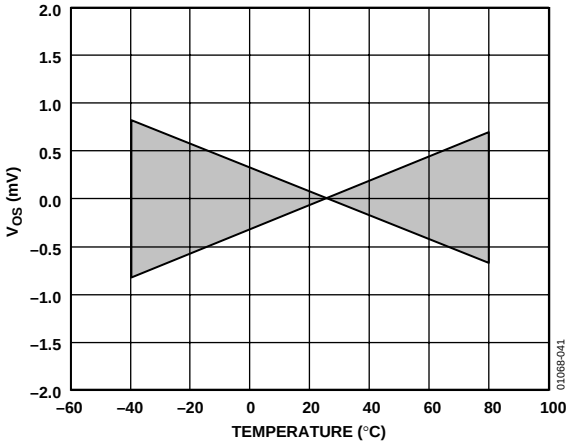


Figure 36. AD8108 Offset Voltage Drift vs. Temperature (Normalized at 25°C)

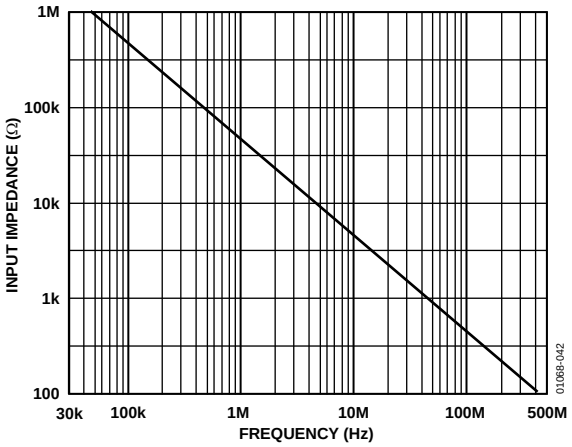


Figure 37. AD8109 Input Impedance vs. Frequency

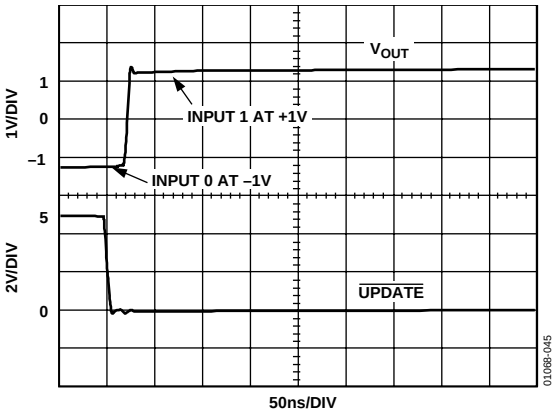


Figure 40. AD8109 Switching Time

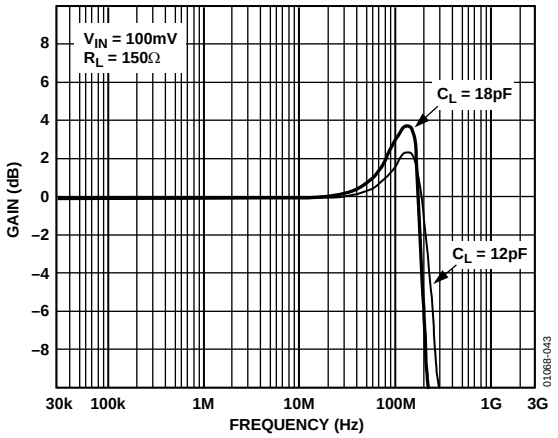


Figure 38. AD8109 Frequency Response vs. Capacitive Load

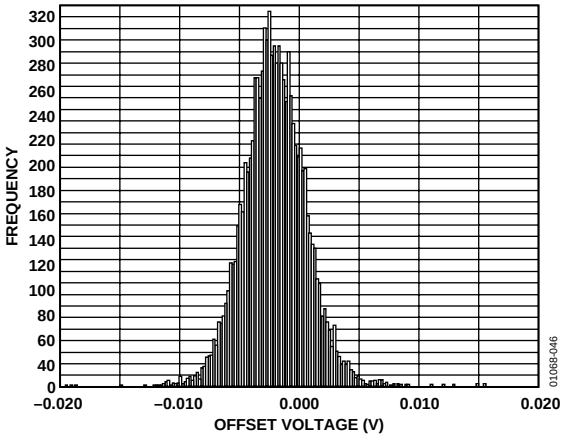


Figure 41. AD8109 Offset Voltage Distribution (RTI)

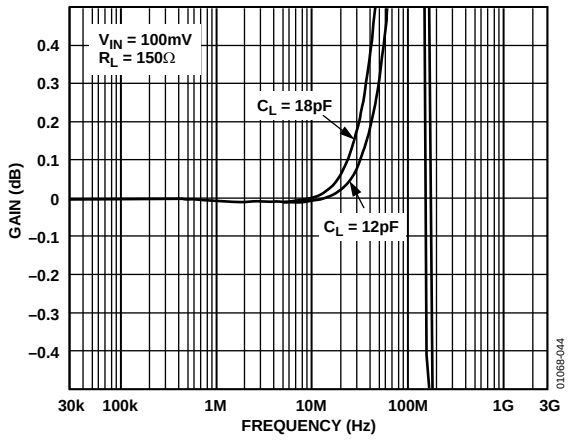


Figure 39. AD8109 Flatness vs. Capacitive Load

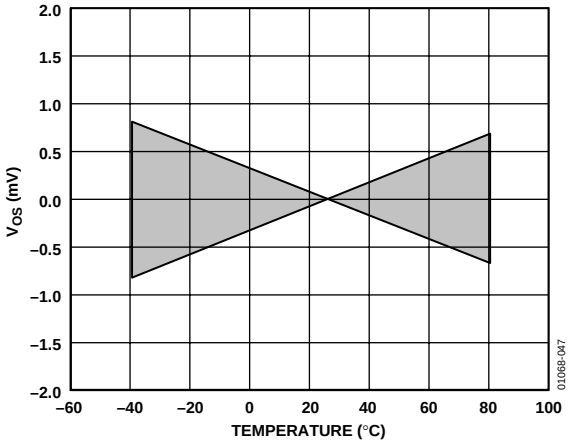


Figure 42. AD8109 Offset Voltage Drift vs. Temperature (Normalized at 25°C)

INPUT/OUTPUT SCHEMATICS

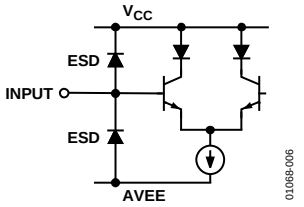


Figure 43. Analog Input

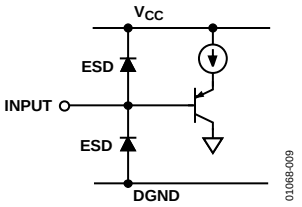


Figure 46. Logic Input

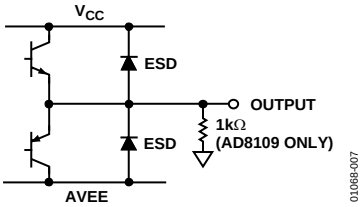


Figure 44. Analog Output

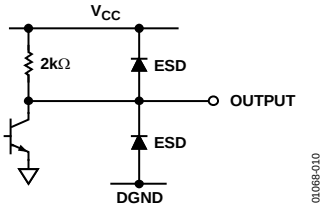


Figure 47. Logic Output

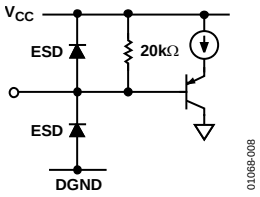


Figure 45. Reset Input

THEORY OF OPERATION

The AD8108 (G = 1) and AD8109 (G = 2) share a common core architecture consisting of an array of 64 transconductance (gm) input stages organized as eight 8:1 multiplexers with a common 8-line analog input bus. Each multiplexer is basically a folded-cascode, high impedance voltage feedback amplifier with eight input stages. The input stages are NPN differential pairs whose differential current outputs are combined at the output stage, which contains the high impedance node, compensation and a complementary emitter follower output buffer. In the AD8108, the output of each multiplexer is fed back directly to the inverting inputs of its eight gm stages. In the AD8109, the feedback network is a voltage divider consisting of two equal resistors.

This switched-gm architecture results in a low power crosspoint switch that is able to directly drive a back terminated video load (150 Ω) with low distortion (differential gain and differential phase errors are better than 0.02% and 0.02°, respectively). This design also achieves high input resistance and low input capacitance without the signal degradation and power dissipation of additional input buffers. However, the small input bias current at any input increases almost linearly with the number of outputs programmed to that input.

The output disable feature of these crosspoints allows larger switch matrices to be built by simply busing together the outputs of multiple 8 × 8 ICs. However, while the disabled output impedance of the AD8108 is very high (10 MΩ), that of the AD8109 is limited by the resistive feedback network (which has a nominal total resistance of 1 kΩ) that appears in parallel with the disabled output. If the outputs of multiple AD8109 devices are connected through separate back termination resistors, the loading due to these finite output impedances lowers the effective back termination impedance of the overall matrix. This problem is eliminated if the outputs of multiple AD8109 devices are connected directly and share a single back termination resistor for each output of the overall matrix. This configuration increases the capacitive loading of the disabled AD8109 devices on the output of the enabled AD8109.

APPLICATIONS

The AD8108/AD8109 have two options for changing the programming of the crosspoint matrix. In the first, a serial word of 32 bits can be provided that updates the entire matrix each time. The second option allows for changing the programming of a single output via a parallel interface. The serial option requires fewer signals, but requires more time (clock cycles) for changing the programming, while the parallel programming technique requires more signals, but can change a single output at a time and requires fewer clock cycles to complete programming.

Serial Programming

The serial programming mode uses the device pins $\overline{\text{CE}}$, CLK, DATA IN, $\overline{\text{UPDATE}}$, and $\overline{\text{SER}}$/PAR. The first step is to assert a low on $\overline{\text{SER}}$/PAR to enable the serial programming mode. $\overline{\text{CE}}$ for the chip must be low to allow data to be clocked into the device. The $\overline{\text{CE}}$ signal can be used to address an individual device when devices are connected in parallel.

The $\overline{\text{UPDATE}}$ signal should be high during the time that data is shifted into the serial port of the device. Although the data still shifts in when $\overline{\text{UPDATE}}$ is low, the transparent, asynchronous latches allow the shifting data to reach the matrix. This causes the matrix to try to update to every intermediate state as defined by the shifting data.

The data at DATA IN is clocked in at every down edge of CLK. A total of 32 data bits must be shifted in to complete the programming. For each of the eight outputs, there are three bits (D0 to D2) that determine the source of its input followed by one bit (D3) that determines the enabled state of the output. If D3 is low (output disabled), the three associated bits (D0 to D2) do not matter because no input is switched to that output.

The most significant output address data is shifted in first and is followed in sequence until the least significant output address data is shifted in. At this point, $\overline{\text{UPDATE}}$ can be taken low, which causes the programming of the device according to the data that was just shifted in. The $\overline{\text{UPDATE}}$ registers are asynchronous, and when $\overline{\text{UPDATE}}$ is low, they are transparent.

If more than one AD8108/AD8109 device is to be serially programmed in a system, the DATA OUT signal from one device can be connected to the DATA IN of the next device to form a serial chain. All of the CLK, $\overline{\text{CE}}$, $\overline{\text{UPDATE}}$, and $\overline{\text{SER}}$/PAR pins should be connected in parallel and operated as described above. The serial data is input to the DATA IN pin of the first device of the chain, and it ripples on through to the last. Therefore, the data for the last device in the chain should come at the beginning of the programming sequence. The length of the programming sequence is 32 times the number of devices in the chain.

Parallel Programming

While using the parallel programming mode, it is not necessary to reprogram the entire device when making changes to the matrix. In fact, parallel programming allows the modification of a single output at a time. Since this takes only one CLK/$\overline{\text{UPDATE}}$ cycle, significant time savings can be realized by using parallel programming.

One important consideration in using parallel programming is that the $\overline{\text{RESET}}$ signal does not reset all registers in the AD8108/AD8109. When taken low, the $\overline{\text{RESET}}$ signal only sets each

output to the disabled state. This is helpful during power-up to ensure that two parallel outputs are not active at the same time.

After initial power-up, the internal registers in the device generally has random data, even though the $\overline{\text{RESET}}$ signal was asserted. If parallel programming is used to program one output, that output is properly programmed, but the rest of the device has a random program state depending on the internal register content at power-up. Therefore, when using parallel programming, it is essential that all outputs be programmed to a desired state after power-up. This ensures that the programming matrix is always in a known state. From then on, parallel programming can be used to modify a single, or more, output at a time.

In a similar fashion, if both $\overline{\text{CE}}$ and $\overline{\text{UPDATE}}$ are taken low after initial power-up, the random power-up data in the shift register is programmed into the matrix. Therefore, to prevent the crosspoint from being programmed into an unknown state, do not apply low logic levels to both $\overline{\text{CE}}$ and $\overline{\text{UPDATE}}$ after power is initially applied. Programming the full shift register one time to a desired state by either serial or parallel programming after initial power-up eliminates the possibility of programming the matrix to an unknown state.

To change the programming of an output via parallel programming, $\overline{\text{SER}}$/PAR and $\overline{\text{UPDATE}}$ should be taken high and $\overline{\text{CE}}$ should be taken low. The CLK signal should be in the high state. The address of the output that is to be programmed should be put on A0 to A2. The first three data bits (D0 to D2) should contain the information that identifies the input that is programmed to the output that is addressed. The fourth data bit (D3) determines the enabled state of the output. If D3 is low (output disabled), the data on D0 to D2 does not matter.

After the desired address and data signals have been established, they can be latched into the shift register by a high to low transition of the CLK signal. The matrix is not programmed, however, until the $\overline{\text{UPDATE}}$ signal is taken low. Thus, it is possible to latch in new data for several or all of the outputs first via successive negative transitions of CLK while $\overline{\text{UPDATE}}$ is held high, and then have all the new data take effect when $\overline{\text{UPDATE}}$ goes low. This technique should be used when programming the device for the first time after power-up when using parallel programming.

POWER-ON $\overline{\text{RESET}}$

When powering up the AD8108/AD8109, it is usually desirable to have the outputs come up in the disabled state. When taken low, the $\overline{\text{RESET}}$ pin causes all outputs to be in the disabled state. However, the $\overline{\text{RESET}}$ signal does not reset all registers in the AD8108/AD8109. This is important when operating in the parallel programming mode. Please refer to that section for information about programming internal registers after power-up. Serial programming programs the entire matrix each time, so no special considerations apply.

Since the data in the shift register is random after power-up, it should not be used to program the matrix, or the matrix can enter unknown states. To prevent this, do not apply logic low signals to both $\overline{\text{CE}}$ and $\overline{\text{UPDATE}}$ initially after power-up. The shift register should first be loaded with the desired data, and then $\overline{\text{UPDATE}}$ can be taken low to program the device.

The $\overline{\text{RESET}}$ pin has a 20 kΩ pull-up resistor to DVDD that can be used to create a simple power-up reset circuit. A capacitor from $\overline{\text{RESET}}$ to ground holds $\overline{\text{RESET}}$ low for some time while the rest of the device stabilizes. The low condition causes all the outputs to be disabled. The capacitor then charges through the pull-up resistor to the high state, thus allowing full programming capability of the device.

GAIN SELECTION

The 8 × 8 crosspoints come in two versions, depending on the desired gain of the analog circuit paths. The AD8108 device is unity gain and can be used for analog logic switching and other applications where unity gain is desired. The AD8108 can also be used for the input and interior sections of larger crosspoint arrays where termination of output signals is not usually used. The AD8108 outputs have very high impedance when their outputs are disabled.

The AD8109 can be used for devices that is used to drive a terminated cable with its outputs. This device has a built-in gain of 2 that eliminates the need for a gain-of-2 buffer to drive a video line. Because of the presence of the feedback network in these devices, the disabled output impedance is about 1 kΩ.

If external amplifiers are used to provide a G = 2, the AD8079 is a fixed gain-of-2 buffer.

CREATING LARGER CROSSPOINT ARRAYS

The AD8108/AD8109 are high density building blocks for creating crosspoint arrays of dimensions larger than 8 × 8. Various features, such as output disable, chip enable, and gain-of-1 and-2 options, are useful for creating larger arrays. For very large arrays, they can be used along with the AD8116, a 16 × 16 video cross-point device. In addition, systems that require more inputs than outputs can use the AD8110 and/or the AD8111, which are (gain-of-1 and gain-of-2) 16 × 8 crosspoint switches.

The first consideration in constructing a larger crosspoint is to determine the minimum number of devices required. The 8 × 8 architecture of the AD8108/AD8109 contains 64 points, which is a factor of 16 greater than a 4 × 1 crosspoint. The PC board area and power consumption savings are readily apparent when compared to using these smaller devices.

For a nonblocking crosspoint, the number of points required is the product of the number of inputs multiplied by the number of outputs. Nonblocking requires that the programming of a given input to one or more outputs does not restrict the availability of that input to be a source for any other outputs.

Some nonblocking crosspoint architectures require more than this minimum as calculated above. Also, there are blocking architectures that can be constructed with fewer devices than this minimum. These systems have connectivity available on a statistical basis that is determined when designing the overall system.

The basic concept in constructing larger crosspoint arrays is to connect inputs in parallel in a horizontal direction and to wire-OR the outputs together in the vertical direction. The meaning of horizontal and vertical can best be understood by looking at a diagram.

An 8 input by 16 output crosspoint array can be constructed as shown in Figure 48. This configuration parallels two inputs per channel and does not require paralleling of any outputs. Inputs are easier to parallel than outputs because there are lower parasitics involved. For a 16 × 8 crosspoint, the AD8110 (gain of 1) or AD8111 (gain of 2) device can be used. These devices are already configured into a 16 × 8 crosspoint in a single device.

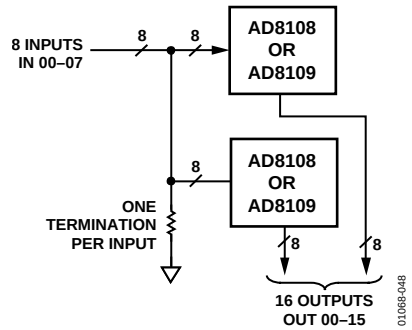


Figure 48. 8 × 16 Crosspoint Array Using Two AD8108 Devices (Unity Gain) or Two AD8109 Devices (Gain of 2)

Figure 49 illustrates a 16 × 16 crosspoint array, while a 24 × 24 crosspoint is illustrated in Figure 50. The 16 × 16 crosspoint requires that each input driver drive two inputs in parallel and each output be wire-OR'ed with one other output. The 24 × 24 crosspoint requires driving three inputs in parallel and having the outputs wire-OR'ed in groups of three. It is required of the system programming that only one output of a wired-OR node be active at a time.

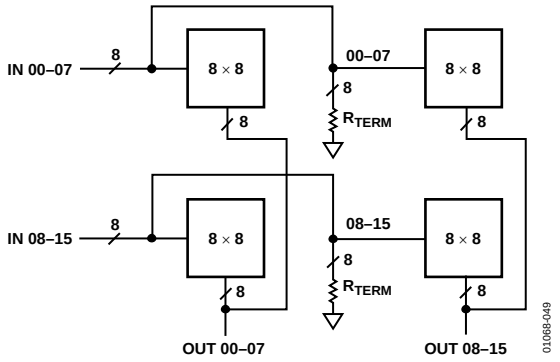


Figure 49. 16 × 16 Crosspoint Array Using Four AD8108 Devices or AD8109 Devices

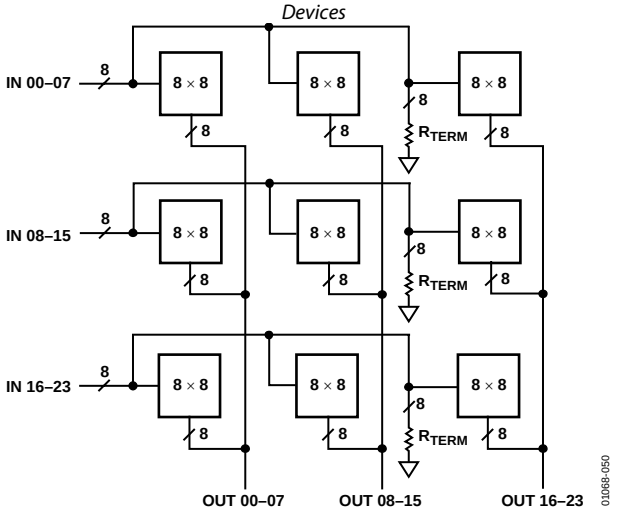


Figure 50. 24 × 24 Crosspoint Array Using Nine AD8108 Devices or AD8109 Devices

At some point, the number of outputs that are wire-OR'ed becomes too great to maintain system performance. This varies according to which system specifications are most important. For example, a 64 × 8 crosspoint can be created with eight AD8108/AD8109 devices. This design has 64 separate inputs and has the corresponding outputs of each device wire-OR'ed together in groups of eight.

Using additional crosspoint devices in the design can lower the number of outputs that must be wire-OR'ed together. Figure 51 shows a block diagram of a system using eight AD8108 devices and two AD8109 devices to create a nonblocking, gain-of-2, 64 × 8 crosspoint that restricts the wire-OR'ing at the output to only four outputs. The rank 1 wire-OR'ed devices are AD8108 devices, which have higher disabled output impedance than the AD8109.

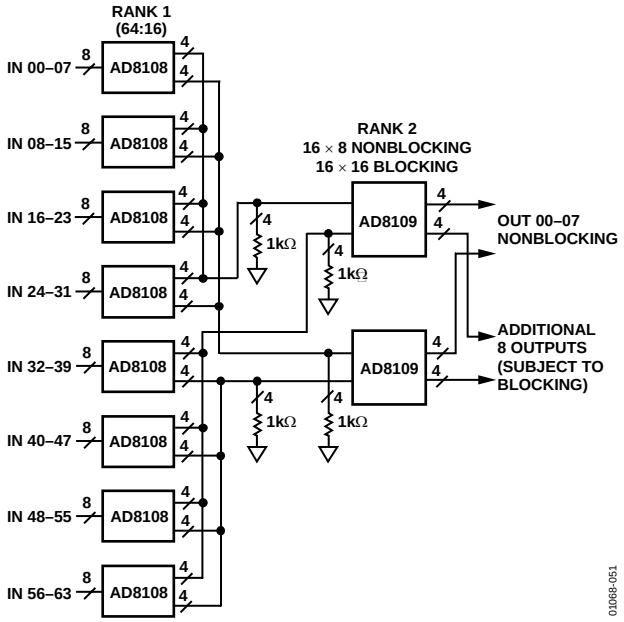


Figure 51. Nonblocking 64 × 8 Array with Gain of 2 (64 × 16 Blocking)

Additionally, by using the lower four outputs from each of the two rank 2 AD8109 devices, a blocking 64 × 16 crosspoint array can be realized. There are, however, some drawbacks to this technique. The offset voltages of the various cascaded devices accumulate, and the bandwidth limitations of the devices compound. In addition, the extra devices consume more current and take up more board space. Once again, the overall system design specifications determine how to make the various tradeoffs.

MULTICHANNEL VIDEO

The excellent video specifications of the AD8108/AD8109 make them ideal candidates for creating composite video crosspoint switches. These can be made quite dense by taking advantage of the high level of integration of the AD8108/AD8109 and the fact that composite video requires only one crosspoint channel per system video channel. There are, however, other video formats that can be routed with the AD8108/AD8109 requiring more than one crosspoint channel per video channel.

Some systems use twisted-pair wiring to carry video signals. These systems utilize differential signals and can lower costs because they use lower cost cables, connectors, and termination methods. They also have the ability to lower crosstalk and reject common-mode signals, which can be important for equipment that operates in noisy environments or where common-mode voltages are present between transmitting and receiving equipment.

In such systems, the video signals are differential; there is a positive and negative (or inverted) version of the signals. These complementary signals are transmitted onto each of the two wires of the twisted pair, yielding a first-order zero common-mode signal. At the receive end, the signals are differentially received and converted back into a single-ended signal.

When switching these differential signals, two channels are required in the switching element to handle the two differential signals that make up the video channel. Thus, one differential video channel is assigned to a pair of crosspoint channels, both input and output. For a single AD8108/AD8109, four differential video channels can be assigned to the eight inputs and eight outputs. This effectively forms a 4 × 4 differential crosspoint switch.

Programming such a device requires that inputs and outputs be programmed in pairs. This information can be deduced by inspection of the programming format of the AD8108/AD8109 and the requirements of the system.

There are other analog video formats requiring more than one analog circuit per video channel. One 2-circuit format that is commonly being used in systems such as satellite TV, digital cable boxes, and higher quality VCRs is called S-video or Y/C video. This format carries the brightness (luminance or Y) portion of the video signal on one channel and the color (chrominance, chroma, or C) on a second channel.

Since S-video also uses two separate circuits for one video channel, creating a crosspoint system requires assigning one video channel to two crosspoint channels, as in the case of a differential video system. Aside from the nature of the video format, other aspects of these two systems are the same.

There are yet other video formats using three channels to carry the video information. Video cameras produce RGB (red, green, blue) directly from the image sensors. RGB is also the usual format used by computers internally for graphics. RGB can be converted to Y, R-Y, B-Y format, sometimes called YUV format. These 3-circuit video standards are referred to as component analog video.

The component video standards require three crosspoint channels per video channel to handle the switching function. In a fashion similar to the 2-circuit video formats, the inputs and outputs are assigned in groups of three, and the appropriate logic programming is performed to route the video signals.

CROSSTALK

Many systems, such as broadcast video, that handle numerous analog signal channels have strict requirements for keeping the various signals from influencing any of the others in the system. Crosstalk is the term used to describe the coupling of the signals of other nearby channels to a given channel.

When there are many signals in proximity in a system, as is undoubtedly be the case in a system that uses the AD8108/AD8109, the crosstalk issues can be quite complex. A good understanding of the nature of crosstalk and some definition of terms is required to specify a system that uses one or more AD8108/AD8109 devices.

Types of Crosstalk

Crosstalk can be propagated by means of any of three methods. These fall into the categories of electric field, magnetic field, and sharing of common impedances. This section explains these effects.

Every conductor can be both a radiator of electric fields and a receiver of electric fields. The electric field crosstalk mechanism occurs when the electric field created by the transmitter propagates across a stray capacitance (for example, free space) and couples with the receiver and induces a voltage. This voltage is an unwanted crosstalk signal in any channel that receives it.

Currents flowing in conductors create magnetic fields that circulate around the currents. These magnetic fields then generate voltages in any other conductors whose paths they link. The undesired induced voltages in these other channels are crosstalk signals. The channels that crosstalk can be said to have a mutual inductance that couples signals from one channel to another.

The power supplies, grounds, and other signal return paths of a multichannel system are generally shared by the various channels. When a current from one channel flows in one of these paths, a voltage that is developed across the impedance becomes an input crosstalk signal for other channels that share the common impedance.

All these sources of crosstalk are vector quantities, so the magnitudes cannot simply be added together to obtain the total crosstalk. In fact, there are conditions where driving additional circuits in parallel in a given configuration can actually reduce the crosstalk.

Areas of Crosstalk

A practical AD8108/AD8109 circuit must be mounted to some sort of circuit board to connect it to the power supplies and the measurement equipment. Take great care to create a board that adds minimum crosstalk to the intrinsic device. Note that the crosstalk of a system is a combination of the intrinsic crosstalk of the devices in addition to the circuit board to which they are mounted. It is important to try to separate these two areas of crosstalk when attempting to minimize its effect.

In addition, crosstalk can occur among the inputs to a crosspoint and among the outputs. It can also occur from input to output. Techniques are discussed for diagnosing which part of a system is contributing to crosstalk.

Measuring Crosstalk

Crosstalk is measured by applying a signal to one or more channels and measuring the relative strength of that signal on a desired selected channel. The measurement is usually expressed as dB down from the magnitude of the test signal. The crosstalk is expressed by:

$$|XT| = 20 \log_{10} \left(Asel(s) / Atest(s) \right)$$

where $s = j\omega$ is the Laplace transform variable, $Asel(s)$ is the amplitude of the crosstalk-induced signal in the selected channel, and $Atest(s)$ is the amplitude of the test signal. It can be seen that crosstalk is a function of frequency, but not a function of the magnitude of the test signal (to first order). In addition, the crosstalk signal has a phase relative to the test signal associated with it.

A network analyzer is most commonly used to measure crosstalk over a frequency range of interest. It can provide both magnitude and phase information about the crosstalk signal.

As a crosspoint system or device grows larger, the number of theoretical crosstalk combinations and permutations can become extremely large. For example, in the case of the 8 × 8 matrix of the AD8108/AD8109, we can examine the number of crosstalk terms that can be considered for a single channel, say IN00 input. IN00 is programmed to connect to one of the AD8108/AD8109 outputs where the measurement can be made.

We can first measure the crosstalk terms associated with driving a test signal into each of the other seven inputs one at a time. We can then measure the crosstalk terms associated with driving a parallel test signal into all seven other inputs taken two at a time in all possible combinations, and then three at a time, and so on, until there is only one way to drive a test signal into all seven other inputs.

Each of these cases is legitimately different from the others and might yield a unique value depending on the resolution of the measurement system, but it is hardly practical to measure all these terms and then to specify them. In addition, this describes the crosstalk matrix for just one input channel. A similar crosstalk matrix can be proposed for every other input. In addition, if the possible combinations and permutations for connecting inputs to the other (not used for measurement) outputs are taken into consideration, the numbers rather quickly grow to astronomical proportions. If a larger crosspoint

array of multiple AD8108/AD8109 devices is constructed, the numbers grow larger still.

Obviously, some subset of all these cases must be selected to be used as a guide for a practical measure of crosstalk. One common method is to measure all hostile crosstalk. This term means that the crosstalk to the selected channel is measured while all other system channels are driven in parallel. In general, this yields the worst crosstalk number, but this is not always the case due to the vector nature of the crosstalk signal.

Other useful crosstalk measurements are those created by one nearest neighbor or by the two nearest neighbors on either side. These crosstalk measurements are generally higher than those of more distant channels, so they can serve as a worst-case measure for any other 1-channel or 2-channel crosstalk measurements.

Input and Output Crosstalk

The flexible programming capability of the AD8108/AD8109 can be used to diagnose whether crosstalk is occurring more on the input side or the output side. Some examples are illustrative. A given input channel (IN03 in the middle for this example) can be programmed to drive OUT03. The input to IN03 is just terminated to ground (via 50 Ω or 75 Ω) and no signal is applied.

All the other inputs are driven in parallel with the same test signal (practically this is provided by a distribution amplifier), with all other outputs except OUT03 disabled. Since grounded IN03 is programmed to drive OUT03, there should be no signal present. Any signal that is present can be attributed to the other seven hostile input signals because no other outputs are driven. (They are all disabled.) Thus, this method measures the all-hostile input contribution to crosstalk into IN03. Of course, the method can be used for other input channels and combinations of hostile inputs.

For output crosstalk measurement, a single input channel is driven (IN00, for example) and all outputs other than a given output (IN03 in the middle) are programmed to connect to IN00. OUT03 is programmed to connect to IN07 (far away from IN00), which is terminated to ground. Thus OUT03 should not have a signal present since it is listening to a quiet input. Any signal measured at the OUT03 can be attributed to the output crosstalk of the other seven hostile outputs. Again, this method can be modified to measure other channels and other crosspoint matrix combinations.

Effect of Impedances on Crosstalk

The input side crosstalk can be influenced by the output impedance of the sources that drive the inputs. The lower the impedance of the drive source, the lower the magnitude of the crosstalk. The dominant crosstalk mechanism on the input side is capacitive coupling. The high impedance inputs do not have significant current flow to create magnetically induced crosstalk. However, significant current can flow through the input termination resistors and the loops that drive them. Thus, the PC board on the input side can contribute to magnetically coupled crosstalk.

From a circuit standpoint, the input crosstalk mechanism looks like a capacitor coupling to a resistive load. For low frequencies, the magnitude of the crosstalk is given by

$$|XT| = 20 \log_{10} \left(\left(R_S \; C_M \right) \times s \right)$$

where R_S is the source resistance, C_M is the mutual capacitance between the test signal circuit and the selected circuit, and s is the Laplace transform variable.

From the equation, it can be observed that this crosstalk mechanism has a high-pass nature; it can be minimized by reducing the coupling capacitance of the input circuits and lowering the output impedance of the drivers. If the input is driven from a 75 Ω terminated cable, the input crosstalk can be reduced by buffering this signal with a low output impedance buffer.

On the output side, the crosstalk can be reduced by driving a lighter load. Although the AD8108/AD8109 is specified with excellent differential gain and phase when driving a standard 150 Ω video load, the crosstalk is higher than the minimum obtainable due to the high output currents. These currents induce crosstalk via the mutual inductance of the output pins and bond wires of the AD8108/AD8109.

From a circuit standpoint, this output crosstalk mechanism looks like a transformer, with a mutual inductance between the windings, that drives a load resistor. For low frequencies, the magnitude of the crosstalk is given by

$$|XT| = 20 \log_{10} \left(Mxy \times s / R_L \right)$$

where Mxy is the mutual inductance of Output x to Output y, and R_L is the load resistance on the measured output. This crosstalk mechanism can be minimized by keeping the mutual inductance low and increasing R_L. The mutual inductance can be kept low by increasing the spacing of the conductors and minimizing their parallel length.

PCB LAYOUT

Extreme care must be exercised to minimize additional crosstalk generated by the system circuit board(s). The areas that must be carefully detailed are grounding, shielding, signal routing, and supply bypassing.

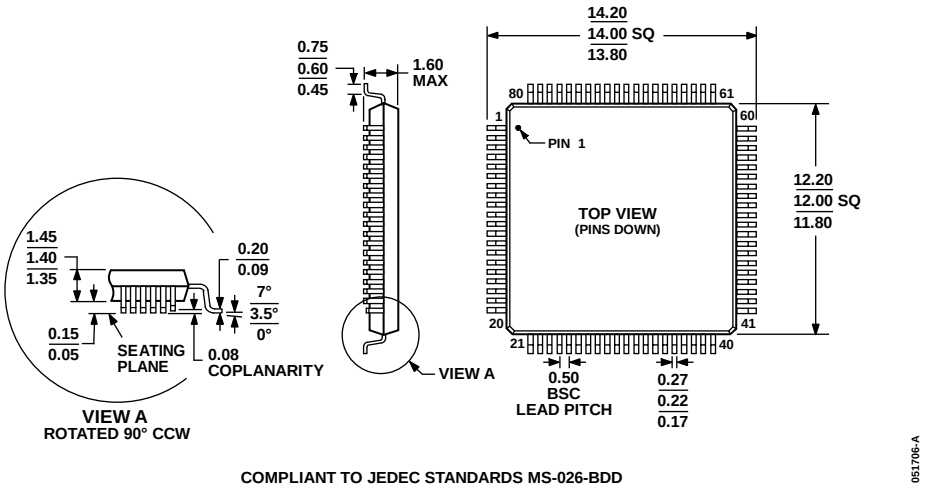
The packaging of the AD8108/AD8109 is designed to help keep the crosstalk to a minimum. Each input is separated from each other input by an analog ground pin. All of these AGNDs should be directly connected to the ground plane of the circuit board. These ground pins provide shielding, low impedance return paths, and physical separation for the inputs. All of these help to reduce crosstalk.

Each output is separated from its two neighboring outputs by an analog ground pin in addition to an analog supply pin of one polarity or the other. Each of these analog supply pins provides power to the output stages of only the two nearest outputs. These supply pins and analog grounds provide shielding, physical separation, and a low impedance supply for the outputs. Individual bypassing of each of these supply pins with a 0.01 µF chip capacitor directly to the ground plane minimizes high frequency output crosstalk via the mechanism of sharing common impedances.

Each output also has an on-chip compensation capacitor that is individually tied to the nearby analog ground pins AGND00 through AGND07. This technique reduces crosstalk by preventing the currents that flow in these paths from sharing a common impedance on the IC and in the package pins. These AGNDxx signals should all be directly connected to the ground plane.

The input and output signals have minimum crosstalk if they are located between ground planes on layers above and below, and separated by ground in between. Vias should be located as close to the IC as possible to carry the inputs and outputs to the inner layer. The only place the input and output signals surface is at the input termination resistors and the output series back-termination resistors. These signals should also be separated, to the extent possible, as soon as they emerge from the IC package.

OUTLINE DIMENSIONS



COMPLIANT TO JEDEC STANDARDS MS-026-BDD

Figure 52. 80-Lead Low Profile Quad Flat Package [LQFP]
(ST-80-1)
Dimensions shown in millimeters

ORDERING GUIDE

Model[1, 2]	Temperature Range	Package Description	Package Option
AD8108ASTZ	−40°C to +85°C	80-Lead Low Profile Quad Flat Package [LQFP]	ST-80-1
AD8109ASTZ	−40°C to +85°C	80-Lead Low Profile Quad Flat Package [LQFP]	ST-80-1

[1] Details of the lead finish composition can be found on the Analog Devices website at www.analog.com by reviewing the Material Description of each relevant package.
[2] Z = RoHS Compliant Part.

NOTES

NOTES

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AD8108ASTZ AD8109ASTZ