



155.52 MHz Frequency Synthesizer

AD809

FEATURES

Frequency Synthesis to 155.52 MHz
19.44 MHz or 9.72 MHz Input
Reference Signal Select Mux
Single Supply Operation: +5 V or -5.2 V
Output Jitter: 2.0 Degrees RMS
Low Power: 90 mW
10 KH ECL/PECL Compatible Output
10 KH ECL/PECL/TTL/CMOS Compatible Input
Package: 16-Pin Narrow 150 Mil SOIC

PRODUCT DESCRIPTION

The AD809 provides a 155.52 MHz ECL/PECL output clock from either a 19.44 MHz or a 9.72 MHz TTL/CMOS/ECL/PECL reference frequency. The AD809 functionality supports a distributed timing architecture, allowing a backplane or PCB 19.44 MHz or 9.72 MHz timing reference signal to be distributed to multiple

155.52 Mbps ports. The AD809 can be applied to create the transmit bit clock for one or more ports.

An input signal multiplexer supports loop-timed applications where a 155.52 MHz transmit bit clock is recovered from the 155.52 Mbps received data.

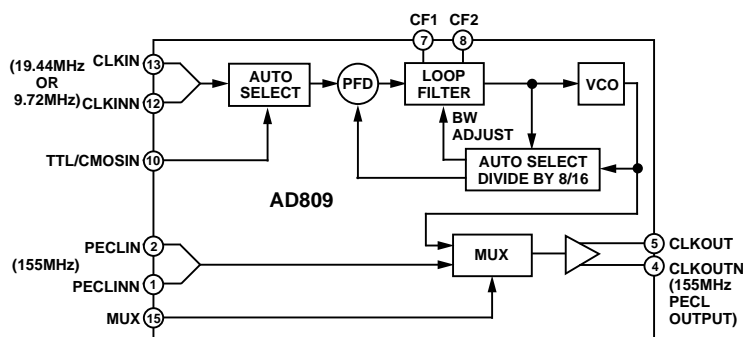
The low jitter VCO, low power and wide operating temperature range make the device suitable for generating a 155.52 MHz bit clock for SONET/SDH/Fiber in the Loop systems.

The device has a low cost, on-chip VCO that locks to either 8 \times or 16 \times the frequency at the 19.44 MHz or 9.72 MHz input. No external components are needed for frequency synthesis; however, the user can adjust loop dynamics through selection of a damping factor capacitor whose value determines loop damping.

The AD809 design guarantees that the clock output frequency will drift low (by roughly 20%) in the absence of a signal at the input.

The AD809 consumes 90 mW and operates from a single power supply at either +5 V or -5.2 V.

FUNCTIONAL BLOCK DIAGRAM



REV. A

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AD809—SPECIFICATIONS ($T_A = T_{MIN}$ to T_{MAX} , $V_S = V_{MIN}$ to V_{MAX} , $C_D = 22$ nF, unless otherwise noted)

| Parameter | Condition | Min | Typ | Max | Units |
|---|--|-------------------|---------------------|------------------------|----------------------------------|
| TRACKING AND CAPTURE RANGE ¹ | ×8 Synthesis ×16 Synthesis | 19.42 9.71 | | 19.46 9.73 | MHz MHz |
| OUTPUT JITTER | ×8 Synthesis ×16 Synthesis | | 1.6 1.6 | 2.9 2.9 | Degrees RMS Degrees RMS |
| JITTER TRANSFER Bandwidth Peaking | $C_D = 5.6$ nF ($\zeta = 5$) $C_D = 22$ nF ($\zeta = 10$) | | 200 0.08 0.02 | | kHz dB dB |
| DUTY CYCLE TOLERANCE | ×8 or ×16 Synthesis Output Jitter ≤ 2.9 Degrees RMS | 15 | | 85 | % |
| INPUT VOLTAGE LEVELS PECL Input Logic High, V_{IH} Input Logic Low, V_{IL} TTL Input Logic High, V_{IH} Input Logic Low, V_{IL} | @ CLKIN/N and PECLIN/N Inputs @ TTL/CMOSIN and MUX Inputs | 3.8 3.1 2.0 | | V_{CC} 3.6 0.8 | Volts Volts Volts Volts |
| OUTPUT VOLTAGE LEVELS PECL Output Logic High, V_{OH} Output Logic Low, V_{OL} | Referenced to V_{CC} | -1.2 -2.0 | -1.0 -1.8 | -0.7 -1.7 | Volts Volts |
| SYMMETRY (Duty Cycle) | ×8 Synthesis or ×16 Synthesis | 46 | 52 | 62 | % % |
| OUTPUT RISE/FALL TIMES 1.5 Rise Time (t_R) Fall Time (t_F) | 20%–80% 80%–20% | | 1.1 1.1 | 1.5 1.5 | ns ns |
| POWER SUPPLY VOLTAGE | V_{MIN} to V_{MAX} | 4.5 | | 5.5 | Volts |
| POWER SUPPLY CURRENT | | | 17 | 26 | mA |
| OPERATING TEMPERATURE RANGE | T_{MIN} to T_{MAX} | -40 | | +85 | °C |

NOTES

¹Device design is guaranteed for operation over Capture Ranges and Tracking Ranges, however the device has wider capture and tracking ranges (for both ×8 and ×16 synthesis).

Specifications subject to change without notice.

ABSOLUTE MAXIMUM RATINGS*

Supply Voltage +12 V
Input Voltage (Pin 12 or Pin 13) $V_{CC} + 0.6$ V
Maximum Junction Temperature. +165°C
Storage Temperature Range -65°C to +150°C
Lead Temperature Range (Soldering 10 sec) +300°C
ESD Rating (Human Body Model) 1500 V

*Stresses above those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Thermal Characteristics:

16-Pin Narrow Body SOIC Package: $\theta_{JA} = 110^\circ\text{C/W}$.

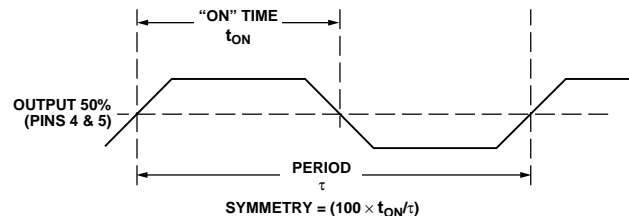


Figure 1. Symmetry

ORDERING GUIDE

| Model | Temperature Range | Package Description | Package Option |
|---------------|-------------------|-------------------------|----------------|
| AD809BR | -40°C to +85°C | 16-Pin Narrow Body SOIC | R-16A |
| AD809BR-REEL7 | -40°C to +85°C | 750 Pieces, 7" Reel | R-16A |

PIN DESCRIPTIONS

| Pin No. | Mnemonic | Description |
|---------|-------------------|--|
| 1 | PECLINN | Differential 155 MHz Input |
| 2 | PECLIN | Differential 155 MHz Input |
| 3 | V _{CC2} | Digital V _{CC} for PECL Outputs |
| 4 | CLKOUTN | Differential 155 MHz Output |
| 5 | CLKOUT | Differential 155 MHz Output |
| 6 | V _{CC1} | Digital V _{CC} for Internal Logic |
| 7 | CF1 | Loop Damping Capacitor |
| 8 | CF2 | Loop Damping Capacitor |
| 9 | AV _{EE} | Analog V _{EE} |
| 10 | TTL/CMOSIN | TTL/CMOS Reference Clock Input |
| 11 | AV _{CC1} | Analog V _{CC} for PLL |
| 12 | CLKINN | PECL Differential Reference Clock Input |
| 13 | CLKIN | PECL Differential Reference Clock Input |
| 14 | AV _{CC2} | Analog V _{CC} for Input Stage |
| 15 | MUX | Input Signal Mux Control Input |
| 16 | V _{EE} | Digital V _{EE} |

PIN CONFIGURATION

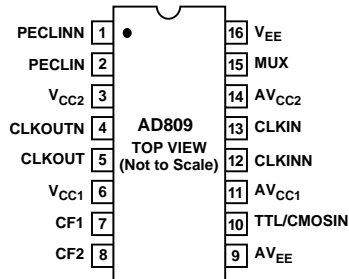


Table I.

| MUX Input | Input Selected |
|-----------|----------------|
| TTL "0" | CLKIN/CLKINN |
| TTL "1" | PECLIN/PECLINN |

Table II. Applying a PECL/ECL or CMOS/TTL Reference Input to the AD809

| Input Reference | AD809 Configuration |
|-----------------------|---|
| PECL/ECL Differential | Apply the valid PECL-level reference frequency to Pins 13 and 12. AD809 frequency synthesizer ignores the input at Pin 10. |
| TTL/CMOS Single-Ended | Apply the reference frequency to Pin 10. Connect Pins 13 and 12 to AV _{EE} (Pins 9 and 16). The AD809 senses the common-mode signal at these pins as less than valid PECL and selects the TTL/CMOS input as active. |

AD809 Phase Skew

The AD809 output is in phase with the input. The falling edge at Pin 4, CLKOUTN, occurs 700 ps before the rising edge at Pin 10, TTL/CMOSIN at 27°C. The phase skew remains relatively constant over temperature. Refer to Table III for phase skew data.

Table III. Phase Skew vs. Temperature

| Temperature (°C) | Skew (CLKOUTN, Pin 4, Relative to TTL/CMOSIN, Pin 10 Measured in ps at Package Pins) |
|------------------|--|
| -35 | -1000 |
| -20 | -950 |
| 0 | -850 |
| 10 | -750 |
| 30 | -700 |
| 50 | -600 |
| 70 | -450 |
| 80 | -450 |
| 90 | -350 |
| 100 | -250 |

CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although the AD809 features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.



AD809

DEFINITION OF TERMS

Maximum, Minimum and Typical Specifications

Specifications for every parameter are derived from statistical analyses of data taken on multiple devices from multiple wafer lots. Typical specifications are the mean of the distribution of the data for that parameter. If a parameter has a maximum (or a minimum), that value is calculated by adding to (or subtracting from) the mean six times the standard deviation of the distribution. This procedure is intended to tolerate production variations: if the mean shifts by 1.5 standard deviations, the remaining 4.5 standard deviations still provide a failure rate of only 3.4 parts per million. For all tested parameters, the test limits are guardbanded to account for tester variation to thus guarantee that no device is shipped outside of data sheet specifications.

Capture and Tracking Range

This is the range of input data rates over which the AD809 will remain in lock.

Jitter

This is the dynamic displacement of digital signal edges from their long term average positions, measured in degrees rms. Jitter on the input clock causes jitter on the synthesized clock.

Output Jitter

This is the jitter on the synthesized clock (OUTPUT, $\overline{\text{OUTPUT}}$), in degrees rms.

Jitter Transfer

The AD809 exhibits a low-pass filter response to jitter applied to its input data.

Bandwidth

This describes the frequency at which the AD809 attenuates sinusoidal input jitter by 3 dB.

Peaking

This describes the maximum jitter gain of the AD809 in dB.

Damping Factor, ζ

Damping factor, ζ describes the compensation of the second order PLL. A larger value of ζ corresponds to more damping and less peaking in the jitter transfer function.

Duty Cycle Tolerance

The AD809 exhibits a duty cycle tolerance that is measured by applying an input signal (nominal input frequency) with a known duty cycle imbalance and measuring the $\times 8$ or $\times 16$ output frequency.

Symmetry-Recovered Clock Duty Cycle

Symmetry is calculated as $(100 \times \text{on time})/\text{period}$, where on time equals the time that the clock signal is greater than the midpoint between its "0" level and its "1" level.

Typical Characteristic Curves

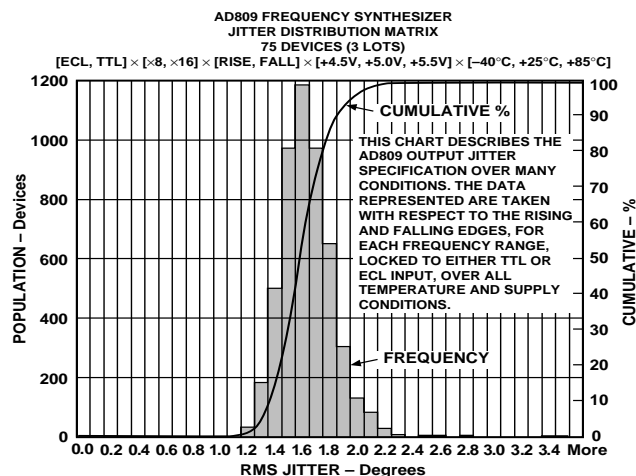


Figure 2. Jitter Histogram

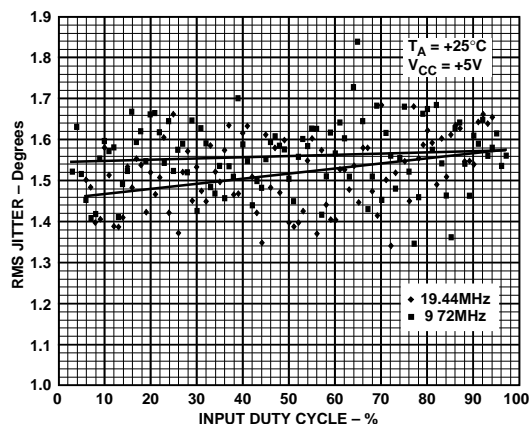


Figure 3. Jitter vs. Input Duty Cycle

USING THE AD809

Ground Planes

Use of one ground plane for connections to both analog and digital grounds is recommended.

Power Supply Connections

Use of a 10 μF capacitor between V_{CC} and ground is recommended. Care should be taken to isolate the +5 V power trace to V_{CC2} (Pin 3). The V_{CC2} pin is used inside the device to provide the CLKOUT/CLKOUTN signals.

Use of a trace connecting Pin 14 and Pin 6 (AV_{CC2} and V_{CC1} respectively) is recommended. Use of 0.1 μF capacitors between IC power supply and ground is recommended. Power supply decoupling should take place as close to the IC as possible. Refer to the schematic, Figure 5, for advised connections.

Transmission Lines

Use of 50 Ω transmission lines are recommended for PECL inputs.

Terminations

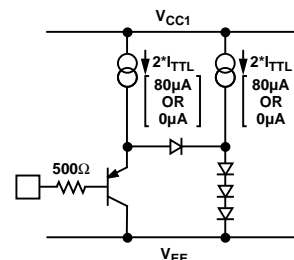
Termination resistors should be used for PECL input signals. Metal, thick film, 1% tolerance resistors are recommended. Termination resistors for the PECL input signals should be placed as close as possible to the PECL input pins.

Connections from the power supply to load resistors for input and output signals should be individual, not daisy chained. This will avoid crosstalk on these signals.

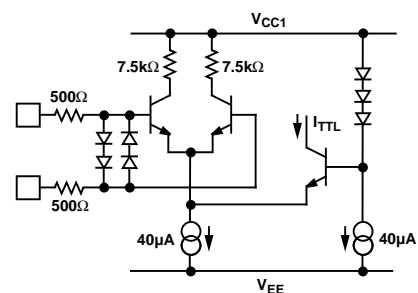
Loop Damping Capacitor, C_D

A ceramic capacitor may be used for the loop damping capacitor. A 22 nF capacitor provides a damping factor of 10.

Synthesizer Input
TTL/CMOSIN



Synthesizer Input
CLKIN/CLKINN
PECL INPUT



PLL Differential
Output Stage—
CLKOUT/CLKOUTN

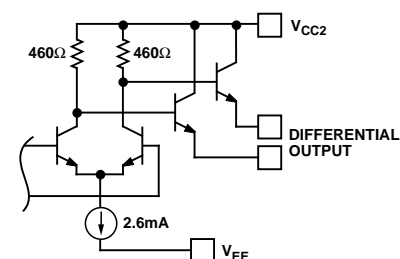


Figure 4. Simplified Schematics

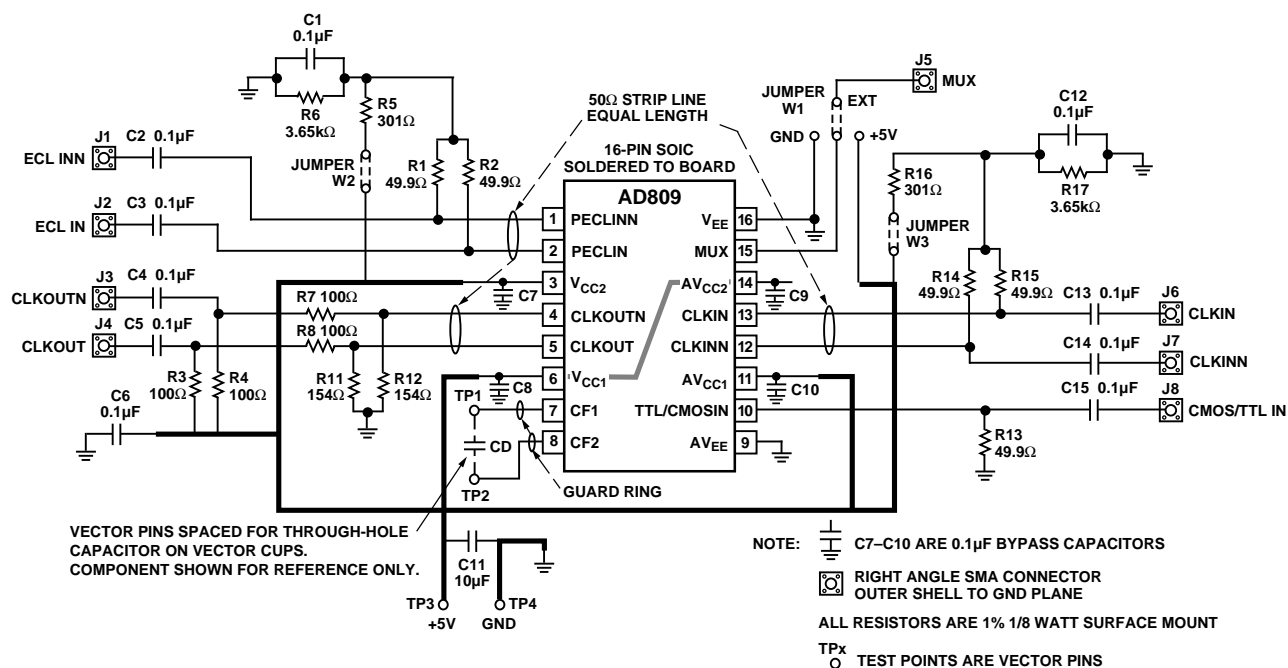


Figure 5. Evaluation Board Schematic

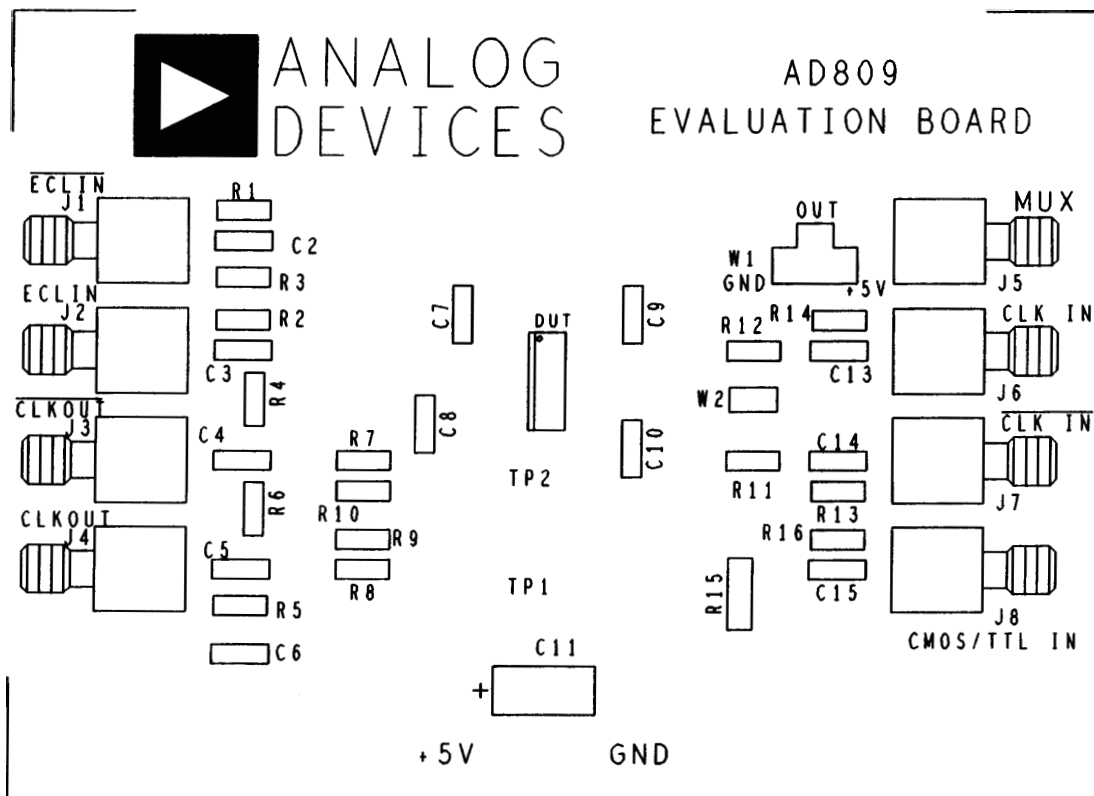


Figure 6. Evaluation Board: Component Side

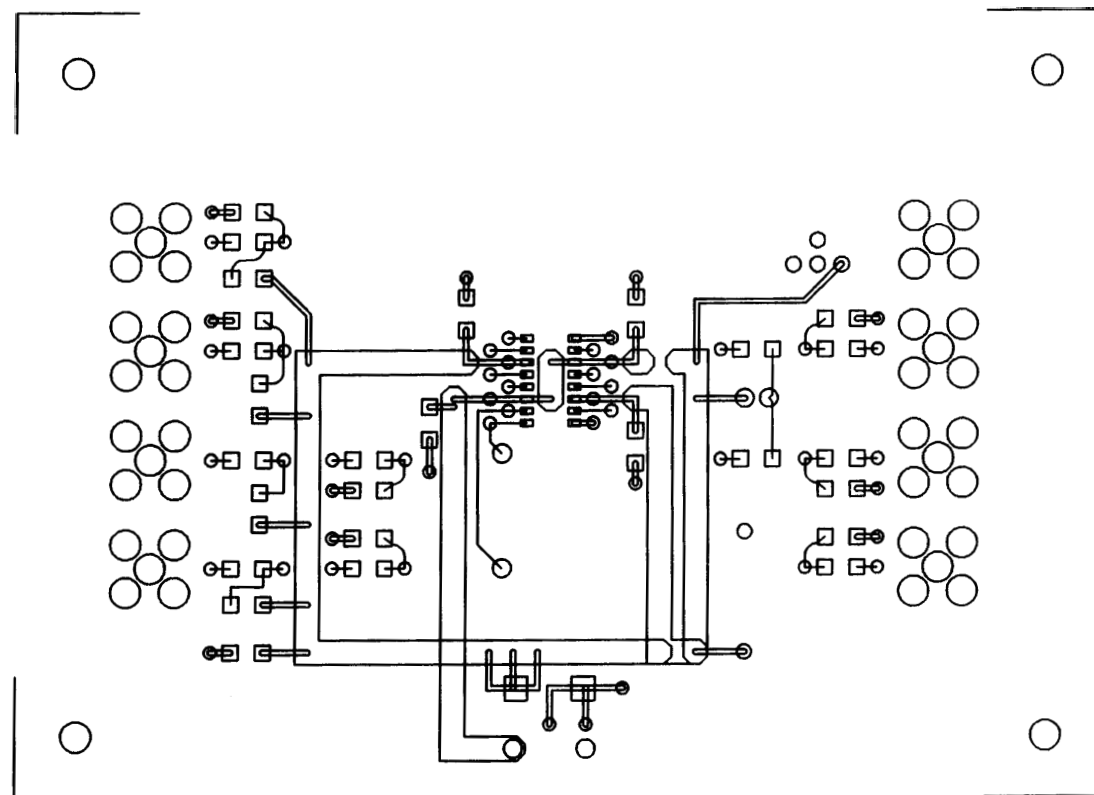


Figure 7. Evaluation Board: Solder Side

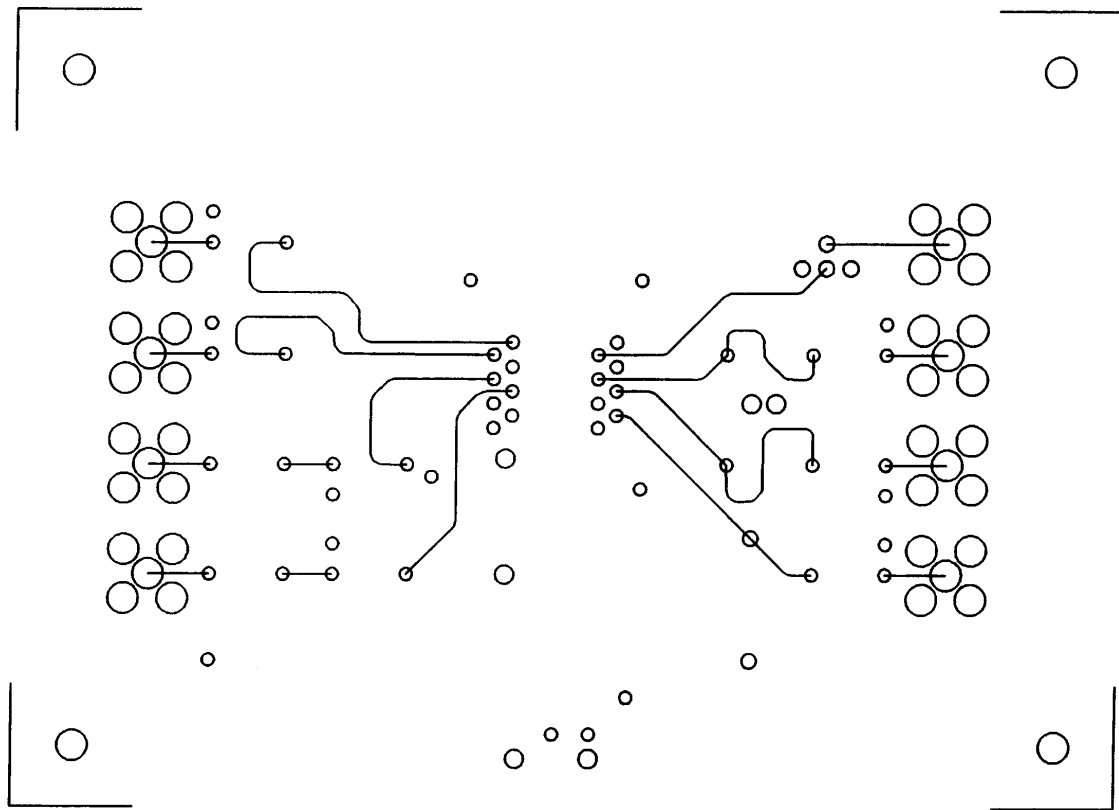
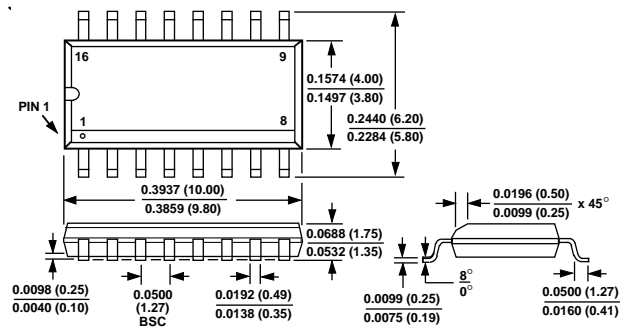


Figure 8. Evaluation Board: INT2

OUTLINE DIMENSIONS
Dimensions shown in inches and (mm).

16-Lead Small Outline IC Package
(R-16A)



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