

FEATURES

High speed 1650 MHz (G = +1)730 MHz (G = +2, V_o = 2 V p-p) 4300 V/µs (G = +2, 4 V step) Settling time 12 ns to 0.1%, 2 V step **Excellent for QXGA resolution video** Gain flatness 0.1 dB to 190 MHz 0.05% differential gain error, $R_L = 150 \Omega$ 0.01° differential phase error, $R_L = 150 \Omega$ Low voltage offset: 0.7 mV (typical) Low input bias current: 7 µA (typical) Low noise: 1.8 nV/√Hz Low distortion over wide bandwidth: SFDR -73 dBc @ 20 MHz High output drive: 100 mA output load drive Supply operation: +5 V to ±5 V voltage supply Supply current: 9.5 mA/amplifier

APPLICATIONS

High resolution video graphics Professional video Consumer video High speed instrumentation Muxing

GENERAL DESCRIPTION

The AD8003 is a triple ultrahigh speed current feedback amplifier. Using ADI's proprietary eXtra Fast Complementary Bipolar (XFCB) process, the AD8003 achieves a bandwidth of 1.5 GHz and a slew rate of 4300 V/µs. Additionally, the amplifier provides excellent dc precision with an input bias current of 50 µA maximum and a dc input voltage of 0.7 mV.

The AD8003 has excellent video specifications with a frequency response that remains flat out to 190 MHz and 0.1% settling within 12 ns to ensure that even the most demanding video systems maintain excellent fidelity. For applications that use NTSC video, as well as high speed video, the amplifier provides a differential gain of 0.05% and a differential gain of 0.01°.

The AD8003 has very low spurious-free dynamic range (SFDR) (-73 dBc @ 20 MHz) and noise $(1.8 \text{ nV}/\sqrt{\text{Hz}})$. With a supply range between 5 V and 11 V and ability to source 100 mA of output current, the AD8003 is ideal for a variety of applications.

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Document Feedback

Triple, 1.5 GHz Op Amp

AD8003

CONNECTION DIAGRAM



The AD8003 operates on only 9.5 mA of supply current per amplifier. The independent power-down function of the AD8003 reduces the quiescent current even further to 1.6 mA.

The AD8003 amplifier is available in a compact $4 \text{ mm} \times 4 \text{ mm}$, 24-lead LFCSP_WQ. The AD8003 is rated to work over the industrial temperature range of -40°C to +85°C.



Figure 2. Large Signal Frequency Response for Various Gains

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REVISION HISTORY

3/14—Rev. B to Rev. C
Changed LFCSP_VQ to LFCSP_WQ (Throughout) 1
Added EPAD Note to Figure 1 1
Updated Outline Dimensions 15
Changes to Ordering Guide 15
9/08—Rev. A to Rev. B Changes Applications Section
Changes to Ordering Guide 15
2/06—Rev. 0 to Rev. A Changes to Figure 3411

10/05—Revision 0: Initial Version

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SPECIFICATIONS WITH ±5 V SUPPLY

 T_{A} = 25°C, V_{S} = ±5 V, R_{L} = 150 $\Omega,$ Gain = +2, R_{F} = 464 $\Omega,$ unless otherwise noted.

Table 1.

Parameter	Conditions	Min	Тур	Max	Unit
DYNAMIC PERFORMANCE					
–3 dB Bandwidth	$G = +1, V_0 = 0.2 V p-p, R_F = 432 \Omega$		1650		MHz
	$G = +2, V_0 = 2 V p - p$		730		MHz
	G = +10, V _O = 0.2 V p-p		290		MHz
	$G = +5, V_0 = 2 V p - p$		330		MHz
Bandwidth for 0.1 dB Flatness	$V_0 = 2 V p - p$		190		MHz
Slew Rate	$G = +2, V_{\Omega} = 2 V \text{ step}, R_{L} = 150 \Omega$		3800		V/µs
Settling Time to 0.1%	$G = +2, V_0 = 2V$ step		12		ns
Overload Recovery Input/Output			30/40		ns
NOISE/HARMONIC PERFORMANCE					
Second/Third Harmonic @ 5 MHz	$G = +1, V_0 = 2 V p - p$		76/97		dBc
Second/Third Harmonic @ 20 MHz	$G = +1, V_0 = 2V p - p$		79/73		dBc
Input Voltage Noise	f = 1 MHz		1.8		nV/√Hz
Input Current Noise (I ⁻ /I ⁺)	f = 1 MHz		36/3		pA/√Hz
Differential Gain Error	NTSC, G = +2, R _L = 150 Ω		0.05		%
Differential Phase Error	NTSC, G = +2, R _L = 150 Ω		0.01		Degree
DC PERFORMANCE					
Input Offset Voltage		-9.3	+0.7	+9.3	mV
	$T_{MIN} - T_{MAX}$		1.08		mV
Input Offset Voltage Drift			7.4		μV/°C
Input Bias Current	$+I_{B}/-I_{B}$	-19/-40	-7/-7	+4/+50	μΑ
	$T_{MIN} - T_{MAX} (+I_B/-I_B)$		-3.8/+29.5		μΑ
Input Offset Current			±14.2		μΑ
Transimpedance	$V_0 = \pm 2.5 V$	400	600	1100	kΩ
INPUT CHARACTERISTICS					
Noninverting Input Impedance			1.6/3		MΩ/pF
Input Common-Mode Voltage Range			±3.6		V
Common-Mode Rejection Ratio	$V_{CM} = \pm 2.5 V$	-51	-48	-46	dB
OUTPUT CHARACTERISTICS					
Output Voltage Swing	$R_L = 150 \Omega$	±3.85	±3.9	±3.92	V
Linear Output Current	$V_0 = 2 V p-p$, second harmonic < $-50 dBc$		100		mA
Capacitive Load Drive	40% over shoot		27		pF
POWER DOWN PINS					
Power-Down Input Voltage	Power down		<vs 2.5<="" td="" –=""><td></td><td>V</td></vs>		V
T	Enable		>Vs - 2.5		V
Turn-Oπ Time	50% of power-down voltage to $10%$ of Volta final Vin = 0.5 V p-p		40		ns
Turn-On Time	50% of power-down voltage to		130		ns
	90% of V_{OUT} final, $V_{IN} = 0.5 \text{ V p-p}$				-
Input Current					
Enabled			0.1		μΑ
Power-Down		-365	-235	-85	μA
POWER SUPPLY					
Operating Range		4.5		10	V
Quiescent Current per Amplifier	Enabled	8.1	9.5	10.2	mA
Quiescent Current per Amplifier	Power down	1.2	1.4	1.6	mA
Power Supply Rejection Ratio (+PSRR/–PSRR)		-59/-57	-57/-53	-55/-50	dB

SPECIFICATIONS WITH +5 V SUPPLY

 T_{A} = 25°C, V_{S} = 5 V, R_{L} = 150 $\Omega,$ Gain = +2, R_{F} = 464 $\Omega,$ unless otherwise noted.

Table 2.

$ \begin{array}{c c c c c c c c c c c c c c c c c c c $	Parameter	Conditions	Min	Тур	Max	Unit
$ \begin{array}{cccccccccccccccccccccccccccccccccccc$	DYNAMIC PERFORMANCE					
$ \begin{array}{cccccccccccccccccccccccccccccccccccc$	–3 dB Bandwidth	$G = +1, V_0 = 0.2 V p-p, R_F = 432 \Omega$		1050		MHz
$ \begin{array}{ c c c c c } & G = +10, V_0 = 0.2 V p \cdot p & 240 & MHz \\ G = +5, V_0 = 2 V p \cdot p & 310 & MHz \\ S = +5, V_0 = 2 V p \cdot p & 83 & V/\mu S \\ S = +5, V_0 = 2 V s tep, R_i = 150 \Omega & 2860 & V/\mu S \\ G = +2, V_0 = 2 V s tep, R_i = 150 \Omega & 2860 & NHz \\ \hline Overload Recovery Input/Output & 40/60 & NS \\ S = -2, V_0 = 2 V s tep & 12 & NS \\ S = -2, V_0 = 2 V s tep & -2V S + 12 & 0.2 \\ S = -1, V_0 = 2 V p \cdot p & 66/61 & dBc \\ Input Voltage Noise & f = 1 MHz & 1.8 & NV/Hz \\ Input Current Noise (1/1') & f = 1 MHz & -2V p \cdot p & 66/61 & 0.04 & 0.04 \\ \hline Input Offset Voltage Noise & f = 1 MHz & -2, R_i = 150 \Omega & 0.04 & 0.04 \\ \hline Differential Phase Error & NTSC, G = +2, R_i = 150 \Omega & 0.01 & Degree \\ \hline D C PERFORMANCE & -2V S + R_i = 150 \Omega & 0.01 & -2V & 9 \\ Input Offset Voltage Drift & T_{MMI} - T_{MAX} & -4/S & -2/S & +5/+48 & \muA \\ Input Offset Voltage Drift & T_{MMI} - T_{MAX} & -1/42 & -4/-27.8 & +5/+48 & \muA \\ Input Offset Voltage Drift & T_{MMI} - T_{MAX} & -1/42 & -4/-27.8 & +5/+48 & \muA \\ T_{MMI} - T_{MAX} & -1/48 & -4/-27.8 & +5/+48 & \muA \\ T_{MMI} - T_{MAX} & -1/48 & -4/-27.8 & -4$		$G = +2, V_0 = 2 V p - p$		590		MHz
$ \begin{array}{c c c c c c c c c c c c c c c c c c c $		$G = +10, V_0 = 0.2 V p - p$		290		MHz
$ \begin{array}{ c c c c c } \hline \begin{tabular}{ c c c } \hline \begin{tabular}{ c c c c } \hline \begin{tabular}{ c c c c } \hline \begin{tabular}{ c c c c c c c } \hline \begin{tabular}{ c c c c c c c } \hline \begin{tabular}{ c c c c c c c } \hline \begin{tabular}{ c c c c c c c c } \hline \begin{tabular}{ c c c c c c c } \hline \begin{tabular}{ c c c c c c c c c c c c c c c c c c c$		$G = +5$, $V_0 = 2V p - p$		310		MH7
$\begin{array}{ c c c c } \hline \begin{tabular}{ c c c c } \hline \begin{tabular}{ c c c c c } \hline \begin{tabular}{ c c c c c } \hline \begin{tabular}{ c c c c c c } \hline \begin{tabular}{ c c c c c c } \hline \begin{tabular}{ c c c c c c } \hline \begin{tabular}{ c c c c c c } \hline \begin{tabular}{ c c c c c c c } \hline \begin{tabular}{ c c c c c c c c c c c c c c c c c c c$	Bandwidth for 0.1 dB Flatness	$V_{\rm p} = 2 V \mathrm{p} \cdot\mathrm{p}$		83		MHz
Set Mate $G = +2, V_0 = 2.V \operatorname{step} A_1 = 130 \Omega$ 23000 V/μ Setting Time to 0.1% $G = +2, V_0 = 2.V \operatorname{step}$ 12nsOverload Recovery Input/Output $G = +1, V_0 = 2.V \operatorname{p-p}$ $40/60$ nsNOISE/HARMONIC PERFORMANCE $G = +1, V_0 = 2.V \operatorname{p-p}$ $66/61$ dBc Second/Third Harmonic @ 5 MHz $G = +1, V_0 = 2.V \operatorname{p-p}$ $66/61$ dBc Input Voltage Noise $f = 1$ MHz 1.8 $nV//Hz$ Input Current Noise (I'/I') $f = 1$ MHz $36/3$ pA/\sqrt{Hz} Differential Gain ErrorNTSC, $G = +2, R_L = 150 \Omega$ 0.04 %Differential Phase ErrorNTSC, $G = +2, R_L = 150 \Omega$ 0.01 DegreeDC PERFORMANCE $Input Offset Voltage$ -6.5 $+2.7$ $+11$ mVInput Offset Voltage Drift $Input Offset Voltage DriftmV_L = 150 \Omega-21/-50-7.7/-2.3+5/+48\muAInput Offset CurrentInm - T_{MAX}-4/-27.8\muA\muATransimpedance3005301500kQ/PFNoninverting Input Impedance-50-48-45dBOUTPUT CHARACTERISTICSV_1 = 150 \Omega-50-48-45dBOutput Voltage SwingR_L = 150 \Omega-50-48-45dBOUTPUT CHARACTERISTICSV_1 = 25 V_1-p, second harmonic < -50 dBc70-50-48-45dBOUTPUT Voltage SwingR_L = 150 \Omega27y_L = 1.52y_L = 1.52y_L = 1.52<$	Slow Pato	$G = 12 V_{\rm c} = 2V_{\rm c}$ top $P_{\rm c} = 150 O_{\rm c}$		2960		
Secting Inflet 00.1%G = +2, V ₀ = 2.V step1218Overload Recovery Input/Output-40/60nsNOISE/HARMONIC PERFORMANCEG = +1, V ₀ = 2.V p-p66/61dBcSecond/Third Harmonic @ 20 MHzG = +1, V ₀ = 2.V p-p66/61dBcInput Voltage Noisef = 1 MHz1.8nV/\HzInput Current Noise (7/1')f = 1 MHz36/3pA/\HzDifferential Gain ErrorNTSC, G = +2, R _L = 150 Ω0.04%Differential Phase ErrorNTSC, G = +2, R _L = 150 Ω0.01DegreeDC PERFORMANCE-6.5+2.7+11mVInput Offset VoltageT _{MIN} – T _{MAX} -6.5+2.7+11Input Offset VoltageTT_MIN – T _{MAX} (+In/-In)-6.5+2.7+11Input Offset Voltage DriftTT-7.1/-2.3+5/+48µAInput Offset Voltage DriftT-2.1/-50-7.7/-2.3+5/+48µAInput Offset CurrentTT±5.4µATanismipedance3005301500kΩINPUT CHARACTERISTICS-50-48-45dBOUTPUT CHARACTERISTICS-50-48-45dBOutput Voltage SwingR _L = 150 Ω±1.52±1.57±1.62VLinear Output CurrentV ₀ = 2 V p-p, second harmonic < -50 dBc	Settling Time to 0.10	$G = +2, V_0 = 2V$ step, $N_1 = 150.02$		10		v/µs
Overload Recovery Input/OutputImage: Instant output ins	Setting time to 0.1%	$G = +2$, $v_0 = 2v$ step		12		ns
$ \begin{array}{cccc} \text{NOISE/TRANIONIC PERFORMANCE} & \text{G} = +1, V_0 = 2 \text{V} \text{p-p} & 57/78 & \text{dBc} \\ \text{Second/Third Harmonic @ 20 MHz} & \text{G} = +1, V_0 = 2 \text{V} \text{p-p} & 66/61 & \text{dBc} \\ \text{Input Voltage Noise} & \text{f} = 1 \text{ MHz} & 1.8 & \text{nV/\Hz} \\ \text{Input Current Noise} (l^-/l^-) & \text{f} = 1 \text{ MHz} & 36/3 & \text{pA/\Hz} \\ \text{Differential Gain Error} & \text{NTSC, G} = +2, R_L = 150 \Omega & 0.04 & \ 0.01 $				40/60		ns
$\begin{array}{cccc} \text{Second/Third Harmonic @ 20 MHz} & \text{G} = +1, \ V_0 = 2 \ V \text{ p-p} & \text{G}^{77/8} & \text{dbC} \\ \text{Second/Third Harmonic @ 20 MHz} & \text{G} = +1, \ V_0 = 2 \ V \text{ p-p} & \text{G}^{6/6/1} & \text{I} \\ \text{Input Voltage Noise} & \text{f} = 1 \ \text{MHz} & 1.8 & \text{NV/Hz} \\ \text{Input Current Noise (\Gamma/\Gamma)} & \text{f} = 1 \ \text{MHz} & 36/3 & \text{O} \\ \text{Differential Gain Error} & \text{NTSC, G} = +2, \ R_L = 150 \ \Omega & 0.04 & \ \% \\ \text{Differential Phase Error} & \text{NTSC, G} = +2, \ R_L = 150 \ \Omega & 0.01 & \ \text{Degree} \\ \text{DC PERFORMANCE} & -6.5 & +2.7 & +11 & \text{mV} \\ \text{Input Offset Voltage} & -6.5 & +2.7 & +11 & \text{mV} \\ \text{Input Offset Voltage Drift} & 14.2 & 2.06 & \ 14.2 & \ \mu^{2} \\ \text{Input Offset Voltage Drift} & 14.2 & 2.06 & \ -21/-50 & -7.7/-2.3 & +5/+48 & \ \mu^{2} \\ \text{Input Offset Voltage Drift} & -4/-27.8 & \ -21/-50 & -7.7/-2.3 & +5/+48 & \ \mu^{2} \\ \text{Input Offset Current} & -4/-27.8 & \ \mu^{2} \\ \text{Transimpedance} & 16.7 & -4/-27.8 & \ \mu^{2} \\ \text{Input CMRMO-Mode Range} & -45 & \ 300 & 530 & 1500 & \ \chi^{2} \\ \text{OUTPUT CHARACTERISTICS} & -50 & -48 & -45 & \ \text{dBC} \\ \text{OUTPUT CHARACTERISTICS} & -50 & -48 & -45 & \ \text{dBC} \\ \text{Output Voltage Swing} & R_L = 150 \ \Omega & -50 & -50 & -48 & -45 & \ \text{dBC} \\ \text{Output Voltage Swing} & R_L = 150 \ \Omega & -50 & -50 & -70 & \ 70 & \ \text{mA} \\ \text{Capacitive Load Drive} & 45\% \text{ over shoot} & -50 & \ 70 & \ \text{mA} \\ \text{Capacitive Load Drive} & 45\% \text{ over shoot} & 27 & \ \text{mA} \\ \text{Fower-Down Input Voltage} & Power down voltage to \\ \text{Fower-Down Input Voltage} & Power down voltage to \\ \text{Fower-Down Input Voltage} & Power-down voltage to \\ \text{Fower-Down Input Voltage} & \text{Fower-down voltage to} \\ \text{Fower-Down Input Voltage} & Power-down voltage to \\ \text{Fower-Down Input Voltage} & \text{Fower-Down Voltage to} \\ \text$	NOISE/HARMONIC PERFORMANCE			75/70		dDa
$\begin{array}{cccc} Second/Ihrid Harmonic @ 20 MHz & G = 1, V_0 = 2 V p-p & 66/61 & dBc \\ Input Voltage Noise & f = 1 MHz & 1.8 & nV//Hz \\ Input Current Noise (Ir/I^h) & f = 1 MHz & 36/3 & 0.04 & % \\ Differential Gain Error & NTSC, G = +2, R_L = 150 \Omega & 0.01 & 0.01 & Degree \\ DC PERFORMANCE & -6.5 & +2.7 & +11 & mV \\ Input Offset Voltage & -6.5 & +2.7 & +11 & mV \\ 1nput Offset Voltage Drift & 14.2 & 0.04 & 0$		$G = +1, v_0 = 2v p - p$		/5//8		abc
$\begin{array}{ c c c c } \mbox{Input Voltage Noise} & f = 1 MHz & 1.8 & nV/ Hz \\ \mbox{Input Current Noise (1/1') } f = 1 MHz & 36/3 & pA/ Hz \\ \mbox{Differential Gain Error NTSC, G = +2, RL = 150 \Omega & 0.04 & 0.04 & Degree \\ \mbox{Differential Phase Error NTSC, G = +2, RL = 150 \Omega & 0.01 & Degree \\ \mbox{DC PERFORMANCE } & -6.5 & +2.7 & +11 & mV \\ \mbox{Input Offset Voltage Drift Input Offset Current (+Ig/-Ig) & -21/-50 & -7.7/-2.3 & +5/+48 & \muA \\ \mbox{Input Offset Current } & -21/-50 & -7.7/-2.3 & +5/+48 & \muA \\ \mbox{Input Offset Current } & \pm5.4 & \muA \\ \mbox{Input Offset Current } & \pm5.4 & \muA \\ \mbox{Input Common-Mode Voltage Range Common-Mode Rejection Ratio & -50 & -48 & -45 & dB \\ \mbox{OUTPUT CHARACTERISTICS } & & & & & & & & & & & & & & & & & & $	Second/Third Harmonic @ 20 MHz	$G = +1, V_0 = 2V p - p$		66/61		dBc
$\begin{array}{ c c c } \mbox{Input Current Noise (Ir/I')} & f = 1 \mbox{MHz} & 36/3 & pA/Mz \\ \mbox{Differential Gain Error} & NTSC, G = +2, R_L = 150 \mbox{Ω} & 0.04 & 0.01 & 0egree \\ \mbox{Degree NTSC, G = +2, R_L = 150 \mbox{Ω} & 0.01 & 0.01 & 0egree \\ \mbox{Degree NTSC, G = +2, R_L = 150 \mbox{Ω} & 0.01 & 0.01 & 0egree \\ \mbox{Input Offset Voltage Drift } & -6.5 & +2.7 & +11 & mV \\ \mbox{Input Offset Voltage Drift } & -6.5 & +2.7 & +11 & mV \\ \mbox{Input Offset Voltage Drift } & -21/-50 & -7.7/-2.3 & +5/+48 & \muA \\ \mbox{Input Offset Current } & -21/-50 & -7.7/-2.3 & +5/+48 & \muA \\ \mbox{Input Offset Current } & -4/-27.8 & \muA \\ \mbox{Input Offset Current } & \pm5.4 & \muA \\ \mbox{Input Cmmon-Mode Voltage Range } & 1.6/3 & 1500 & k\Omega \\ \mbox{INPUT CHARACTERISTICS } & -50 & -48 & -45 & dB \\ \mbox{OUTPUT CHARACTERISTICS } & -50 & -48 & -45 & dB \\ \mbox{OUTPUT CHARACTERISTICS } & -50 & -48 & -45 & dB \\ \mbox{Output Voltage Swing } & R_L = 150 \mbox{Ω} & -50 & -48 & -45 & dB \\ \mbox{Output Voltage Swing } & R_L = 150 \mbox{Ω} & -50 & -48 & -45 & dB \\ \mbox{Output Voltage Swing } & R_L = 150 \mbox{Ω} & -50 & -27 & -2.5 & V \\ \mbox{Linear Output Current } & V_0 = 2 V p-p, second harmonic < -50 dBc & 70 & -27 & pF \\ \mbox{Power-Down Input Voltage } & Power down & $	Input Voltage Noise	f = 1 MHz		1.8		nV/√Hz
Differential Gain ErrorNTSC, G = +2, R_i = 150 Ω 0.04 $\%$ Differential Phase ErrorNTSC, G = +2, R_i = 150 Ω 0.01 DegreeDC PERFORMANCE -6.5 $+2.7$ $+11$ mVInput Offset Voltage -6.5 $+2.7$ $+11$ mVInput Offset Voltage Drift 14.2 μ //°C μ //°CInput Offset Voltage Drift -14.2 μ //°C μ //°CInput Offset Current ($+1_{0}/-1_{0}$) $T_{MIN} - T_{MAX}$ ($+1_{0}/-1_{0}$) $-21/-50$ $-7.7/-2.3$ $+5/+48$ μ AInput Offset Current $T_{MIN} - T_{MAX}$ ($+1_{0}/-1_{0}$) $-21/-50$ $-7.7/-2.3$ $+5/+48$ μ AInput Offset Current $T_{MIN} - T_{MAX}$ ($+1_{0}/-1_{0}$) $-21/-50$ $-7.7/-2.3$ $+5/+48$ μ AInput Offset Current $T_{MIN} - T_{MAX}$ ($+1_{0}/-1_{0}$) 300 500 1500 $K\Omega$ INPUT CHARACTERISTICS 1500 1.50 1.50 $M\Omega/pF$ Input Common-Mode Voltage Range -50 -48 -45 dB OUTPUT CHARACTERISTICS 50 or $2 V$ p-p, second harmonic < -50 dBc 70 $= 1.62$ V Output Voltage Swing $R_L = 150 \Omega$ ± 1.52 ± 1.52 ± 1.62 V Quiptur Lurent $V_0 = 2 V$ p-p, second harmonic < -50 dBc 70 $= 77$ $= 77$ $= 77$ POWER DOWN PINS P P P P $= 0.5V$ p- 2.5 V Power-Down Input VoltagePower-down voltage to $>V_5 - 2.5$ V Iurn-Off T	Input Current Noise (I ⁻ /I ⁺)	f = 1 MHz		36/3		pA/√Hz
Differential Phase ErrorNTSC, G = +2, R_L = 150 Ω 0.01DegreeDC PERFORMANCEInput Offset Voltage-6.5+2.7+11mVInput Offset Voltage DriftT_MIN - T_MAX2.06mVmVInput Bias Current (+lg/-lg)-21/-50-7.7/-2.3+5/+48 μ AInput Offset CurrentT_MIN - T_MAX (+lg/-lg)-21/-50-7.7/-2.3+5/+48 μ AInput Offset Current±5.4 μ A±5.4 μ ATransimpedance3005301500k Ω INPUT CHARACTERISTICSI.6/3M Ω/pF 1.3 to 3.7VNoninverting Input Impedance50-48-45d8OUTPUT CHARACTERISTICS-50-50-48-45d8OUTPUT CHARACTERISTICS-50-50-70T.8.VOutput Voltage SwingRL = 150 Ω ±1.52±1.57±1.62VLinear Output CurrentVo = 2 V p-p, second harmonic < -50 dBc	Differential Gain Error	NTSC, $G = +2$, $R_L = 150 \Omega$		0.04		%
$\begin{array}{cccc} DC PERFORMANCE & -6.5 & +2.7 & +11 & mV \\ Input Offset Voltage Drift & 14.2 & \mu V^{\circ \mathbb{C} \\ Input Bias Current (+l_g/-l_g) & 14.2 & & \mu A \\ Input Bias Current (+l_g/-l_g) & -21/-50 & -7.7/-2.3 & +5/+48 & \mu A \\ Input Offset Current & & -21/-50 & -7.7/-2.3 & +5/+48 & \mu A \\ Input Offset Current & & -4/-27.8 & & \mu A \\ Transimpedance & 300 & 530 & 1500 & k\Omega \\ \hline INPUT CHARACTERISTICS & & & & & & & & & \\ \mathsf{Noninverting Input Impedance & 1.6/3 & & & & & & & & & & \\ \mathsf{Input Common-Mode Voltage Range & 1.6/3 & & & & & & & & & & & & & \\ \mathsf{OUTPUT CHARACTERISTICS & & & & & & & & & & & & & & & & & & &$	Differential Phase Error	NTSC, G = +2, R _L = 150 Ω		0.01		Degree
Input Offset Voltage-6.5 ± 2.7 ± 11 mVInput Offset Voltage DriftT_MIN - T_MAX 2.06 mVInput Bias Current ($\pm _{b}/- _{b}$) $-21/-50$ $-7.7/-2.3$ $\pm 5/\pm 48$ μA Input Offset CurrentT_MIN - T_MAX ($\pm _{b}/- _{b}$) $-21/-50$ $-7.7/-2.3$ $\pm 5/\pm 48$ μA Input Offset Current ± 5.4 μA ± 5.4 μA Transimpedance3005301500 $k\Omega$ INPUT CHARACTERISTICS $1.6/3$ $1.6/3$ $M\Omega/pF$ Noninverting Input Impedance $1.6/3$ 1.3 to 3.7 V OUTPUT CHARACTERISTICS 1.3 to 3.7 V V Output Voltage Swing $R_L = 150 \Omega$ ± 1.52 ± 1.57 ± 1.62 Output Voltage Swing $R_L = 150 \Omega$ ± 1.52 $27.$ pF POWER DOWN PINS 27 P pF Power-Down Input VoltagePower down $< V_S - 2.5$ V Fnable $>V_S - 2.5$ V V Turn-Off Time 10% of power-down voltage to 125 V	DC PERFORMANCE					
Input Offset Voltage Drift Input Bias Current (+IB/-IB)Imput Diffset Voltage Drift Imput Bias Current (+IB/-IB)mVInput Offset Current Transimpedance $-21/-50$ $-7.7/-2.3$ $+5/+48$ μ AInput Offset Current Transimpedance $-4/-27.8$ μ AINPUT CHARACTERISTICS Noninverting Input Impedance 300 530 1500 $K\Omega$ Input Common-Mode Voltage Range Common-Mode Rejection Ratio -50 -48 -45 dB OUTPUT CHARACTERISTICS Noninverting Input Impedance -50 -48 -45 dB OUTPUT CHARACTERISTICS Common-Mode Rejection Ratio $V_0 = 2 V p - p$, second harmonic < -50 dB 70 T T OUTPUT CHARACTERISTICS Output Voltage Swing Linear Output Current Capacitive Load Drive $A5\%$ over shoot 27 V mA POWER DOWN PINS Power-Down Input VoltagePower down Enable $VVTurn-Off Time50\% of power-down voltage to50\% of power-down voltage to125VV$	Input Offset Voltage		-6.5	+2.7	+11	mV
Input Offset Voltage Drift Input Bias Current (+I _B /-I _B) -14.2 μ V/°CInput Bias Current (+I _B /-I _B) $-21/-50$ $-7.7/-2.3$ $+5/+48$ μ AInput Offset Current $-4/-27.8$ μ ATransimpedance 300 530 1500 $k\Omega$ INPUT CHARACTERISTICS $1.6/3$ $1.6/3$ $M\Omega/pF$ Noninverting Input Impedance $1.6/3$ $1.3 to 3.7$ V Common-Mode Voltage Range -50 -48 -45 dB OUTPUT CHARACTERISTICS $F_L = 150 \Omega$ ± 1.52 ± 1.57 ± 1.62 V Output Voltage Swing $R_L = 150 \Omega$ ± 1.52 ± 1.57 ± 1.62 V Linear Output Current $V_0 = 2 V p$ - p , second harmonic < $-50 dBc$ 70 -4 PF POWER DOWN PINS $Power down$ $VVPower-Down Input VoltagePower downVVTurn-Off Time50\% of power-down voltage to125VN$		$I_{MIN} - I_{MAX}$		2.06		mv
Input Bias current (+lg/-lg) $-21/-50$ $-7.7/-2.3$ $+5/+48$ μA Input Offset Current $T_{MIN} - T_{MAX} (+lg/-lg)$ $-4/-27.8$ μA Input Offset Current 300 530 1500 $k\Omega$ INPUT CHARACTERISTICS 300 530 1500 $k\Omega$ Noninverting Input Impedance $1.6/3$ $1.6/3$ V Input Common-Mode Voltage Range $1.3 \text{ to } 3.7$ V Common-Mode Rejection Ratio -50 -48 -45 dB OUTPUT CHARACTERISTICS V -50 -48 -45 dB OUTPUT CHARACTERISTICS V -50 -48 -45 dB OUTPUT CHARACTERISTICS V $V_0 = 2V p$ -p, second harmonic $< -50 dB$ 70 V P Output Voltage Swing $R_L = 150 \Omega$ ± 1.52 ± 1.57 ± 1.62 V V Linear Output Current $V_0 = 2V p$ -p, second harmonic $< -50 dBc$ 70 V P POWER DOWN PINS P V $V_5 - 2.5$ V V Power-Down Input VoltagePower down $VVTurn-Off Time50\% of power-down voltage to10\% of for V or p for N125VN$	Input Offset Voltage Drift		21/ 50	14.2		μν/°C
Imput Offset CurrentImpact (+IB/-IB) $-4/-27.3$ Impact (Impact (+IB/-IB))Input Offset Current ± 5.4 μA Transimpedance3005301500 $k\Omega$ INPUT CHARACTERISTICS $1.6/3$ $M\Omega/pF$ Input Common-Mode Voltage Range $1.3 \text{ to } 3.7$ V Common-Mode Rejection Ratio -50 -48 -45 dBOUTPUT CHARACTERISTICS -50 -48 -45 dBOUTPUT CHARACTERISTICS 1.52 ± 1.57 ± 1.62 V Output Voltage Swing $R_L = 150 \Omega$ ± 1.52 ± 1.57 ± 1.62 V Linear Output Current $V_0 = 2 V p$ -p, second harmonic < -50 dBc 70 mA Capacitive Load Drive 45% over shoot 27 pF POWER DOWN PINS P V $V_S - 2.5$ V Power-Down Input VoltagePower down $VTurn-Off Time10\% of power-down voltage to10\% of Vour final Vw = 0.5 V p-p125V$	Input Bias Current $(+I_B/-I_B)$		-21/-50	-/.//-2.3	+5/+48	μΑ
Input OnservationImplementationImplementationImplementationImplementationImplementationTransimpedance3005301500kQINPUT CHARACTERISTICS1.6/3MQ/pFInput Common-Mode Voltage Range1.3 to 3.7VCommon-Mode Rejection Ratio-50-48-45dBOUTPUT CHARACTERISTICS-50-48-45dBOUTPUT CHARACTERISTICS ± 1.52 ± 1.57 ± 1.62 VLinear Output Voltage Swing $R_L = 150 \Omega$ ± 1.52 ± 1.57 ± 1.62 VLinear Output Current $V_0 = 2 V p$ -p, second harmonic < -50 dBc	Input Offcat Current	$I_{MIN} - I_{MAX} (+IB/-IB)$		-4/-2/.8 +5.4		μΑ
Inaristripedance5005001500KYINPUT CHARACTERISTICSNoninverting Input Impedance $1.6/3$ M Ω /pFInput Common-Mode Voltage Range 1.3 to 3.7 VCommon-Mode Rejection Ratio -50 -48 -45 OUTPUT CHARACTERISTICS -50 -48 -45 dBOUTPUT CHARACTERISTICS ± 1.52 ± 1.57 ± 1.62 VLinear Output Current $V_0 = 2$ V p-p, second harmonic < -50 dBc 70 -50 70 Capacitive Load Drive 45% over shoot 27 pF POWER DOWN PINS $Power$ down $VPower-Down Input VoltagePower down voltage to50\% of power-down voltage to10\% of Vorr final Vw = 0.5 V p-p125V$	Transimpodanco		300	±3.4 530	1500	μA
INFO C CHARACTERISTICSMQ/pFNoninverting Input Impedance1.6/3MQ/pFInput Common-Mode Voltage Range1.3 to 3.7VCommon-Mode Rejection Ratio -50 -48 -45 dBOUTPUT CHARACTERISTICS -50 -48 -45 VOutput Voltage Swing $R_L = 150 \Omega$ ± 1.52 ± 1.57 ± 1.62 VLinear Output Current $V_0 = 2 V p$ -p, second harmonic < $-50 dBc$ 70 ± 1.62 VCapacitive Load Drive45% over shoot 27 pF pF POWER DOWN PINS $enable$ $V_S - 2.5$ VVTurn-Off Time 50% of power-down voltage to 10% of Vour final Vu = 0.5 V p-p 125 V na			300	330	1300	K12
Noninverting input inipedanceInterviewInterviewInterviewInterviewInterviewInput Common-Mode Voltage Range1.3 to 3.7VCommon-Mode Rejection Ratio -50 -48 -45 dBOUTPUT CHARACTERISTICS $\pm 1.50 \Omega$ ± 1.52 ± 1.57 ± 1.62 VOutput Voltage Swing $R_L = 150 \Omega$ ± 1.52 ± 1.57 ± 1.62 VLinear Output Current $V_0 = 2 V p$ -p, second harmonic < $-50 dBc$ 70 ± 1.62 VCapacitive Load Drive45% over shoot 27 pF pF POWER DOWN PINS $Power down$ $VPower-Down Input VoltagePower down voltage to10\% of Vour final Vw = 0.5 V p-p125VTurn-Off Time10\% of Vour final Vw = 0.5 V p-p125N$	Noninverting Input Impedance			16/3		MO/nF
Input common Mode Voltage hangeVCommon-Mode Rejection Ratio -50 -48 -45 dBOUTPUT CHARACTERISTICS $\pm 1.50 \Omega$ ± 1.52 ± 1.57 ± 1.62 VLinear Output Voltage Swing $R_L = 150 \Omega$ ± 1.52 ± 1.57 ± 1.62 VLinear Output Current $V_0 = 2 V p$ -p, second harmonic < $-50 dBc$ 70 mACapacitive Load Drive 45% over shoot 27 pF POWER DOWN PINS $Power down$ $VPower-Down Input VoltagePower down voltage to10\% of Vour final Vw = 0.5 V p-p125V$	Input Common-Mode Voltage Bange			1.0/5 1.3 to 3.7		V
OUTPUT CHARACTERISTICS Output Voltage Swing Linear Output Current Capacitive Load Drive $R_L = 150 \Omega$ 	Common-Mode Rejection Ratio		-50	-48	-45	dB
Output Voltage Swing $R_L = 150 \Omega$ $\pm 1.52 \qquad \pm 1.57 \qquad \pm 1.62$ V Linear Output Current $V_0 = 2 V p$ -p, second harmonic < -50 dBc	OUTPUT CHARACTERISTICS				10	
Linear Output Current $V_0 = 2 V p$ -p, second harmonic < -50 dBc70mACapacitive Load Drive45% over shoot27pFPOWER DOWN PINSPower down <v_s -="" 2.5<="" td="">VPower-Down Input VoltagePower down voltage to 10% of Your final Vw = 0.5 V p-p125ns</v_s>	Output Voltage Swing	$R_1 = 150 \Omega$	±1.52	±1.57	±1.62	v
Capacitive Load Drive45% over shoot27pFPOWER DOWN PINS Power-Down Input VoltagePower down $VEnable>V_s - 2.5VTurn-Off Time50% of power-down voltage to10\% of Vour final Vw = 0.5 V p-p125ns$	Linear Output Current	$V_0 = 2 V p - p$, second harmonic < -50 dBc		70		mA
POWER DOWN PINS Power down <vs -="" 2.5<="" th=""> V Power-Down Input Voltage Power down >Vs - 2.5 V Enable >Vs - 2.5 V Turn-Off Time 50% of power-down voltage to 10% of Vour final Vw = 0.5 V p-p 125 ns</vs>	Capacitive Load Drive	45% over shoot		27		pF
Power-Down Input Voltage Power down <vs -="" 2.5<="" th=""> V Enable >Vs - 2.5 V Turn-Off Time 50% of power-down voltage to 10% of Vour final Vw = 0.5 V n-n 125 ns</vs>	POWER DOWN PINS					
Enable >Vs - 2.5 V Turn-Off Time 50% of power-down voltage to 10% of Vour final Vw = 0.5 V p-p 125 ns	Power-Down Input Voltage	Power down		<vs -="" 2.5<="" td=""><td></td><td>V</td></vs>		V
Turn-Off Time50% of power-down voltage to125ns10% of Vour final Viv = 0.5 Vip-p		Enable		>Vs - 2.5		V
10% of Vour final V _N = 0.5 V p-p	Turn-Off Time	50% of power-down voltage to		125		ns
		10% of V_{OUT} final, $V_{IN} = 0.5 \text{ V p-p}$				
Turn-On Time50% of power-down voltage to80ns	Turn-On Time	50% of power-down voltage to		80		ns
90% of V_{OUT} final, $V_{IN} = 0.5 V p-p$		90% of V_{OUT} final, $V_{IN} = 0.5 V p-p$				
Input Current	Input Current			0.1		
Enabled U.I µA	Enabled		160	0.1	. 00	μΑ
Power-Down -160 -43 +80 μA	Power-Down		-160	-43	+80	μΑ
POWER SUPPLI	POWER SUPPLY		4.5		10	V
Oujescent Current per Amplifier Enchled 6.2 70 0.4 m A	Oujescent Current per Amplifier	Enabled	4.5	70	0.4	m^
Quiescent Current per Amplifier Enabled 0.5 7.9 9.4 MA	Quiescent Current per Amplifier	Power down	0.5	7.9 0.0	9.4 1 1	mΑ
Power Supply Rejection Ratio (+PSRR/–PSRR)	Power Supply Rejection Ratio (+PSRR/–PSRR)		-59/-56	-57/-53	-55/-50	dB

ABSOLUTE MAXIMUM RATINGS

Table 3.

Parameter	Rating
Supply Voltage	11 V
Power Dissipation	See Figure 3
Common-Mode Input Voltage	$-V_{s} - 0.7 V$ to $+V_{s} + 0.7 V$
Differential Input Voltage	±Vs
Exposed Paddle Voltage	-Vs
Storage Temperature Range	–65°C to +125°C
Operating Temperature Range	-40°C to +85°C
Lead Temperature (Soldering 10 sec)	300°C
Junction Temperature	150°C

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

THERMAL RESISTANCE

 θ_{JA} is specified for the worst-case conditions, that is, θ_{JA} is specified for device soldered in circuit board for surface-mount packages.

Table 4. Thermal Resistance

Package Type	Αιθ	Unit
24-Lead LFCSP_WQ	70	°C/W

Maximum Power Dissipation

The maximum safe power dissipation for the AD8003 is limited by the associated rise in junction temperature (T_J) on the die. At approximately 150°C, which is the glass transition temperature, the plastic changes its properties. Even temporarily exceeding this temperature limit may change the stresses that the package exerts on the die, permanently shifting the parametric performance of the AD8003. Exceeding a junction temperature of 175°C for an extended period can result in changes in silicon devices, potentially causing degradation or loss of functionality.

The power dissipated in the package (P_D) is the sum of the quiescent power dissipation and the power dissipated in the die due to the AD8003 drive at the output. The quiescent power is the voltage between the supply pins (V_S) times the quiescent current (I_S) .

 P_D = Quiescent Power + (Total Drive Power – Load Power)

$$P_{D} = \left(V_{S} \times I_{S}\right) + \left(\frac{V_{S}}{2} \times \frac{V_{OUT}}{R_{L}}\right) - \frac{V_{OUT}^{2}}{R_{L}}$$

RMS output voltages should be considered. If R_L is referenced to $-V_s$, as in single-supply operation, the total drive power is $V_S \times I_{OUT}$. If the rms signal levels are indeterminate, consider the worst case, when $V_{OUT} = V_s/4$ for R_L to midsupply.

$$P_D = \left(V_S \times I_S\right) + \frac{\left(V_S/4\right)^2}{R_L}$$

In single-supply operation with R_L referenced to $-V_s$, worst case is $V_{OUT} = V_s/2$.

Airflow increases heat dissipation, effectively reducing θ_{JA} . In addition, more metal directly in contact with the package leads and exposed paddle from metal traces, through holes, ground, and power planes reduce θ_{JA} .

Figure 3 shows the maximum safe power dissipation in the package vs. the ambient temperature for the exposed paddle, $4 \text{ mm} \times 4 \text{ mm} \text{ LFCSP}_WQ$ (70°C/W) package on a JEDEC standard 4-layer board. θ_{JA} values are approximations.



Figure 3. Maximum Power Dissipation vs. Temperature for a 4-Layer Board

ESD CAUTION



ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

TYPICAL PERFORMANCE CHARACTERISTICS



Figure 4. Small Signal Frequency Response for Various Gains



Figure 5. Small Signal Frequency Response for Various Supplies



Figure 6. Small Signal Feedback Resistor (R_F) Optimization



Figure 7. Small Signal Frequency Response for Various Gains



Figure 8. Small Signal Frequency Response for Various Temperatures



Figure 9. Large Signal Feedback Resistor (R_F) Optimization

6 G = +1 $V_S = \pm 5V$ $R_L = 150\Omega$ $V_{OUT} = 200mV p-p$ = 0Ω NORMALIZED CLOSED-LOOP GAIN (dB) 3 Rs 25Ω Ш C R_S = 50Ω -6 -9 -12 1000 10000 10 100 1 FREQUENCY (MHz)





Figure 11. Large Signal Frequency Response for Various Gains



Figure 12. Harmonic Distortion vs. Frequency for Various Supplies



Figure 13. 0.1 dB Flatness Response



Figure 14. Large Signal Frequency Response for Various Temperatures



Figure 15. Harmonic Distortion vs. Frequency for Various Supplies



Figure 16. Harmonic Distortion vs. RL







Figure 18. Small Signal Pulse Response for Various Capacitive Loads











Figure 21. Short-Term 0.1% Settling Time

6000 -- FALL G = +2 R_L = 150Ω V_S = ±5V 5000 4000 3000 2000 V V_S = +5V 1000 05721-013 0 3 4 V_{OUT p-p} (V) 0 1 2 5 6 7

Figure 22. Slew Rate vs. Output Voltage







Figure 24. Common-Mode Rejection vs. Frequency



Figure 25. Input Overdrive Recovery







Figure 27. Power Supply Rejection vs. Frequency



Figure 28. Offset Voltage vs. Input Common-Mode Range



Figure 29. Inverting Input Bias Current Linearity







Figure 31. Noninverting Input Bias Current vs. Common-Mode Range





05721-029

1000 $V_S = \pm 5V$ R_F = 1k Ω INPUT VOLTAGE NOISE (nVI/Hz) 100 10 Π 05721-034 1 └ 10 100 1k 10k 100k 1M 10M FREQUENCY (Hz)

Figure 34. Input Voltage Noise vs. Frequency



Figure 35. Worst-Case Crosstalk



Figure 36. Input Current Noise vs. Frequency



Figure 37. Transimpedance

APPLICATIONS INFORMATION

GAIN CONFIGURATIONS

Unlike conventional voltage feedback amplifiers, the feedback resistor has a direct impact on the closed-loop bandwidth and stability of the current feedback op amp circuit. Reducing the resistance below the recommended value can make the amplifier response peak and can even become unstable. Increasing the size of the feedback resistor reduces the closed-loop bandwidth.

Table 5 provides a convenient reference for quickly determining the feedback and gain set resistor values, and the small and large signal bandwidths for common gain configurations. The feedback resistors in Table 5 have been optimized for 0.1 dB flatness frequency response.

Tuble 5. Recommended values and Frequency Response						
Gain	R _F (Ω)	R _G (Ω)	Rs (Ω)	–3 dB SS BW (MHz)	Large Signal –3 dB BW	Large Signal 0.1 dB BW
-1	300	300	0	734	668	
+1	432	N/A	24.9	1650	822	
+2	464	464	0	761	730	190
+5	300	75	0	567	558	165
+10	300	33.2	0	446	422	170

Table 5. Recommended Values and Frequency Response¹

¹Conditions: $V_s = \pm 5 V$, $T_A = 25^{\circ}C$, $R_L = 150 \Omega$.

Figure 38 and Figure 39 show the typical noninverting and inverting configurations and recommended bypass capacitor values.



Figure 38. Noninverting Gain



Figure 39. Inverting Gain

RGB VIDEO DRIVER

Figure 40 shows a typical RGB driver application using bipolar supplies. The gain of the amplifier is set at +2, where $R_F = R_G = 464 \Omega$. The amplifier inputs are terminated with shunt 75 Ω resistors, and the outputs have series 75 Ω resistors for proper video matching. In Figure 40, the POWER DOWN pins are not shown connected to any signal source for simplicity. If the powerdown function is not used, it is recommended that the POWER DOWN pins be tied to the positive supply and not be left floating (not connected).

In applications that require a fixed gain of +2, as previously mentioned, the designer may consider the ADA4862-3. The ADA4862-3 is another high performance triple current feedback amplifier. The ADA4862-3 has integrated feedback and gain set resistors that reduce board area and simplify designs.



Figure 40. RGB Video Driver

PRINTED CIRCUIT BOARD LAYOUT

Printed circuit board (PCB) layout is usually one of the last steps in the design process and often proves to be one of the most critical. A high performance design can be rendered mediocre due to poor or sloppy layout. Because the AD8003 can operate into the RF frequency spectrum, high frequency board layout considerations must be taken into account. The PCB layout, signal routing, power supply bypassing, and grounding must all be addressed to ensure optimal performance.

LOW DISTORTION PINOUT

The AD8003 LFCSP features ADI's low distortion pinout. The pinout lowers the second harmonic distortion and simplifies the circuit layout. The close proximity of the noninverting input and the negative supply pin creates a source of second harmonic distortion. Physical separation of the noninverting input pin and the negative power supply pin reduces this distortion.

By providing an additional output pin, the feedback resistor can be connected directly between the feedback pin and the inverting input. This greatly simplifies the routing of the feedback resistor and allows a more compact circuit layout, which reduces its size and helps to minimize parasitics and increase stability.

SIGNAL ROUTING

To minimize parasitic inductances, ground planes should be used under high frequency signal traces. However, the ground plane should be removed from under the input and output pins to minimize the formation of parasitic capacitors, which degrades phase margin. Signals that are susceptible to noise pickup should be run on the internal layers of the PCB, which can provide maximum shielding.

EXPOSED PADDLE

The AD8003 features an exposed paddle, which lowers the thermal resistance by approximately 40% compared to a standard SOIC plastic package. The paddle can be soldered directly to the ground plane of the board. Thermal vias or heat pipes can also be incorporated into the design of the mounting pad for the exposed paddle. These additional vias improve the thermal transfer from the package to the PCB. Using a heavier weight copper also reduces the overall thermal resistance path to ground.

POWER SUPPLY BYPASSING

Power supply bypassing is a critical aspect of the PCB design process. For best performance, the AD8003 power supply pins need to be properly bypassed.

Each amplifier has its own supply pins brought out for the utmost flexibility. Supply pins can be commoned together or routed to a dedicated power plane. Commoned supply connections can also reduce the need for bypass capacitors on each supply line. The exact number and values of the bypass capacitors are dictated by the design specifications of the actual circuit.

A parallel combination of different value capacitors from each of the power supply pins to ground tends to work the best. Paralleling different values and sizes of capacitors helps to ensure that the power supply pins see a low ac impedance across a wide band of frequencies. This is important for minimizing the coupling of noise into the amplifier. Starting directly at the power supply pins, the smallest value and physical-sized component should be placed on the same side of the board as the amplifier, and as close as possible to the amplifier, and connected to the ground plane. This process should be repeated for the next largest capacitor value. It is recommended that a 0.1 µF ceramic 0508 case be used for the AD8003. The 0508 offers low series inductance and excellent high frequency performance. The 0.1 µF case provides low impedance at high frequencies. A 10 µF electrolytic capacitor should be placed in parallel with the 0.1 µF. The 10 µF capacitor provides low ac impedance at low frequencies. Smaller values of electrolytic capacitors can be used depending on the circuit requirements. Additional smaller value capacitors help provide a low impedance path for unwanted noise out to higher frequencies but are not always necessary.

Placement of the capacitor returns (grounds), where the capacitors enter into the ground plane, is also important. Returning the capacitor grounds close to the amplifier load is critical for distortion performance. Keeping the capacitors distance short, but equal from the load, is optimal for performance.

In some cases, bypassing between the two supplies can help improve PSRR and maintain distortion performance in crowded or difficult layouts. Designers should note this as another option for improving performance.

Minimizing the trace length and widening the trace from the capacitors to the amplifier reduces the trace inductance. A series inductance with the parallel capacitance can form a tank circuit, which can introduce high frequency ringing at the output. This additional inductance can also contribute to increased distortion due to high frequency compression at the output. The use of vias should be minimized in the direct path to the amplifier power supply pins because vias can introduce parasitic inductance, which can lead to instability. When required, use multiple large diameter vias because this lowers the equivalent parasitic inductance.

GROUNDING

The use of ground and power planes is encouraged as a method of proving low impedance returns for power supply and signal currents. Ground and power planes can also help to reduce stray trace inductance and provide a low thermal path for the amplifier. Ground and power planes should not be used under any of the pins of the AD8003. The mounting pads and the ground or power planes can form a parasitic capacitance at the amplifiers input. Stray capacitance on the inverting input and the feedback resistor form a pole, which degrades the phase margin, leading to instability. Excessive stray capacitance on the output also forms a pole, which degrades phase margin.

OUTLINE DIMENSIONS



ORDERING GUIDE

Model ¹	Temperature Range	Package Description	Package Option	Ordering Quantity
AD8003ACPZ-R2	–40°C to +85°C	24-Lead LFCSP_WQ	CP-24-10	250
AD8003ACPZ-REEL7	–40°C to +85°C	24-Lead LFCSP_WQ	CP-24-10	1,500
AD8003ACHIPS		Die		
AD8003ACPZ-EBZ		Evaluation Board		

 1 Z = RoHS Compliant Part.

NOTES



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